Report
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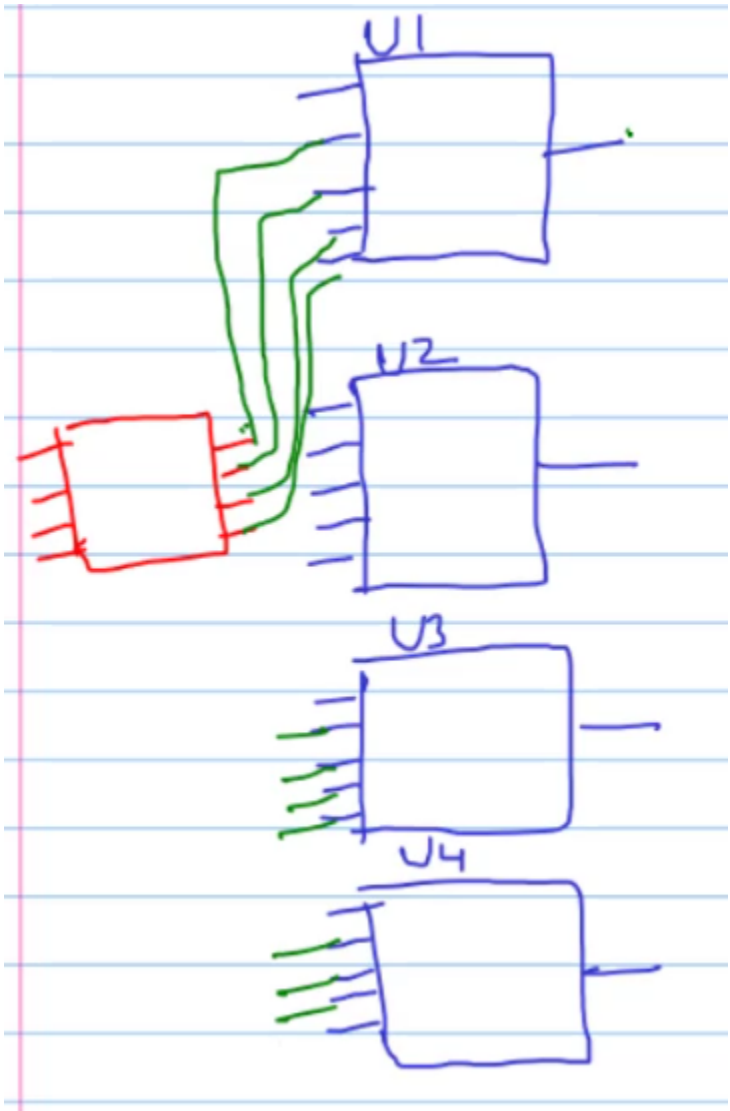
Logic tile

In the logic tile we initialize the q and then we select d from mem according to the input and then finally we assign flip flop output or mem output according to the value of q.

Switch box

Switch box is used to alter the 4 input with any other 4 output as seen in the below figure.



Truth tables

```
00000 => 0
00001 => 1
00010 => 0
00011 => 1
00100 => 0
00101 => 1
00110 => 0
00111 => 1
01000 => 0
01001 => 1
01010 => 0
01011 => 1
01100 => 0
01101 => 1
01110 => 0
01111 => 1
10000 => 0
10001 => 0
10010 => 1
10011 => 1
10100 => 0
10101 => 0
10110 => 1
10111 => 1
11000 => 0
11001 => 0
11010 => 1
11011 => 1
11100 => 0
11101 => 0
11110 => 1
11111 => 1
```

Suppose we get this truth table then we get the bits as 1100 1100 1100 1100 1010 1010 1010 1010 1010 which is CCCCAAAA there the first line in the lab6 configure.mem is CCCCAAAA. Suppose we get the truth table as this then

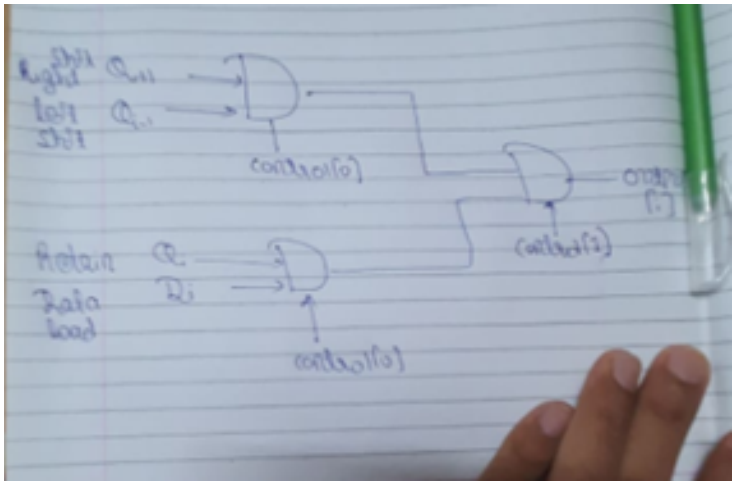
Combination of Universal Shift Register Decoder and four bit sum

Universal Shift Register

In universal shift register we will select right shift or left shift according to c0 and then we will select retain or data load according to c1

Again using c1 we will select which of the two outputs should be selected.

Thus we can assume these as 4:1 mux using three 2:1 where output1 is selected using c0 then out2 is selected using c1 and then the final output is selected using c1.



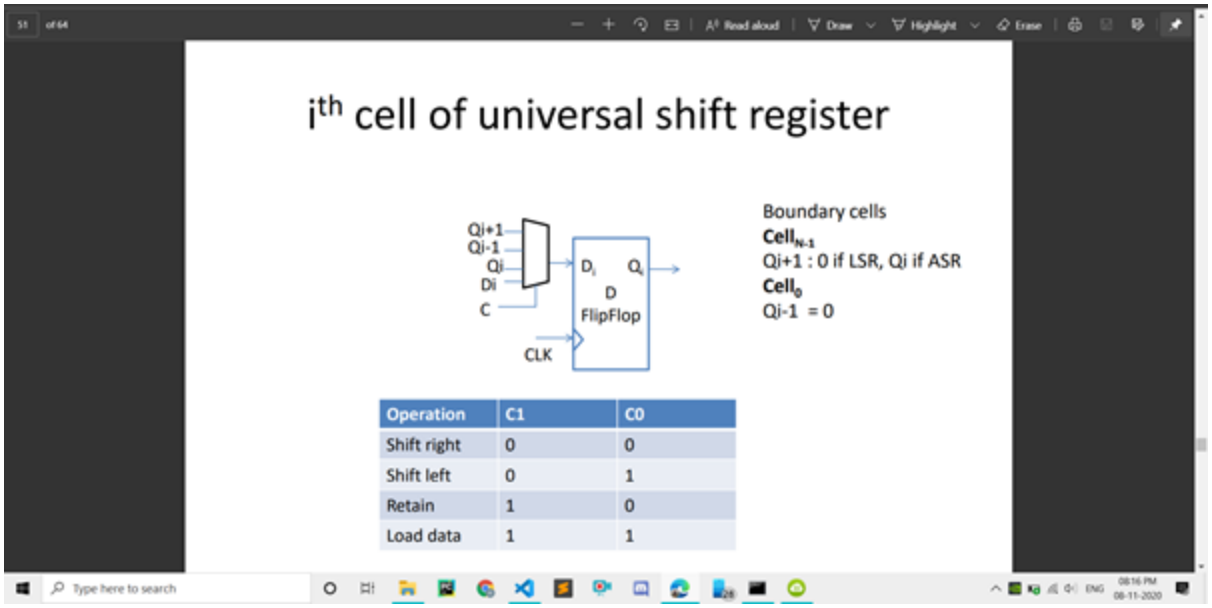
Selection of the output using three 2:1 mux.

The difference in the final selection of the output is that we will use flip flop output in the last mux and in the two mux above we will use mem output.

Thus we will get the final output.

We will also get serial left input using right shift where we will shift all the digits and the first digit will be serial input.

We will also get serial right input using left shift where we will shift all the digits left and the digit0 will be serial input.



As you can see in the above figure we will select shift right when the control bit is 00 and so on.

4 bit adder

In the 4 bit adder we will generate the carry0, carry1, carry2 and carry3 using the ripple carry method.
Then we will generate sum0 sum1 sum2 and sum3 thus we get all the output.
For this we will need the truth tables according to the need .

Decoder

In the decoder we will select out0, out1, out2, out3, out4 and so on using the 3 inputs available. Only one of the out0, out1, .. will be one. We will use the truth table in such a way that only one will be one.

Combination of Universal Shift Register Decoder and four bit sum

As seen in the below figure we can use the switch box to connect any input to any output.

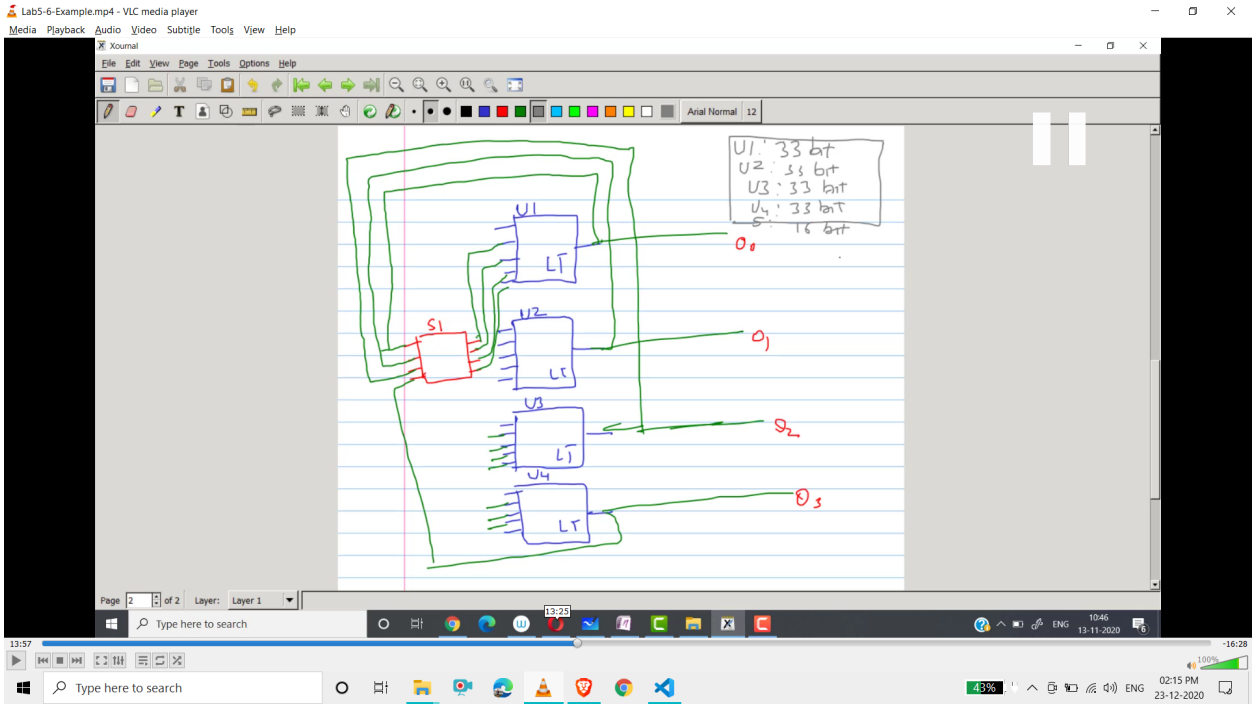


Fig 2

We will make 3 test benches according to all the parts and then we will combine them using the switch boxes and then we will get the output which we will display using the display function.
We will also generate the vcd files.