## L1 Instruction Cache



Warp Scheduler (32 thread/clk)								
Dispatch Unit (32 thread/clk)								
Register File (16,384 x 32-bit)								
FP	64	INT	INT	FP32	FP32	$\blacksquare$		
FP64		INT	INT	FP32	FP32			
FP64		INT	INT	FP32	FP32	TENSOR CORE		
FP64		INT	INT	FP32	FP32		TENSOR	
FP64		INT	INT	FP32	FP32		CORE	
FP64		INT	INT	FP32	FP32			
FP64		INT	INT	FP32	FP32			
FP64		INT	INT	FP32	FP32	oxdot		
LD/ ST	LD/ ST	LD/ ST	LD/ ST	LD/ ST	LD/ ST	LD/ ST	LD/ ST	SFU

L0 Instruction Cache

## **L0 Instruction Cache** Warp Scheduler (32 thread/clk) Dispatch Unit (32 thread/clk) Register File (16,384 x 32-bit) INT FP32 FP32 FP64 INT FP64 INT INT FP32 FP32 FP64 INT INT FP32 FP32 INT FP32 FP32 FP64 INT **TENSOR TENSOR** CORE CORE FP32 FP32 FP64 INT INT FP64 INT INT FP32 FP32 INT INT FP32 FP32 FP64 FP64 FP32 FP32 INT INT LD/ LD/ LD/ LD/ LD/ LD/ LD/ LD/ SFU ST ST ST ST ST ST ST ST



**L0 Instruction Cache** 

Warp Scheduler (32 thread/clk)

Dispatch Unit (32 thread/clk)

## 128KB L1 Data Cache / Shared Memory

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