Trap-Return Instructions	31	27 26 25	24 20	19 15	14 12	11 7	6	0	
Trap-Return Instructions		funct7	rs2	rs1	funct3	rd	opcode	R-type	
Main		imm[11:0]		rs1	funct3	rd	opcode	I-type	
Main									
Interrupt-Management Instructions									
Supervisor Memory-Management Instructions		0011000	00010	00000	000	00000	1110011	MRET	
Supervisor Memory-Management Instructions									
Hypervisor Memory-Management Instructions		0001000	00101	00000	000	00000	1110011	WFI	
Hypervisor Memory-Management Instructions									
Hypervisor Memory-Management Instructions									
Mathematical Columbia		0001001	rs2	rs1	000	00000	1110011	SFENCE.VMA	
Mathematical Columbia									
Hypervisor Virtual-Machine Load and Store Instructions							1110011	THEENCE WWW	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$									
0110000 00000 rs1 100 rd 1110011 HLV.B 0110000 00001 rs1 100 rd 1110011 HLV.BU 0110010 00000 rs1 100 rd 1110011 HLV.H 011010 000001 rs1 100 rd 1110011 HLV.HU 011010 00000 rs1 100 rd 1110011 HLV.W 011010 00011 rs1 100 rd 1110011 HLVX.HU 011010 00011 rs1 100 rd 1110011 HLVX.WU 0110100 00011 rs2 rs1 100 00000 1110011 HSV.B 0110101 rs2 rs1 100 00000 1110011 HSV.H Hypervisor Virtual-Machine Load and Store Instructions, RV64 only Hypervisor HEV.WU HIV.D.D HLV.WU 011010 00000 rs1 100 rd 1110011 HLV.WU 0110110 <		0110001	rsz	rs1	000	00000	1110011	HFENCE.GVMA	
0110000 00000 rs1 100 rd 1110011 HLV.B 0110000 00001 rs1 100 rd 1110011 HLV.BU 0110010 00000 rs1 100 rd 1110011 HLV.H 011010 000001 rs1 100 rd 1110011 HLV.HU 011010 00000 rs1 100 rd 1110011 HLV.W 011010 00011 rs1 100 rd 1110011 HLVX.HU 011010 00011 rs1 100 rd 1110011 HLVX.WU 0110100 00011 rs2 rs1 100 00000 1110011 HSV.B 0110101 rs2 rs1 100 00000 1110011 HSV.H Hypervisor Virtual-Machine Load and Store Instructions, RV64 only Hypervisor HEV.WU HIV.D.D HLV.WU 011010 00000 rs1 100 rd 1110011 HLV.WU 0110110 <	Hypervisor Virtual-Machine Load and Store Instructions								
0110000 00001 rs1 100 rd 1110011 HLV.BU							1110011	HLV.B	
0110010 00000 rs1 100 rd 1110011 HLV.H 0110010 00001 rs1 100 rd 1110011 HLV.HU 0110100 00000 rs1 100 rd 1110011 HLV.W 0110010 00011 rs1 100 rd 1110011 HLV.W 0110001 00011 rs1 100 rd 1110011 HLV.W 0110001 rs2 rs1 100 00000 1110011 HSV.B 0110011 rs2 rs1 100 00000 1110011 HSV.H 0110101 rs2 rs1 100 00000 1110011 HSV.W Hypervisor Virtual-Machine Load and Store Instructions, RV64 only 0110100 00001 rs1 100 rd 1110011 HLV.W 0110110 00000 rs1 100 rd 1110011 HLV.D 0110111 rs2 rs1 100 00000 1110011 HSV.D Svinval Memory-Management Instructions 0001011 rs2 rs1 000 00000 1110011 SFENCE.W.INVAL 0001100 00001 00000 00000 00000 1110011 SFENCE.W.INVAL 0001100 00001 00000 00000 00000 1110011 SFENCE.INVAL.IR 0010011 rs2 rs1 000 00000 1110011 HIV.V.D HIV.V.D HIV.V.D HIV.V.D HIV.D HIV.D SFENCE.W.INVAL O010011 rs2 rs1 000 00000 1110011 SFENCE.W.INVAL O011001 00001 00000 00000 00000 1110011 SFENCE.W.INVAL O010011 rs2 rs1 000 00000 1110011 HIV.V.D O010011 rs2 rs1 000 00000 1110011 HIV.V.D O010011 RS2 RS1 000 00000 1110011 HIV.D.D O010011 RS2 RS1 000 00000 1110011 HIV.D.D O010011 RS2 RS1 000 00000 1110011 HIV.D.D O010011 HIV.D.D O010011 HIV.B.D O01001 O0000 O0000 O0000 00000 1110011 HIV.D.D O01001 HIV.B.D O01001 H				rs1	100	rd			
0110100			00000		100				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0110010	00001	rs1	100	rd	1110011	HLV.HU	
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$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0110010	00011	rs1	100	rd	1110011	HLVX.HU	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		0110100	00011	rs1	100	rd	1110011	HLVX.WU	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			rs2	rs1	100		1110011	HSV.B	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0110011	rs2	rs1	100	00000	1110011	HSV.H	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0110101	rs2	rs1	100	00000	1110011	HSV.W	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$									
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0001100 00000 00000 00000 1110011 SFENCE.W.INVAL 0001100 00001 00000 000 00000 1110011 SFENCE.INVAL.IR 0010011 rs2 rs1 000 00000 1110011 HINVAL.VVMA							1110011	SINVAL.VMA	
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U110011 rs2 rs1 U00 U0000 1110011 HINVAL.GVMA		0110011	rs2	rs1	000	00000	1110011	HINVAL.GVMA	

Table 1: RISC-V Privileged Instructions