31	27	26	25	24	20	19		15	14	12	11		7	6		0	
	funct	7		rs	2		rs1		fun	ct3		$^{\rm rd}$		C	pcode		R-type
		$_{\mathrm{imm}}$	[11:0]				rs1		fun	ct3		rd		C	pcode		I-type
	imm[1	1:5]		rs	2		rs1		fun	ct3	in	nm[4:0]		C	pcode		S-type
	imm[12	10:5]		rs	2		rs1		fun	ct3	imr	n[4:1 1]	1]	C	pcode		B-type
				imm[31:12]							$^{\rm rd}$		C	pcode		U-type
			imn	n[20 10:	1 11 19	9:12]						rd		C	pcode		J-type

RV32I	Base	Incten	otion	Sot

			rd	0110111	LUI
imm[31:12			rd	0010111	AUIPC
imm[20 10:1 11	19:12]		rd	1101111	JAL
imm[11:0]	rs1	000	rd	1100111	JALR
imm[12 10:5] rs2	rs1	000	imm[4:1 11]	1100011	BEQ
imm[12 10:5] rs2	rs1	001	imm[4:1 11]	1100011	BNE
imm[12 10:5] rs2	rs1	100	imm[4:1 11]	1100011	BLT
imm[12 10:5] rs2	rs1	101	imm[4:1 11]	1100011	BGE
imm[12 10:5] rs2	rs1	110	imm[4:1 11]	1100011	BLTU
imm[12 10:5] rs2	rs1	111	imm[4:1 11]	1100011	BGEU
imm[11:0]	rs1	000	rd	0000011	LB
imm[11:0]	rs1	001	rd	0000011	LH
imm[11:0]	rs1	010	rd	0000011	LW
imm[11:0]	rs1	100	rd	0000011	LBU
imm[11:0]	rs1	101	rd	0000011	LHU
imm[11:5] rs2	rs1	000	imm[4:0]	0100011	SB
imm[11:5] rs2	rs1	001	imm[4:0]	0100011	SH
imm[11:5] rs2	rs1	010	imm[4:0]	0100011	SW
imm[11:0]	rs1	000	rd	0010011	ADDI
imm[11:0]	rs1	010	rd	0010011	SLTI
imm[11:0]	rs1	011	rd	0010011	SLTIU
imm[11:0]	rs1	100	rd	0010011	XORI
imm[11:0]	rs1	110	rd	0010011	ORI
imm[11:0]	rs1	111	rd	0010011	ANDI
0000000 rs2	rs1	000	rd	0110011	ADD
0100000 rs2	rs1	000	rd	0110011	SUB
0000000 rs2	rs1	001	rd	0110011	SLL
0000000 rs2	rs1	010	rd	0110011	SLT
0000000 rs2	rs1	011	rd	0110011	SLTU
0000000 rs2	rs1	100	rd	0110011	XOR
0000000 rs2	rs1	101	rd	0110011	SRL
0100000 rs2	rs1	101	rd	0110011	SRA
0000000 rs2	rs1	110	rd	0110011	OR
0000000 rs2	rs1	111	rd	0110011	AND
fm pred succ	rs1	000	rd	0001111	FENCE
0000000 00000	00000	000	00000	1110011	ECALL
0000000 00001	00000	000	00000	1110011	EBREAK
0000000 shamt	rs1	001	rd	0010011	SLLI
0000000 shamt	rs1	101	rd	0010011	SRLI
0100000 shamt	rs1	101	rd	0010011	SRAI
1000001 10011	rs1	000	rd	0001111	FENCE.TSC
0000000 10000	00000	000	00000	0001111	PAUSE

l 27		25	24	20	19	15		12	11	7	6	0	_
funct7			rs2		rs1		funct		rd		opcode		R-type
i	mm[11	.:0]			rs1		funct	3	$_{\mathrm{rd}}$		opcode	е	I-type
imm[11:	5]		rs2	:	rs1		funct	3	imm[4:0)]	opcode	е	S-type
	RV6	4I I	Base I	nstru	ction Se	t (ir	ı addit	ion	to RV32	I)			
i	mm[11				rs1		110		rd	<u>′</u> Т	000001	1	LWU
	mm 11				rs1		011		rd		000001		LD
imm[11:	5	Ť	rs2)	rs1		011		imm[4:0)]	010001	1	$_{\rm SD}$
000000	Ť		shamt		rs1		001		rd		001001	1	SLLI
000000			shamt		rs1		101		rd		001001	1	SRLI
010000			shamt		rs1		101		rd		001001	1	SRAI
i	mm [11	.:0]			rs1		000		rd		001101	1	ADDIW
000000	0	Ť	shar	nt	rs1		001		rd		001101	1	SLLIW
000000	0		shar	nt	rs1		101		rd		001101	1	SRLIW
010000	0		shar	nt	rs1		101		rd		001101	1	SRAIW
000000	0		rs2	;	rs1		000		$_{\mathrm{rd}}$		011101	1	ADDW
010000	0		rs2		rs1		000		rd		011101	1	SUBW
000000	0		rs2		rs1		001		rd		011101		SLLW
000000	0		rs2		rs1		101		rd		011101	1	SRLW
010000	0		rs2		rs1		101		rd		011101	1	SRAW
	Ta a		32/R	64 2	Zifencei S	stan		Σxte			000444		7 PPNOP
i	mm[11	:0]	,		rs1		001		rd		000111	1	FENCE.
i		:0]	,				001		rd				_
i	csr	:0]	,		rs1		ard Ex	ten	rd nsion		000111 111001 111001	.1	CSRRW CSRRS
i	csr	:0]	,		Zicsr St		001 ard Ex	ten	rd asion		111001	1	CSRRW
i	csr	:0]	,		rs1	and	001 ard Ex 001 010	ten	rd asion rd rd		111001 111001	.1 .1 .1	CSRRW CSRRS CSRRC
i	csr csr	:0]	,		Zicsr St rs1 rs1 rs1	and	001 ard Ex 001 010 011	cten	rd sion rd rd rd		111001 111001 111001	.1 .1 .1	CSRRW CSRRS CSRRC CSRRW
i	csr csr csr	:0]	,		rs1 Zicsr St rs1 rs1 rs1 uimn	and	001 ard Ex 001 010 011 101	cten	rd sion rd rd rd rd rd		111001 111001 111001 111001	1 .1 .1 .1	CSRRW CSRRS CSRRC CSRRW CSRRSI
i	csr csr csr csr	:0]	RV32/I	RV64	rs1 Zicsr St rs1 rs1 uimm uimm	and	001 ard Ex 001 010 011 101 110 111	cten	rd rd rd rd rd rd rd rd		111001 111001 111001 111001 111001	1 .1 .1 .1	CSRRW CSRRS CSRRC CSRRW CSRRSI
	CST CST CST CST CST CST	:0]	RV32/I	RV64	Zicsr St rs1 rs1 rs1 uimm uimm	and	001 ard Ex 001 010 011 101 110 1110 Extensi	on	rd		111001 111001 111001 111001 111001 111001	.1 .1 .1 .1 .1	CSRRW CSRRS CSRRC CSRRW CSRRSI CSRRCI
000000 000000	csr csr csr csr csr	:0]	RV32/I	/32M	zicsr St rs1 rs1 rs1 uimn uimn uimn	and	001 ard Ex 001 010 011 101 110 111	on	rd rd rd rd rd rd rd rd		111001 111001 111001 111001 111001	1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRW CSRRSI
000000	CST CST CST CST CST TST CST	:0]	RV32/I	/32N	rs1 Zicsr St rs1 rs1 rs1 uimm uimm uimm I Standa rs1	and	001 ard Ex 001 010 011 101 110 111 Extensi	cten	rd sion rd rd rd rd rd rd rd rd		111001 111001 111001 111001 111001 111001	1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRW CSRRSI CSRRCI
000000	csr csr csr csr csr	:0]	RV32/I RV rs2 rs2	/32N	rs1 Zicsr St rs1 rs1 rs1 uimm uimm uimm rs1 Standa	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001	cten	rd r		111001 111001 111001 111001 111001 111001 011001	1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRW CSRRSI CSRRCI MUL MULH MULHS
000000 000000 000000	csr csr csr csr csr	:0]	RV32/I RV rs2 rs2 rs2	/32N	rs1 rs1 rs1 rs1 rs1 rs1 uimm uimm uimm uimm rs1	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001 010	on	rd r		111001 111001 111001 111001 111001 111001 011001 011001	1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRW CSRRSI CSRRCI MUL MULH MULHS
000000 000000 000000 000000	CST CST CST CST CST TST TST	:0]	RV32/H RV rs2 rs2 rs2 rs2	/32N	rs1 Zicsr St rs1 rs1 rs1 uimm uimm uimm rs1 Standa rs1 rs1 rs1	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001 010 011	on	rd rd rd rd rd rd rd rd rd rd rd rd rd		111001 111001 111001 111001 111001 111001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRW CSRRSI CSRRCI MUL MULH MULHS MULHS
000000 000000 000000 000000 000000	CST CST CST CST CST TST TST	:0]	RV32/H RV rs2 rs2 rs2 rs2 rs2	/32M	rs1 rs1 rs1 rs1 rs1 uimm uimm uimm uimm uimm uimm rs1 rs1	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001 011 100	on	rd r		111001 111001 111001 111001 111001 111001 011001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRSI CSRRCI CSRRCI MUL MULH MULHS MULHU DIV
000000 000000 000000 000000 000000 00000	CST CST CST CST CST CST TST TST	:0]	RV32/I RV32/I RV rs2 rs2 rs2 rs2 rs2 rs2	/32M	rs1 Zicsr St rs1 rs1 rs1 rs1 uimm uimm Uimm Standa rs1	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001 011 100 101	on	rd r		111001 111001 111001 111001 111001 111001 011001 011001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRSI CSRRCI CSRRCI MUL MULH MULHSI DIV DIVU
000000 000000 000000 000000 000000 00000	CST CST CST CST CST CST T T T T T T T T T	R	RV32/I RV 182 182 182 182 182 182 182	//32M	rs1 Zicsr St rs1 rs1 uimn uimn Uimn I Standa rs1	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001 010 110 110 111 110	on	rd r	M)	111001 111001 111001 111001 111001 111001 011001 011001 011001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRSI CSRRCI MUL MULH MULHS MULHU DIVU DIVU REM
000000 000000 000000 000000 000000 00000	CST CST	R	RV32/I RV 182 182 182 182 182 182 182	/32M	rs1 Zicsr St rs1 rs1 uimn uimn Uimn I Standa rs1	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001 010 110 110 111 110	on	rd r	M)	111001 111001 111001 111001 111001 111001 011001 011001 011001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRSI CSRRCI MUL MULH MULHS MULHU DIVU DIVU REM
000000 000000 000000 000000 000000 00000	CSF CSF CSF CSF CSF CSF T T T T T T T T T	R	RV32/I RV rs2 rs2 rs2 rs2 rs2 rs2	732M	rs1 rs1	and	001 ard Ex 001 010 011 101 110 2xtensi 000 001 010 110 110 111 addit	on	rd rd rd rd rd rd rd rd rd rd rd rd rd	M)	111001 111001 111001 111001 111001 111001 011001 011001 011001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRW CSRRSI CSRRCI MUL MULH MULHS MULHU DIV DIVU REM REMU
000000 000000 000000 000000 000000 00000	CST CST	R	RV32/I RV FS2 FS2 FS2 FS2 FS2 FS2 FS2 FS2	/32M	rs1 Zicsr St rs1 rs1 rs1 uimm uimm Standa rs1 rs	and	001 ard Ex 001 010 011 101 110 111 Extensi 000 001 011 100 111 100 101 110 111 addit:	on	rd r	M)	111001 111001 111001 111001 111001 111001 011001 011001 011001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRW CSRRSI CSRRCI MUL MULH MULHS DIV DIVU REM REMU MULW
000000 000000 000000 000000 000000 00000	CST CST CST CST CST CST T T T T T T T T T	R	RW 182/11 182 182 182 182 182 182 182 182 182 1	/32M	rs1 Zicsr St rs1 rs1 rs1 uimn uimn rs1	and	001 ard Ex 001 010 010 011 101 110 111 Extensi 000 001 011 100 101 110 111 addit:	on	rd r	MM)	111001 111001 111001 111001 111001 111001 011001 011001 011001 011001 011001 011001 011001	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CSRRW CSRRS CSRRC CSRRSI CSRRCI MUL MULH MULHSI MULHU DIVU DIVU REM REMU MULW DIVW

31	27	26	25	24	20	19	15	14	12	11		7	6		0	
-	func	t7		rs2		rs1		fun	ct3		rd	Ť		opcode	Ť	R-type
																• •
				RV	32A	Standa	rd E	xten	sion							
0	0010	aq	rl	00000)	rs1		0.	10		rd		(0101111		LR.W
	0011	aq	rl	rs2		rs1			10		$^{\rm rd}$			0101111		SC.W
0	0001	aq	rl	rs2		rs1		0.3	10		$^{\rm rd}$		(0101111		AMOSWAP.W
0	0000	aq	rl	rs2		rs1		03	10		$^{\rm rd}$		- (0101111		AMOADD.W
0	0100	aq	rl	rs2		rs1		0.	10		$^{\mathrm{rd}}$			0101111		AMOXOR.W
0	1100	aq	rl	rs2		rs1		0.3	10		$^{\mathrm{rd}}$		(0101111		AMOAND.W
0	1000	aq	rl	rs2		rs1		0.	10		rd		(0101111		AMOOR.W
10	0000	aq	rl	rs2		rs1		0.	10		rd		(0101111		AMOMIN.W
10	0100	aq	rl	rs2		rs1		0.	10		$^{\rm rd}$		(0101111		AMOMAX.W
1	1000	aq	rl	rs2		rs1		0.	10		rd		(0101111		AMOMINU.W
1	1100	aq	rl	rs2		rs1		0.	10		rd		(0101111		AMOMAXU.W
						_										
		_		Standar						to I		A)				T.D. D.
	0010	aq	rl	00000)	rs1		01			rd			0101111		LR.D
	0011	aq	rl	rs2		rs1		01			rd			0101111		SC.D
	0001	aq	rl	rs2		rs1		0.			$^{\mathrm{rd}}$			0101111		AMOSWAP.D
	0000	aq	rl	rs2		rs1		0.			$^{\mathrm{rd}}$			0101111		AMOADD.D
	0100	aq	rl	rs2		rs1		0.3	11		$^{\mathrm{rd}}$			0101111		AMOXOR.D
	1100	aq	rl	rs2		rs1		0.			$^{\rm rd}$			0101111		AMOAND.D
	1000	aq	rl	rs2		rs1		0.3	11		rd			0101111		AMOOR.D
10	0000	aq	rl	rs2		rs1		0	11		$^{\mathrm{rd}}$			0101111		AMOMIN.D
10	0100	aq	rl	rs2		rs1		0.3	11		rd		(0101111		AMOMAX.D
1	1000	aq	rl	rs2		rs1		0.3	11		rd		(0101111		AMOMINU.D
	1100	aq	rl	rs2	_	rs1		0.			rd			0101111		AMOMAXU.D

31	27	26	25	24	20	19	15	14	12	11		7	6		0	
	funct	7			rs2	rs	1	fun	ct3		rd			opcode		R-type
	rs3	fun	ct2		rs2	rs	1	fun	ct3		rd			opcode		R4-type
		imm	[11:0]			rs	1	fun	ct3		$^{\rm rd}$			opcode		I-type
	imm[1]	1:5]			rs2	rs	1	fun	ct3	im	1m[4:0]			opcode		S-type

RV32F Standard Extension

RV32F Standard Extension													
	imm[11:0]		rs1	010	$^{\mathrm{rd}}$	0000111	FLW						
imm[1	1:5]	rs2	rs1	010	imm[4:0]	0100111	FSW						
rs3	00	rs2	rs1	rm	$^{\mathrm{rd}}$	1000011	FMADD.S						
rs3	00	rs2	rs1	rm	$^{\mathrm{rd}}$	1000111	FMSUB.S						
rs3	00	rs2	rs1	rm	rd	1001011	FNMSUB.S						
rs3	00	rs2	rs1	rm	rd	1001111	FNMADD.S						
00000	000	rs2	rs1	rm	$^{\mathrm{rd}}$	1010011	FADD.S						
00001	.00	rs2	rs1	rm	$^{\mathrm{rd}}$	1010011	FSUB.S						
00010	000	rs2	rs1	rm	rd	1010011	FMUL.S						
00011	.00	rs2	rs1	rm	$^{\mathrm{rd}}$	1010011	FDIV.S						
01011	.00	00000	rs1	rm	rd	1010011	FSQRT.S						
00100	000	rs2	rs1	000	rd	1010011	FSGNJ.S						
00100		rs2	rs1	001	rd	1010011	FSGNJN.S						
00100	000	rs2	rs1	010	rd	1010011	FSGNJX.S						
00101	.00	rs2	rs1	000	rd	1010011	FMIN.S						
00101	.00	rs2	rs1	001	$^{\mathrm{rd}}$	1010011	FMAX.S						
11000	000	00000	rs1	rm	rd	1010011	FCVT.W.S						
11000	000	00001	rs1	rm	rd	1010011	FCVT.WU.S						
11100	000	00000	rs1	000	$^{\mathrm{rd}}$	1010011	FMV.X.W						
10100		rs2	rs1	010	rd	1010011	FEQ.S						
10100	000	rs2	rs1	001	rd	1010011	FLT.S						
10100	000	rs2	rs1	000	$^{\mathrm{rd}}$	1010011	FLE.S						
11100		00000	rs1	001	rd	1010011	FCLASS.S						
11010		00000	rs1	rm	rd	1010011	FCVT.S.W						
11010		00001	rs1	rm	$^{\mathrm{rd}}$	1010011	FCVT.S.WU						
11110	000	00000	rs1	000	$_{\mathrm{rd}}$	1010011	FMV.W.X						

RV64F Standard Extension (in addition to RV32F)

1100000	00010	rs1	rm	rd	1010011	FCVT.L.S
1100000	00011	rs1	rm	rd	1010011	FCVT.LU.S
1101000	00010	rs1	rm	rd	1010011	FCVT.S.L
1101000	00011	rs1	rm	rd	1010011	FCVT.S.LU

31	27	26	25	24		20	19	15	14	12	11		7	6		0	
	funct	7			rs2		rs	1	fun	ct3		rd			opcode		R-type
1	rs3	fur	ct2		rs2		rs	1	fun	ct3		$_{\rm rd}$			opcode		R4-type
	imm[11:0]						rs	1	fun	ct3		$_{\rm rd}$			opcode		I-type
	imm[1]	l:5]			rs2		rs	1	fun	ct3	in	nm[4:0]]		opcode		S-type

RV32D Standard Extension

		RV 32D	standard E	xtension			
	imm[11:0]		rs1	011	rd	0000111	FLD
imm[1]	1:5]	rs2	rs1	011	imm[4:0]	0100111	FSD
rs3	01	rs2	rs1	rm	rd	1000011	FMADD.D
rs3	01	rs2	rs1	rm	rd	1000111	FMSUB.D
rs3	01	rs2	rs1	rm	rd	1001011	FNMSUB.D
rs3	01	rs2	rs1	rm	rd	1001111	FNMADD.D
00000	01	rs2	rs1	rm	rd	1010011	FADD.D
00001	01	rs2	rs1	rm	rd	1010011	FSUB.D
00010	01	rs2	rs1	rm	rd	1010011	FMUL.D
00011	01	rs2	rs1	rm	rd	1010011	FDIV.D
01011	01	00000	rs1	rm	rd	1010011	FSQRT.D
00100	01	rs2	rs1	000	rd	1010011	FSGNJ.D
00100	01	rs2	rs1	001	rd	1010011	FSGNJN.D
00100	01	rs2	rs1	010	rd	1010011	FSGNJX.D
00101	01	rs2	rs1	000	rd	1010011	FMIN.D
00101	01	rs2	rs1	001	rd	1010011	FMAX.D
01000	00	00001	rs1	rm	rd	1010011	FCVT.S.D
01000	01	00000	rs1	rm	rd	1010011	FCVT.D.S
10100	01	rs2	rs1	010	rd	1010011	FEQ.D
10100	01	rs2	rs1	001	rd	1010011	FLT.D
10100	01	rs2	rs1	000	rd	1010011	FLE.D
11100	01	00000	rs1	001	rd	1010011	FCLASS.D
11000	01	00000	rs1	rm	rd	1010011	FCVT.W.D
11000		00001	rs1	rm	rd	1010011	FCVT.WU.D
11010	01	00000	rs1	rm	rd	1010011	FCVT.D.W
11010	1101001		rs1	rm	rd	1010011	FCVT.D.WU

RV64D Standard Extension (in addition to RV32D)

10 04D Standard Extension (in addition to 10 02D)														
	1100001	00010	rs1	rm	rd	1010011	FCVT.L.D							
	1100001	00011	rs1	rm	rd	1010011	FCVT.LU.D							
	1110001	00000	rs1	000	$^{\mathrm{rd}}$	1010011	FMV.X.D							
	1101001	00010	rs1	rm	rd	1010011	FCVT.D.L							
	1101001	00011	rs1	$^{\mathrm{rm}}$	rd	1010011	FCVT.D.LU							
	1111001	00000	rs1	000	rd	1010011	FMV.D.X							

31	27	26	25	24		20	19		15	14	12	11		7	6		0	
	funct	7			rs2		r	s1		fun	ct3		$^{\rm rd}$			opcode		R-type
r	s3	fur	ct2		rs2		r	s1		fun	ct3		$_{\rm rd}$			opcode		R4-type
	imm[11:0]						r	s1		fun	ct3		$^{\rm rd}$			opcode		I-type
	imm[1]	l:5]			rs2		r	s1		fun	ct3	in	nm[4:0]]		opcode		S-type

RV32Q	Standard	Extension
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RV32Q Standard Extension											
	imm[11:0]		rs1	100	rd	0000111	FLQ				
imm[1]	imm[11:5]		rs1	100	imm[4:0]	0100111	FSQ				
rs3 11		rs2	rs1	rm	rd	1000011	FMADD.Q				
rs3	11	rs2	rs1	rm	rd	1000111	FMSUB.Q				
rs3	11	rs2	rs1	rm	rd	1001011	FNMSUB.Q				
rs3	11	rs2	rs1	rm	rd	1001111	FNMADD.Q				
00000	11	rs2	rs1	rm	rd	1010011	FADD.Q				
0000111		rs2	rs1	rm	rd	1010011	FSUB.Q				
0001011		rs2	rs1	rm	rd	1010011	FMUL.Q				
00011	11	rs2	rs1	rm	rd	1010011	FDIV.Q				
01011	11	00000	rs1	rm	rd	1010011	FSQRT.Q				
0010011		rs2	rs1	000	rd	1010011	FSGNJ.Q				
0010011		rs2	rs1	001	rd	1010011	FSGNJN.Q				
0010011		rs2	rs1	010	rd	1010011	FSGNJX.Q				
0010111		rs2	rs1	000	rd	1010011	FMIN.Q				
0010111		rs2	rs1	001	rd	1010011	FMAX.Q				
0100000		00011	rs1	rm	rd	1010011	FCVT.S.Q				
0100011		00000	rs1	rm	rd	1010011	FCVT.Q.S				
0100001		00011	rs1	rm	rd	1010011	FCVT.D.Q				
0100011		00001	rs1	rm	rd	1010011	FCVT.Q.D				
1010011		rs2	rs1	010	rd	1010011	FEQ.Q				
1010011		rs2	rs1	001	rd	1010011	FLT.Q				
1010011		rs2	rs1	000	rd	1010011	FLE.Q				
1110011		00000	rs1	001	rd	1010011	FCLASS.Q				
1100011		00000	rs1	rm	rd	1010011	FCVT.W.Q				
1100011		00001	rs1	rm	rd	1010011	FCVT.WU.Q				
1101011		00000	rs1	rm	rd	1010011	FCVT.Q.W				
1101011		00001	rs1	rm	rd	1010011	FCVT.Q.WU				

RV64Q Standard Extension (in addition to RV32Q)

1100011	00010	rs1	rm	rd	1010011	FCVT.L.Q
1100011	00011	rs1	$^{\mathrm{rm}}$	rd	1010011	FCVT.LU.Q
1101011	00010	rs1	$^{\mathrm{rm}}$	rd	1010011	FCVT.Q.L
1101011	00011	rs1	$^{\mathrm{rm}}$	rd	1010011	FCVT.Q.LU

31	27	26	25	24	20	19	15	14 12	11	7	6		0	
	funct	7		rs	32	rs1		funct3	$_{\mathrm{rd}}$			opcode		R-type
	rs3	fun	ct2	rs	32	rs1		funct3	rd			opcode		R4-type
		$_{\mathrm{imm}[}$	11:0]			rs1		funct3	rd			opcode		I-type
	imm[11	.:5]		rs	32	rs1		funct3	imm[4:0]			opcode		S-type
			44.01	R	V 32Zt		ard I	Extension				2000444		
		imm[11:0]			rs1		001	rd			0000111		FLH
	imm[11			rs		rs1		001	imm[4:0]			0100111		FSH
	rs3	10		rs		rs1		rm	rd			1000011		FMADD.H
	rs3	10			32	rs1		rm	rd			1000111		FMSUB.H
	rs3	10		r		rs1		rm	rd			1001011		FNMSUB.H
	rs3	10	J		32	rs1		rm	rd			1001111		FNMADD.H
	000001				32	rs1		rm	rd			1010011		FADD.H
	000011			rs		rs1		rm	rd			1010011		FSUB.H
	000101				32	rs1		rm	rd			1010011		FMUL.H
	000111			rs		rs1		rm	rd			1010011		FDIV.H
	010111	-			000	rs1		rm	rd			1010011		FSQRT.H
	001001			rs		rs1		000	rd			1010011		FSGNJ.H
	001001			rs		rs1		001	rd			1010011		FSGNJN.H
	001001			r		rs1		010	rd			1010011		FSGNJX.H
	001011			rs		rs1		000	rd			1010011		FMIN.H
0010110		rs2		rs1		001	$_{\mathrm{rd}}$			1010011		FMAX.H		
0100000		00010		rs1		rm	$^{\mathrm{rd}}$			1010011		FCVT.S.H		
	010001				000	rs1		rm	rd			1010011		FCVT.H.S
	101001			r		rs1		010	$_{\mathrm{rd}}$			1010011		FEQ.H
	101001			rs		rs1		001	$_{\mathrm{rd}}$			1010011		FLT.H
	101001				32	rs1		000	$_{ m rd}$			1010011		FLE.H
	111001				000	rs1		001	$_{\mathrm{rd}}$			1010011		FCLASS.H
	110001			000		rs1		$^{\mathrm{rm}}$	$_{\mathrm{rd}}$			1010011		FCVT.W.H
	110001			000		rs1		rm	$_{\mathrm{rd}}$			1010011		FCVT.WU.H
	111001				000	rs1		000	$^{\mathrm{rd}}$			1010011		FMV.X.H
	110101			000		rs1		rm	rd			1010011		FCVT.H.W
	110101			000	001	rs1		$^{\mathrm{rm}}$	rd		1	1010011		FCVT.H.WU
	111101				000	rs1		000	rd			1010011		FMV.H.X
	010000			000)10	rs1		rm	rd		1	1010011		FCVT.D.H
	010001			000	001	rs1		rm	rd		1	1010011		FCVT.H.D
	010001)10	rs1		$^{\mathrm{rm}}$	rd			1010011		FCVT.Q.H
	010001	10		000)11	rs1		$^{\mathrm{rm}}$	rd		1	1010011		FCVT.H.Q
	RV64Zfh Standard Extension (in addition to RV32Zfh)													
	11000		4Zfh		iard E 010		ı (in			th)		1010011		ECVELII
-	11000			000		rs1		rm	rd rd			1010011 1010011		FCVT.L.H
_						rs1		rm						FCVT.LU.H
_	110101			000		rs1		rm	rd			1010011		FCVT.H.L
	110101	10		000)11	rs1		$^{ m rm}$	$_{\mathrm{rd}}$			1010011		FCVT.H.LU

Table 1: Instruction listing for RISC-V