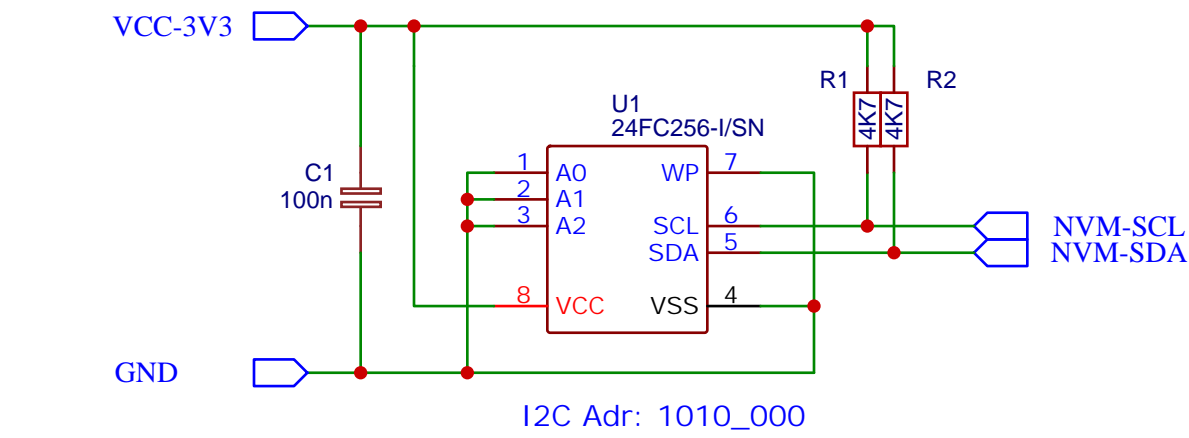
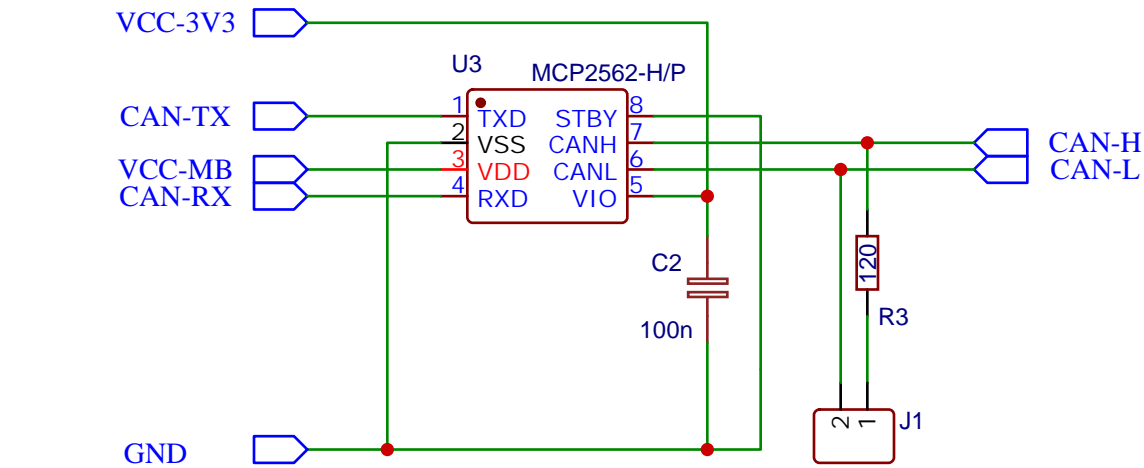


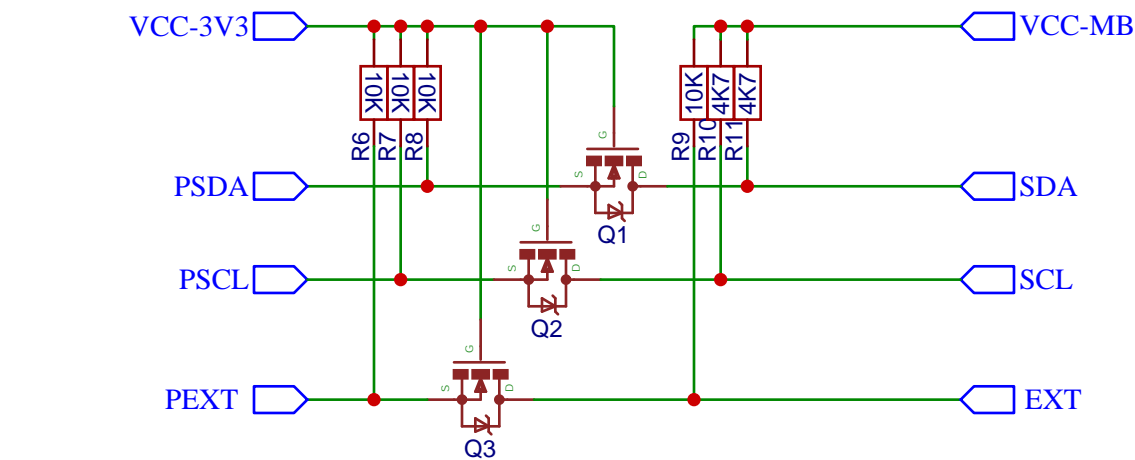
Non-Volatile Memory



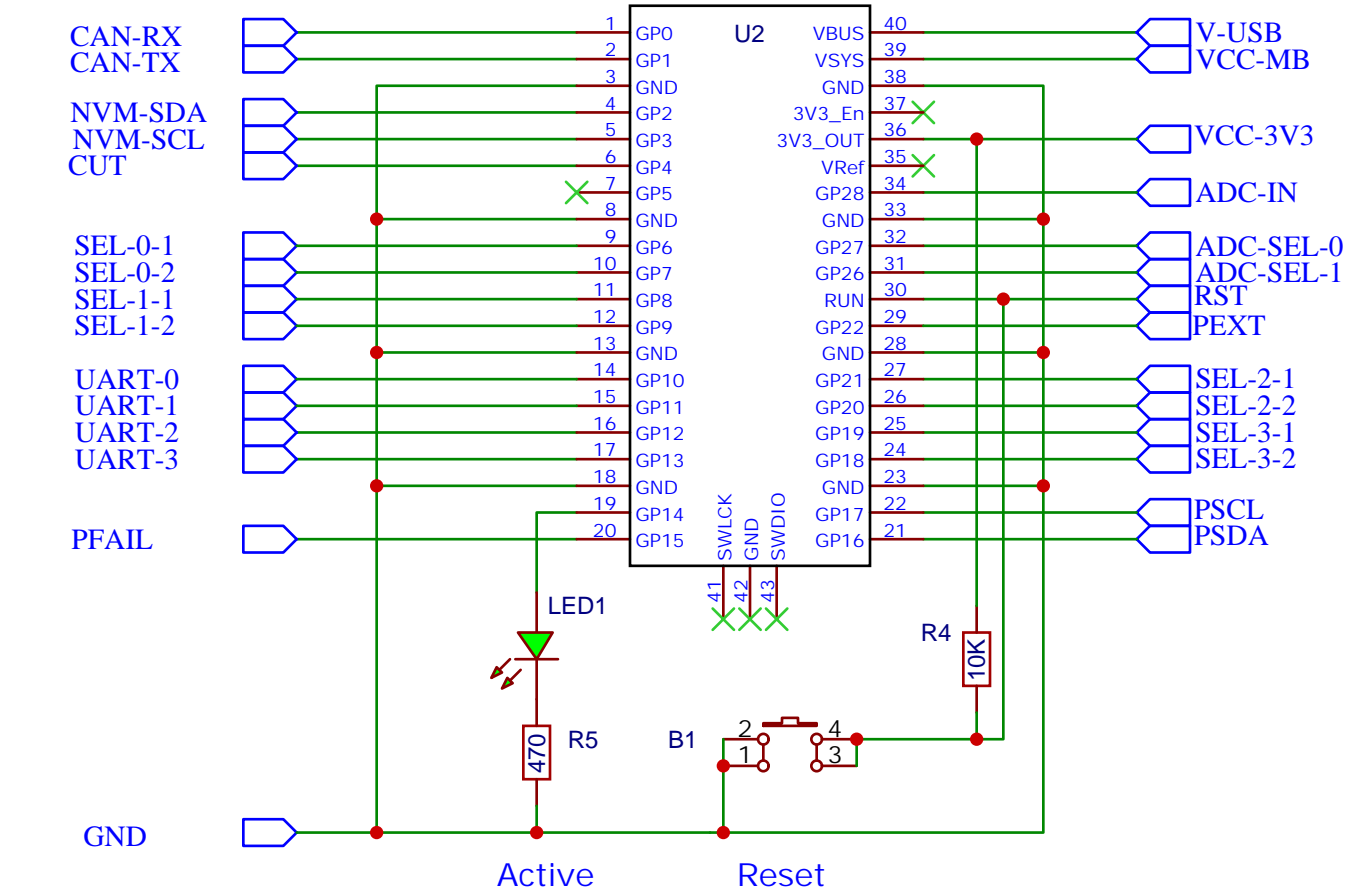
CAN Bus Line Driver

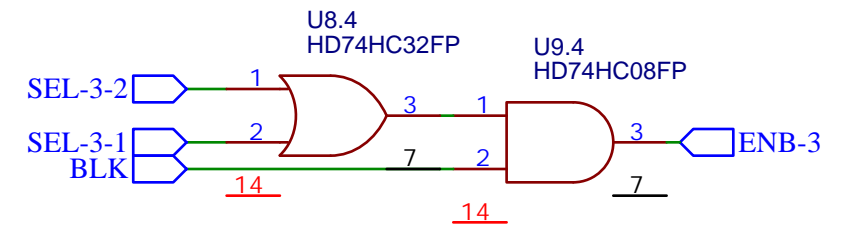
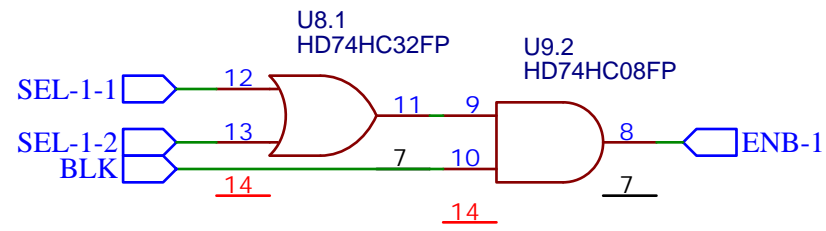
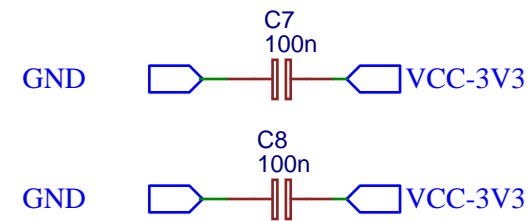
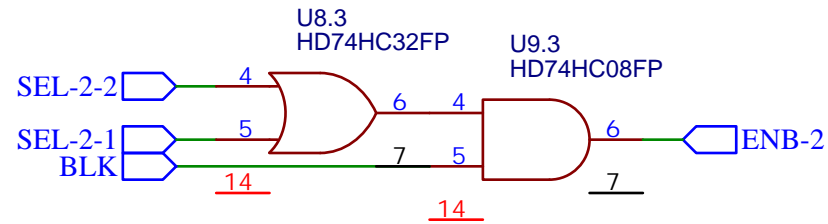
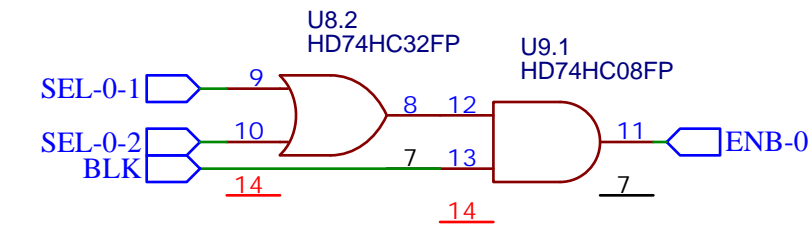
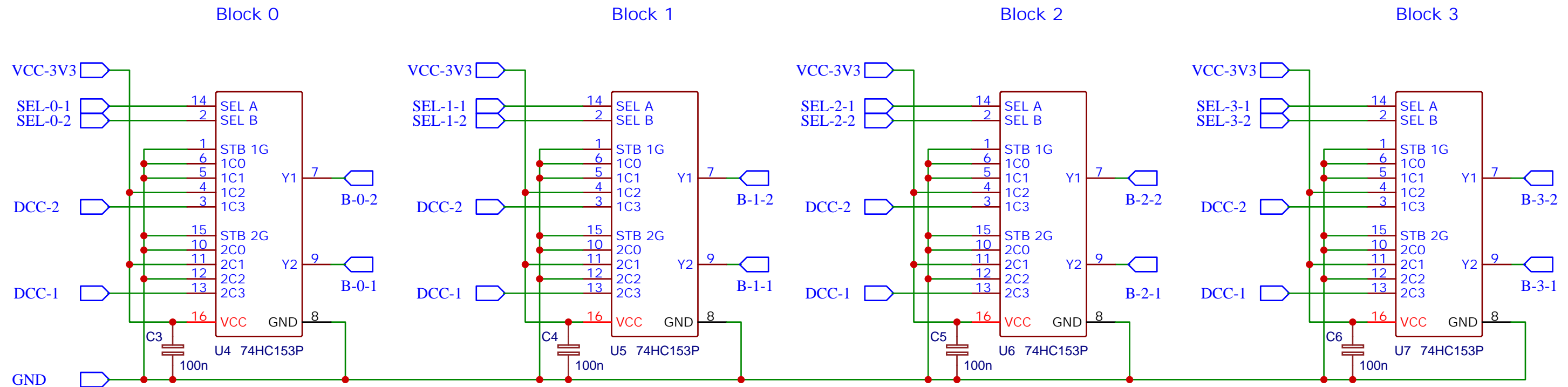


Level shifters



Main Controller - RASPBERRY Pi Pico



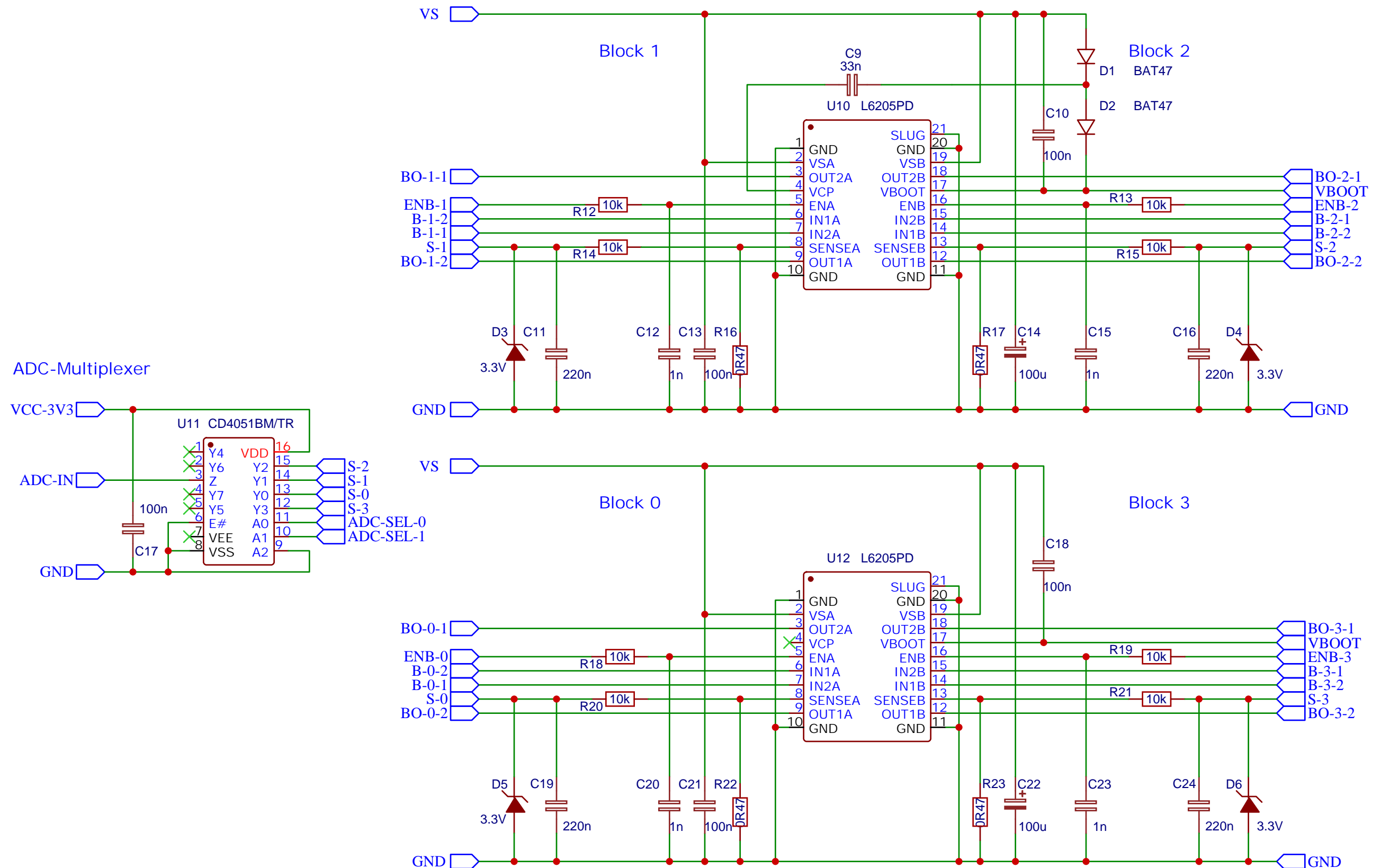


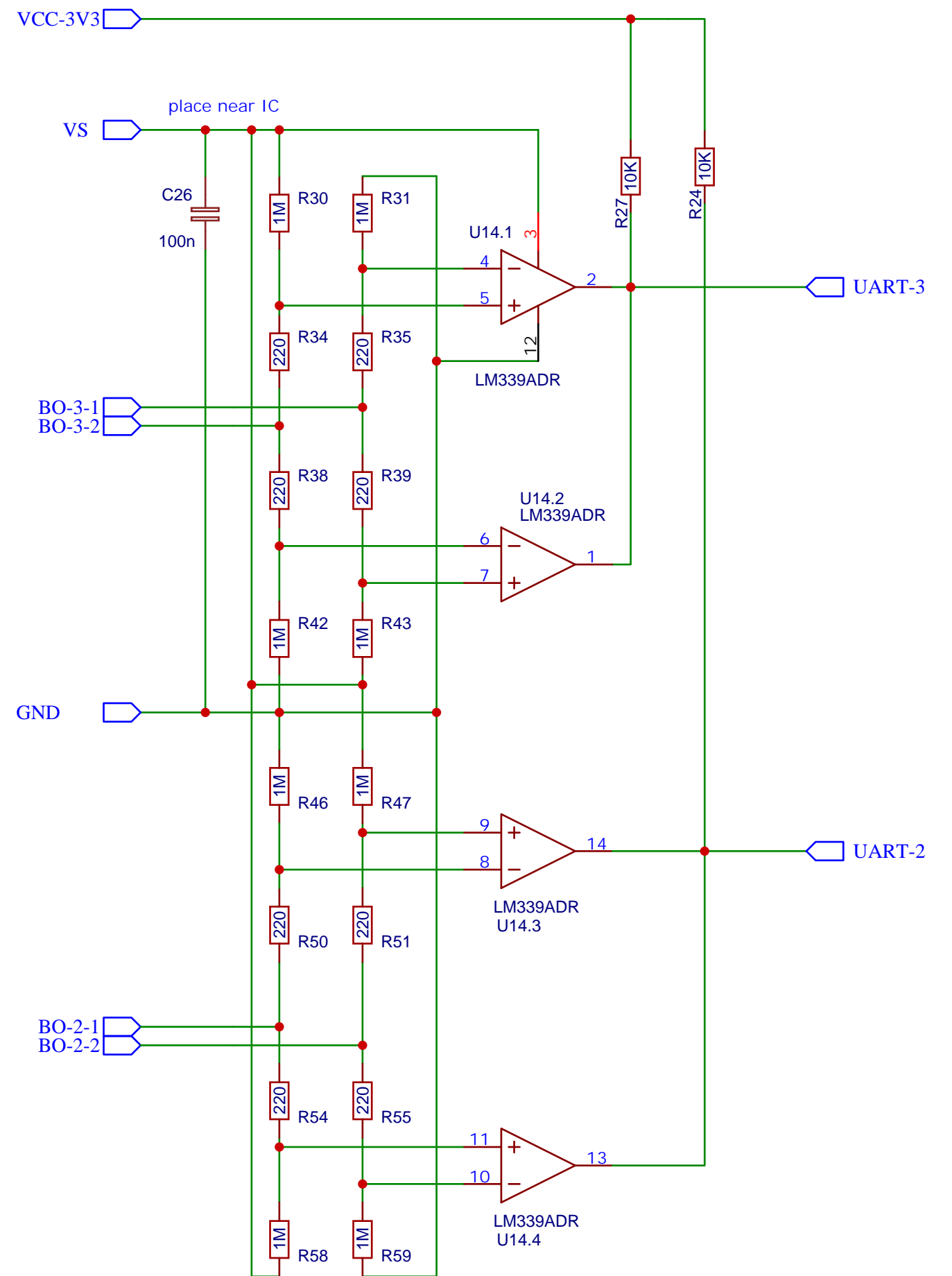
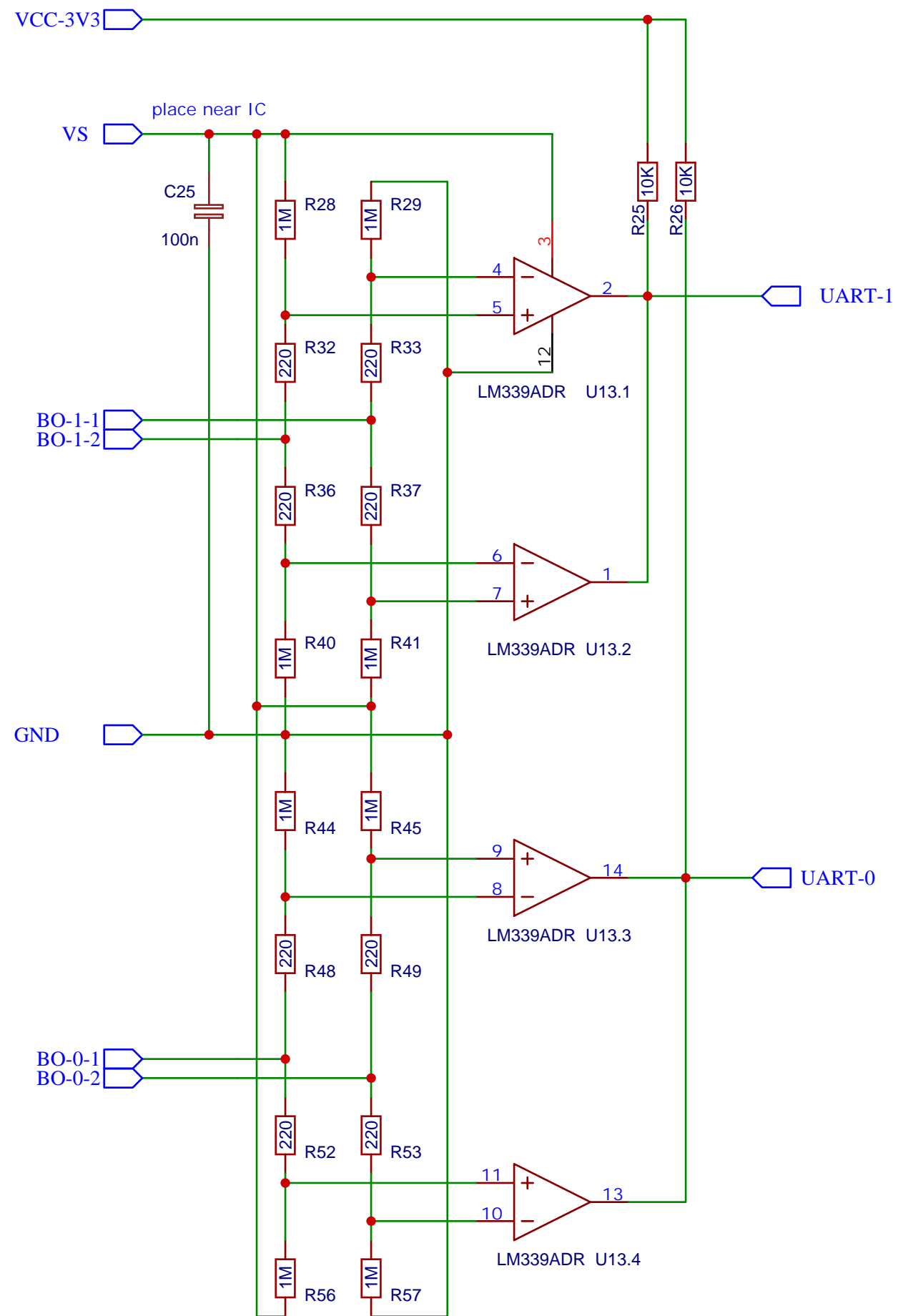
Control Logic Signals:

Sel-2	Sel-1	->	B-x-1	B-x-2	ENB-x	STATE
0	0	->	GND	GND	GND	"Z"
0	1	->	VCC	GND	PWM/BLK	"FWD"
1	0	->	GND	VCC	PWM/BLK	"REV"
1	1	->	DCC1	DCC2	DCC/BLK	"DCC"

ENB == LOW -> Z

H-Bridges





[illegible]

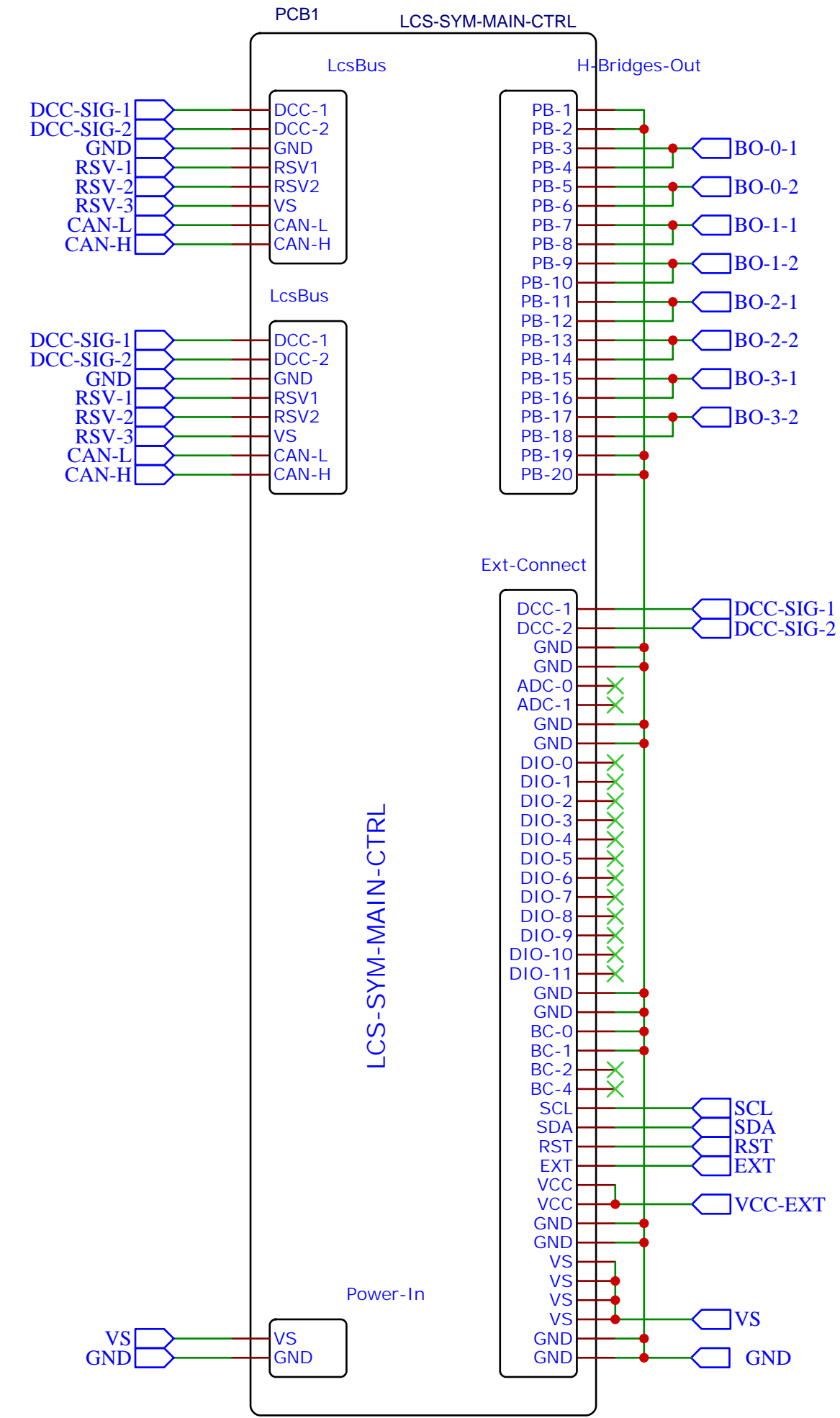
DCC Signal, Cutout and Block Signal.

DCC Input:
00->CUTOUT
01->DCC+
10->DCC-

The diagram illustrates the timing relationship between three signals: DCC, CUT, and BLK. The DCC signal is represented by two lines, DCC+ and DCC-, which are differential. The CUT signal is a single line that is high during the cutout period. The BLK signal is a single line that has two narrow pulses at the start and end of the cutout period. The cutout period is labeled 'Cutout Period' and is indicated by a green line connecting the DCC+ and DCC- lines.

LcsNodes-Quad-Block-Controller-Board - DCC Signal Logic - Page 6 of 7

Block Controller PCB connectors



Power Supply with Powerfail Option

