TWIN-64
Architecture Document

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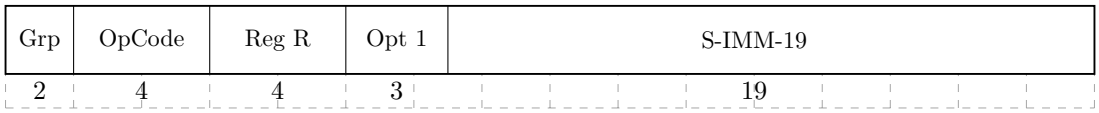
MFCR, MTCR, RSM, SSM, RFI, ITLB, PTLB, PCA, FCA, LDPA, PRBR, PRBW

Instruction Formats

T64 uses few instruction formats. They are grouped by the number of available register slots and the length of the immediate value field.

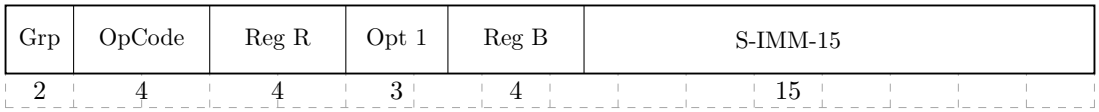
Immediate S19

The immediate S19 instruction format provides one register and a 19 bit signed immediate field. This format is typically used by branch instructions.



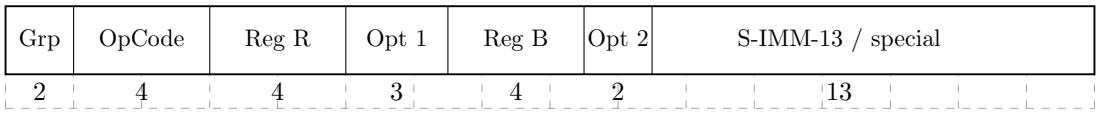
Immediate S15

The immediate S15 instruction format provides two registers and a 15 bit signed immediate field. This format is used by branch instructions as well as instruction which operate on a register and an immediate value.



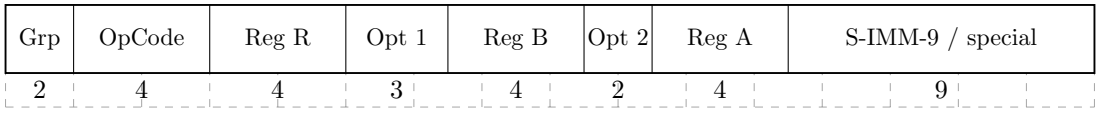
Immediate S13

The immediate S13 instruction format provides two registers, an additional option field and a 13 bit signed immediate field. Some instruction use the S-IMM-13 field for special encodings instead of a signed value. This format is used by memory reference instructions where the address is formed by a base register and a 13-bit signed offset.



Immediate S9

The immediate S9 instruction format provides three registers, an additional option field and a 9 bit signed immediate field. Some instruction use the S-IMM-9 field for special encodings instead of a signed value.instead of a signed value. This instruction format is used for all computational instructions where three registers are needed.



Immediate U20

The immediate U20 format is used by the immediate instruction group to provide a 20bit unsigned value. This value is then placed at certain positions in the register target Reg R.


Grp
OpCode
Reg R
0
U-IMM-20
2
4
4
2
20

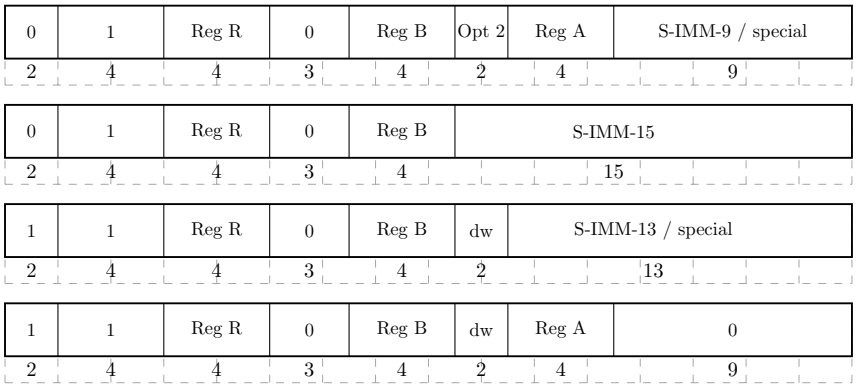
ADD Integer Addition

Syntax

```
ADD RegR, RegB, RegA
ADD RegR, RegB, Immed15
ADD RegR, Immed13( RegB )
ADD RegR, RegX ( RegB )
```

Format

The ADD instruction uses the register, the immediate, the indexed and the register indexed instruction formats.



Description

Adds `RegR` and `RegB`, storing result in `RegR`.

Operation

`RegR <- RegB + RegA` (register format)
`RegR <- RegB + immOperand( )` (immediate format)
`RegR <- RegR + memOperand( )` (indexed formats)

Exceptions

Integer Overflow
Data Alignment
Memory Access Violation
Memory Protection Violation
Data TLB miss

Notes

None.