



# **TWIN-64**

## **Architecture Document**

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# Introduction

## Instruction Formats

Grp	OpCode	Reg R	0	U-IMM-20				
2	4	4	2	20				

Grp	OpCode	Reg R	Opt 1	S-IMM-19				
2	4	4	3	19				

Grp	OpCode	Reg R	Opt 1	Reg B	S-IMM-15			
2	4	4	3	4	15			

Grp	OpCode	Reg R	Opt 1	Reg B	Opt 2	S-IMM-13 / special		
2	4	4	3	4	2	13		

Grp	OpCode	Reg R	Opt 1	Reg B	Opt 2	Reg A	S-IMM-9 / special	
2	4	4	3	4	2	4	9	

This book



# Instruction Set Reference

add general remarks, description format, etc.



## ADD Integer Addition

### Syntax

ADD RegR, RegB, RegA  
ADD RegR, RegB, Immed15  
ADD RegR, Immed13( RegB )  
ADD RegR, RegX ( RegB )

### Format

The ADD instruction uses the register, the immediate, the indexed and the register indexed instruction formats.

0	1	Reg R	0	Reg B	Opt 2	Reg A	S-IMM-9 / special
2	4	4	3	4	2	4	9

0	1	Reg R	0	Reg B	S-IMM-15		
2	4	4	3	4	15		

1	1	Reg R	0	Reg B	dw	S-IMM-13 / special	
2	4	4	3	4	2	13	

1	1	Reg R	0	Reg B	dw	Reg X	0
2	4	4	3	4	2	4	9

### Description

Adds RegR and RegB, storing result in RegR.

### Operation

RegR <- RegB + RegA (register format)  
RegR <- RegB + immOperand( ) (immediate format)  
RegR <- RegR + memOperand( ) (indexed formats)

### Exceptions

OVERFLOW\_TRAP  
ALIGNMENT\_TRAP  
mem ref traps...

### Notes

None.