

# **TWIN-64**

## **Architecture Document**

Helmut Fieres  
June 9, 2025



# Contents

<b>Introduction</b>	<b>1</b>
Concepts . . . . .	1
This Book . . . . .	1
<b>Architecture Overview</b>	<b>3</b>
<b>System Organization</b>	<b>5</b>
Data Types . . . . .	5
General Registers . . . . .	5
Control Registers . . . . .	5
Processor Status Register . . . . .	5
Byte Ordering . . . . .	5
TLB . . . . .	5
Caches . . . . .	5
<b>System Memory</b>	<b>7</b>
Virtual Memory . . . . .	7
Physical Memory . . . . .	7
<b>Addressing and Access Control</b>	<b>9</b>
Address Translation . . . . .	9
Access Control . . . . .	9
Access Protection . . . . .	9
<b>Interrupts</b>	<b>11</b>
Traps . . . . .	11
External Interrupts . . . . .	11
<b>Instruction Set</b>	<b>13</b>
Instruction Overview . . . . .	13
Instruction Formats . . . . .	13
ADD - Integer Addition . . . . .	15



# Introduction

Concepts

This book



# Architecture Overview





# System Organization

Data Types

General Registers

Control Registers

Processor Status Register

Byte Ordering

TLB

Caches



# System Memory

Virtual Memory

Physical Memory



# Addressing and Access Control

Address Translation

Access Control

Access Protection



# Interruptions

## Traps

## External Interrupts





# Instruction Set

## Instruction Overview

### Integer Arithmetic Instructions

ADD, SUB, SHLxA, SHRxA

### Bit Operations Instructions

AND, OR, XOR, EXTR, DEP, DSR

### Immediate Instructions

LDI, ADDIL, LDO

### Memory Reference Instructions

LD, ST, LDR, STC

### Branch Instructions

B, BR, BV, BB, CBR, MBR

### System Instructions

MFCR, MTCR, RSM, SSM, RFI, ITLB, PTLB, PCA, FCA, LDPA, PRBR, PRBW

### memory Access Instructions

## Instruction Formats

Grp	OpCode	Reg R	0	U-IMM-20
2	4	4	2	20

Grp	OpCode	Reg R	Opt 1	S-IMM-19				
2	4	4	3	19				

  

Grp	OpCode	Reg R	Opt 1	Reg B	S-IMM-15			
2	4	4	3	4	15			

  

Grp	OpCode	Reg R	Opt 1	Reg B	Opt 2	S-IMM-13 / special		
2	4	4	3	4	2	13		

  

Grp	OpCode	Reg R	Opt 1	Reg B	Opt 2	Reg A	S-IMM-9 / special	
2	4	4	3	4	2	4	9	

## ADD Integer Addition

### Syntax

ADD RegR, RegB, RegA  
ADD RegR, RegB, Immed15  
ADD RegR, Immed13( RegB )  
ADD RegR, RegX ( RegB )

### Format

The ADD instruction uses the register, the immediate, the indexed and the register indexed instruction formats.

0	1	Reg R	0	Reg B	Opt 2	Reg A	S-IMM-9 / special
2	4	4	3	4	2	4	9

0	1	Reg R	0	Reg B	S-IMM-15		
2	4	4	3	4	15		

1	1	Reg R	0	Reg B	dw	S-IMM-13 / special	
2	4	4	3	4	2	13	

1	1	Reg R	0	Reg B	dw	Reg X	0
2	4	4	3	4	2	4	9

### Description

Adds RegR and RegB, storing result in RegR.

### Operation

RegR <- RegB + RegA (register format)  
RegR <- RegB + immOperand( ) (immediate format)  
RegR <- RegR + memOperand( ) (indexed formats)

### Exceptions

OVERFLOW\_TRAP  
ALIGNMENT\_TRAP  
mem ref traps...

### Notes

None.

