Synthesis of Digital Systems
Lab Lecture -3

Video Processing on ZedBoard
Software Implementation

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Recap from Lab-B

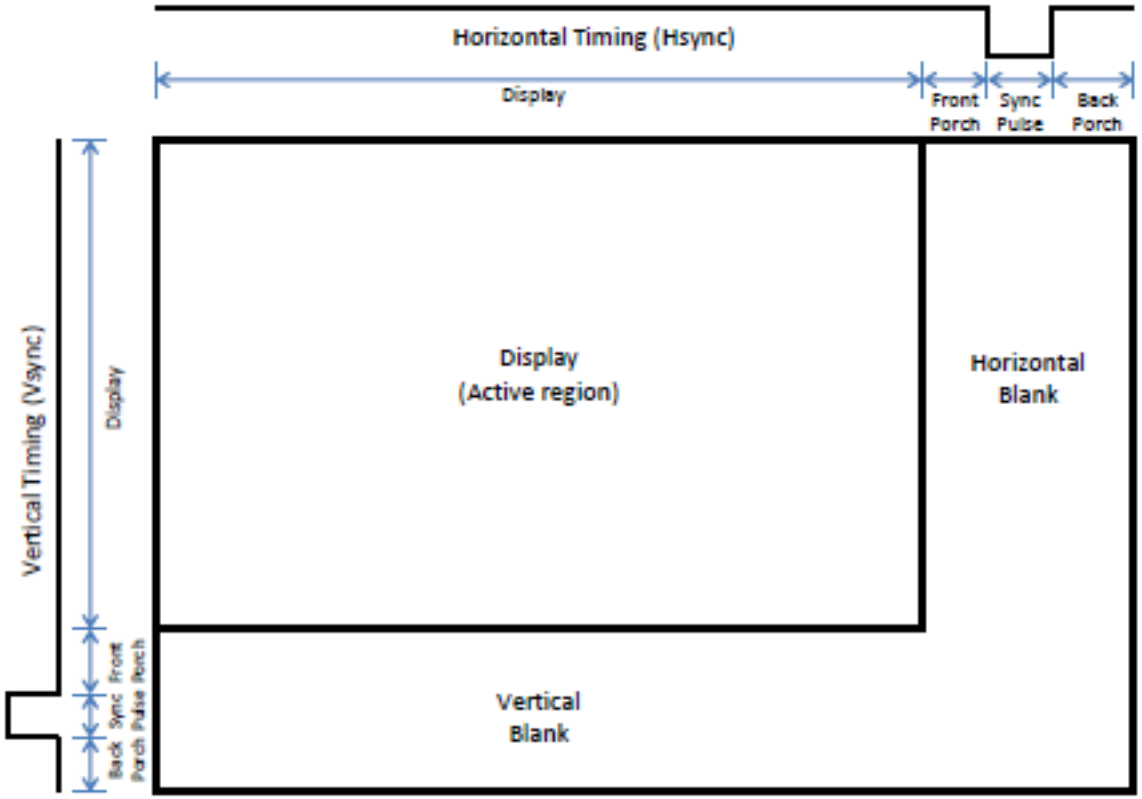
Learnings from Lab-A

- Understanding of High Level Synthesis (HLS).
- Xilinx Tool chain for HLS (Vivado HLS).
- Design constraints and optimization directives.
- Various HLS optimization schemes.
- IP packaging to use it in the IP-library.

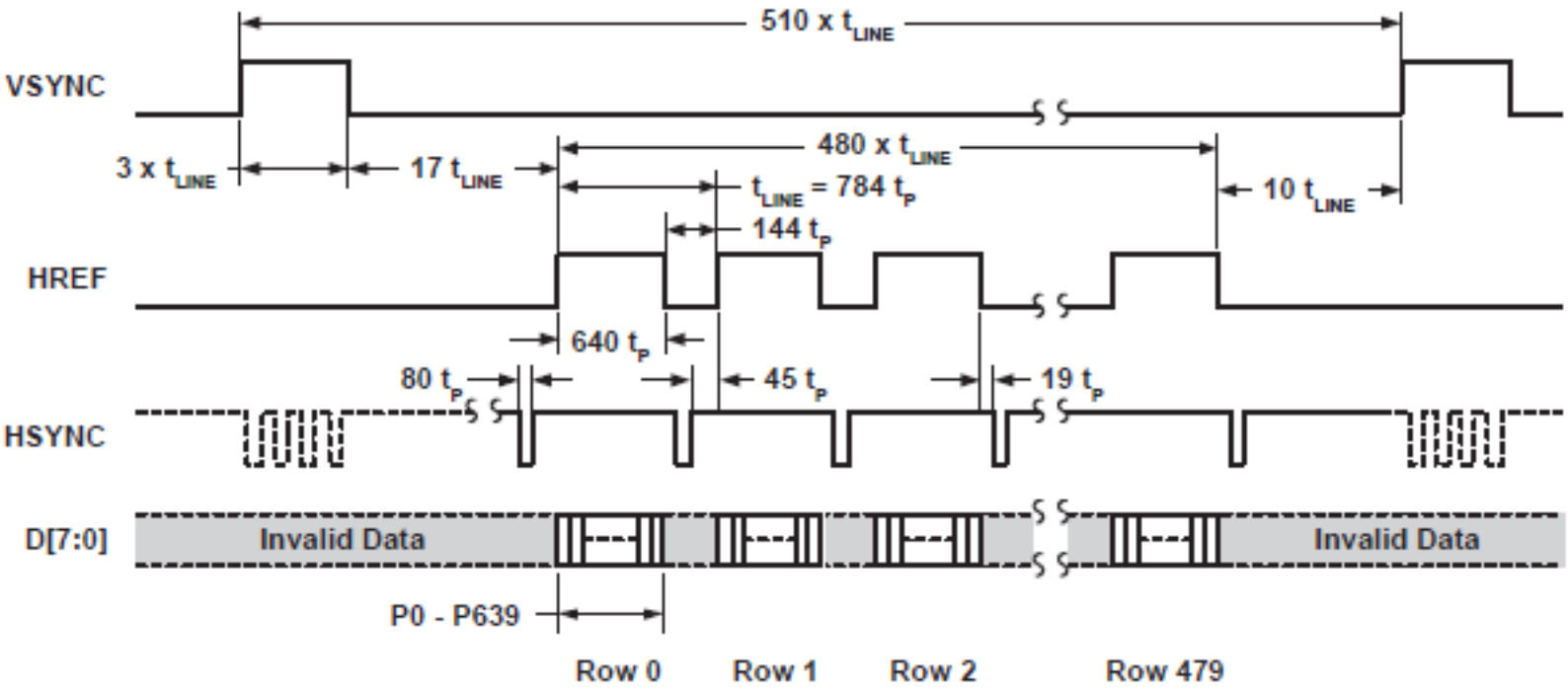
Content of the Lab Course

- System prototyping on FPGA and associated software tool chain.
- Industry standard High Level Synthesis (HLS) tool chain.
- **Implementation of video processing hardware System and software interface.**
- Hardware Accelerator (HA) for performance improvement.

Video Processing SoC: Video Frame Format



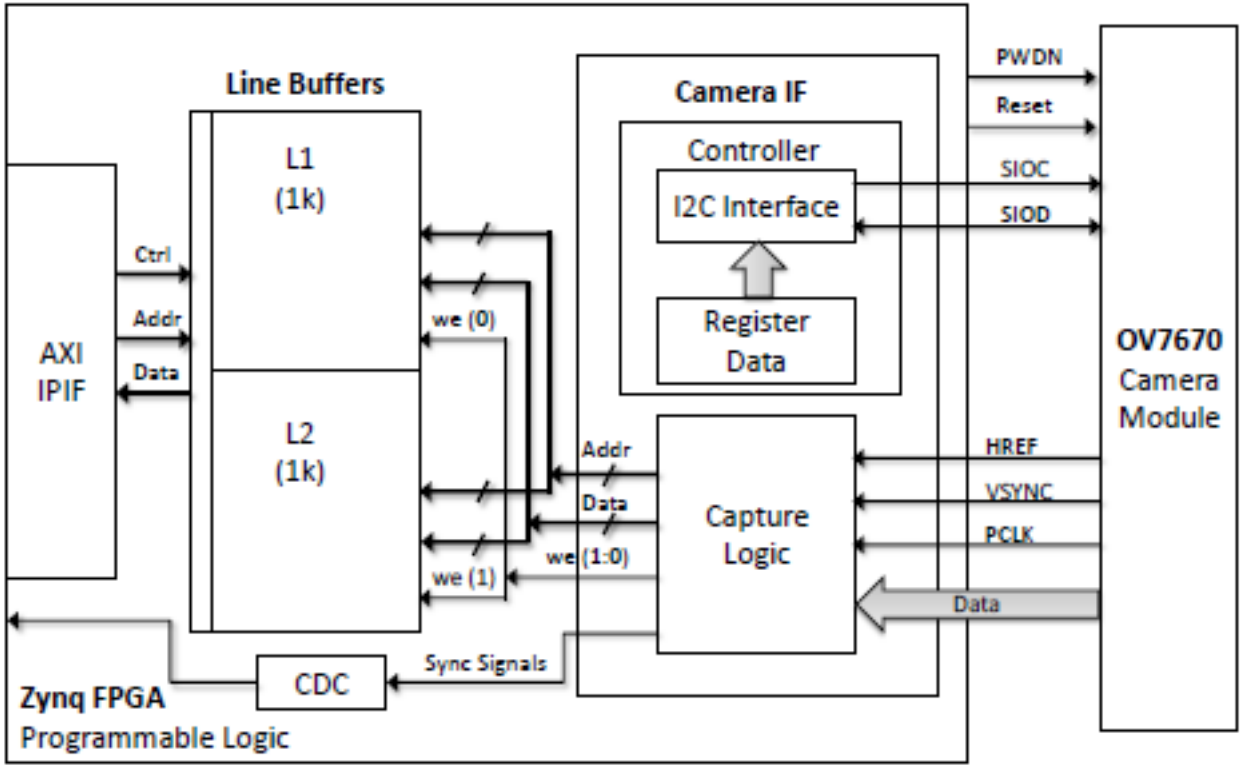
Video Processing SoC: Timing for Video Frame



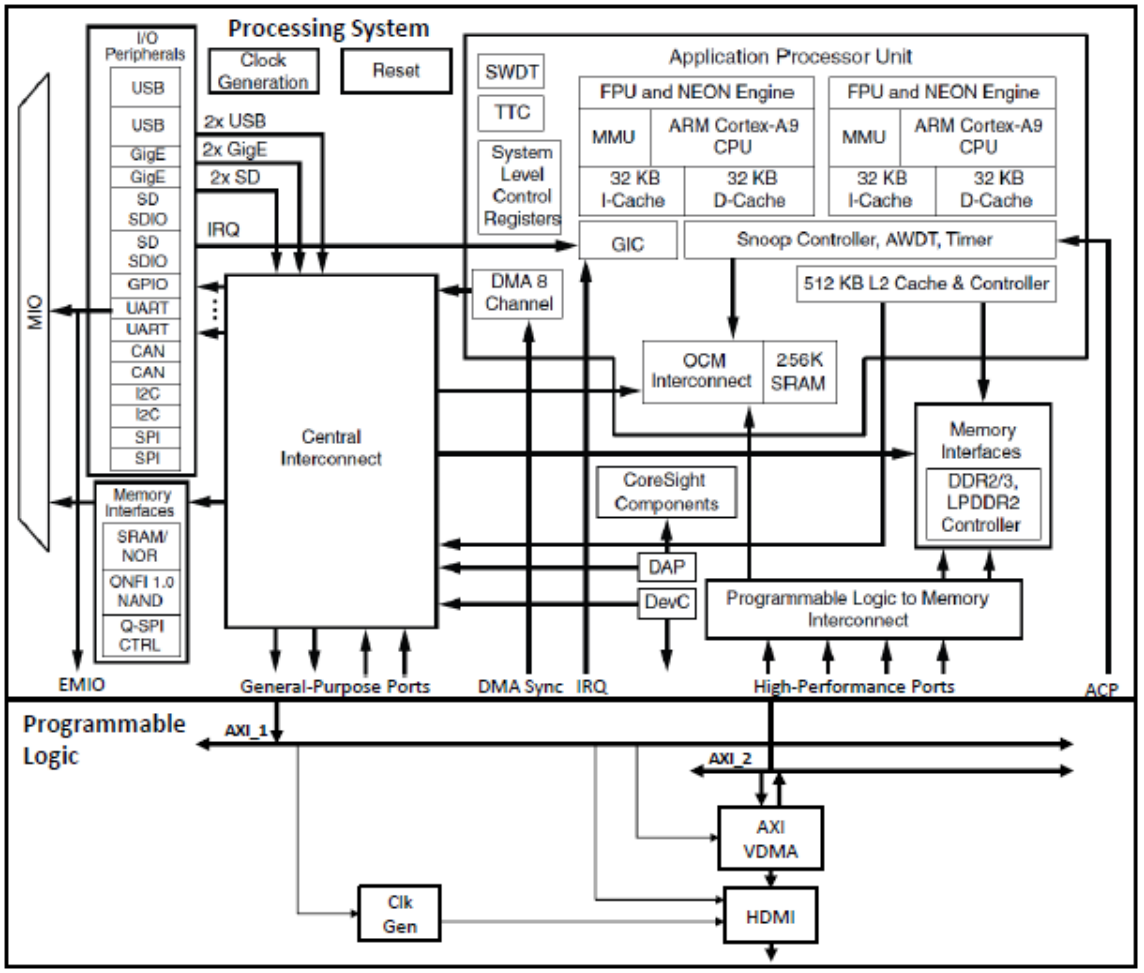
Video Processing SoC: PMOD to OV7670 connections

Name	Type	Description	Pmod connection	Zynq Pin connection
SDIOC	Input	SCCB clock	JB10	V8
SDIOD	In/Out	SCCB data	JB4	W8
VSYNC	Output	Vertical synchronization	JB9	V9
HREF	Output	Horizontal synchronization	JB3	V10
PCLK	Output	Pixel clock	JB8	W10
XCLK	Input	System clock	JB2	W11
D_0	Output	Video data	JA2	AA11
D_1	Output	Video data	JA8	AB10
D_2	Output	Video data	JA3	Y10
D_3	Output	Video data	JA9	AB9
D_4	Output	Video data	JA4	AA9
D_5	Output	Video data	JA10	AA8
D_6	Output	Video data	JB1	W12
D_7	Output	Video data	JB7	V12
RESET	Input	Reset (Active low)	JA7	AB11
PWDN	Input	Power down (Active high)	JA1	Y11
GND	Ground	Camera ground port	GND (JA/JB)	
3V3	Power	Camera power port	VCC (JA/JB)	

Video Processing SoC: Camera Interface



Video Processing SoC: Display Interface



Video Processing SoC: Gray Scale Conversion

- Gray Scale Conversion is a single pixel operation.
- Luminosity method, calculates the weighted average for human perception.

$$Y = (R + G + B)/3$$

$$Y = 0.114R + 0.587G + 0.299B$$

Video Processing SoC: Software Application

File: main.c
Data: Camera video stream
Result: Output stream on display, after processing

```
main() {
<HW Platform initialization >
<ADI peripherals initialization (from Analog devices) >
<HDMI configuration >
<CPU Interrupt controller initilization >
while true do
    if <Keyboard input to change resolution > then
        <Change HDMI configuration to new resolution >
    end
end
return;
}
```

File: axi_interrupt.c

```
AXI_INTERRUPT_VsyncIntr_Handler() {
        <DDRVideoWr: Read form Camera
                     Write to DDR memory>
}
```

Lab C: Steps to follow

1. XPS Project creation and set up of the HDMI display.
2. Adding Camera peripheral core.
3. Software application project in SDK.
4. Hardware set up for Monitor and Camera.
5. FPGA programming and software application execution on ZedBoard.
6. Software application for Gray scale conversion.

Thank You

for your participation