Introduction to Zynq Hardware

Lab 1

Building a Basic Zynq Design

November 2013
Version 02

Lab Setup

To complete all of the Speedway labs, the following software and hardware setups are required.

Software

The recommended software for this Speedway is:

- O/S supported by Xilinx Vivado 2013.3
  - See UG973 v2013.3 *Release Notes* for the supported list
  - Windows-7 64-bit was used to develop this Speedway
- Xilinx Vivado SDK 2013.3
- MicroZed users:
  - Silicon Labs CP201x USB-to-UART Bridge Driver
    - www.microzed.org → Documentation → MicroZed Silicon Labs CP210x USB-to-UART Setup Guide v1.2
- ZedBoard users:
  - Cypress CY7C64225 USB-to-UART Bridge Driver
    - www.zedboard.org → Documentation → ZedBoard Cypress USB-to-UART Setup Guide

Hardware

The recommended target hardware consists of the following:

- PC with minimum amount of RAM available for Xilinx tools as specified at www.xilinx.com/design-tools/vivado/memory.htm for either the 7Z010 or 7Z020 device
- Avnet MicroZed or ZedBoard
- USB cable (Type A to Micro-USB Type B)
- MicroZed users:
  - JTAG Programming Cable (Xilinx Platform Cable, Digilent HS1 or HS2 cable)
    - If you don't already have a JTAG Cable, Avnet recommends the Digilent HS2 Cable
    - http://www.em.avnet.com/en-us/design/drc/Pages/Digilent-JTAG-HS2-Programming-Cable.aspx
- ZedBoard Users:
  - Second USB cable (Type A to Micro-USB Type B)
  - AC/DC 12V Power Adapter

Lab Instruction Notes

Throughout all the Speedway labs, a generalized instruction is given. If you're comfortable completing the task based on that instruction, feel free to do so. If not, step-by-step instructions are provided.

Technical Support

For technical support with any of the labs, please contact your local Avnet/Silica FAE or visit the support forum for MicroZed and ZedBoard:

www.zedboard.org/forum

www.microzed.org/forum

Additional technical support resources are listed below.

Evaluation Kit home pages with Documentation and Reference Designs

www.zedboard.org

www.microzed.org

Xilinx technical support

You may contact your local Avnet/Silica FAE or Xilinx Online Technical Support at www.support.xilinx.com . On this site you will also find the following resources for assistance:

- Software, IP, and Documentation Updates
- Access to Technical Support Web Tools
- Searchable Answer Database with Over 4,000 Solutions
- User Forums
- Training - Select instructor-led classes and recorded e-learning options

Avnet technical support

Contact your Avnet/Silica FAE or the forums for any additional questions regarding the MicroZed or ZedBoard reference designs, kit hardware, or if you are interested in designing any of the kit devices into your next design.

Lab 1 Overview

Vivado Design Suite WebPACK is free and includes all the required tools for creating new FPGA and SoC designs as well as the Software Development Kit (SDK) for developing software. Both MicroZed and ZedBoard kits include a Vivado® Design Suite license voucher which adds Vivado Logic Analyzer capability which will be required to complete the labs.

Unlike a traditional processor, the Zynq Processing System (PS) has a configurable set of built-in peripherals. Additionally it has direct access to Programmable Logic (PL) that can build virtually any custom IP. That said, the PS may be used without anything programmed in the PL. However, in order to use any soft IP in the PL, or to route PS dedicated peripherals to device pins in the PL, programming of the PL is required.

This lab will illustrate how to create a new Zynq project from scratch using Vivado's graphical block design methodology.

Lab 1 Objectives

When you have completed Lab 1, you will know how to do the following:

- Create a new project in Vivado from scratch
- Target the Zynq 7Z010 or 7Z020 device
- Create a new block design utilizing Vivado's IP Integrator design flow
- Add an Embedded ARM processor core to the project

Experiment 1: Create a new Zynq Project in Vivado

Vivado has awareness of several Xilinx development boards built-in, as well as the Avnet ZedBoard and MicroZed. However we will build this design from scratch, just as you would for a custom Zynq design.

Experiment 1 General Instruction:

Launch Vivado 2013.3. Create a New project in the Speedway directory. **C:\Speedway\ZynqHW\2013_3**

Experiment 1 Step-by-Step Instructions:

1. Launch Vivado 2013.3 from either the desktop icon or **Start → All Programs → Xilinx Design Tools → Vivado 2013.3 → Vivado 2013.3**

2. Click on **Create New Project**.

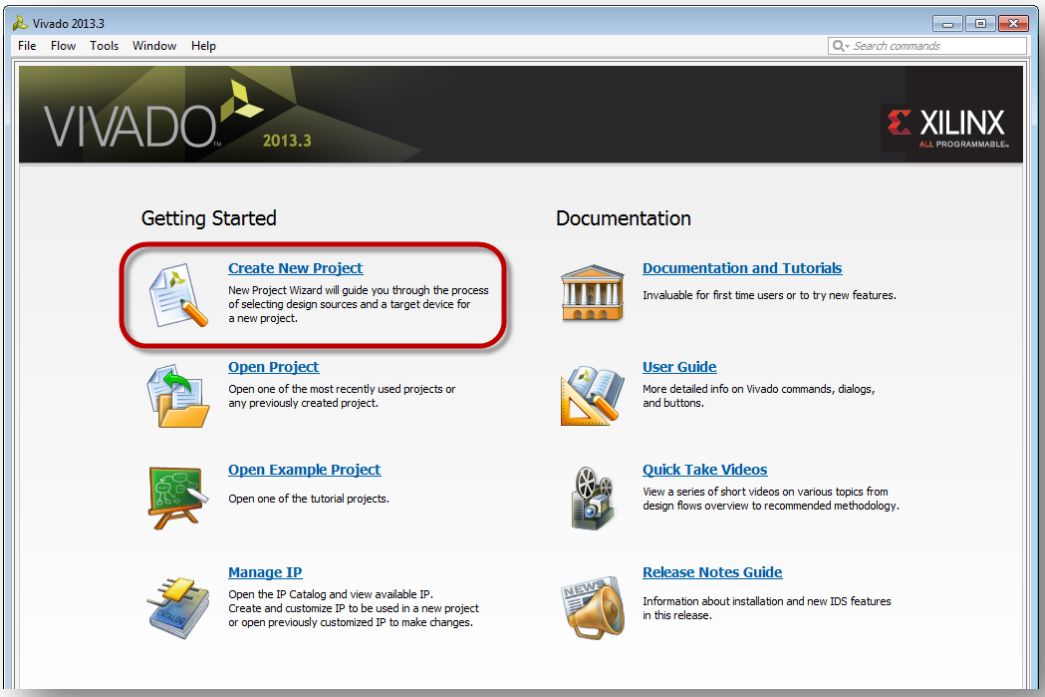

Figure 1 - Vivado Project Creation

3. Click **Next >** in the New Project window.

4. Set the *project name* to **ZynqDesign** and *project location* to the following directory:

C:/Speedway/ZynqHW/2013_3

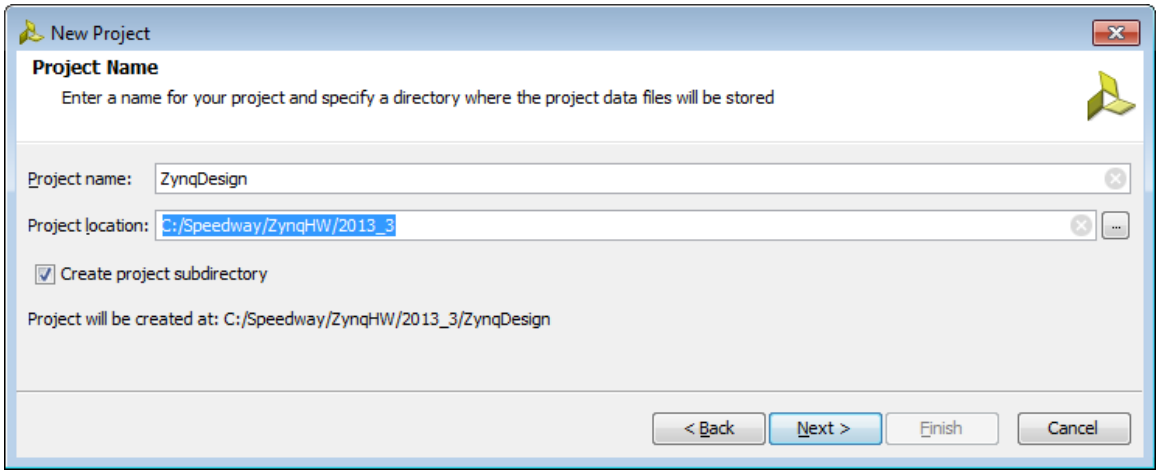

Figure 2 - New Project Name and Location

5. Click **Next >.**

6. For Project type, this will be a RTL-based project, thus leave the radio button for *RTL Project* selected.

7. Check the box for **Do not specify sources at this time**. Click **Next >.**

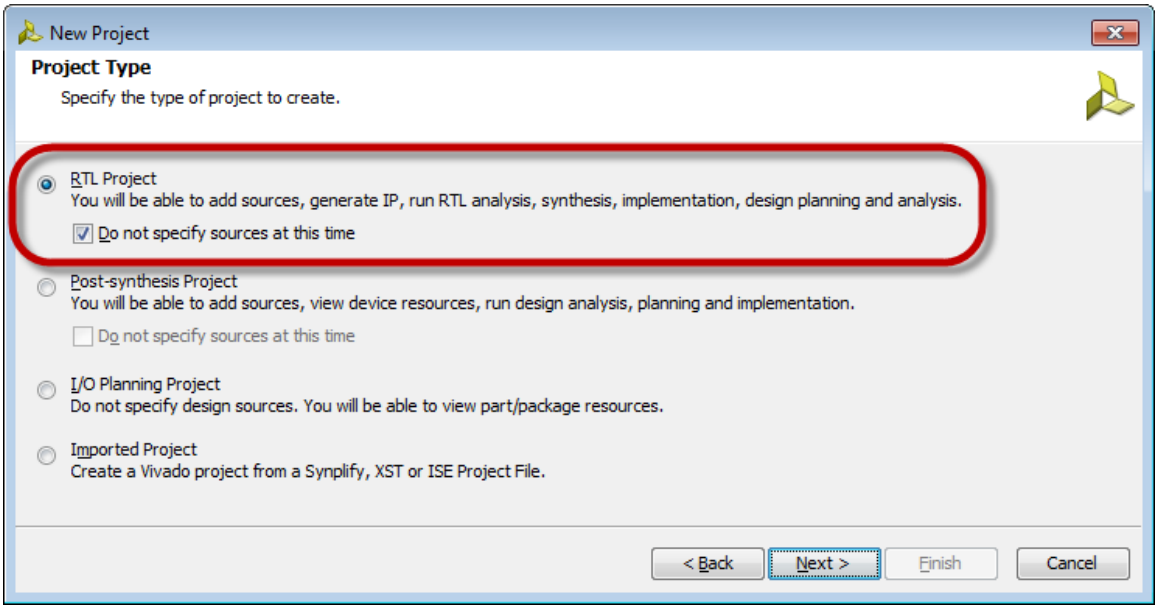

Figure 3 - Project Type Settings

8. Next, select the target device for this design. This can be done by choosing a specific part or by selecting a board. While we can immediately target MicroZed and ZedBoard here, we will not do so as the goal of this tutorial is to learn how to create a custom design from scratch. Choose *Parts* option selected under *Specify*.

   Select the following:

   - Product category — General Purpose
   - Family — Zynq-7000
   - Sub-Family — Zynq-7000
   - Package — CLG400 (MicroZed) or CLG484 (ZedBoard)
   - Speed grade — -1
   - Temp grade — C

   This should minimize the part options:

   For MicroZed select the **xc7z010clg400-1** device.
   For ZedBoard select the **xc7Z020clg484-1** device.

   click **Next >**.

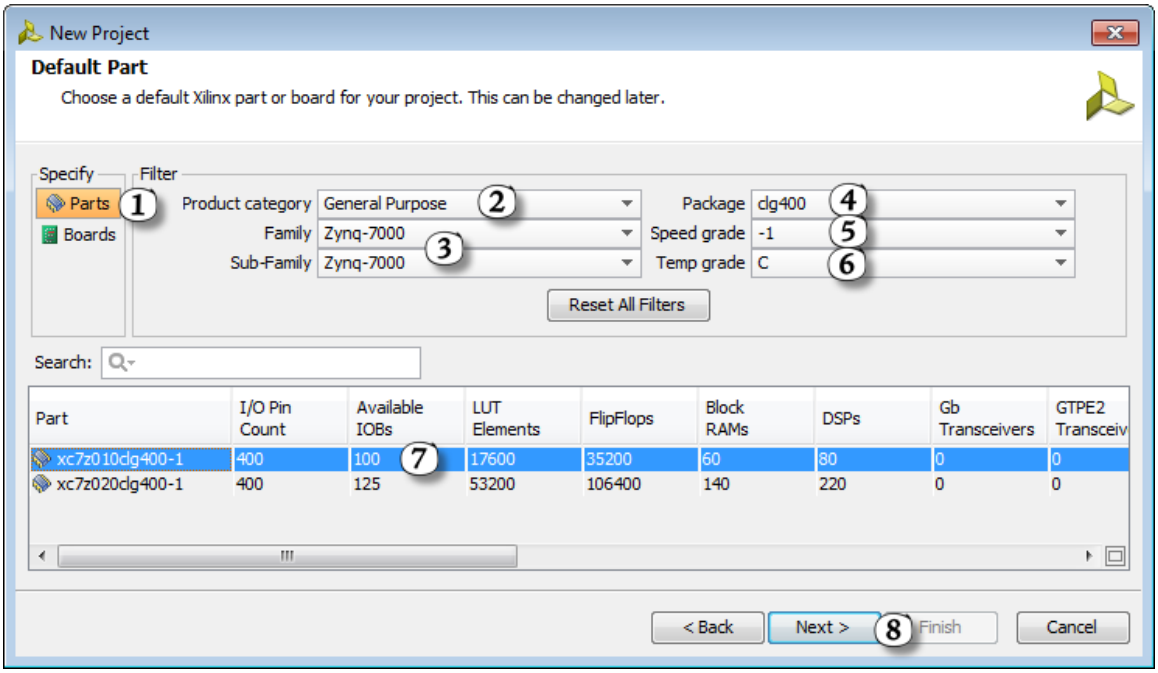

Figure 4 – Target Device - MicroZed Configuration

9. The following project summary is displayed. Click **Finish**.

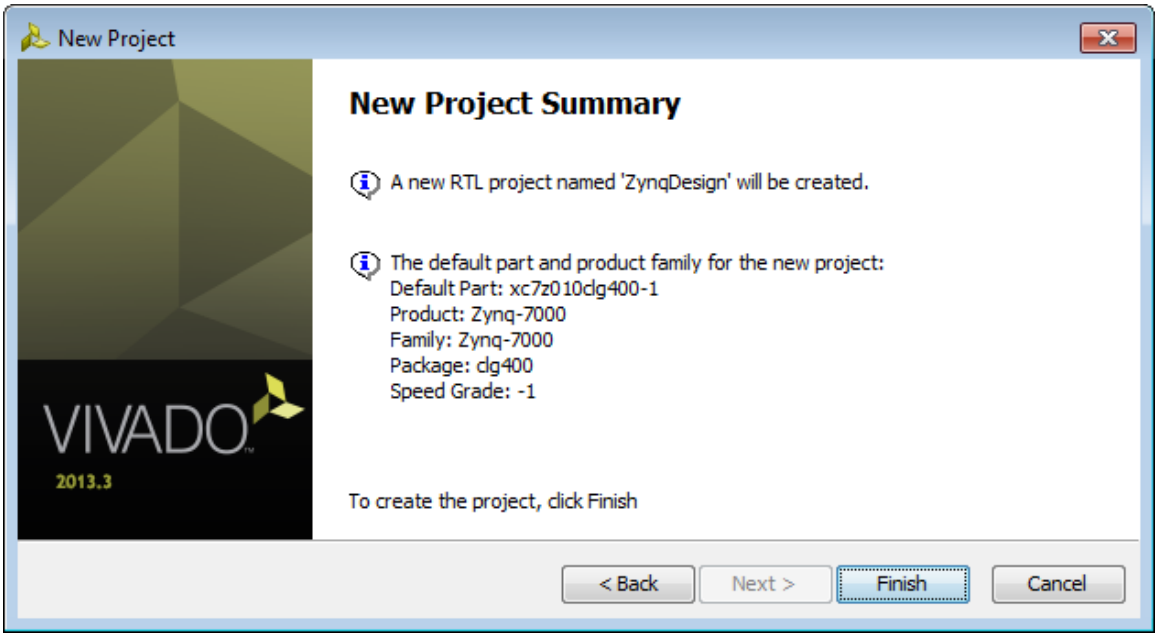

Figure 5 - New Project Summary (MicroZed)

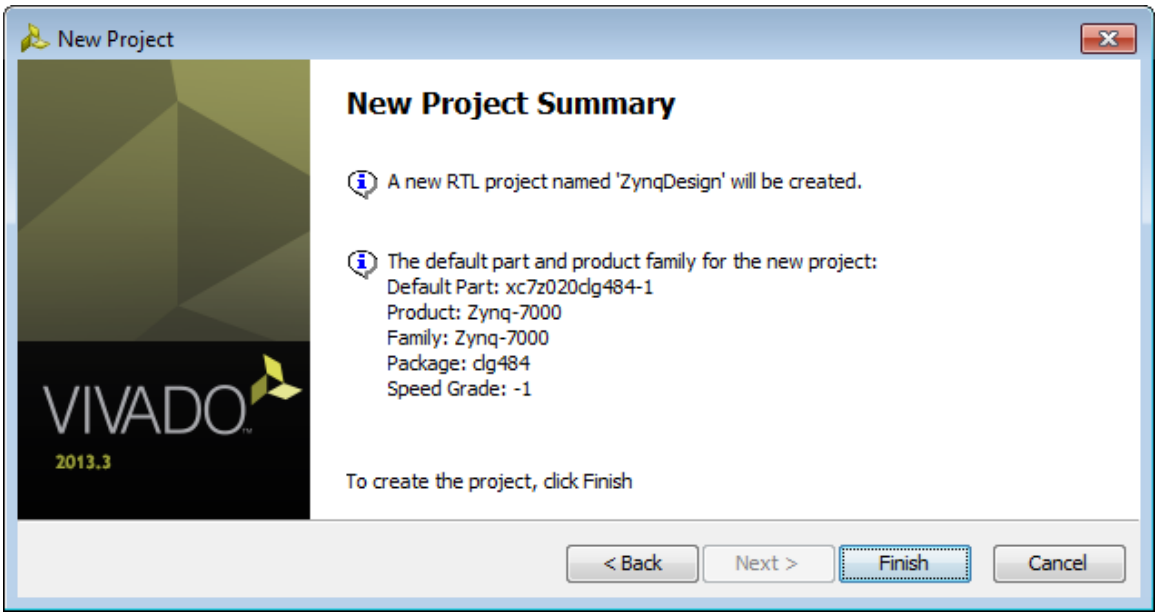

Figure 6 - New Project Summary (ZedBoard)

The Vivado design cockpit will open. Take a minute to explore what's available and answer the questions below. PlanAhead users may find this familiar.

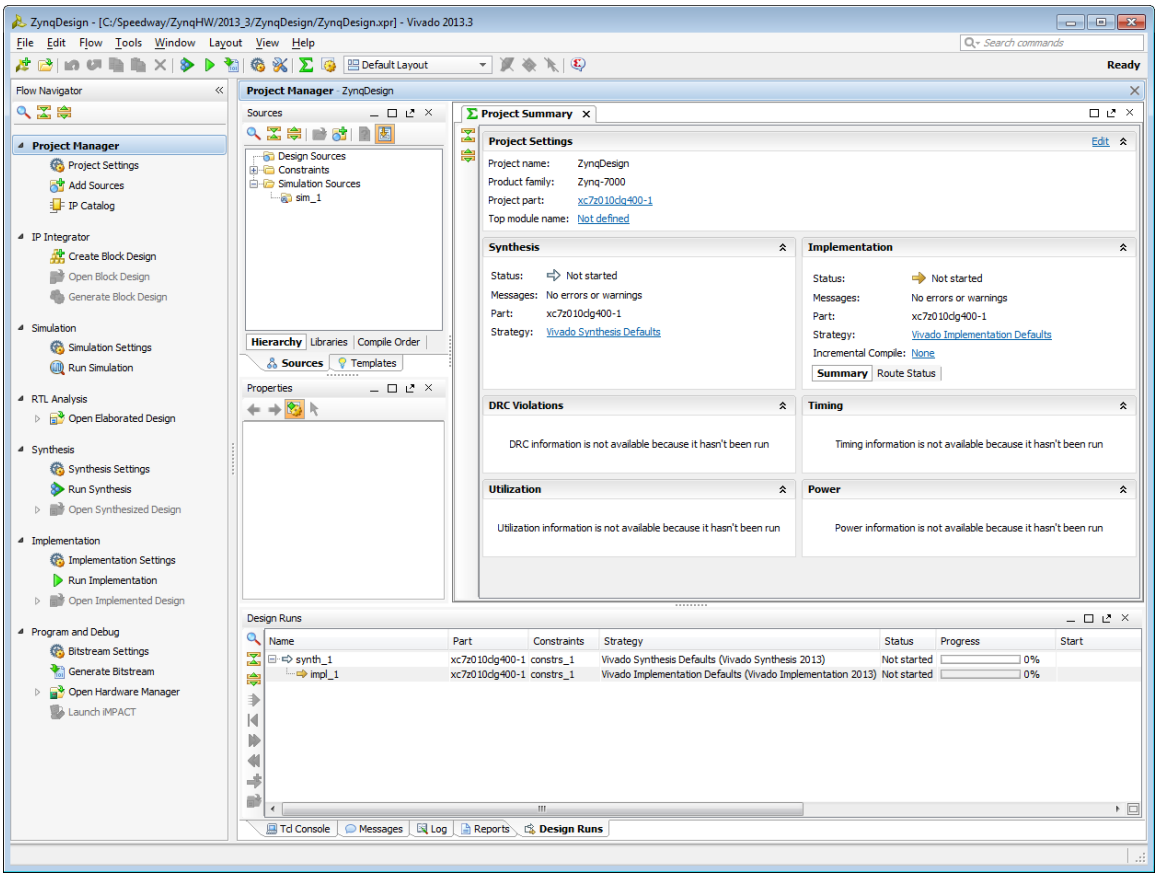

Figure 7 - Vivado Design Cockpit

Questions:

Answer the following questions:

- *What device is selected? What is the Top Module Name?*

_____

- *What are the Vivado Synthesis and Implementation Strategies?*

_____

- *What other information is available in the Project Summary?*

_____

Experiment 2: Create a new Block Design in Vivado

The current project is blank. To access the ARM processing system, we will add an embedded source to the Vivado Project by creating a block design using IP Integrator.

Experiment 1 General Instruction:

Create a block design and add a processor core.

Experiment 2 Step-by-Step Instructions:

1. Under IP Integrator, select **Create Block Design**.

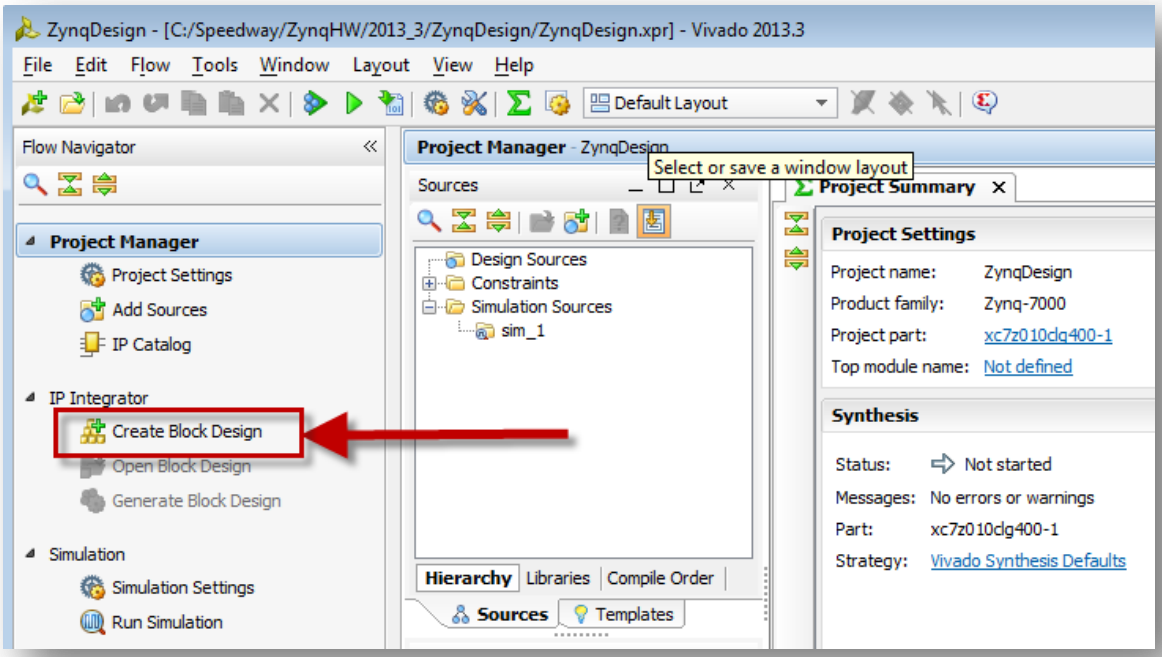

Figure 8 - Create Block Design

2. Enter the name**, Z_system**, for the block design name. Click **OK**.

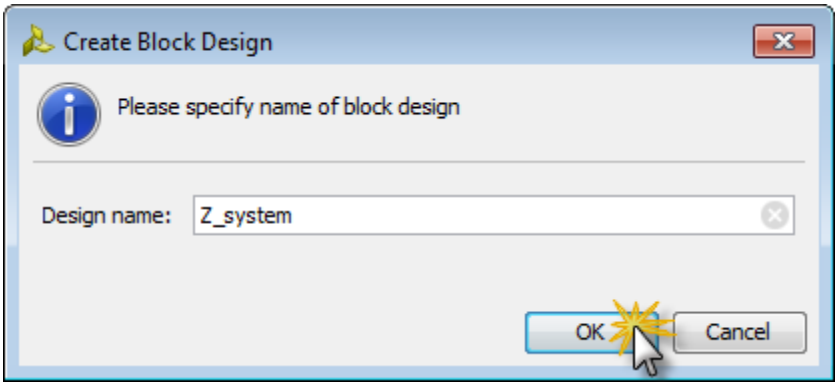

Figure 9 - Block Design Name

3. The Z_system Diagram window will open; select **Add IP** from the green notification bar or from the vertical navigation bar shortcuts.

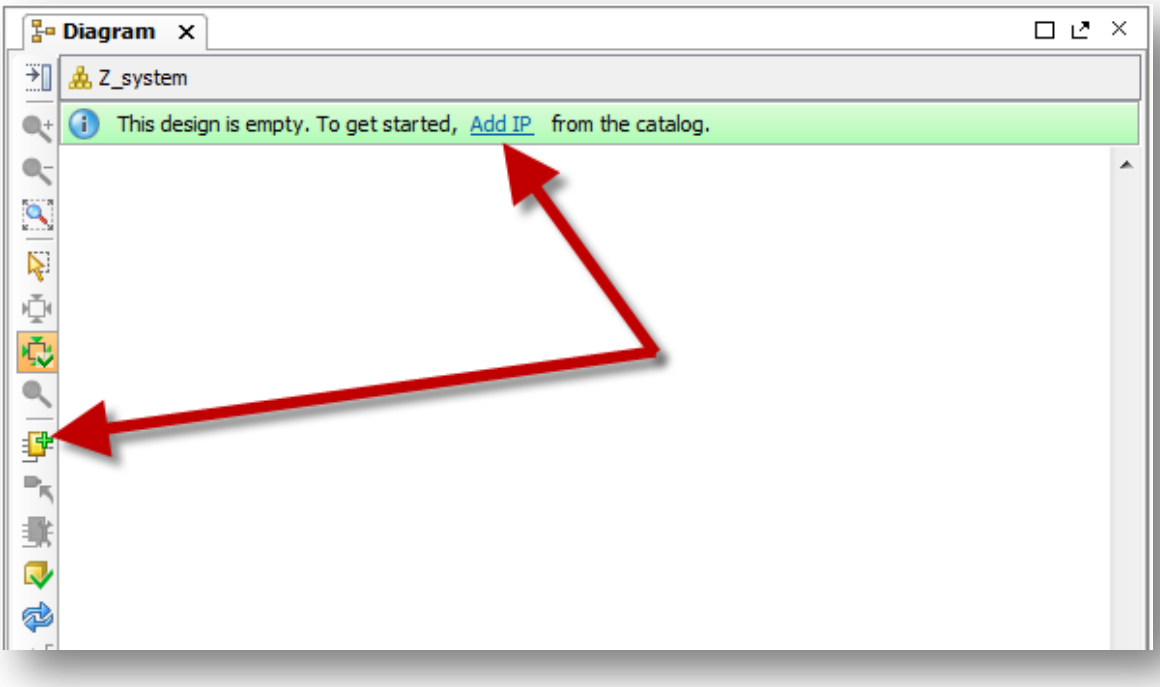

Figure 10 - Add IP

4. In the search window, type **zynq** to filter through the IP. Double-click **ZYNQ7 Processing System**.

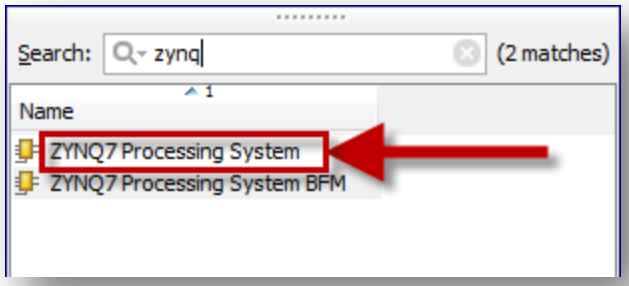

Figure 11 - Zynq Processing System IP

5. The block diagram will now show a *processing_system7_0* IP block. Notice a green navigation bar has reappeared offering *Designer Assistance*. Many of the IPs in a block design can be automatically connected by selecting Run Block Automation. Click on **Run Block Automation** then **/processing_system7_0** to perform this task on the ARM processing core.

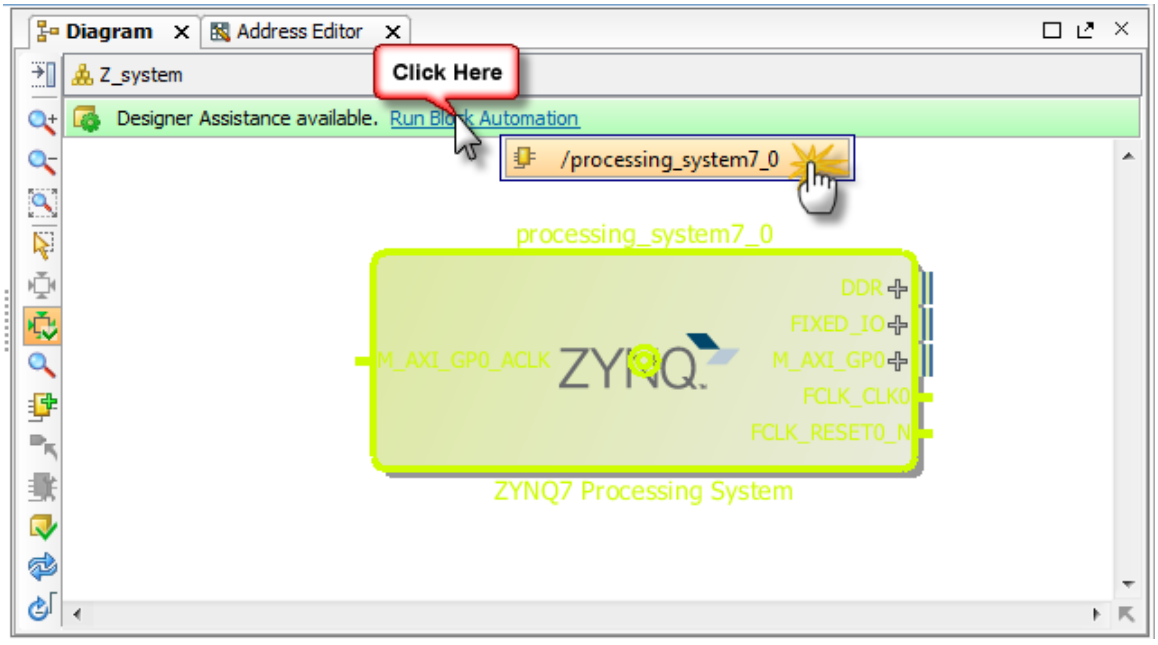

Figure 12 - Run Block Automation

6. The wizard automatically detects it needs to connect external interfaces for FIXED_IO and DDR interfaces. FIXED_IO are I/O dedicated to internal hardened peripherals in the Zynq processing subsystem. These include UARTs, Ethernet, USB and more IP. We'll cover this more later. For now, click **OK** to make these external connections. This simply defines these ports as external interfaces to the block design. Note, the block design may be a small piece of a larger design, thus its external interfaces must be defined.

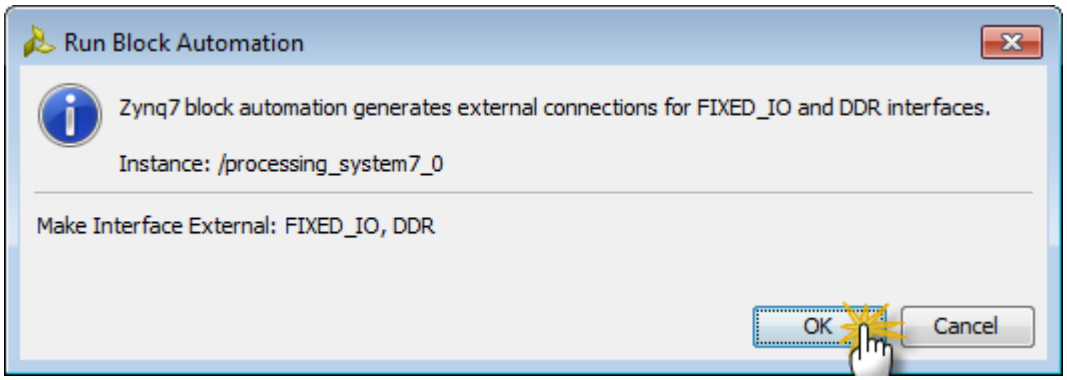

Figure 13 - Click OK to connect external interfaces

Two external ports are now connected to the IP core:

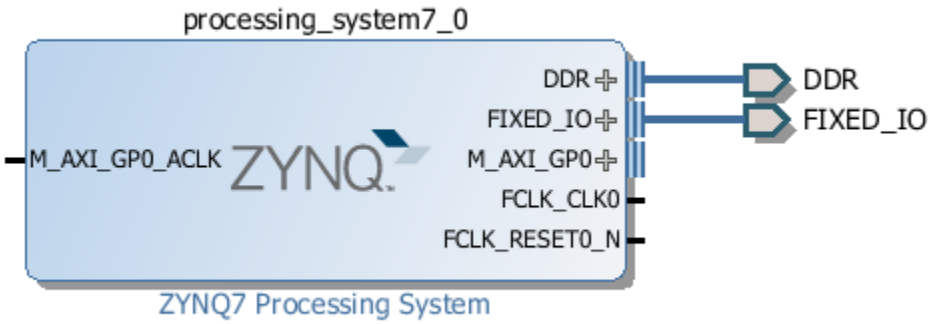

Figure 14 - External Port Connections

7. This is a good time to save the block design. Click the **Save Block Design** button to save the block design.

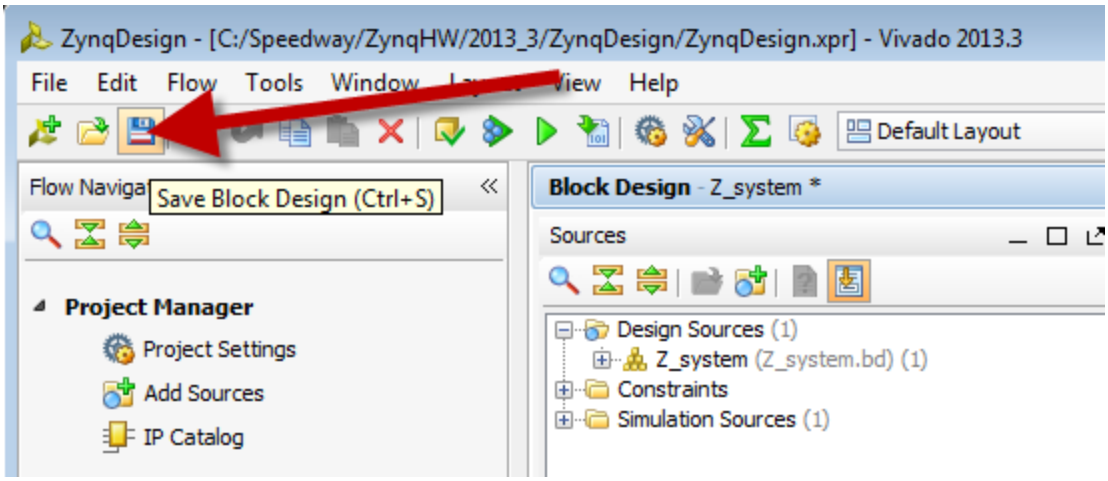

Figure 15 - Save Block Design

8. At this point, the ZYNQ7 Processing System (PS) is completely unconfigured. To start customizing our design, double-click on **the ZYNQ7 Processing System** IP block. Most IP can be customized this way.

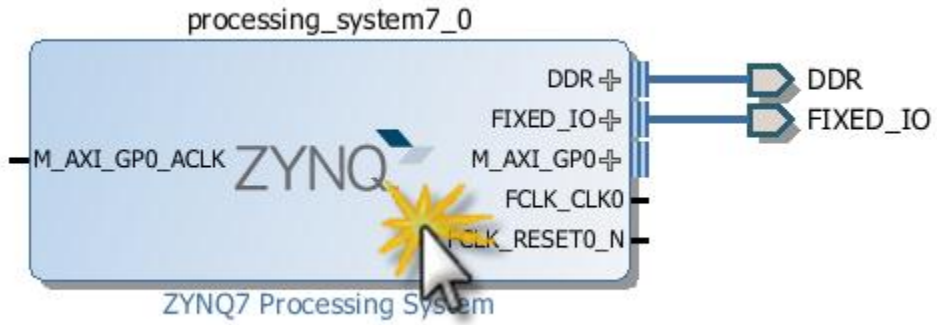

Figure 16 - Double-click on IP to customize the IP

The Zynq Recustomize IP window is now available. Here we can customize the Zynq processing core. All PS features are in their default state, ready to be customized, which is what we will do in the next two labs.

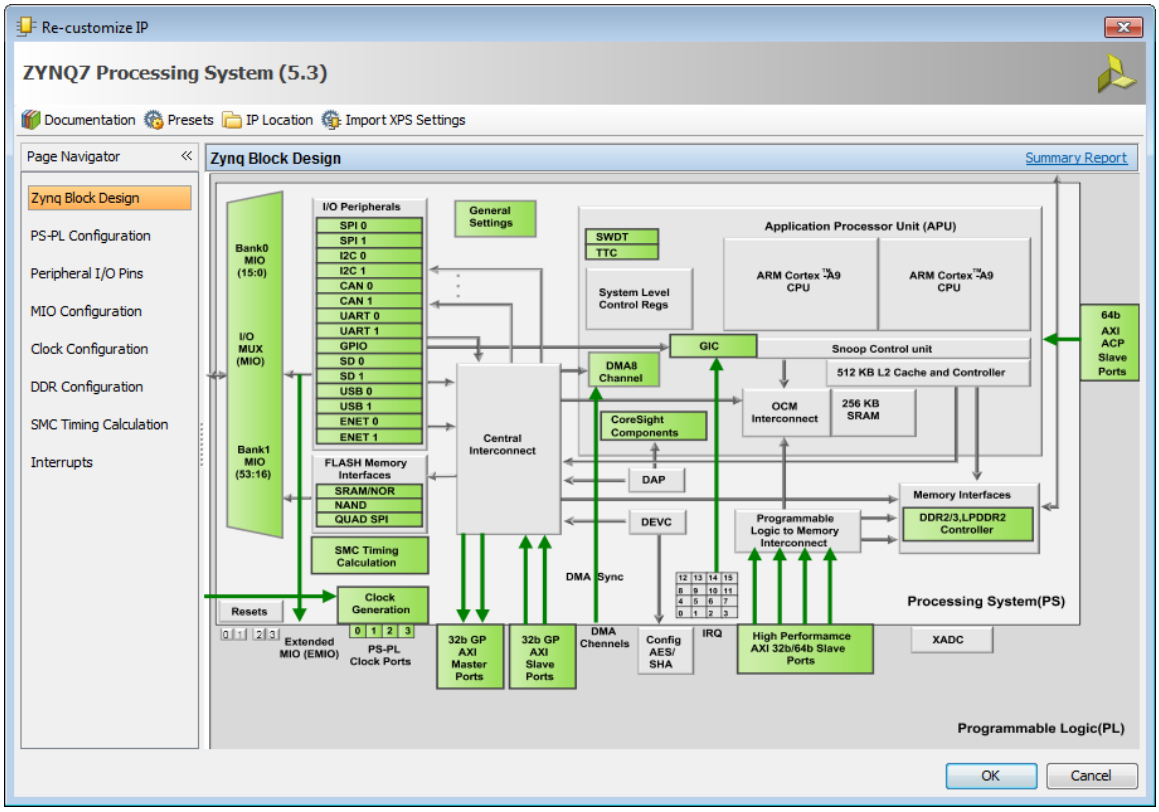

Figure 17 - Re-Customize IP window for the Zynq PS

We now have a new project created and we've added an embedded processing core!

Leave the tools open as Lab 2 starts from this point.

Questions:

Answer the following questions:

- *List some of configurable components, highlighted green boxes in the Zynq PS?*

_____

- *The I/O Peripherals are connected to external I/O through the I/O Mux (MIO), how many I/O are available in the MIO?*

_____

Exploring Further

If you have more time and would like to investigate more…

- Explore some of the configurable PS blocks.
- Open the Zynq Technical Reference Manual (TRM) and view the available sections. This can be found in the Support Documents folder or online: http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf
- For ISE or PlanAhead users, open the Migration Methodology Guide. This document provides instruction for porting designs from ISE to Vivado. Also updating UCF constraints to XDC. This can be found in the Support Documents folder, or online: http://www.xilinx.com/support/documentation/sw_manuals/xilinx2012_3/ug911-vivado-migration.pdf

This concludes Lab 1.

Revision History

Date	Version	Revision
6 Nov 2013	02	Initial Draft

Resources

www.microzed.org

www.zedboard.org

www.xilinx.com/zynq

www.xilinx.com/sdk

www.xilinx.com/vivado

Answers

Experiment 1

- *What device is selected? What is the Top Module Name?*

For MicroZed it is xc7z010clg400-1. For ZedBoard it is xc7z020clg484-1.
The top module name has not been defined yet. But when created, will appear under *Design Sources*.

- *What are the Vivado Synthesis and Implementation Strategies?*

Both are set to Default

- *What other information is available in the Project Summary?*

Synthesis and Implementation status, DRC violations, timing results, device utilization statistics and power information.

Experiment 2

Answer the following questions:

- *List some of configurable components in the Zynq PS?*

I/O Peripherals, General Settings, Flash Memory Interfaces, Clock Generation, AXI Ports, DDR Memory Controller, and more.

- *The I/O Peripherals are connected to external I/O through the I/O Mux (MIO), how many I/O are available in the MIO?*

54 Total – 16 in MIO Bank 0 and 38 in MIO Bank 1.