

Zynq MicroZed	
Avnet Engineering Services	
www.microzed.org	
Function	Sheet Number
Cover Sheet	1
Block Diagram	2
DDR3	3
QSPI FLASH, Micro SD	4
ETHERNET, USB	5
BANK 34, BANK 35	6
BANK 0, BANK 13, JTAG	7
MICROHEADERS JX1, JX2	8
FPGA POWER	9
POWER, RESET	10
Back Page	11



MicroZed_Prod

28 Jan 2014

7:51:21 PM

Copyright 2013, Avnet, Inc. All Rights Reserved.

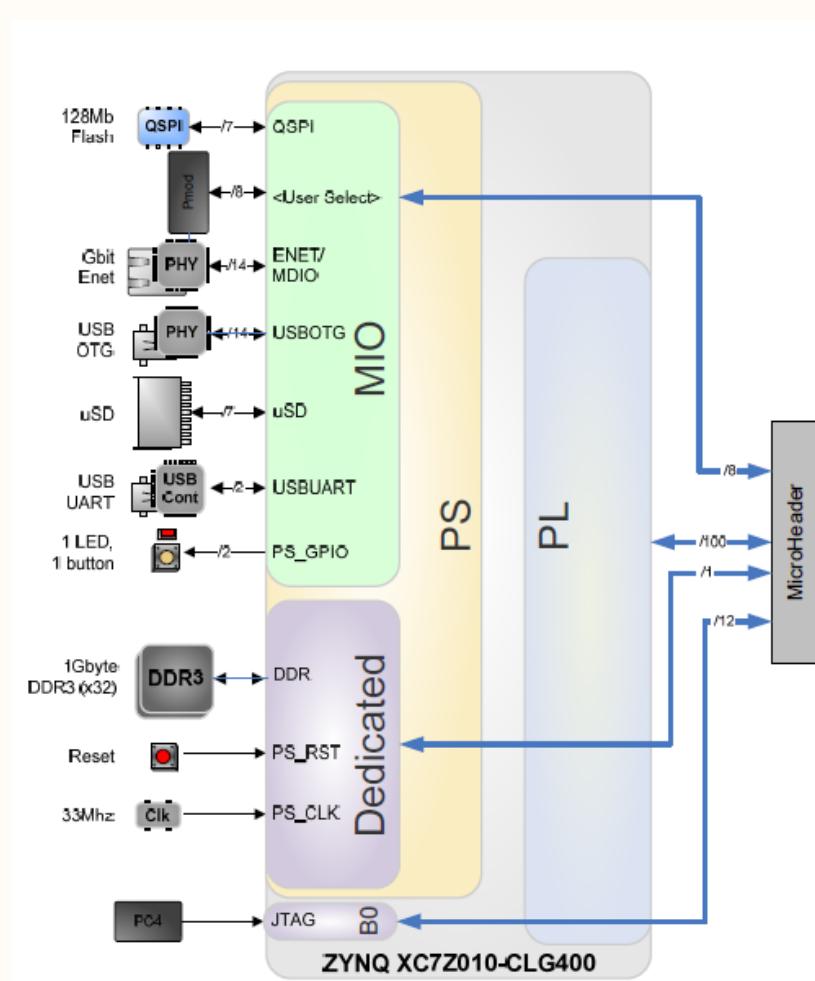
This material may not be reproduced, distributed, republished, displayed, posted, transmitted or copied in any form or by any means without the prior written permission of Avnet, Inc. AVNET and the AV logo are registered trademarks of Avnet, Inc. All trademarks and trade names are the properties of their respective owners and Avnet, Inc. disclaims any proprietary interest or right in trademarks, service marks and trade names other than its own.

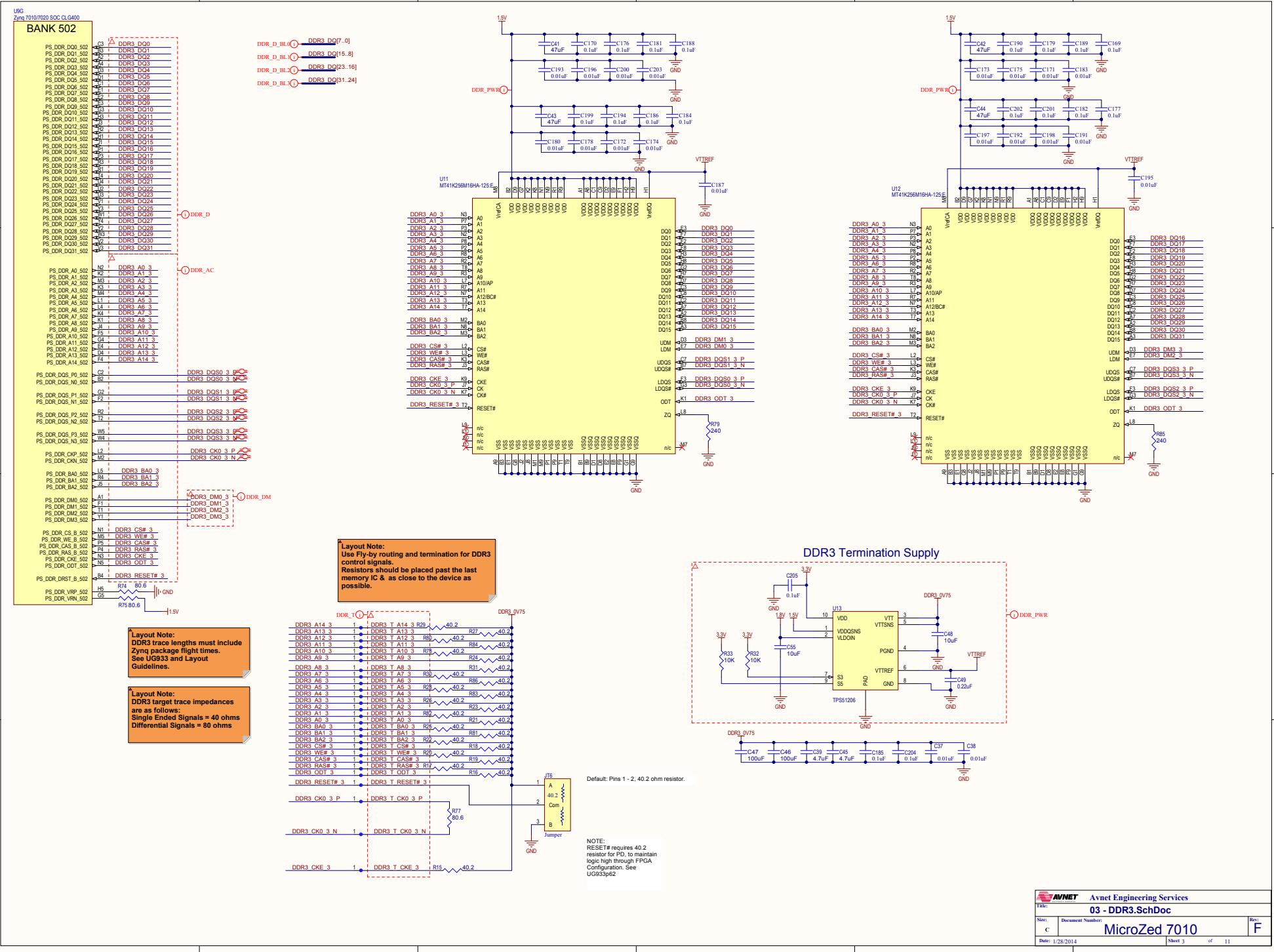
D Avnet is not responsible for typographical or other errors or omissions or for direct, indirect, incidental or consequential damages related to this material or resulting from its use. Avnet makes no warranty or representation respecting this material, which is provided on an "AS IS" basis. AVNET HEREBY DISCLAIMS ALL WARRANTIES OR LIABILITY OF ANY KIND WITH RESPECT THERETO, INCLUDING, WITHOUT LIMITATION, REPRESENTATIONS REGARDING ACCURACY AND COMPLETENESS, ALL IMPLIED WARRANTIES AND CONDITIONS OF MERCHANTABILITY, SUITABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TITLE AND/OR NON-INFRINGEMENT. This material is not designed, intended or authorized for use in medical, life support, life sustaining or nuclear applications or applications in which the failure of the product could result in personal injury, death or property damage. Any party using or selling products for use in any such applications do so at their sole risk and agree that Avnet is not liable, in whole or in part, for any claim or damage arising from such use, and agree to fully indemnify, defend and hold harmless Avnet from and against any and all claims, damages, loss, cost, expense or liability arising out of or in connection with the use or performance of products in such applications.

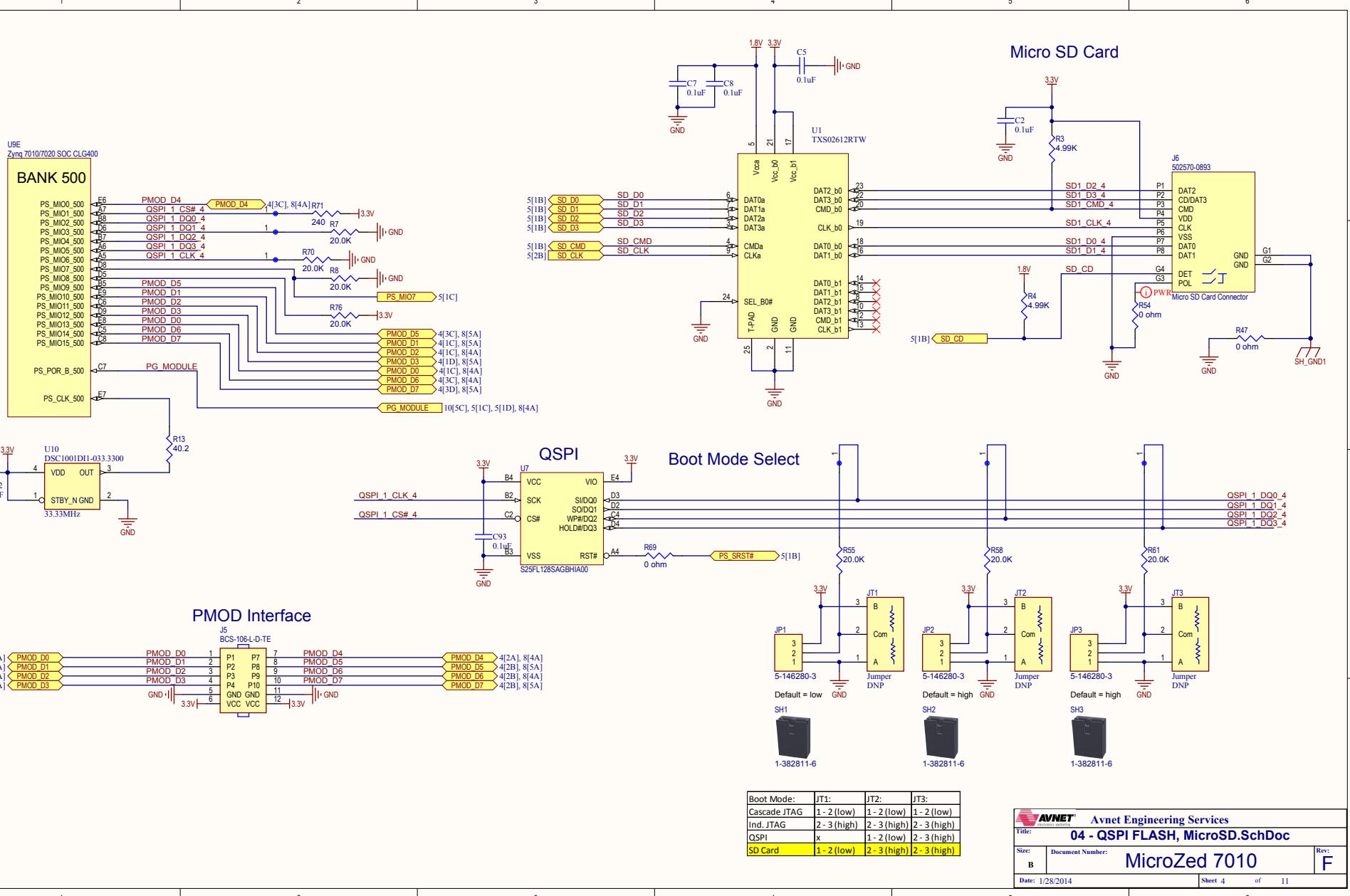
	AVNET® Avnet Engineering Services
Title:	01 - Avnet Lead Sheet_B.SchDoc
Size:	Document Number: MicroZed 7010
B	Rev: F

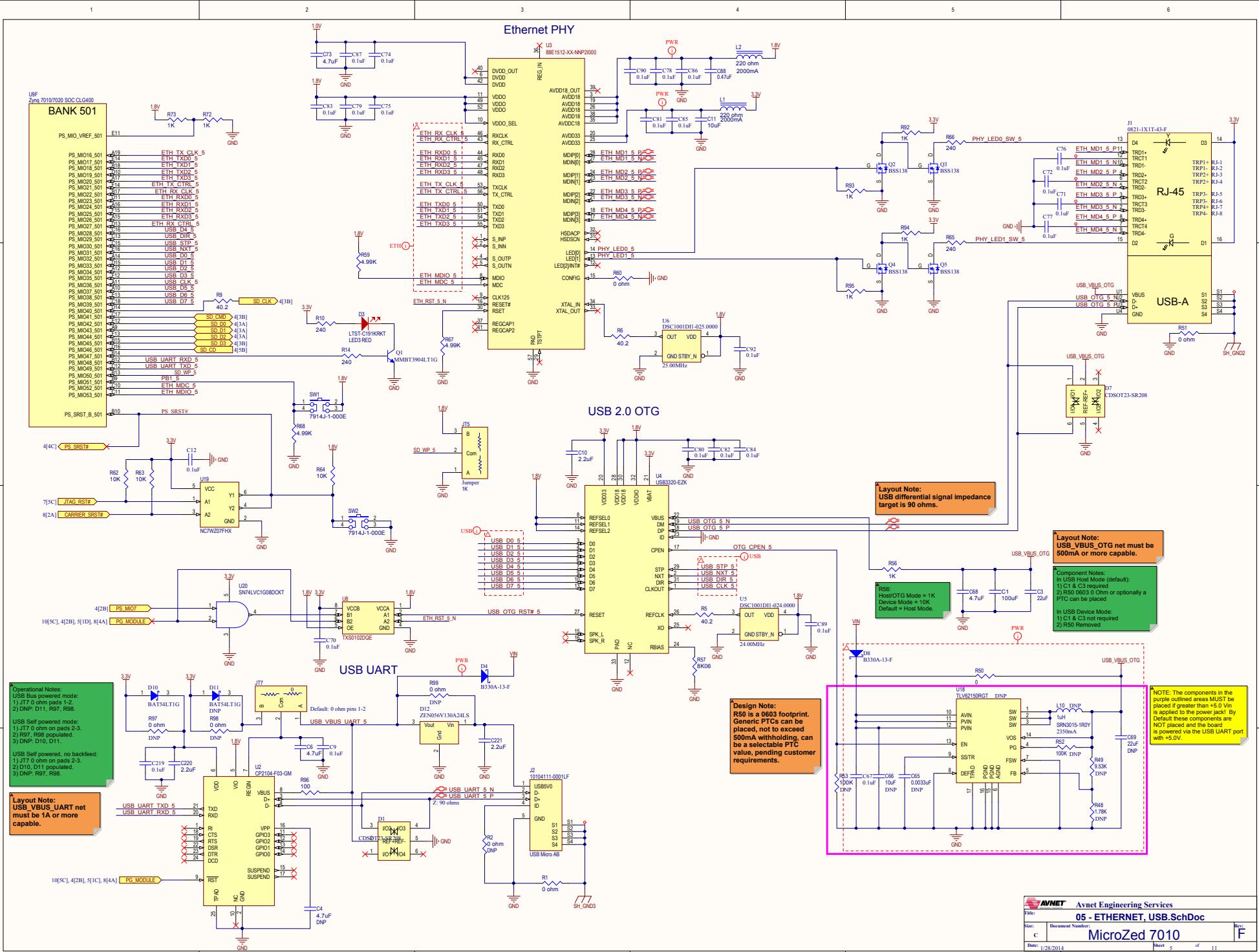
Date: 1/28/2014

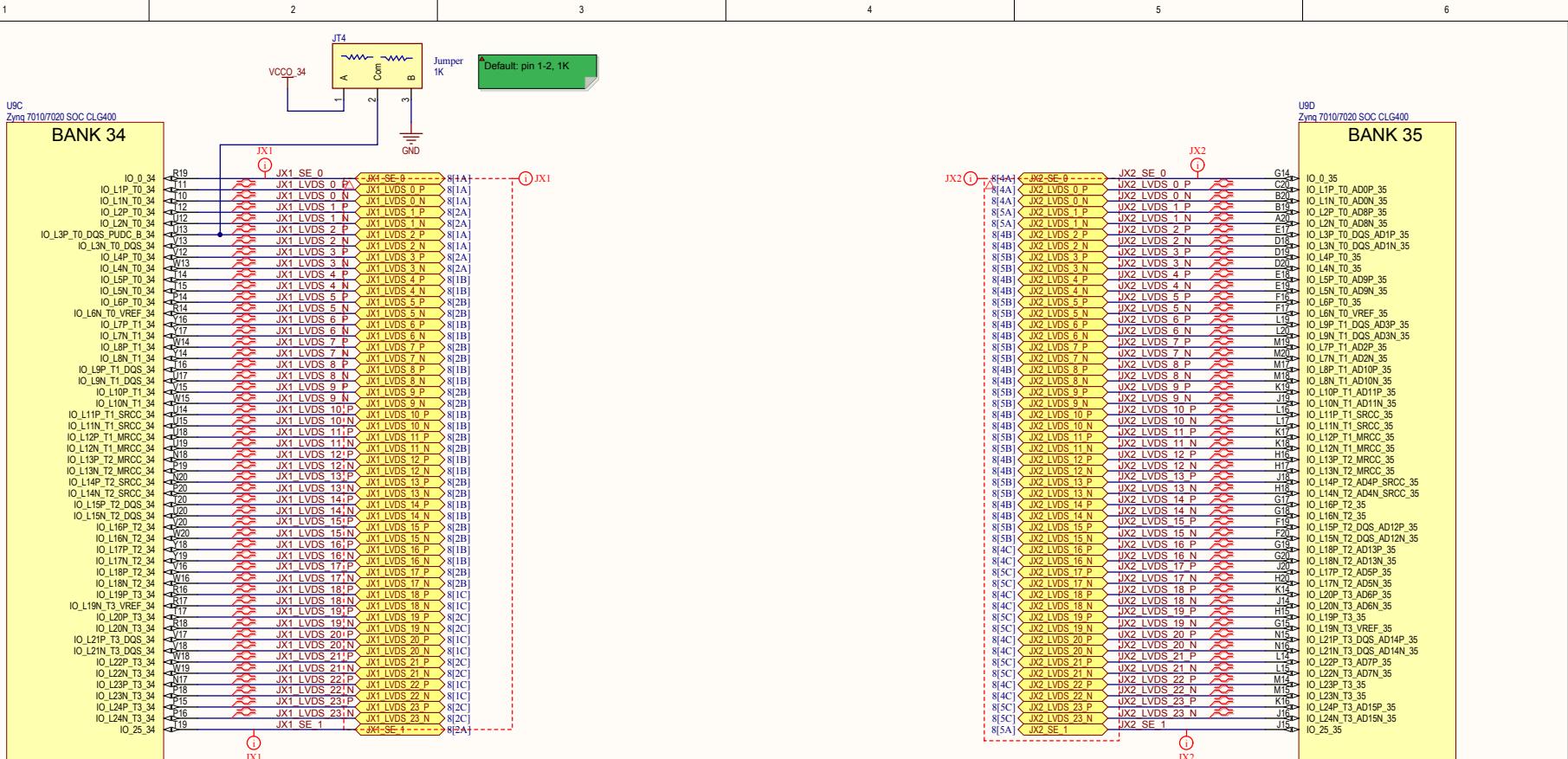
Sheet 1 of 11

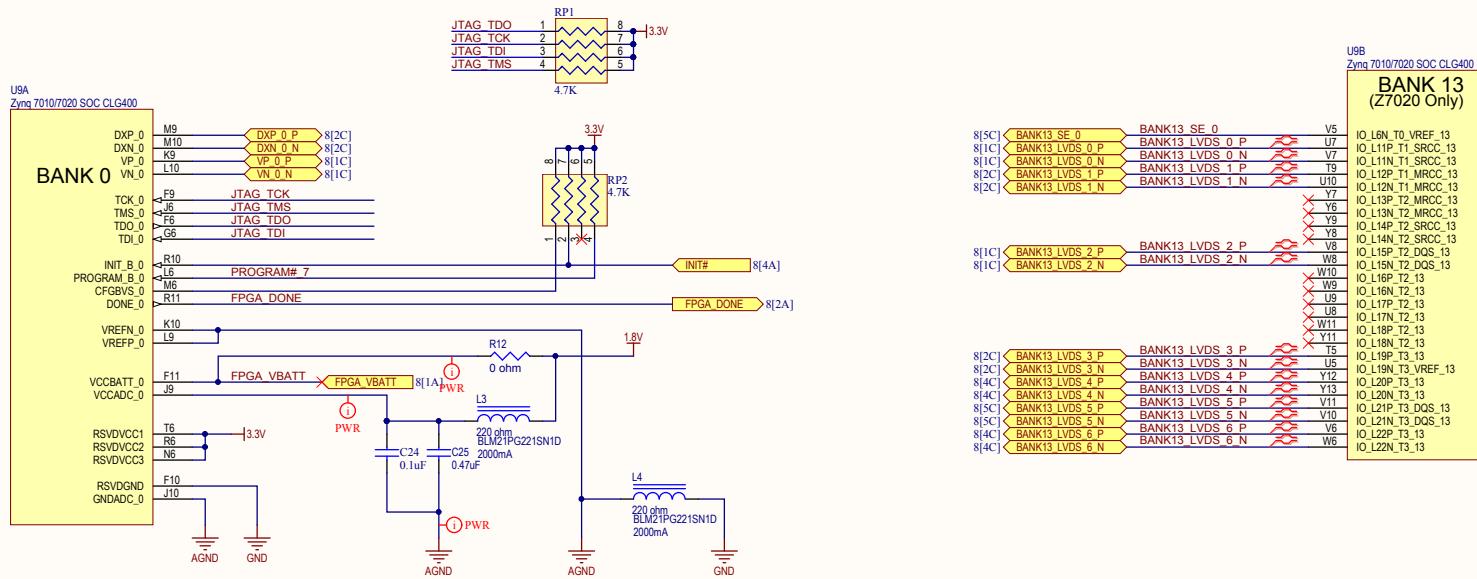




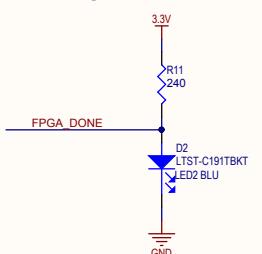




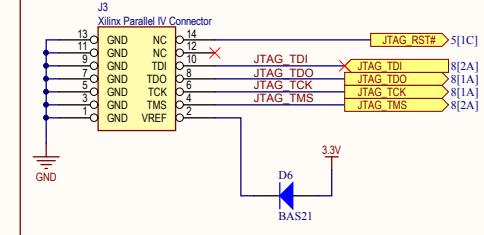


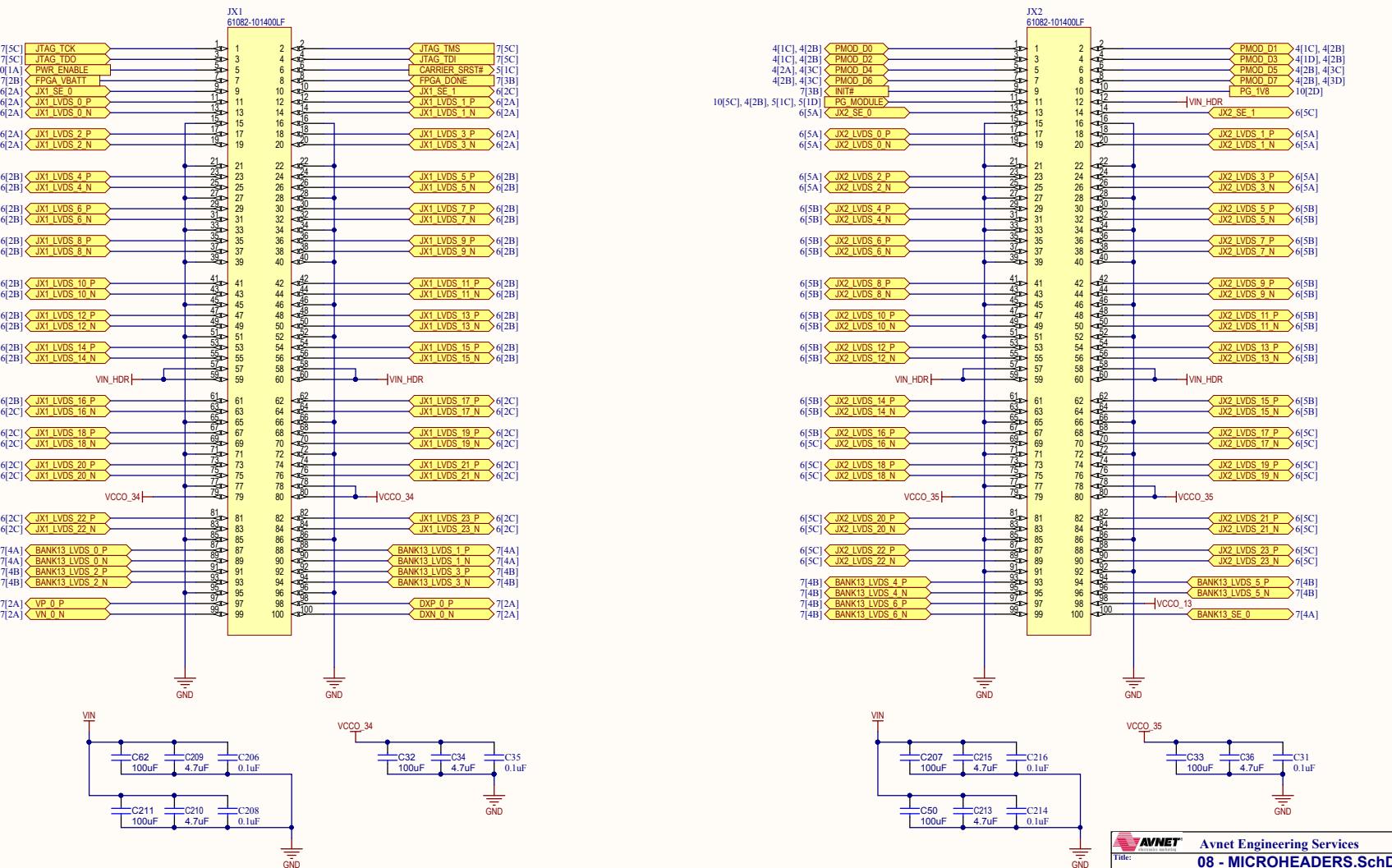


DONE LED

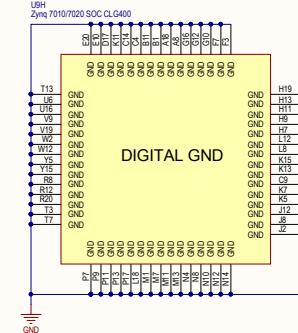
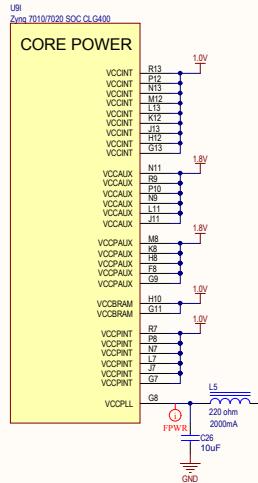
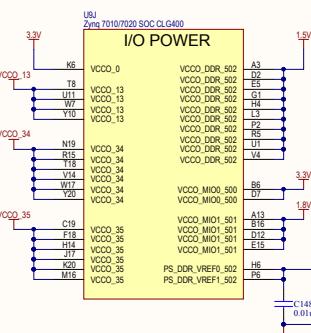


PC4 JTAG





A



B

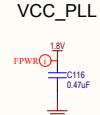
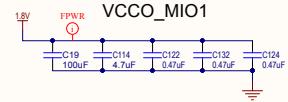
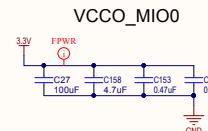
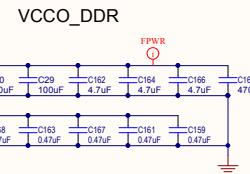
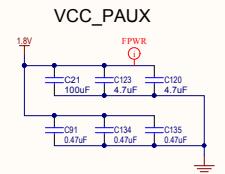
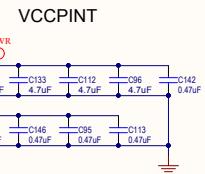
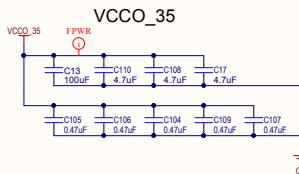
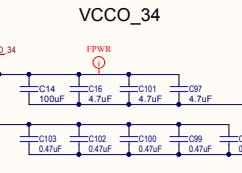
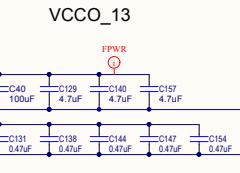
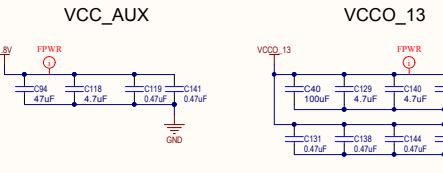
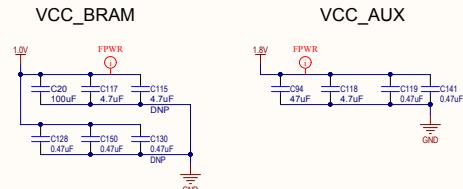
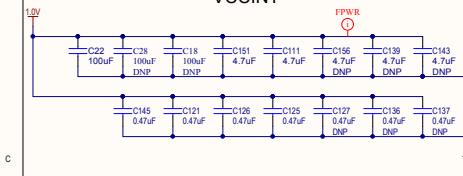
B

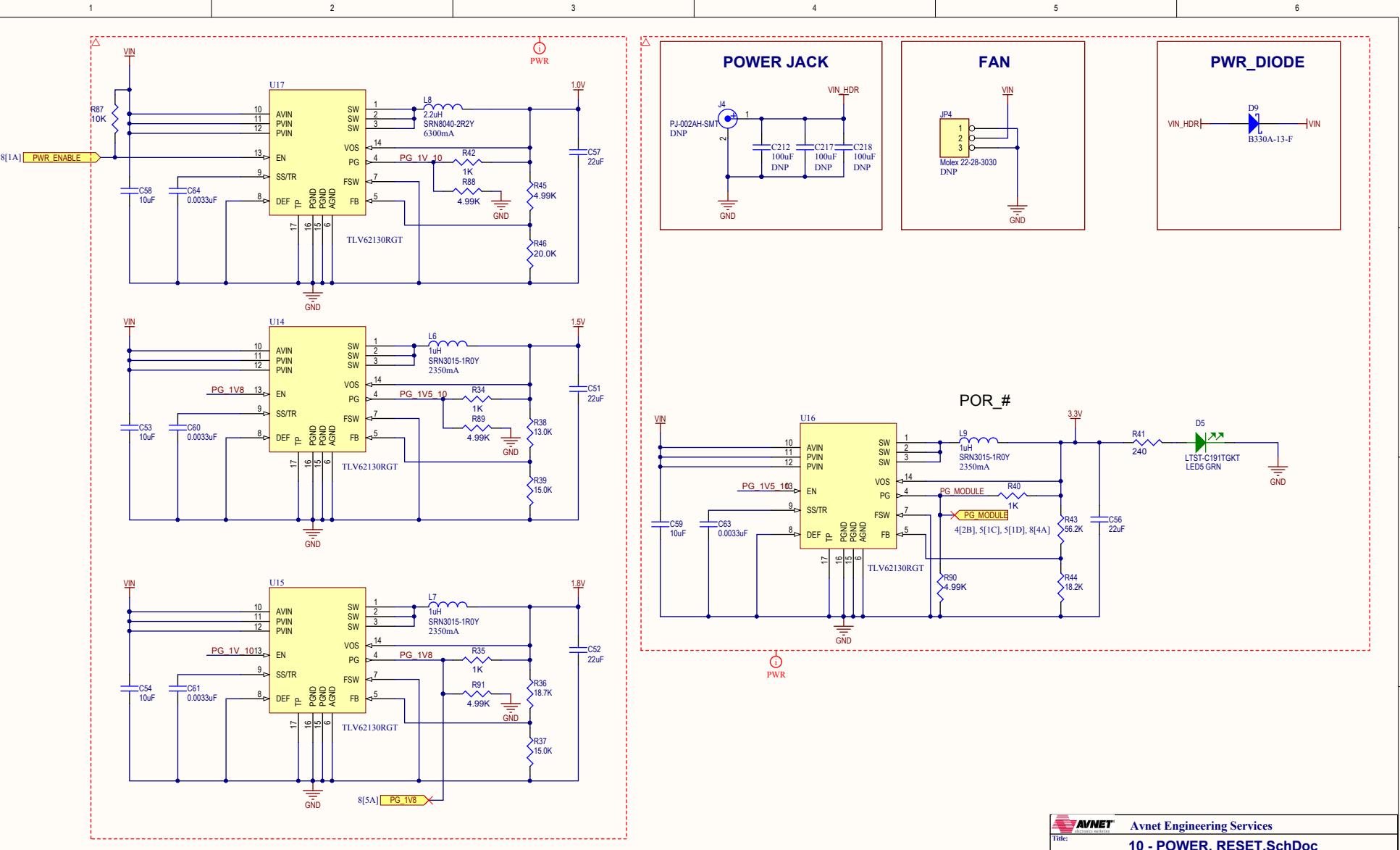
C

C

D

1





Revision Notes:

Revision C Changes:
 1) Add Silkscreen Logos - CE, RoHS and Copper Part Number on board
 2) Reduce R34, 35, (40), 42 from 100K to 1K
 3) Add pulldown resistors to R34, 35, (40), 42 - Value 2.2K - 5.00K
 4) Fuse (PTC) recommendation note for R50, 12V input
 5) Connect: U8.6 to U20.2
 6) Connect: U3.16 to U3.3
 7) Connect: JX2.10 to U15.4
 8) Change 4.75K resistors to 4.99K
 9) Added rubber feet to BOM
 10) Add staple point vias for J2 USB connector.

Revision D Changes (no production):
 1) Attached JX2.10 to U15.4

Revision E Changes (no production):
 1) Replaced UI from MAX13035EETE+ to TI TXS02612ZQSR part.
 2) Added Sheet 11.
 3) Moved mechanical information to back page.

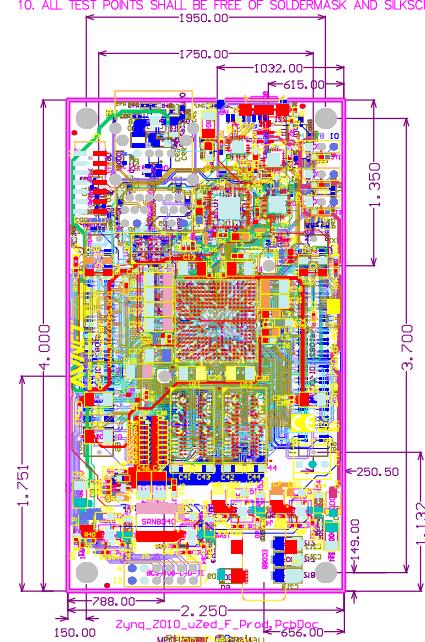
Revision F Changes:
 1) Changed USB UART default power to bus power. Attach VBUS power net to U2.7 REGIN pin. Disconnect Vdd pin from +3.3V.
 2) Added Ethernet LED drive buffer circuit to reduce 3.3V PHY backfeed.
 3) Added: D10, D11, JT7, R97, R98 to allow user to configure USB Bus or Self power mode.
 4) Removed two fansink mounting holes. Removed ground attribute to mounting holes (in layout files).
 5) Added D12 PolyZen (PTC-Zen) USB UART protection component as configurable option.
 6) Added R99 0 ohm resistor for D12 bypass (default).
 7) Added C221 2.2uF capacitor for USB transient and flyback voltage protection.
 8) Revised notes (above).
 9) 28 Jan 14: Updated USB OTG configuration notes.

Mechanicals:**PCB Mounting Holes****Fansink Mounting Holes**



NOTES: UNLESS OTHERWISE SPECIFIED

1. BOARD SHALL BE FABRICATED – PERFORMANCE CLASS II AS PER IPC-6011 AND IPC-6012
2. VENDOR LOGO, VENDOR P/N, REVISION, AND DATE CODE OF THE MANUFACTURING SHALL BE ETCHED ON THE SOLDER SIDE. THE DATE CODE SHALL BE IN THE FORMAT: WWYY WHERE WW=WEEK AND YY=YEAR
3. FABRICATE USING FILM FAB/DRILL IDENT FOR REFERENCE
4. PERMANENTLY MARK BARE BOARD WITH TEST STAMP USING NON-CONDUCTIVE, RoHS COMPLIANT INK
5. SILKSCREEN BOTH SIDES WITH NON-CONDUCTIVE, RoHS COMPLIANT INK, NOT ALLOWED ON COMPONENT PADS, COMPONENT MOUNTING HOLES, OR VIAS (COLOR = WHITE)
6. MATERIAL: PER IPC-4101A/24/26/29/99, COPPER CLAD, HIGH TEMPERATURE FR4 CLASS EPOXY GLASS RATED UL94V-0, 0.5 OZ COPPER FOR EXTERNAL LAYERS AND 0.5 OZ COPPER FOR INTERNAL LAYERS. MUST BE RoHS COMPLIANT AND SURVIVE A LEAD-FREE ASSEMBLY MAX REFLOW OF 260 DEG C (6 PASSES)
 - Td RATING > 340 DEG C
 - Z AXIS CTE < 3.5%
 - Tg > 170 DEG C (MIN)
7. SOLDER MASK: SMBC PER IPC-SM-840C, CLASS T, MUST BE RoHS COMPLIANT, TYP LPI 0.0002 MIN TO 0.0008 MAX MEASURED OVER COPPER PLATING, MUST CLEAR ALL LANDS AS INDICATED ON GERBER SOLDER MASK LAYERS, (COLOR = RED)
8. FINISH: ELECTRO-LESS NICKEL IMMERSION GOLD (ENIG), 2-8 MICRO INCHES GOLD OVER 150-250 MICRO INCHES NICKEL. EDGE FINGERS SHALL HAVE A MINIMUM OF 30 MICRO INCHES OF HARD GOLD.
9. SOLDERABILITY TEST: CATEGORY 2 OF J-STD-003
10. ALL TEST POINTS SHALL BE FREE OF SOLDERMASK AND SILKSCREEN



11. ALL HOLE SIZES ARE AFTER PLATING
12. VENDOR MAY USE TEAR DROPS TO IMPROVE ANNUAL RINGS AS LONG AS DRC RULES ARE FOLLOWED
13. FINISHED BOARDS SHALL NOT HAVE NICKS, SCRATCHES, VOIDS, EXPOSED COPPER, POOR PLATING, MISDRILLED HOLES, AND MUST BE FREE OF ANY RESIDUES
14. TE-BARS ON THERMAL PADS SHOULD BE 15 MILS MINIMUM WIDTH
15. VENDOR MAY ADD COPPER THEIVING AS NEEDED TO IMPROVE MANUFACTURABILITY, THEIVING TO BE 0.030 ROUND PADS AT 0.050 SPACING. THEIVING WILL HAVE A MINIMUM OF 0.100 CLEARANCE FROM EXISTING COPPER AND SHOULD NOT BE PLACED UNDER SURFACE MOUNT DEVICES
16. VENDOR SHALL REMOVE NON-FUNCTIONAL PADS
17. ALL FINISHED BOARDS TO BE 100% ELECTRICALLY TESTED
18. UNLESS OTHERWISE INDICATED, ALL LINEAR TOLERANCES SHALL BE XX +/- 0.010 AND XXX +/- 0.005
19. VENDOR SHALL PROVIDE TDR TEST COUPON AND IMPEDANCE REPORT
20. TENT ALL VIAS ON TOP SIDE WITH RoHS COMPLIANT SOLDER MASK
21. NO PARTS CONTAINING LEAD MAY BE INSTALLED ON THE ASSEMBLY WITHOUT PRIOR WRITTEN CONSENT FROM AVNET ENGINEERING
22. ALL SOLDERING AND CLEANING PROCESSES FOR THIS ASSEMBLY MUST BE LEAD-FREE
23. MANUAL ASSEMBLY AND REWORK MUST USE LEAD-FREE SOLDER AND FOLLOW RoHS PROCEDURES.
24. THIS ASSEMBLY SHALL BE RoHS COMPLIANT. VENDOR SHALL DELIVER ASSEMBLY WITH ACCOMPANYING CERTIFICATE OF COMPLIANCE

ADDITIONAL NOTES:

25. FINISHED BOARD THICKNESS = 0.063 +/- 0.007
26. CONTROLLED IMPEDANCE REQUIREMENTS: VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 25% WITHOUT WRITTEN CONSENT, ANY GREATER THAN 25% REQUIRES WRITTEN CONSENT FROM AVNET ENGINEERING
27. CONTROL TRACE-GND IMPEDANCE TO 50 OHMS +/- 10% ON ALL INTERNAL AND EXTERNAL SIGNAL LAYERS OF WIDTH 5 MLS
28. CONTROL DIFFERENTIAL IMPEDANCE TO 100 OHMS +/- 10% ON EXTERNAL SIGNALS WITH WIDTH OF 4 MLS AND 12 MLS SPACING.
29. Intentionally left blank. Note deleted.
30. CONTROL DIFFERENTIAL IMPEDANCE TO 100 OHMS +/- 10% ON INTERNAL SIGNALS WITH WIDTH OF 4 MLS AND 12 MLS SPACING.
31. CONTROL DIFFERENTIAL IMPEDANCE TO 90 OHMS +/- 10% ON INTERNAL SIGNALS WITH WIDTH OF 4.5 MLS AND 10 MLS SPACING.
32. CONTROL DIFFERENTIAL IMPEDANCE TO 80 OHMS +/- 10% ON INTERNAL SIGNALS WITH WIDTH OF 5 MLS AND 10 MLS SPACING.
33. CONTROL TRACE-GND IMPEDANCE TO 40 OHMS +/- 10% ON ALL INTERNAL SIGNAL LAYERS OF WIDTH 6 MLS

AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 1/28/2014
	TITLE: ZYNQ 2010 UZED	REV: F
	LEVEL:	

BUILD INFO: PAD COUNT — 2093
HOLE COUNT — 1485
VIA COUNT — 1323
COMPONENTS — 440
NET COUNT — 402

