Implementation of Memristor circuits using LTspice

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ABSTRACT

Memristor as a fourth fundamental circuit element was first postulated by Prof. Leon Chua in 1971.The physical implementation of this device was developed by HP team in 2008.Thereafter memristor as a fundamental circuit element has shown tremendous potential for development of analog and digital circuit. To design circuits with memristors, it is essential to understand the memristor behavior with a simulator.SPICE is a general purpose simulator which is used in the analysis of integrated circuits. This paper will discuss memristor behavior with LTspice simulator which is a popular version of SPICE and implement Memristor model for the analysis of MC(Memristor Capacitor) circuits.

Index Terms: Memristor, LTspice, MC circuits

I. INTRODUCTION

Memristor was postulated by Prof. Leon Chua in 1971 as the fourth missing circuit element in the list of three fundamental electric circuit elements such as Resistor, Capacitor, Inductor[1]. For its future reliable applications, modeling of the device is an essential part. Memristor being a non-linear device, its modeling can be handled by simulator like SPICE(Simulation Program with Integrated-Circuit Emphasis) efficiently. SPICE is a general – purpose circuit simulator capable of performing nonlinear circuit analysis. The purpose of this paper is to discuss LTspice based memristor model and analyzed MC circuits on the basis of the mathematical definitions and model demonstrated by HP labs [1][2].
Section II, of this paper will discuss fundamental definitions of Memristor. HP Memristor model is discussed in Section III. Memristor model with nonlinear dopant drift is discussed in section IV. LTspice based nonlinear dopant drift model of memristor and Simulation results based on LTspice for MC circuits are explained in section V.

II. MEMRISTOR FUNDAMENTS

Memristor was first postulated by Prof. Leon Chua in 1971 [1] as the fourth fundamental Passive circuit element. Based on the symmetry of the equations that governs the resistor, capacitor and inductor. Prof Leon Chua hypothesized that fourth device should exist that holds a functional relationship between magnetic flux linkage and electric charge. This would complete the square where the resistor holds the relation between current and voltage, the

inductor holds the relationship between current and flux, and the capacitor holds the relationship between voltage and charge is as shown in Figure 1.

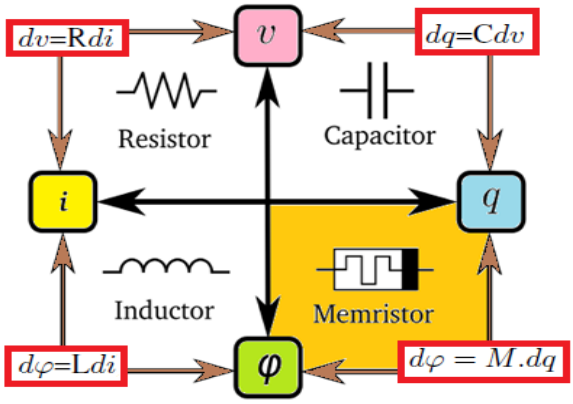


Figure 1: Fundamental Passive circuit elements

Memristor is defined as a fourth fundamental passive circuit element which shows a nonlinear relationship between magnetic flux linkage(ø)and the amount of charge(q) flowing through it.
However, according to the postulation by Prof. Chua Memristor relates flux and charge (dφ = M dq). Mathematically flux and charge is defined by,

$$\emptyset = \int \boldsymbol{v\,dt} \quad \textbf{(1)}$$

$$\mathbf{q} = \int \boldsymbol{i\,dt} \quad \textbf{(2)}$$

Defined by equation (1) and (2), there are two types of Memristor such as charge Controlled (Current Controlled) Memristor and flux controlled (Voltage Controlled) Memristor.
Each memristor and memristive systems are characterized by its Memristance function. Memristor with its function describing the charge dependent rate of change of flux with charge is called as current controlled memristor and the one describing flux dependent rate of charge of flux with charge is called as voltage controlled memristor is shown in equation (3) (4) respectively [3].
A Current controlled Memristor, also termed as charge controlled Memristor, is mathematically expressed as

$\varphi = f(q)$ (i)

Differentiating equation (i) with respect to t

$$\frac{d\varphi}{dt} = \frac{df(q)}{dq}\frac{dq}{dt} \quad \text{(ii)}$$

Substituting v= $\frac{d\varphi}{dt}$, i = $\frac{dq}{dt}$

$v(t) = M(q)\, i(t)$ (iii)

Where, M **(q)** = $\boldsymbol{\frac{df(q)}{dq}}$ **(3)**

A voltage controlled Memristor , also termed as flux controlled Memristor, is mathematically expressed as,

$q = f(\varphi)$ (iv)

Differentiating equation (iv) with respect to t

$$\frac{dq}{dt} = \frac{df(\varphi)}{d\varphi}\frac{d\varphi}{dt}$$

But, i = $\frac{dq}{dt}$, v = $\frac{d\varphi}{dt}$

$i(t) = G(\varphi)\, v(t)$ (v)

Where ; **G (φ)** = $\frac{df(\varphi)}{d\varphi}$ **(4)**

G (φ) = Memductance (for Memory Conductance), which is reciprocal of Memristance.One of the highlighting properties of memristor is the existence of pinched hysteresis effect is as shown in Figure 2[4].

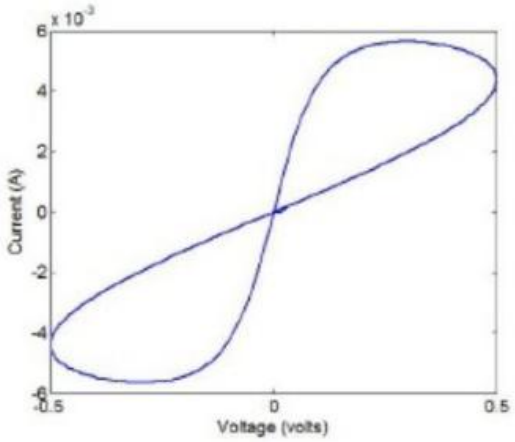


Figure 2: I-V characteristics of memristor

III. PHYSICAL MODELOF MEMRISTOR

The physical implementation of memristor was successfully observed by HP research team with simple device structure comprising of Pt–TiO2–Pt.this model was a linear ion dopant drift model where a uniform field and the ions with equal average ion mobility μv were assumed. This model exhibits the definition of the original Memristor and is structured with a combination of two series resistors as shown in Figure 3[4].

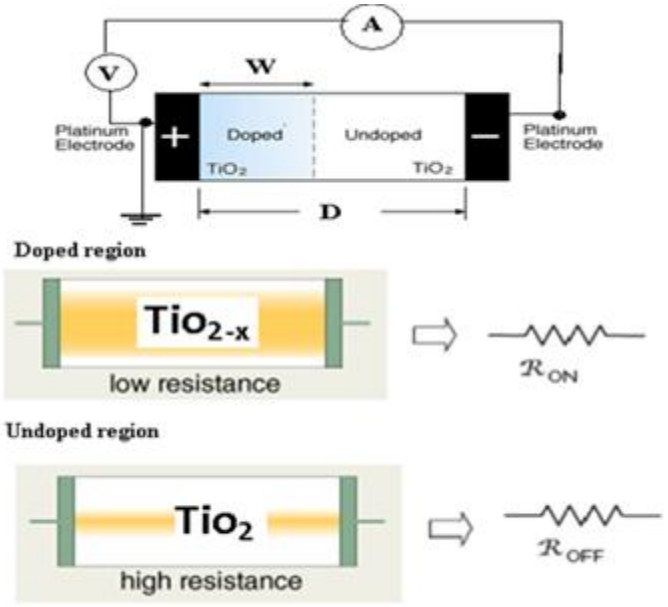


Figure 3 Memristor Device Structure and Model[3]

The Memristor device in the form of general memristive system, is described by[4]

$v = R(w) \cdot i$ **(5)**

$dw / dt = f(w) = \frac{\mu V R_{ON}}{D} i$ **(6)**

Where w is a set of state variables, μV is the carrier mobility and R and f can be explicit functions of time. The length of the doped region w, in fact is the internal state variable representing the position of a sharp dividing line between the doped and undoped semiconductor. It is bounded between two limits 0 and D, corresponding to the positions of the metal contacts at either side of a TiO_2 semiconductor film. When the doped region extends to the full length D, that is w/D=1, then the device resistivity is dominated by low resistivity region (R_{ON}). When the un-doped region extends to the full length D, i.e. w/D=0, the total resistance is high(R_{OFF}).At any instance of time, the static resistance R(w) of the Memristor is the sum of the resistances across the doped and un doped regions which can be described as

$$\mathbf{R(w) = R_{ON} .w/D + R_{OFF}.(1- (w/D))} \quad \textbf{(7)}$$

From equation (7) it is observed that the resistivity of the device is controlled by the length of the doped region (w) as summarized in Table 1.

Table 1.w/D Ratio and Device Resistance relation

w/D Ratio	Device Resistance
0	HIGH (R_{OFF})
1	LOW (R_{ON})

The effective Memristance derived is given by

$$\mathbf{M(q) = R_{OFF}\left(1 - \frac{\mu v R_{ON}}{D^2}\right) q(t)} \quad \textbf{(8)}$$

From equation (8) it is observed that the Memristance and the resistive switching behavior will be primarily affected by carrier mobility μV and the metal oxide film thicknesses D. It is the factor $1/D^2$ that is making memristive systems and Memristance more significant at nano scale. The device is observed to lose its nonlinear behavior as the device thickness increases. This fact is leading to future device shrinkage possible with Memristor devices. From equation (2) it is observed that, a Linear dopant drift model is applicable only for charge controlled Memristor.

IV. MEMRISTOR MODEL

There are four different types of memristor model developed as on today [4][5]. However this paper is based on nonlinear dopant drift model of memristor .Though the linear ion drift model satisfies the basic memristive system equations, this model is inaccurate as compared to physical memristive devices, which are is highly nonlinear. A nonlinear dopant drift model of bipolar switching is derived from the experimental results of a set of Pt–TiO2–Pt cross point devices. This model assumes a nonlinear dependence between the voltage and the internal state derivative exhibited by a voltage-controlled memristor (also termed as Flux controlled memristor). After experimentation of memristor device

fabrication it was observed that the linear ion dopant drift model was significantly deviating from nonlinear characteristics, a model based on experimental results suggested a relationship between current and voltage as in equation(9)[7].

$$i(t) = w(t)n\,\beta \sinh(\alpha\, v(t)) + \delta\left[\exp\left(\gamma\, v(t)\right) - 1\right] \quad \textbf{(9)}$$

Where α, β,γ,δ are parameters used in experiment and nis the parameter that shows the influence of the state variable on the current. This model assumes an asymmetrical switching behavior and a voltage controlled memristor exhibits a nonlinear dependence on voltage in the state variable differential equation as given in equation (10)[7].

$$\frac{dw(t)}{dt} = a\,.\,f(w).\,v(t)^m \quad \textbf{(10)}$$ Where a and m are constants, m is an odd integer, and f(w)is a window function. In this model, the state variable w is a normalized parameter within the interval (0,1).Introduction of window function is a significant feature of nonlinear ion dopant drift model due to boundary effects.In this model parameter of the window function for modeling nonlinear boundary condition is p=1. Window function is a function of the state variable. It forces to create the boundary for the memristor[4]. The window function decreases as the state variables drift speed approaches the boundaries until it reaches zero when reaching either boundaries .The speed of the boundary between the doped and undoped regions decreases gradually to zero at the film edges [4][6]. We simulate the nonlinear ion drift memristor model with these window function to observe the difference and study the related issue.

V. MEMRISTOR CIRCUITS USING LTspice

LTspice is an analog circuit simulator with integrated schematic capture and waveform viewer. In this section we implemented LTspice based nonlinear dopant drift model of memristor as shown in Figure 4. This model is implemented as a LTspice subcircuit with parameters as the initial resistance $R_{INIT,}$ the resistance of doped and undoped regions are R_{ON} and R_{OFF} respectively, the dopant mobility μv ,the width of thin film D and the exponent p of the window function. The SPICE model of [5] was used for the simulation of experiments described in [1]. Figure 5 shows simulation results of nonlinear dopant drift model of memristor for window function of applied voltage, current flowing through memristor. Figure 5(d) shows the I-V hysteresis loop of the memristor and the relationship between charge and flux. When positive voltage is applied, the conductivity of the device increases thus the memristance is decreased. When negative voltage is applied, the resistivity of the device increases and the memristance increases. The current of the memristor is observed to vary up to 120μA for maximum of 1V voltage applied.

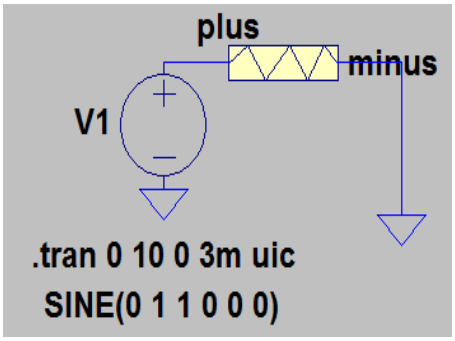
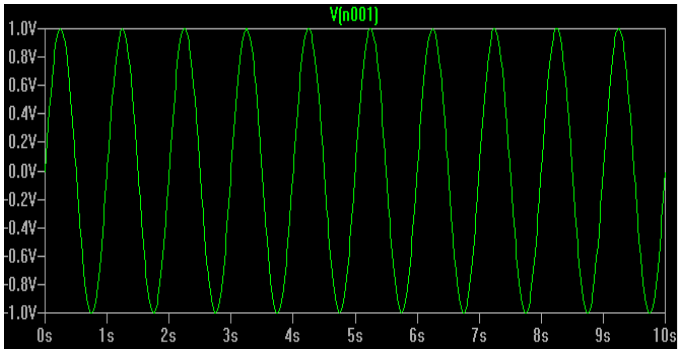
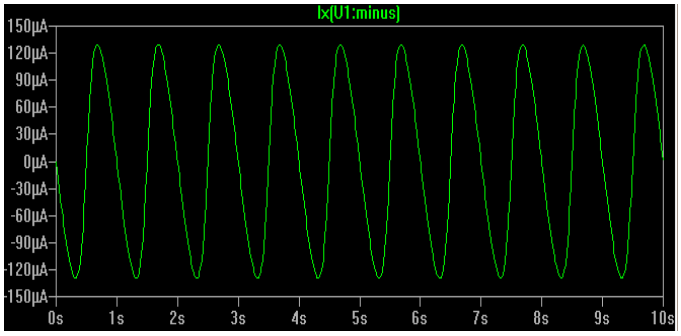


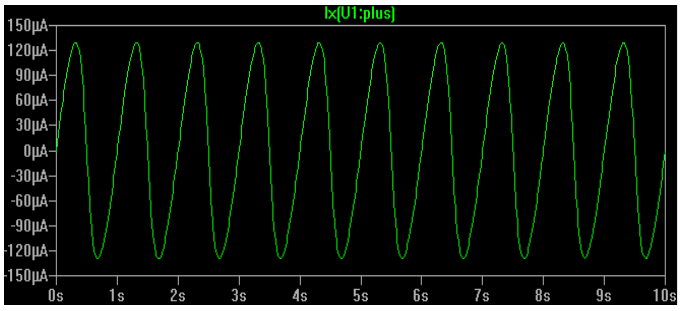
Figure 4 : Nonlinear dopant drift model of memristor


V(n001)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
-0.4V
-0.6V
-0.8V
-1.0V
0s
1s
2s
3s
4s
5s
6s
7s
8s
9s
10s

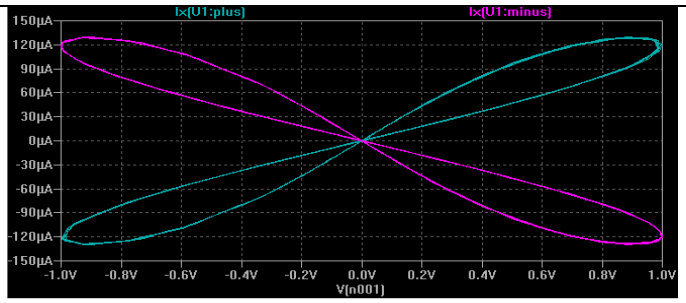
a)


Ix(U1:minus)
150µA
120µA
90µA
60µA
30µA
0µA
-30µA
-60µA
-90µA
-120µA
-150µA
0s
1s
2s
3s
4s
5s
6s
7s
8s
9s
10s

b)


Ix(U1:plus)
150µA
120µA
90µA
60µA
30µA
0µA
-30µA
-60µA
-90µA
-120µA
-150µA
0s
1s
2s
3s
4s
5s
6s
7s
8s
9s
10s

c)



d)

Figure 5: simulation results of memristor model a) input voltage applied to memristor b) current flowing through minus terminal of memristor c) current flowing through plus terminal of memristor d) I-V characteristics of memristor

The LTspice based MC circuit is as shown in Figure 6 and the simulated results of MC circuits with varying applied frequency from 1HZ to 20HZ is as shown in Figure 7. From various simulation results as shown in Figure 7 it was observed that for 10 nm thickness of memristor device the ratio of R_{ON}/R_{OFF} is having significant effect on I-V characteristics.

- 10 nm thickness memristor can perform better at 1 Hz frequency with 1Volt supply which is suggesting a significant power reduction.
- The hysteretic characteristics of memristor change with the variation in applied frequency from 1 HZ to 20 HZ.
- At 20HZ the characteristics become linear as the action of oxygen vacancy drift is sluggish.

These results verify with the experimental results of memristor device fabricated by HP Lab Research team [1].

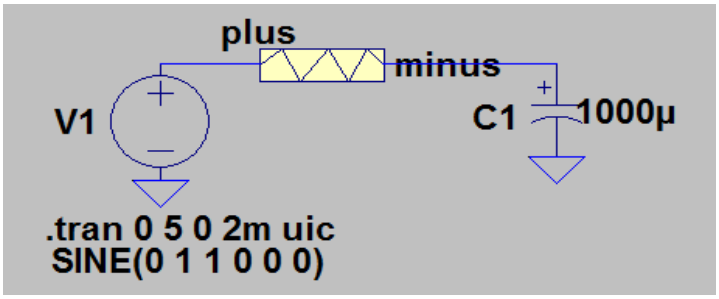
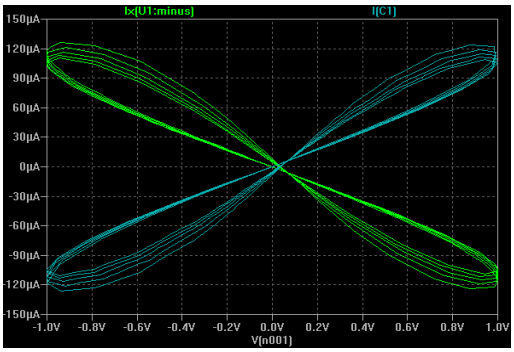
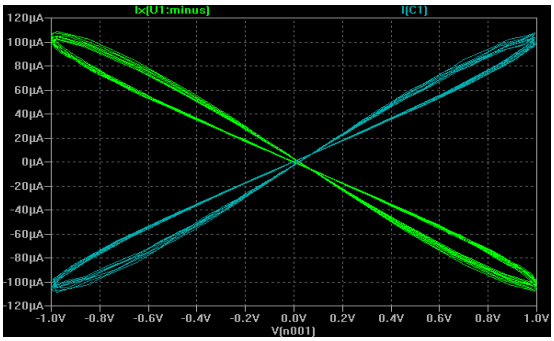


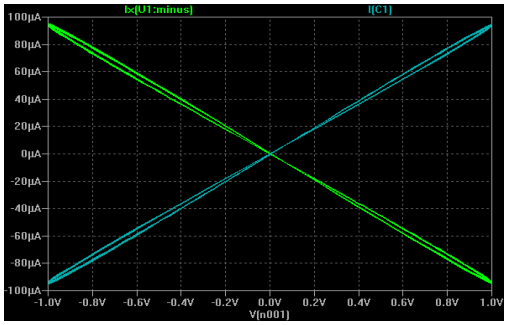
Figure 6 : Schematic of MC circuit



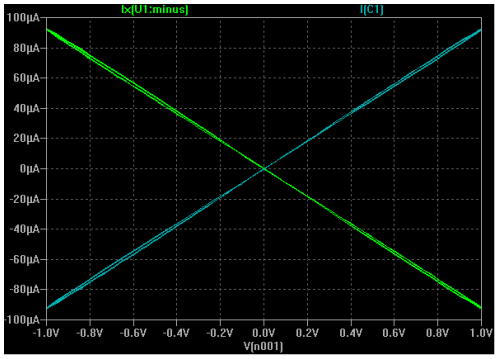
At 1HZ



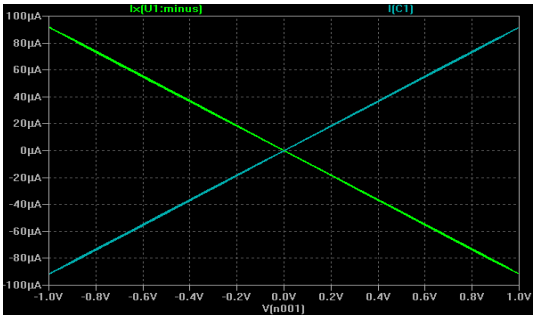
At 1.5 HZ



At 5HZ



At 10 HZ



At 20 HZ

Input Parameters :

D = 10N

R_{ON} = 1KΩ

R_{OFF} = 100KΩ

R_{INIT} = 80KΩ

µv = 10F

Applied frequency = 1 to 20 HZ

Applied voltage = 1V

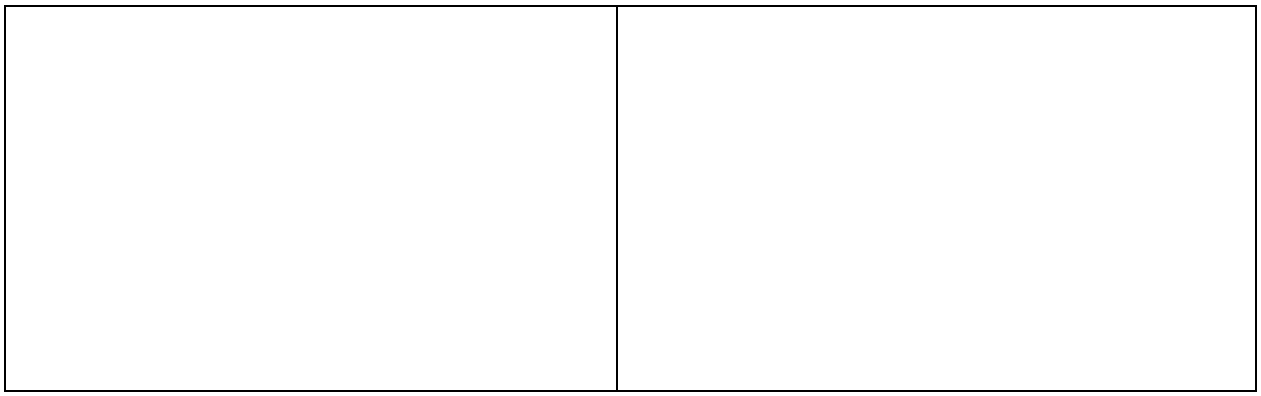


Figure 7: I-V characteristics of memristor at variable frequency

VI. CONCLUSION

LTspice can implement a nonlinear dopant drift model of memristor .The simulation results of this model show similar behavior of HP model . The results of Memristor capacitor circuit simulation will be helpful for further memristor based analog circuit implementation and also for experimentation with ML (Memristor-inductor), MLC(Memristor-Inductor-Capacitor) circuits.

VII. REFERNCES

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