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GENERAL SPICE MODELS FOR MEMRISTOR AND APPLICATION TO CIRCUIT SIMULATION OF MEMRISTOR-BASED SYNAPSES AND MEMORY CELLS*

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Memristor had been first theorized nearly 40 years ago by Prof. Chua, as the fourth fundamental circuit element beside the three existing elements (Resistor, Capacitor and Inductor) but because no one has succeeded in building a memristor, it has long remained a theoretical element. Some months ago, Hewlett-Packard (hp) announced it created a memristor using a TiO_2/TiO_{2-X} structure. In this paper, the characteristics, structures and relations for the invented hp's memristor are briefly reviewed and then two general SPICE models for the charge-controlled and flux-controlled memristors are introduced for the first time. By adjusting the model parameters to the hp's memristor characteristics some circuit properties of the device are studied and then two important memristor applications as the memory cell in a nonvolatile-RAM structure and as the synapse in an artificial neural network are studied. By utilizing the introduced models and designing the appropriate circuits for two most important applications; a nonvolatile memory structure and a programmable logic gate, circuit simulations are done and the results are presented.

Keywords: Memristor; SPICE; nonvolatile memory; artificial neural network; programmable logic gate.

1. Introduction

For nearly 150 years, the known fundamental passive circuit elements were limited to capacitor, resistor, and inductor. Then, in 1971, Chua predicted the existence of a fourth fundamental device, which he called a memristor. He proved that memristor behavior could not be obtained by any combination of the other three existing elements, even of nonlinear types, which is why the memristor is truly fundamental.[1] Then he analyzed the memristor systems and showed that the hysteresis behavior in

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some of the electronic devices with nonlinear current-voltage characteristic such as thermistor is due to their memristor attribute.[2] However absences of direct relationship between the memristor theory and practical physical phenomena caused limited memristor studies and only theoretical researches were done from mathematical point of view,[2,3] and memristor as a physical useful device was unknown until recent times.

During the investigations on the two terminals nanometric devices such as switching resistances,[4] in which their Current-Voltage characteristics showed some hysteresis effect, it was concluded by the hp investigators that the phenomena must be related to the memristor attribute. This conclusion led them to build a real memristor. Some months ago, this news was announced in news sites and science journals.[5,6] There are some applications proposed for the memristor,[7] but the followings are noted as the two major findings: the memory cell in a Nonvolatile-RAM structure[8] and the synapse in an artificial neural network.[10]

In this paper we have extended our previous work[9] regarding circuit model of memristor and its application as nonvolatile memory and introduced general SPICE models for two types of memristor, its theory and interesting characteristics, especially the hysteresis effects and its most important applications. The arrangement of the paper is as follows: in Sec. 2 we review general characteristics of memristors and hp's Titanium-dioxide memristor structure and formulas. In Sec. 3 our general SPICE models for the charge- and flux-controlled memristors are introduced and then, by adjusting the model's parameters to hp's memristor characteristics, some circuit features of this device are briefly studied. In Sec. 4 a comparison between the benefits of today's nonvolatile memories based on the Flash technology[11] and the memristor nonvolatile memories is performed first and then simulation results are introduced for a simple memory cell using hp's memristor and the proposed model. As the second example of application of memristor and the proposed model, in Sec. 5, the memristor synapses characteristics is considered in contrast to the previously CMOS based technology[12,13] at first and then a sample artificial neural network,[14,15] based on the memristor synapses structure is designed and utilized as a programmable logic gate and by training the network, two logical gates of XOR and XNOR are demonstrated. Finally conclusions of the paper are drawn in Sec. 6.

2. Structure, Properties and Formulas of Memristor

In this section general characteristics of memristors are examined and then the structure of hp's titanium dioxide memristor and its equations are reviewed.

2.1. *Properties and general attributes of memristors*

Since 1971 there were five known mathematical equations for relating the four fundamental circuit variables. Figure 1(a) demonstrates the current, the voltage, the electrical charge and the magnetic flux as the fundamental variables and the five

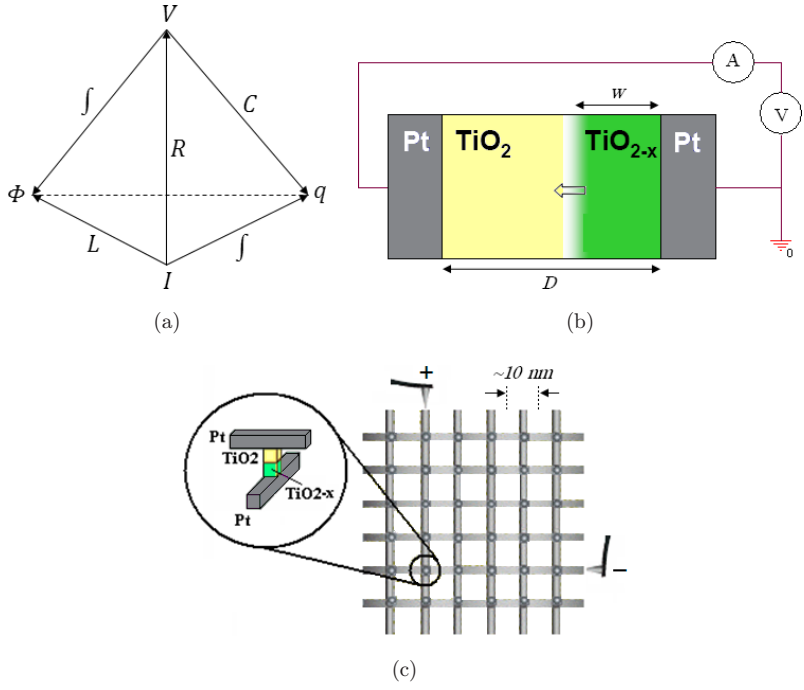


Fig. 1. Relationship, structure and architecture of memristor, (a) shows the Chua's pyramid and the new proposed element — memristor. The old circuit elements and relations are shown with solid lines and the new element is shown with a dashed line, (b) shows a conceptual graph of hp's memristor. By moving the boundary between TiO_2 (high resistance) and TiO_2-x (low resistance) regions, under the applying electric field, the total resistance of the device changes which results in a memristive effect, (c) shows hp's memristors in a crossbar ultra dense structure.

relations among them. The sixth relation that is proposed by Prof. Chua relates the flux to the charge (dashed line in Fig. 1)[1] and the corresponding device called as memristor. This relation can be written in the following form:

$$\phi = F(q)\,. \tag{1}$$

On the basis of the behavior of F function, we will obtain different voltage-current characteristics.[2] However, if F is a linear function, we will only have a simple resistor, and only if the F is nonlinear, the memristor property will emerge. Using Faraday's Law, we can rewrite the above relation as the following charge-controlled (current-controlled) relation:

$$V = \frac{\partial \phi}{\partial t} = \frac{\partial F}{\partial q}\frac{\partial q}{\partial t} = M(q)i\,, \tag{2}$$

where M is a function of memristor charge and called memristance. A dual form of these equations holds for the so-called flux-controlled (voltage-controlled)

memristor:

$$q = G(\phi)\,, \tag{3}$$

$$i = \frac{\partial q}{\partial t} = \frac{\partial G}{\partial \phi}\,\frac{\partial \phi}{\partial t} = W(\phi)V\,, \tag{4}$$

where W is called memductance and is a function of flux of memristor. In a memristor there would be any kind of complicated nonlinear relationships between flux and charge, and in different cases there would be different interesting interpretations for memristor behavior. If we rewrite Eq. (2) as:

$$V = M\left[\int idt\right] i\,. \tag{5}$$

Then by comparing this equation with a $I - V$ equation of a normal capacitor; $V_c = M[\int i_c dt]$, we conclude that memristor is an strange capacitor whose voltage immediately goes to zero when its charging current goes to zero without any loss in its information, i.e., its charge. With the same skin we may rewrite Eq. (4) as:

$$i = W\left[\int Vdt\right] V\,. \tag{6}$$

And in a similar fashion, this relation shows that memristor is an strange inductor whose current immediately goes to zero when its charging voltage goes to zero without any loss in its information, i.e., its flux. As the second conclusion, the relations 5 and 6 contain a product operation of two terms therefore, from another point of view, we may consider memristor as an analog multiplier that is able to multiply the instant applied current and or voltage by a pre-stored quantity. These two interesting circuit concepts will be referred to many times.

2.2. *Physical structure of the titanium-dioxide memristor*

In this kind of memristor which is invented by hp, a piece of Titanium-dioxide is placed between two platinum metal junctions. Titanium-Dioxide is a semiconducting material with high resistance (R_{OFF}) but if some oxygen atoms are removed from it, the vacancies act as donor dopants, hence the resistance drops to a low value (R_{ON}). Figure 1(b) shows a simple conceptual graph of this structure. It is believed that the main mechanism of the device is the drift of oxygen atoms in response to the applied electric field and flowing current such that the passing electrons cause the interface ions to be able to overcome the Schottky barrier, tunneling through the barrier and changing the boundary position (w) between the high and the low resistance regions. In this way, the coupling among ions transfer and electrons transfer would result in a memristor attribute with a nonlinear relation, as will be discussed later. However, the exact mechanism of charge transfer and its effect on resistance variation is still unknown and studies on the interface effects and filament formations are continued.

Making a superlattice by memristors in a crossbar structure is illustrated in Fig. 1(c). This structure helps to implement large nonvolatile memories and leads to minimum addressing switching circuit and transistor count and promises ultra-dense 3D implementation.[10]

2.3. *Equations of hp's memristor*

Exact relations for hp's memristor are difficult to obtain because of the complexity of the mechanisms of ion drifting and their way of coupling with electrons movement. However, hp introduces the following simple relations based on assumptions of ohmic conductance, flat electrical field and average ion mobility.[5]

$$R(w) = \left[R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right], \tag{7}$$

where w and D are the length of ionized region and total region, respectively, and R_{OFF} and R_{ON} are the highest and lowest resistance of the device when w is equal to *zero* and or D (see Fig. 1(b)). The below equation is proposed for w:

$$\frac{\partial w(t)}{\partial t} = \mu_v \frac{R_{ON}}{D} i(t), \tag{8}$$

where μ_v is the average ion mobility. Following the above model and referring to Eqs. (1) and (2), the memristance of the device may be obtained easily:

$$M(q) = R_{OFF} \left(1 - \frac{\mu_v R_{ON}}{D^2} q(t) \right), \tag{9}$$

$$\phi = R_{OFF} \left(q - \frac{\mu_v R_{ON}}{2D^2} q^2 \right). \tag{10}$$

The hp's memristor can be considered as a flux-controlled element too. In this mode, refer to Eqs. (3) and (4), the memductance will be:

$$W(\phi) = \frac{2}{R_{OFF}} \left(1 - \frac{2\mu_v R_{ON}}{D^2 R_{OFF}} \phi \right)^{-1/2}, \tag{11}$$

$$q = \frac{D^2}{\mu_v R_{ON}} \left[1 - \left(1 - \frac{2\mu_v R_{ON}}{D^2 R_{OFF}} \phi \right)^{1/2} \right]. \tag{12}$$

Equations (10) and (12) will be adjusted to the general SPICE models of memristor that will be introduced in the next section and then will be used in simulation of some memristor based circuits.

3. General SPICE Models for Memristors

The fourth fundamental circuit element still does not have any model in circuit simulators such as SPICE. In this section, we introduce two general circuit models for

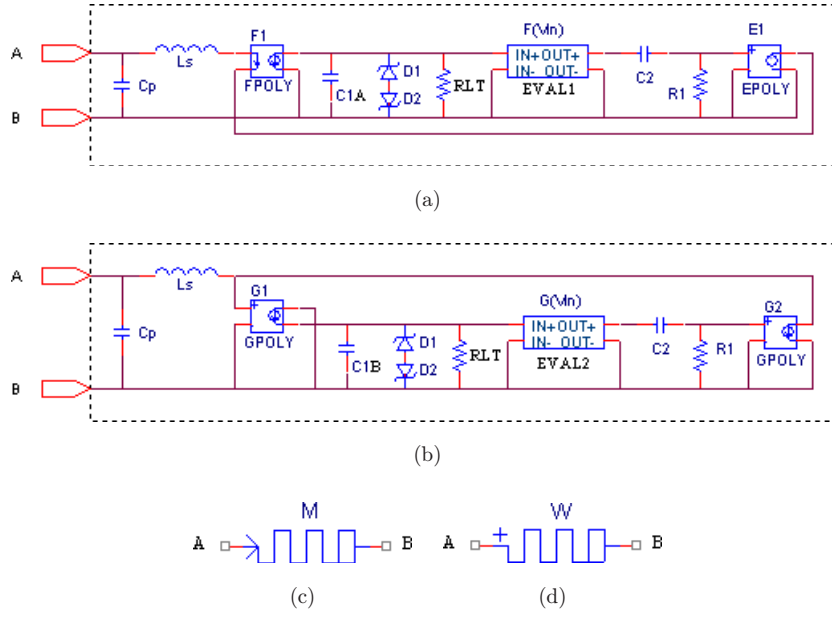


Fig. 2. Introduced General SPICE Models of Memristors and their Circuit Schematics, (a)−(b) shows SPICE model of charge-(current) controlled/flux-(voltage) controlled memristor including three second-order effects (see text for details), (c)−(d) shows the circuit symbol of charge-controlled (*M*: memristance)/flux-controlled (*W*: memductance) memristor.

two types of memristor — charge-controlled and flux-controlled. Figures 2(a) and 2(b) show the circuit models which implement Eqs. (2) and (4), respectively. We focus on Fig. 2(a) and Eq. (2) first. A SPICE tool, which is called *FPOLY,* is used to buffer the current of the device. Then, the buffered current is integrated by $C1A$ capacitor to get a voltage signal proportional to the charge, i.e., $q(t)$. This signal is applied to another SPICE element, called *EVALUE*, which implements the general nonlinear function of Eq. (1), i.e., F. At last a RC differentiator has been used to produce $V = \partial F(q(t))/\partial t$ (see Eq. (2)). Finally an *EPOLY* element buffers the produced voltage and connects it to the device's terminal. Reader must note that this type of memristor is a current-controlled device. Therefore, the input signal, which must be determined by the external circuit, is its current and the output signal, which will be determined by this element, is its voltage. This input/output scheme is the heart of the structure of the introduced equivalent circuit shown in Fig. 2(a).[16]

In a same way, Fig. 2(b) introduces a general SPICE model for the second type of memristors, i.e., the voltage controlled memristors. Again a *GPOLY* element buffers the input signal (i.e., the input voltage) and converts it to current which is then integrated by $C1B$ capacitor to produce time dependent flux, i.e., $\phi(t)$. The desired nonlinear function should be implemented in the *EVALUE* element and we will have

$G(\phi(t))$ at its output. Then the RC differentiator will produce a voltage proportional to the correct current of the device. Finally, another $GPOLY$ element buffers this voltage and converts it into current. Again, note that this type of memristor is a voltage-controlled device. Therefore, the input signal is its voltage and the output signal is its current.

The introduced models contain three second-order effects as well. Applying either large amplitude signal or at a long time causes the boundary to reach the contacts of the device and this will end in a saturation effect. There exist two zener diodes in the introduced models in parallel with the integrating capacitors which model the mentioned saturation effect. Breakdown voltage of these diodes may be calculated from Eqs. (13) and (14) for the charge-controlled and the flux-controlled memristors, respectively.

$$\left(1 - \frac{2\mu_v R_{ON}}{D^2 R_{OFF}}\phi\right) > 0 \Rightarrow \phi < \frac{D^2 R_{OFF}}{2\mu_v R_{ON}} = V_{ZD} + 0.7\,, \tag{13}$$

$$\left(1 - \frac{\mu_v R_{ON}}{D^2}q\right) > 0 \Rightarrow q < \frac{D^2}{\mu_v R_{ON}} = V_{ZD} + 0.7\,. \tag{14}$$

Moreover, a memristor in practical cases, like any other physical element, has limited lifetime for keeping the information due to the existence of various relaxation mechanisms. This phenomenon is included to the models by adding a resistor; R_{LT}, in parallel to the integrating capacitors. So the lifetime of memristance (or memductance) has been modeled by the following time constant:

$$\tau_M = R_{LT} C_1\,. \tag{15}$$

There exists an inductor; Ls, in series with the whole equivalent circuits as well. This inductor models the parasitic wiring effects and also the limited response time of memristors. Finally a capacitor has been included in the models, Cp, for the parasitic capacitance of the contacts. Two circuit schematics, which are shown in Figs. 2(c) and 2(d), are assigned to the two explained models, respectively, and are added to the SPICE library and will be used in the proposed applications.

The introduced models are quite general and may be adjusted to any desired physical memristor having their special dependency function ($q - \phi$ relation in F and or G form see Eqs. (1) and (3)). We have adjusted these models to hp's memristor and used them in the simulations for the introduced applications (the model parameters will be given in each case) but before going into details of those simulations, here we consider memristor specifications, especially the hysteresis phenomenon, in some cases.

In a simulation with sine wave, in order to observe the $q - \phi$ nonlinearity clearly, the amplitude to frequency ratio (V_0/f_0) of the sine wave must follow a definite value so that it could sweep w in a vast region from *zero* to D.

$$\frac{\partial w(t)}{\partial t} = \mu_v \frac{R_{ON}}{D} I_0 \,\mathrm{Sin}(\omega_0 t)\,,$$

$$w_{\max} = \mu_v \frac{R_{ON}}{D} \frac{V_0}{\omega_0} = \frac{D}{2}\,,$$

$$\frac{V_0}{f_0} = \frac{\pi D^2}{\mu_v} \frac{R_{OFF}}{R_{ON}}\,. \tag{16}$$

f_0 is the least frequency, for a predefined value of V_0, that results in the maximum sweep. For frequencies less than f_0, the device will saturate and for frequencies above f_0 the amplitude of the sweep becomes inadequate. Equation (16) shows that this characteristic frequency depends on $\alpha = R_{OFF}/R_{ON}$ and by decreasing α, becomes better. It also improves by increasing μ_v and decreasing D. Figure 3 shows the response of hp memristor to some input sinusoidal waves with same amplitude and different frequencies and the resulted hysteresis loops. We see that the size of hysteresis loops decreases by increasing frequency. This is due to the fact that the ions have a low mobility and slow inherent motions, so finally lose their effectiveness on changing the memristor resistance. In this way memristor reduces to a simple resistor at the frequencies equal to few f_0.

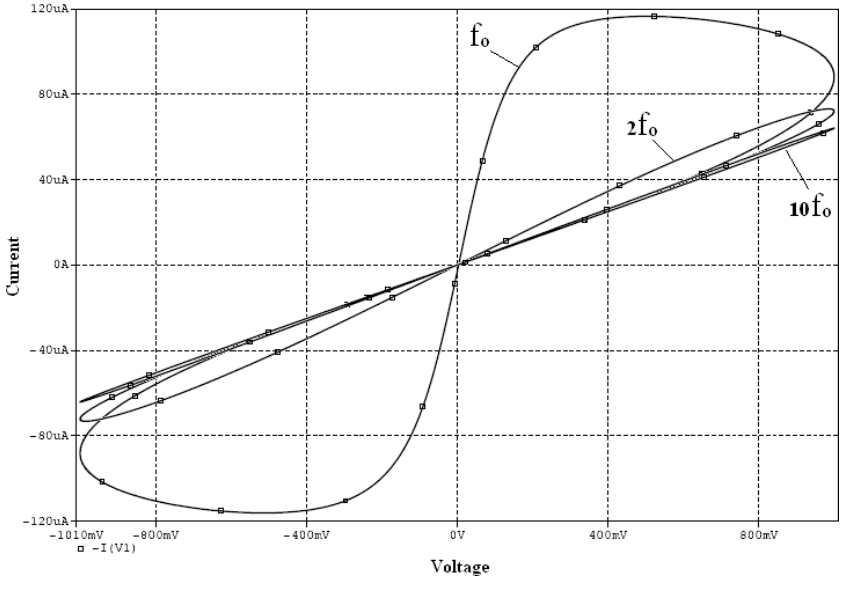
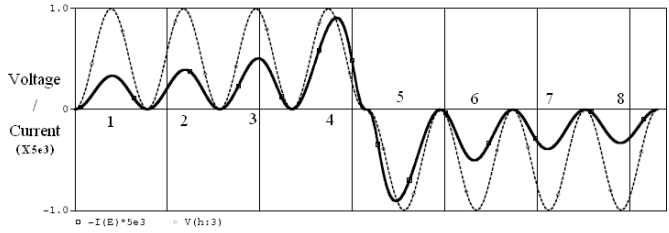
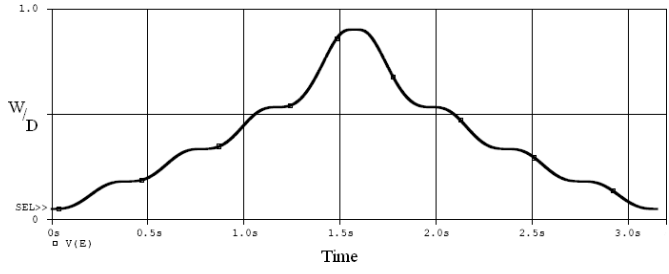


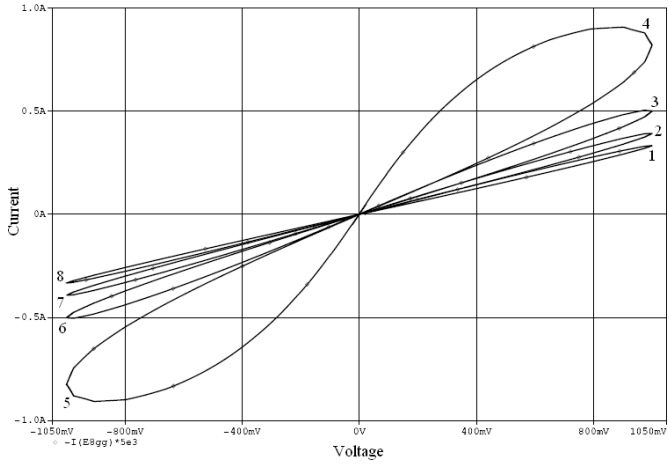
Fig. 3. Hysteresis characteristics of memristor in response to a sine wave with different frequencies. The memristor physical parameters were $D = 10\,\mathrm{nm}$, $\mu_V = 2 \times 10^{-10}\,\mathrm{cm^2 v^{-1} s^{-1}}$, $R_{OFF} = 16\,\mathrm{K\Omega}$, $R_{ON} = 100\,\Omega$ and the corresponding circuit model parameters for the flux-controlled model were $V_{ZD1,2} = 9.3\,\mathrm{V}$, $RLT = 100\,\mathrm{M\Omega}$, $C2 = 10\,\mathrm{nF}$, $R1 = 10\,\mathrm{K\Omega}$, $G1 = 1$, $C1B = 80\,\mathrm{mF}$, $G2 = 1e4$, $EVAL2 = 1e - 4(1 - PWR(1 - PWR[(1 - 0.1V_{in}), 0.5]))$.



(a)



(b)



(c)

Fig. 4. Memristor response to an asymmetric sine squared input, (a) shows the input voltage (dotted line) and resulting output current (solid line), (b) shows the state of memristor, i.e., the boundary position, (c) shows the hysteresis loop corresponding to eight sections of the input. The memristor physical parameters and the resulted model parameters are the same as Fig. 3.

Application of nonsymmetrical waves to memristor can create various resistivity conditions. Figures 4(a) and 4(b) show the input voltage, the output current and the boundary position (w) in memristor for a nonsymmetrical input. Figure 4(c) shows eight hysteresis loops resulted from eight sections of the applied input.

4. Memristor as a Nonvolatile Memory Cell

As it is suggested by its name (memory + resistor), one of the main predicted applications of memristor is in nonvolatile memories.[1] In the next two subsections, we will investigate the useful characteristics of memristors as memory cells and then simulate a memristor based memory cell using the proposed model.

4.1. *Superiority of memristor as a nonvolatile memory cell*

In recent years, nonvolatile memory has been mainly based on the flash technology.[11] In flash memories, nonvolatile property is usually made by tunneling hot electrons into a polysilicon floating gate of a MOSFET. Hence the oxide layer between the channel and the floating gate must be thick enough (thicker than 6 nm) in order to prevent back tunneling, and this requirement has always been an obstacle in the scaling down of MOSFETs.[11] The specifications of memristor makes it a perfect alternate of flash memory in future. By memristor we have a quasi capacitor type of data storage like as DRAMs but with long life time. The main issue is that in the $I - V$ characteristics of this device, there exists both the current and the integral of current which are multiplied by each other. Therefore without need to any extra circuit, only by cutting the charging current, the voltage of the device goes to zeros instantly although the stored information do not alter and therefore the control circuit of memory becomes much simpler. From an integrated circuits point of view, arrangement of memristors in crossbar structure[10] from one hand and its physical dimensions, which are only a few nanometers, on the other hand may lead to an ultra dense integration of memristors compared to flash memories. Furthermore the power dissipation of memristors is low compared to flash memories and their access time in reading process is very fast although the writing pulse must have more amplitude and longer time,[4,8] but it is less than in other kinds of devices which are probable candidates for substituting flash memories like as Phase Changing RAMs and Magnetic RAMs. By using the fast ions[17] in future, it is expected that the writing pulse in memristors will become even less than flash memories.

4.2. *Simulation of a memristor based nonvolatile memory cell*

It is possible to use both types of voltage and current controlled memristors in memory cell design. However we have used the current controlled type presented in Fig. 2(a). In this design the excitation (inputting data) is of the current type and the measurement (output data) is of voltage type as shown in Fig. 5(a). Moreover, instead of hp memristor, which because of using of TiO_{2-X}, can only operate in the frequency ranges around $10\,H_z$, we have used Rubidium Silver Iodide, which is an advanced super ionic conductor with a high ion mobility ($\mu_V = 2 \times 10^{-4}\,cm^2v^{-1}s^{-1}$ instead of $\mu_V = 10^{-10}\,cm^2v^{-1}s^{-1}$ in TiO_{2-X}).

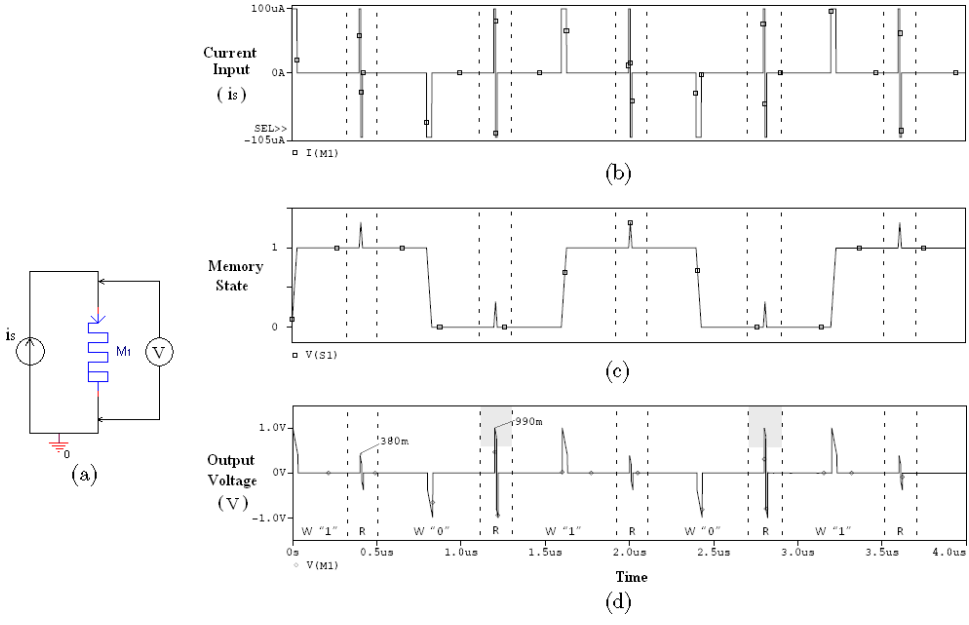


Fig. 5. Simulation results of a memristor-based nonvolatile memory cell, (a) shows a simple schematic circuit of the memory cell, (b) shows the excitation current pulses. Some sequences of write, read and recovery pulses are shown in the figure (see text for details), (c) shows the memory state in response to excitation pulses, (d) shows the output voltage. The memristor which was used in this simulation had the following parameters: $R_{OFF} = 10\,\mathrm{K}\Omega$, $D = 3.3\,\mathrm{nm}$, $\mu_V = 2 \times 10^{-4}\,\mathrm{cm^2 v^{-1} s^{-1}}$, $R_{ON} = 1\,\mathrm{K}\Omega$. The model parameters that describe this charge-controlled memristor were: $V_{ZD1,2} = 9.3\,\mathrm{V}$, $RLT = 100\,\mathrm{M}\Omega$, $C2 = 10\,\mathrm{nF}$, $R1 = 10\,\mathrm{K}\Omega$, $F1 = 1$, $C1A = 10\,\mu\mathrm{F}$, $E1 = 1e4$, $EVAL1 = 0.16(V_{in} - 0.05PWR(V_{in}, 2))$. The read and write pulses had 10 ns and 30 ns duration respectively. The output signal amplitude was about 950 mv for "0" logic and 350 mv for "1" logic so, there is adequate margin between two logic states.

Resistance switching mechanism in metal oxide memristors is similar to some types of Resistive Random Access Memories (RRAMs) such as the devices based on organic films, Chalcogendes and Perovskites, and is based on Bipolar Resistance Switching (BRS). Therefore writing the "0" and "1" logics (corresponding to low and high resistance states) are performed by controlling amplitude, frequency and polarity of the writing pulse. In these kinds of memory cells we need also a recovery pulse, in order to recover the former state before reading the pulse, which must have the same duration and amplitude as the reading pulse but with opposite polarity. These two pulses (read and recovery) may have much higher frequencies than the write pulses. Duration and amplitude of write pulses should be large enough to respect the needed margin between "0" and "1" logics. Faster write operation may be achieved by decreasing the R_{OFF}/R_{ON} ratio (see Eq. (18)) but it also causes lower margin. A nonvolatile memory cell has been designed based on the above discussions, satisfactory performance (product of write-speed by power dissipation) and enough margins between logic states. Figure 5 shows the simulation results in three graphs.

The upper graph shows the designed excitation pulses (the current source waveforms). The middle graph shows the amount of charge (memory state) and the lower graph shows the output voltages.

As shown in Fig. 5, a "1" writing pulse is applied which has changed the state of the system from zero to one. Then a pulse for reading operation is applied. In response to this pulse, the output voltage that is read will be interpreted as "1" because its amplitude is lower than 0.6 V. This pulse causes the system state to be distorted (see middle graph) so a recovery pulse has applied with the same amplitude but in the opposite direction. The next pulse in the figure is the "0" writing pulse and after that, once again, a read pulse is applied. The output voltage in response to this pulse is raised up to 990 mv and is interpreted as logic "0". After this reading pulse, a recovery pulse is once again applied. In this memory the control circuitry must be such that it always performs a read operation before any write operation to prevent successive writes of ones or zeros.

5. Memristor as Synapse in an Artificial Neural Network

An application of memristors that has recently gained much attention[10] is the application of memristor as a synapse in artificial neural networks.[14] In this section we briefly compare the synapses made by memristors versus those made by CMOS technology[12,13] and then introduce a programmable logic gate[15] based on neural network architecture using memristor synapses, and will give the simulation results using the introduced general voltage controlled SPICE model of memristor.

5.1. *Useful characteristics of memristor synapse*

CMOS is the most common technology used in analog neural network chips.[12,13] Implementation of synapse in this technology requires a circuit with three sections: a section for saving multiplying weights, a section for updating the weights and a section for implementing the multiplier itself. A single memristor can perform all of these three tasks. According to Eq. (6), if dt is small enough, which means that the duration of training phase is much longer than the operating phase, the value of the weight ($\int V dt$) does not alter considerably during the operation phase although V may be large enough. In this way, a memristor would be a linear multiplier and may act as a synapse in a neural network. Moreover the memristor synapse has almost no speed limitation in the operating phase, compared to other implementation of synapse. This will result in much higher operating frequency at the operation phase and therefore require less retraining phase and this will compensate the relatively long time required at the training phase (writing phase) of memristor synapse. Below, we have compared the CMOS synapse with the memristor synapse regarding the three mentioned roles of a memristor synapse:

(1) Usually for implementation of the weight memory in a synapse, a large capacitor in conjunction with a circuit for weight refreshing is used, which requires a vast

area of the chip.[13] In such circuits, the power dissipation is also too high. The memristor, on the other hand, is a very fine device (in nanometer scale) that works at the $V = 0$, $I = 0$ working point of its $I - V$ curve at the non-operating phase. Using the memristor, we may have fully tunable weights with good resolution. The only drawback of the memristor is that we may implement only the positive weights by the memristor. This problem may be solved by using the inverse inputs and outputs at each layer of the network in addition to the normal signals, as will be shown later.

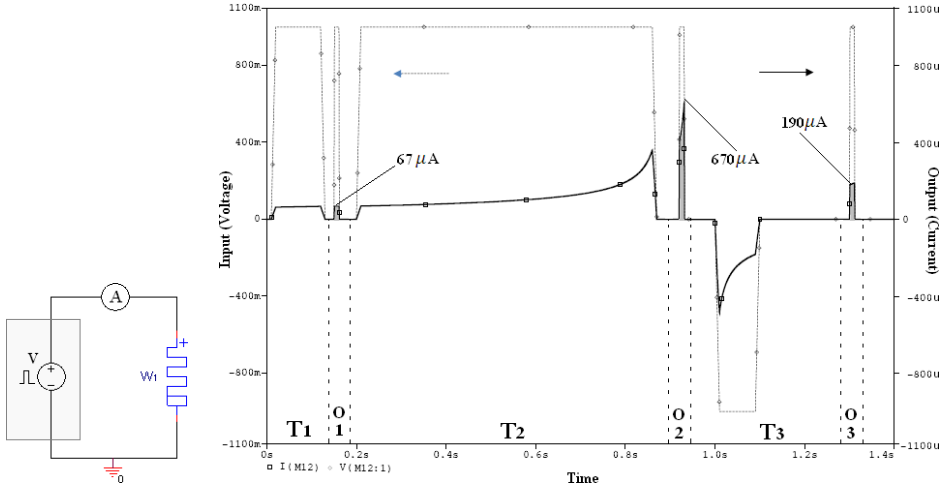
(2) A multiplying circuit in CMOS technology is usually implemented using Gilbert multiplier cells that contain many transistors,[12,13] whereas a memristor is a single element multiplier. Moreover, because of the limitation on the linearity of CMOS multiplier, the neuron nonlinear function usually takes place in the synapses instead of the neurons,[12,13] which actually is not compatible with neural network basic concepts. On the other hand, the memristor multiplication operation is quite linear so we no longer have to implement the neuron function in synapses and this will end to less network errors.

(3) Implementation of the weight modification circuit, in the circuits which are capacitor based, is very complex in CMOS technology. For example in Ref. 13 many elements (6 Switches + 1 Transistor + 2 Capacitors + 1 XOR gate + 3 NOT gates) were used for designing the weight storage and modification circuit. On the other hand, by a memristor, we can implement both the operation phase and learning phase of the network in the same crossbar structure (see next section) because the memristor is an interesting two terminal device which is used for both multiplication and weight storage. Therefore, we can easily implement on the existing crossbar structure the learning circuits too by adding a simple control circuitry. Details of this design will be introduced in the next section.

Table 1 shows characteristics of a memristor synapse in comparison with various CMOS designs. Low power consumption (because of nonvolatile capacitor-like weight memory and less transistor counts), linear behavior of the network (because of linear multiplier), more speed in the operation phase (because of using very fast memristor multiplier instead of slow Gilbert multipliers) and smaller size (because of the replacement of many transistors and a big capacitor with a nanometer memristor) are some of the main advantages of memristor based artificial neural networks.[14]

Table 1. Comparison of synapse specifications in some different neural network architecture.

Architecture	Digital[12] (1.2 μm)	Analogue CMOS-Based[12] (2 μm)	Analogue CMOS-Based[12] (0.7 μm)	Memristor-Based
Synapse size	Not Mentioned	34865 μm^2	22100 μm^2	$\sim 3\,nm \times 5\,nm$
Synapse structure	140 Transistor	17 Transistor + 2 Capacitor	14 Transistor + 1 Capacitor	Only 1 memristor



(a) (b)

Fig. 6. Application of a memristor as a neural network synapse, (a) shows a simple circuit for driving the memristor synapse, (b) shows the simulation results. Applied voltage is shown with dotted line and the response, i.e., the output current, is shown with solid line. "O" represents operation phase and "T" represents train phases. There are three train phases in the figure in which the synapse has learned the weights of $\times 1$, $\times 10$ and $\times 2.8$, respectively. Memristor characteristics in this simulation were as follows: $D = 10\,\text{nm}$, $\mu_V = 2 \times 10^{-10}\,\text{cm}^2\text{v}^{-1}\text{s}^{-1}$, $R_{OFF} = 16\,\text{K}\Omega$, $R_{ON} = 100\,\Omega$ and the corresponding circuit elements of the current-controlled model were as follows: $V_{ZD1,2} = 9.3\,\text{V}$, $RLT = 100\ \text{M}\Omega$, $C2 = 10\,\text{nF}$, $R1 = 10\,\text{K}\Omega$, $G1 = 1$, $C1B = 80\,\text{mF}$, $G2 = 1e4$, $EVAL2 = 1e-4\ (1 - PWR(1 - PWR[(1 - 0.1V_{in}), 0.5]))$.

Before going into details of the introduced memristor based network, a simple cell and its simulation results are introduced in this section. Figure 6 shows the cell and its simulation results for three periods of train phases and operation phases. We have used a type two memristor (flux-controlled memristor) and the circuit model of Fig. 2(b). The amplitude of the writing pulse is fixed (one volt) and it is assumed that the output current of 67 μA is equal to unit weight. In the simulation, the synapse learns to achieve the weights of $\times 1$, $\times 10$ and $\times 2.8$ successively at three learning phases (see Fig. 6(b)). Considering the desired weights and their sequence from one side and the characteristic frequency of the used memristor on the other, we have applied two positive learning pulses of 100 ms and 660 ms for weight increments and one negative pulse of 80 ms for weight decrement successively. As Fig. 6(b) shows, after any learning phase, an operation phase is performed and the output is examined by applying a reading pulse.

5.2. *Simulation of memristor based artificial neural network*

Programmable logic gates can be implemented by means of artificial neural networks in a feed-forward multi-layer architecture.[15] These circuits are usually tested by means of XOR or XNOR problems, because these two problems are nonlinear

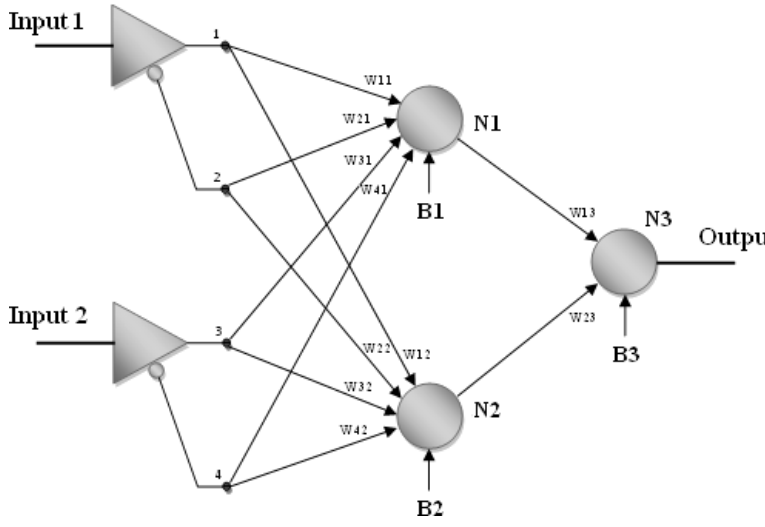


Fig. 7. A two-layer feed forward neural network that has been used as a programmable two input logic gate in this work.

problems and need two layers of feed forward network to be solved, so they can verify the learning ability of a neural network in a simple fashion.[12,13,15]

The neural network shown in Fig. 7 is a two layer network and can be trained to behave as any of two input logical gates. This network has actually four inputs, instead of two, to overcome the mentioned limitations of the memristor that cannot implement negative weights. Figure 8 shows the circuit implementation of this programmable gate in SPICE. As shown in the figure, ten synapses of this design are implemented by ten flux-controlled memristors and three used neurons are implemented by three simple diode based circuits. The control circuitry which switches the network structure between the two phases of operation and learning is also shown in the figure. This control circuit will select a set of memristor synapse (the memristors which connected to a single neuron) at a time and in this way, the learning process will be completed in three phases corresponding to the three neurons.

The network shown in Fig. 8 has been learned by the weight values shown in Table 2. Table 2 has two rows corresponding to two logic gates of XOR and XNOR, respectively. The introduced simulation has four sections. The first section is a learning phase in which all ten memristor synapses have been learned according to the first row of Table 2 assuming the "*rest*" state at $t = 0$ (rest means *zero* weight which is corresponds to high resistance state (R_{OFF})). The second section is an operating phase in which all four possible input states are applied to the two inputs and the correct output state of XOR is obtained. The third section is another learning phase in which the memristors are learned according to the second row of

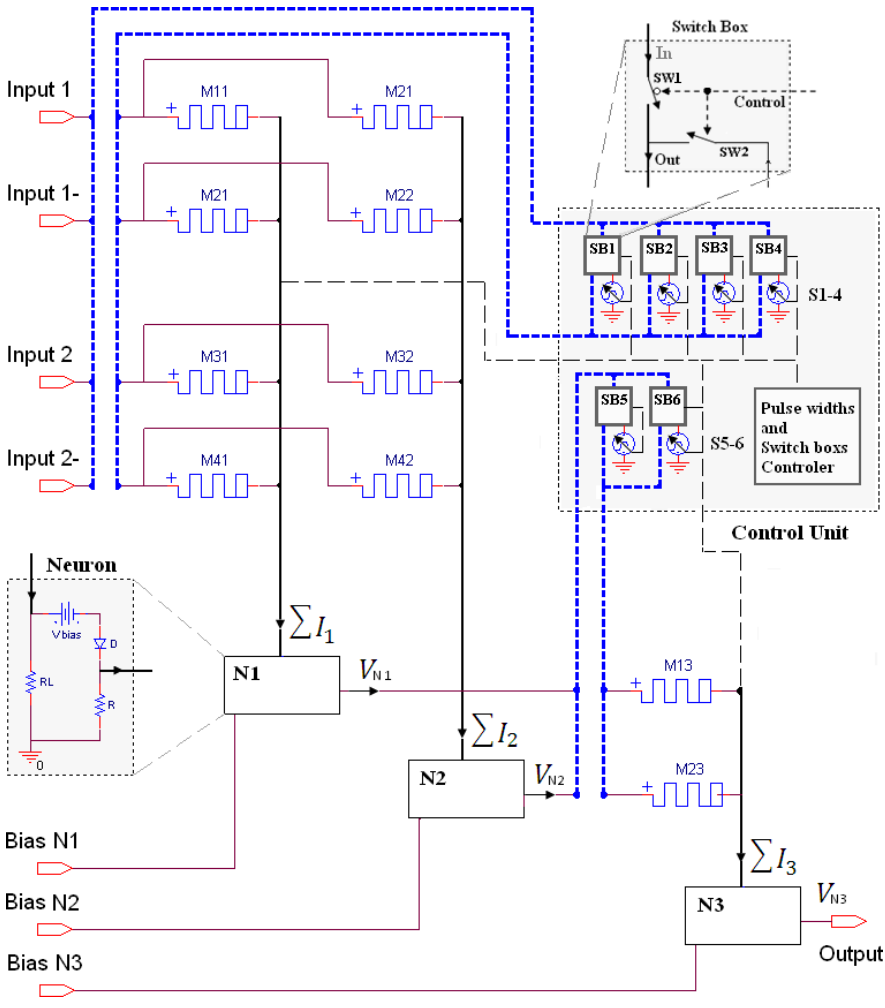


Fig. 8. Circuit implementation of the neural network of Fig. 7 by ten memristor synapses. Circuit implementation of the neurons and the control circuit are also shown in the figure. Control unit sets the circuit into the operation phase and or the learning phase. Dotted lines show the control buses. The memristors will be connected to the inputs and neurons in the operating phase. At the learning phase, all memristors corresponding to a single neuron will be connected to the voltage sources at a time.

Table 2. The required weights to be implemented in the memristor synapses (see Fig. 7) for operating the network as XOR and XNOR gates.

	W11	W21	W31	W41	W12	W22	W32	W42	W13	W23
XOR	0	1	1	0	1	0	0	1	1	1
XNOR	1	0	1	0	0	1	0	1	1	1
		B1 = −1.5				B2 = −1.5			B3 = −0.5	

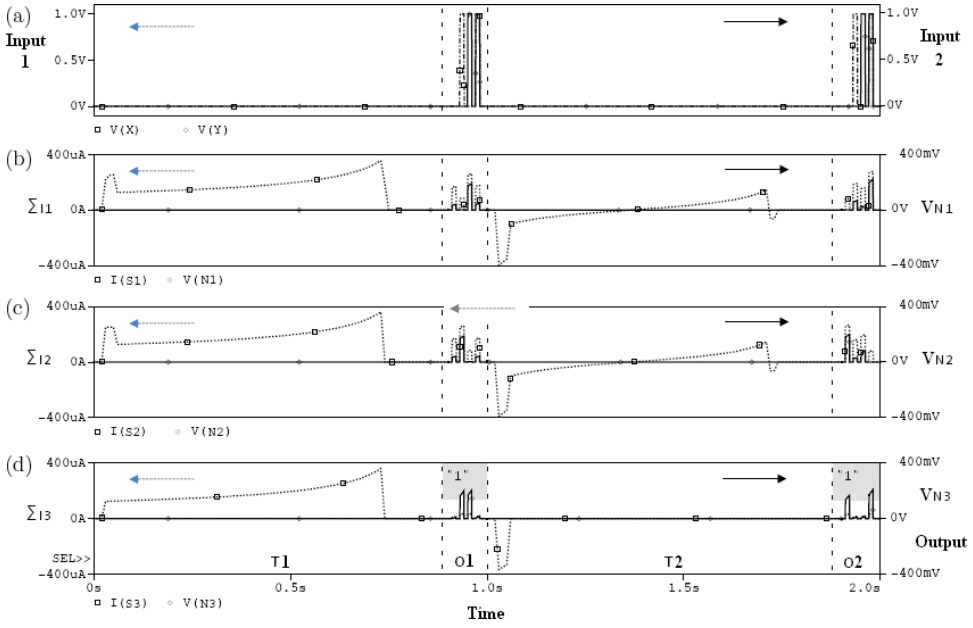


Fig. 9. Simulation result of the programmable logic gate that shown in Fig. 8, (a) shows the input signals (dotted line for input A and the solid line for input B), (b)−(d) show the input currents (dashed lines-left axes) and the output voltages (solid lines-right axes) of the three neurons respectively (N1, N2 and N3). As shown in (d) the correct logic of XOR and XNOR is obtained in the first (O1) and the last (O2) operating phases correspondingly. Memristor characteristics in this simulation are as follows: $D = 10\,\text{nm}$, $\mu_V = 2 \times 10^{-10}\,\text{cm}^2\text{v}^{-1}\text{s}^{-1}$, $R_{OFF} = 16\,\text{K}\Omega$, $R_{ON} = 100\,\Omega$ and the circuit elements of the proposed flux-controlled model, which is used in this simulation, are as follows: $\text{V}_{ZD1,2} = 9.3\,\text{V}$, $RLT = 100\,\text{M}\Omega$, $C2 = 10\,\text{nF}$, $R1 = 10\,\text{K}\Omega$, $G1 = 1$, $C1B = 80\,\text{mF}$, $G2 = 1\text{e}4$, $EVAL2 = 1e-4(1 - PWR(1 - PWR[(1 - 0.1V_{in}), 0.5]))$.

Table 2 to get an XNOR gate. Finally, the fourth section of the introduced simulation is an operating phase in which again all possible logical states are applied to the two inputs and the correct output of XNOR is shown.

The simulation results for these four sections are shown in Fig. 9 that contains four graphs in four rows. The upper graph shows the input signals (solid and dashed curves) at the two operating phase (O1 and O2). The three other graphs show the input and output signals of the three neurons, respectively, so the solid line at the third graph shows the final output of this programmable logic gate. It shows the correct output of XOR and XNOR gates at the first and second operating phases, respectively.

6. Conclusion

For a long time, memristor was only a theoretic circuit element and did not have a place in actual electronic circuits. Now, by introducing a practical memristor by hp, it seems that the situation alters and many practical circuits based on memristor will

be introduced in near future. In this paper, by examining the general characteristics of memristor, two general SPICE circuit models were introduced for the two types of memristors. Then by focusing on the different circuit aspects of memristor and by using the introduced models, two most important applications of memristor — the nonvolatile memory cell and the synapse in an artificial neural network — were discussed in two sections of the paper and in each section, by designing proper circuits, the simulation results were introduced. Memristor can be used in other areas such as signal processing,[3,7] control systems[7] and nonlinear filters. Introducing a circuit model, such as the one introduced in this paper, can greatly help designers to examine their ideas.

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