Memristor Resistance Modulation for Analog Applications

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***Abstract*—The resistance modulation (RM) of TaO_x-based memristors can be precisely controlled by the SET switching compliance current. After electroforming, switching occurs in a rebuilt oxide between the electroformed conductive filament and the Pt electrode. RM is independent of initial oxide thickness. The switching mechanism is postulated as dielectric breakdown at the sidewall of the conductive channel created within the rebuilt oxide: During a SET operation to a lower resistance state, the conductive channel increases in size, conducting a larger current until limited by the external compliance; during a RESET operation to a higher resistance state, the tip of the oxygen-saturated tantalum conductive channel is oxidized, reforming the rebuilt oxide. The conduction of the rebuilt oxide follows a power law function of voltage, in parallel with the modulated channel conductance. The linear resistance can be randomly programmed with accuracy and reproducibility. Analog circuits of tunable memristive low-pass and high-pass filters demonstrate frequency tuning by RM.**

***Index Terms*—Dielectric breakdown, filters, memristor, tuning.**

I. Introduction

PRECISION variable resistors are important for analog IC design. They are widely used, for example, in gain adjustment or impedance matching. Memristors, demonstrated at nanoscale sizes [2], show a continuous change in resistance which can act as a variable resistor in an analog circuit. In one memristive system, TaO_x (x denotes a nonstoichiometric compound), the resistance can be set to a predetermined value by using current compliance (CC) in a SET operation [1]. Importantly, its SET state resistance is linear; however, to be useful for analog applications, the resistance setting must be reproducible and precise, with an adequate modulation range. The vulnerability of resistance value to disturbs, retention, and overvoltage must also be specified. A physical switching model must address these important requirements [2]–[4] and explain the resistance modulation (RM) mechanism. In this letter, we show that memristors exhibit useful analog behavior, present a physical switching model, and demonstrate the application of TaO_x variable resistors in tuning analog filters.

II. Experiment

The memristor system studied is composed of Pt (30 nm)/TaO_x (z nm)/Ta (30 nm) stacked layers, where z varies from 5 to 20 nm. The Pt and Ta metals were deposited by E-beam evaporation: The devices were defined by either photolithographically patterned leads (5- and 8-nm oxide devices), or by shadow masks (10- and 20-nm oxide devices). All devices were micrometer sized. Blanket TaO_x films were sputter deposited. The Fig. 1 inset shows a SEM micrograph of a crossbar structure. Positive external voltage V is applied to the top Ta electrode; the bottom Pt electrode is grounded. An electroforming process [5], [6] was required to initiate switching ($+3$ V external with a 10-μA compliance). The electroforming (i.e., oxide breakdown) creates a local conductive filament (CF) whose resistance can then be modulated by external voltage or current [7], [8]. All electrical measurements utilize four terminals, and the internal voltage V_{internal} is plotted. The black envelope curve in Fig. 1 shows a typical memristive I–V; the external voltage V was swept to -1.2 V without CC then to $+1.0$ V with a 5-mA compliance. The SET and RESET states correspond to the high and low slope sections through the origin on the I–V curve. The SET state is a linear resistance near $V = 0$ V; the RESET state exhibits a diodelike I–V, with forward bias at negative polarity. Electrical measurements were conducted using an HP4155A semiconductor analyzer and an Agilent 4294A impedance analyzer.

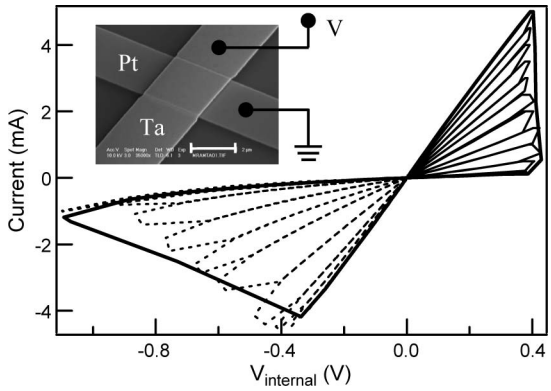

Fig. 1. Envelope curve is a four-terminal full I–V loop. The thin solid curves are current-limited incremental SET switching, with the compliance current increasing in small steps. The dashed curves are voltage-limited incremental RESET switching, with the maximum sweep voltage increasing in small steps but without CC. The inset is a SEM snapshot of a 3 μm $\times$ 3 μm crossbar. The scale bar length is 2 μm.

III. Results and Discussion

In Fig. 1, the loci of solid curves are sequential incremental SET switching curves with increasing CC I_{comp} ($V_{\mathrm{SET}} = +1.0$ V external). The loci of dashed curves are sequential incremental RESET switching curves with the maximum applied

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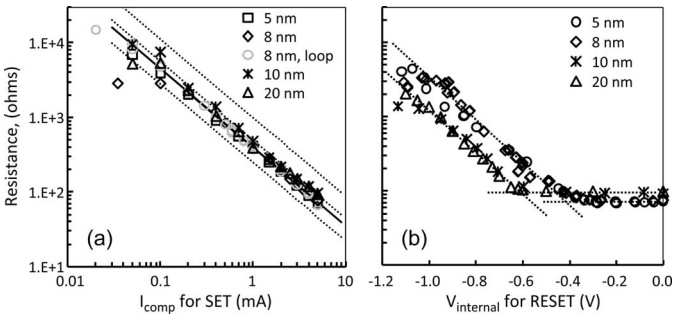

Fig. 2. (a) LRS resistances measured after incremental (5–20 nm) and full (8 nm only) SET switchings as functions of compliance current. The RM data follow a simple relation, (solid line) $R * I_{\rm comp} = 0.4$ V. (b) HRS resistances measured after incremental RESET switching as functions of maximum device voltage. RM onset voltages are ~ -0.4 and -0.6 V (see text).

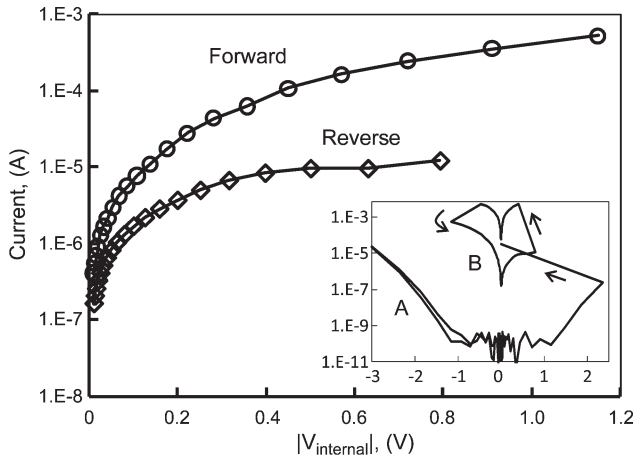

Fig. 3. Diodelike I–V of the RESET state (from curve B in the inset). The inset shows the (curve A) I–V of as-deposited 8-nm oxide, the forming of CF in oxide at +2.4 V, and (curve B) the subsequent switching loop.

negative voltage ($V_{\rm RESET}$) increasing up to -1.2 V without CC. The RM is measured as the I–V slope at small device voltages (-0.1–$+0.1$ V) after each SET or RESET operation. The I–V curves after large $V_{\rm RESET}$ approach the forward diodelike I–V of the black envelope curve.

A second series of RM data was obtained from multiple full switching loops (not shown), similar to the black envelop curve in Fig. 1, with sequentially increasing CC. Each full switching loop consists of a RESET at $V_{\rm RESET} = -1.15$ V, without CC, followed by a SET at $V_{\rm SET} = +1.0$ V, at increasing $I_{\rm comp}$ with each sweep. After each SET operation, the RM is measured (see above).

For SET, the measured resistances of both incremental and full switching loops are plotted as functions of $I_{\rm comp}$ in Fig. 2(a); they fall on a straight line with the simple relation [1] $R * I_{\rm comp} = 0.4$ V. Note that the data of all four oxide thicknesses fall on the same line. $R * I_{\rm comp}$ is the voltage across the memristor; thus, the device voltage remains constant at all $I_{\rm comp}$ values spanning about two decades. The final state of a SET operation is always 0.4 V across the device for a given $I_{\rm comp}$, independent of the SET operation (incremental or a full switching loop) or device switching history. Consequently, the resistance R can be calculated from $I_{\rm comp}$ regardless of switching history. The initial leakage current shows high resistance saturation at low $I_{\rm comp}$ values. The high resistance is limited by the RESET diode leakages to about 10 000 Ω. The 0.4 V across the device represents a localized dielectric breakdown responsible for the RM. If the dielectric strength is 0.4 V/8 nm, then the other oxide thicknesses (5, 10, and 20 nm) should switch at different voltages (0.25, 0.5, and 1.0 V, respectively) as shown by the three dotted lines. Thus, the switching mechanism is independent of initial oxide thickness.

Fig. 2(b) shows RESET switching where the resistance R, measured after incremental switching, is plotted as a function of maximum (negative) device voltage. RM initiates near the interceptions of dotted lines, about -0.4 and -0.6 V, and then increases with $|V_{\rm internal}|$ until reaching saturation at about -1.0 V. The onset voltages of RM are affected by the fabrication processes (i.e., 5 and 8 nm are patterned crossbar process; 10 and 20 nm are shadow mask process) but do not depend on the oxide thicknesses. The resistance saturation is due to the interfacial leakage current of the RESET diode, shown hereinafter.

The inset in Fig. 3 is the electroforming I–V described earlier. Curve A is the I–V of as-deposited oxide which shows the Fowler–Nordheim tunneling current for $|V_{\rm internal}| > 1$ V. At +2.4 V, electroforming initiates the lower resistance state (LRS) of curve B, which correlates to the black envelope curve in Fig. 1. The LRS is a linear resistance; the higher resistance state (HRS) has a diodelike I–V. The HRS diode is not an ideal Schottky diode as its forward current is not an exponential function of voltage, i.e., a linear line in Fig. 3. The HRS I–V is characteristic of an oxide rebuilt between the CF and the Pt electrode during RESET. The rebuilt-oxide thickness is not correlated with the initial oxide thickness; thus, $R * I_{\rm comp} = 0.4$ V can apply for all initial oxide thicknesses in Fig. 2. The constant device voltage, 0.4 V, after an $I_{\rm comp}$-limited SET, can be explained by a channel sidewall switching model (CSSM). The electroforming process creates a local CF composed of oxygen-saturated Ta metal, Ta(O), which is surrounded by the as-deposited nonconductive TaO_x matrix [9]. A negative RESET voltage rebuilds a leaky oxide, TaO_y, between the CF and the Pt electrode. Its thickness may depend on $V_{\rm RESET}$, which is restricted by the forward diode current. A positive $V_{\rm SET}$ creates a conductive channel in the rebuilt oxide TaO_y. The channel sidewall will break first because of weaker bonding, and the oxide dissociates into Ta^+ and $O^=$. The channel sidewall dielectric strength multiplied by the rebuilt-oxide thickness gives a constant device voltage, 0.4 V, which is independent of the as-deposited oxide thickness. For SET, with a CC $I_{\rm comp}$, the polarity of the electrical field causes the $O^=$ ions to drift up, adding reduced Ta(O) to the conductive channel. The immobile Ta(O) increases the conductive channel size and correspondingly decreases its resistance. This localized breakdown process continues until the current reaches $I_{\rm comp}$, at which point sidewall breakdown ceases. The current-limited SET reaches its final state, and the final resistance is solely determined by $I_{\rm comp}$.

The RESET is voltage controlled without CC [10]. The polarity of the electrical field causes the $O^=$ ions to drift down and

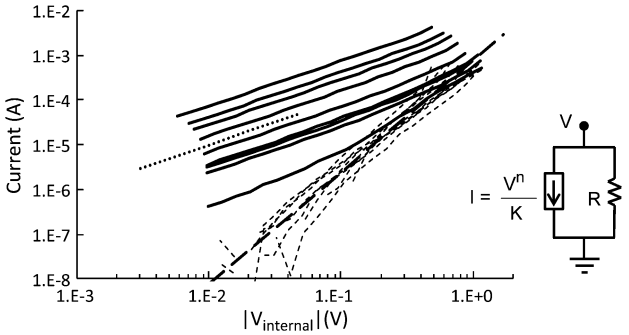

Fig. 4. (Solid curves) Replotted I–V curves after incremental RESET switchings in Fig. 1 and (dash curves) their corresponding power law components. The dotted line is the I–V of a 1000-Ω resistor for comparison. The dashed line is the power law $I = V^n/K$, with $n = 2.5$ and $K = 1200$, where I is in amperes and V is in volts. The inset is a circuit model for the rebuilt oxide.

oxidize the tip of the Ta(O) channel [11], [12]. The resistance increases as the channel size shrinks. The onset is at about the same dielectric strength of the SET process. In the final state, the channel is sealed off by the rebuilt oxide.

To characterize the rebuilt oxide, the negative HRS curves of Fig. 1 are replotted in Fig. 4 (solid). The linear resistances from the low-voltage data points (< 25 mV) are calculated, and then, their shunting currents are subtracted off. The resulting nonlinear current component (dashed) has a narrow distribution, even though the linear component varies over two decades. The nonlinear component is approximated by $I = V^n/K$, with $n = 2.5$. The two components are shown schematically in the inset: The linear component corresponds to RM under the CSSM; the power law component corresponds to the diodelike property of TaO_y to the Pt interface.

Reproducibility was verified by full-switching-loop SET operations using randomly selected $I_{\rm comp}$ (50 μA to 5 mA), which show RM over two decades (15 000–75 Ω). The R values fall on the same $V_{\rm internal} = 0.4$ V line of Fig. 2(a). Thus, resistance can be programmed to a preset value accurately and reproducibly.

The programmable resistor is used for building tunable low-pass and high-pass filters. The insets in Fig. 5(a) and (b) show the simple RC circuits using TaO_x memristor as variable resistor. The transfer functions shown were measured after programming the memristors to predetermined resistance values. In correspondence to the RM, the cutoff frequency, $1/(2\pi RC)$, spans over two decades. Both low-pass and high-pass transfer functions show an abnormal response at high frequencies above 1 MHz. For the low-pass filter, it deviates from continuing roll-off at -6 dB/octave. For the high-pass filter, it deviates from approaching unity gain. These abnormalities are due to the frequency response of the 1-nF capacitor and the interconnection parasitic. Other applications include fully tunable bandpass filters (by cascading low-pass and high-pass filters, with both memristors tunable).

IV. Conclusion

The field programmable resistor or resistor array is a novel circuit element useful for mixed-signal IC design. We have demonstrated the accurate and reproducible tuning of memristor devices by controlling the SET compliance current. The proposed CSSM reproduces the observed phenomenon. Applications of low-pass and high-pass filters have been demonstrated.

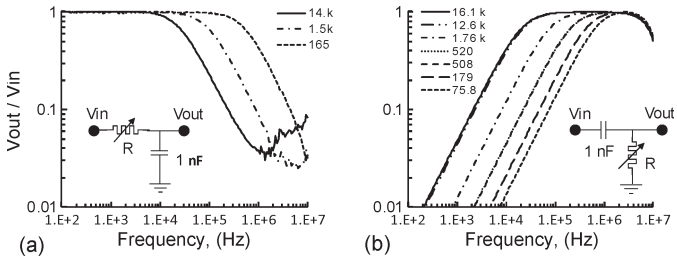

Fig. 5. Transfer functions of (a) low-pass filter and (b) high-pass filter, made by connecting a memristor and a capacitor. The memristor resistances are programmed for tuning the frequency response. In the aforementioned legends, the resistances are in ohms.

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