Path Summary

	Property	Value
1	From Node	IP_Catalog:U3|altsyncram:altsyncram_component|altsyncram_7j14:auto_generated|ram_block1a0~porta_we_reg
2	To Node	IP_Catalog:U3|altsyncram:altsyncram_component|altsyncram_7j14:auto_generated|q_a[9]
3	Launch Clock	Clock
4	Latch Clock	Clock
5	Data Arrival Time	5.243
6	Data Required Time	4.203
7	Slack	-1.040 (VIOLATED)

Statistics

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	1.000					
2	Clock Skew	-0.885					
3	Data Delay	1.055					
4	Number of Logic Levels		0				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		3	1.929	46	0.000	1.696
2	Cell		3	2.259	54	0.273	1.376
2	Data						
1	Cell		1	1.055	100	1.055	1.055
2	uTco		1	0.000	0	0.000	0.000
2	Required Path						
1	Clock						
1	IC		3	1.687	55	0.000	1.620
2	Cell		3	1.353	45	0.252	0.610

Data Path

Data Arrival

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	4.188	4.188					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_AA15	Clock
3	0.000	0.000	RR	IC	1	IOIBUF_X40_Y0_N18	Clock~input|i
4	0.610	0.610	RR	CELL	1	IOIBUF_X40_Y0_N18	Clock~input|o

	Total	Incr	RF	Type	Fanout	Location	Element
5	0.843	0.233	RR	IC	1	CLKCTRL_G6	Clock~inputCLKENA0|inclk
6	1.116	0.273	RR	CELL	10	CLKCTRL_G6	Clock~inputCLKENA0|outclk
7	2.812	1.696	RR	IC	34	M10K_X58_Y2_N0	U3|altsyncram_component|auto_generated|ram_block1a0|clk0
8	4.188	1.376	RR	CELL	12	M10K_X58_Y2_N0	IP_Catalog:U3|altsyncram:altsyncram_component|altsyncram_7j14:auto_generated|ram_block1a0~porta_we_reg
3	5.243	1.055					data path
1	4.188	0.000		uTco	12	M10K_X58_Y2_N0	IP_Catalog:U3|altsyncram:altsyncram_component|altsyncram_7j14:auto_generated|ram_block1a0~porta_we_reg
2	5.243	1.055	RR	CELL	1	M10K_X58_Y2_N0	IP_Catalog:U3|altsyncram:altsyncram_component|altsyncram_7j14:auto_generated|q_a[9]

Data Required

	Total	Incr	RF	Type	Fanout	Location	Element
1	1.000	1.000					latch edge time
2	4.303	3.303					clock path
1	1.000	0.000					source latency
2	1.000	0.000			1	PIN_AA15	Clock
3	1.000	0.000	RR	IC	1	IOIBUF_X40_Y0_N18	Clock~input|i
4	1.610	0.610	RR	CELL	1	IOIBUF_X40_Y0_N18	Clock~input|o
5	1.677	0.067	RR	IC	1	CLKCTRL_G6	Clock~inputCLKENA0|inclk
6	1.929	0.252	RR	CELL	10	CLKCTRL_G6	Clock~inputCLKENA0|outclk
7	3.549	1.620	RR	IC	34	M10K_X58_Y2_N0	U3|altsyncram_component|auto_generated|ram_block1a0|clk0
8	4.040	0.491	RR	CELL	1	M10K_X58_Y2_N0	IP_Catalog:U3|altsyncram:altsyncram_component|altsyncram_7j14:auto_generated|q_a[9]
9	4.303	0.263					clock pessimism removed
3	4.203	-0.100					clock uncertainty
4	4.203	0.000		uTsu	1	M10K_X58_Y2_N0	IP_Catalog:U3|altsyncram:altsyncram_component|altsyncram_7j14:auto_generated|q_a[9]