Polar Code Encoder and Decoder Implementation

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Abstract— Polar codes are error correction codes developed by Erdal Arikan which achieves channel capacity and its reduced complexity makes it more attractive and successful. In the past several decades we are searching for some techniques which will reduce the effect of noise to a very low value so that we can reproduce the transmitted signal more accurately. Erdal Arkan come up with a new concept which known as polar codes, here we use a channel polarization concept and hence named as polar codes. The discovery of polar code is standing as a milestone in coding theory and lot of researches are carrying out on this topic. Variety of schemes have been proposed over these years for the generation, encoding and decoding of polar codes. The important area of research is the decoder section and most widely used one is successive cancellation decoder[3]. Reduced complexity is the most attractive feature with an overall encoding and decoding complexity of O(NlogN) for a block size of N ,which leads to its great success. Polar code concept is used in the most promising 5G technology[10]. In this work a complete implementation of the polar Encoder and decoder is discussed with its MATLAB and Verilog implementations

keywords— AWGN, LLR, Polar codes, Successive cancellation.

I. INTRODUCTION

Polar code is a linear block error correcting code, is also known as capacity achieving error correcting codes. Polar codes are introduced by Erdal Arkan in 2009 [1] at Bilkent University. Polar codes have low encoding and decoding complexity. To obtain a capacity achieving polar code decoder with minimum hardware complexity is the main objective of this work.

In a communication system the most important challenge that we are facing is the effect of noise on the signal that — is transmitted through a channel. Practically channel cannot — be made perfect, so noise can not be avoided completely. Generally in communication system we use AWGN nois model [9]. In the past several decades we are

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searching for some techniques which will reduce the effect of noise to a very low value so that we can reproduce the transmitted signal more accurately. Erdal Arkan come up with a new concept which known as polar codes here we use a channel polarization concept and named polar codes. Here we are dividing the entire channel and we are categorizing them into noisy channels and perfect channels. Data bits are transmitted only through the channel with maximum capacity so that the effect of noise is very less. The main challenge is to find those channels which has maximum capacity. Polar codes are very efficient because of the minimization of error. The Fig.1 shows the general block diagram of a communication system. It consist of a sender receptor and channel. In order to send data over a communication channel we need to encrypt the date and it is done by the encoder. We are receiving the transmitted signal with noise at the receiver and the signal reconstruction is done by the decoder.

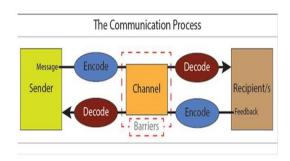


Figure 1 General block diagram of a communication system [1]

Polar encoding is done with the help of a generator matrix. There is a square matrix of order 2 called the standard generator matrix. As the number of the data bits increases we need to use higher order generator matrix and it is obtained from the standard generator matrix by taking the kronecker product. For example if we have an 8 bits of data bits we need to use a generator matrix

of order 8, it is obtained by taking repeated kronecker product of the standard generator matrix. Decoding of the polar code is done with successive cancellation (SC) algorithm. It can achieve the capacity of arbitrary binary-input discrete memory less channels. For the low-complexity and its variant Successive cancellation List (SCL) algorithms, they are using inherent serial decoding approaches. First invented decoding algorithm for polar codes is Successive cancellation algorithm. Due to Successive cancellation algorithm, decoding procedure that can fully utilize the property of polar encoding. The inherent serial decoding manner causes the long latency problems for SC decoder design.

In this work, an 8 by 8 polar encoder and decoder has been implemented, the results shows notable increase in the efficiency because even in highly noisy environment we are able to decode the message signal. Also the complexity of the encoder and decoder has reduced notably which helps in easy implementation of the encoder and decoder which further increases the efficiency of the system? Polar codes can achieve the channel capacity of binary input symmetric memory less channels and arbitrary discrete memory less channels since they are a significant breakthrough in coding theory. A successive cancelation (SC) algorithm with a complexity of O(N logN) will capably decode Polar codes of block length N. While polar codes of very large block length (N ¿ 220) method the capacity of underlying channels under the SC algorithm, for small or moderate polar codes, the error performance of the SC algorithm is poorer than turbo or LDPC codes[6].

Polar codes are a channel coding technology and entire channel coding technology working is similar. Communication links are susceptible to faults due to interference, device impairments, etc. that corrupt the given data stream at the receiving end. Channel coding fundamentally employs a set of algorithmic operations on the given data stream at the transmitter, and additional set of operations on the received data stream at the receiver to correct these errors.

II. CHANNEL POLARIZATION

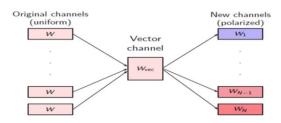


Figure 2 Channel polarization

The Fig.2 shows the channel polarization concept, among the original channel we are dividing them into noisy and perfect channel[1].and we are transmitting data only through perfect channel so the channel is said to be polarized.

An ordinary channel W is transformed into perfect and use- less channels[1]. The process involves three main steps- code construction, encoding and decoding. The channel capacity is simply aggregated and redistributed. The concept of channel polarization was introduced by Arkan. Here a polarization transformation is tested to enhance the probability of making a correct decision of bits transmitted over a memory less channel. Let X be a Binary Discrete Memory less channel with output and input represented as Z and Y, respectively and transition probability X(z-y), where y Y and zZ. The symmetric channel capacity, J(X), and the Bhattacharyya parameter, A(X) are two metric to measure the channel quality and can be defined as

$$J(X) = \sum_{z=Z} \sum_{y=Y} \frac{1}{2} X(x/y) \log \frac{X(\frac{z}{y})}{\frac{1}{2} X(Z/0) + X(Z/1)} [2]$$
 (1)

also

$$A(X) = \sum_{z=Z} \sqrt{X(z/0)X(z/1)}$$
 [2]

The symmetric capacity is the Highest rate at which predictable communications can occur over X and the Bhattacharyya parameter gives an upper constraint on the probability of erroneous detection when ML is used for evaluating a single received symbol z. Both X and Bhattacharyya parameters have values in the range [0, 1] and are connected by the following two inequalities when transmission occurs over a Binary Discrete Memory less channel

$$J(X) \ge \log \frac{2}{1 + A(X)} \tag{3}$$

$$J(X) \le \sqrt{1 + A(X)^2} \tag{4}$$

and it is clear from the observations that $J(X)\approx 1$ iff $A(X)\approx 0$ and $J(X)\approx 0$ iff $A(X)\approx 1$ depicts the error free transmission (a perfect channel) and $J(X)\approx 0$ depicts the case that transmission of information is not possible (a completely-unreliable channel).

The transmission of two bits (u0, u1) $\in X^2$ using two independent instances of Xor with the help of the memory less X twice, the we received two values (y0, y1) $\in Y^2$ with the following mutual information values:

$$J(z0, z1 : U0) = J(X) = J(z0, z1 : U1)$$
 (5)

By transforming (u0, u1) are into (x0, x1) such that: x0 = u0 \bigoplus and x1 = u1, then the mutual information value in between the data and symbols received become:

$$J(z0, z1 : U0) \le J(X) \le J(z0, z1 : U1)$$
 (6)

In other words, the Probability of correctly deciding u0 decreases while probability of correctly deciding u1 increases. To transform multiple instances of X, polarizing transformation can be applied recursively, for eight occasions of the channel. An increase in transformed channels number, that is as the code length, N, tends to infinity, the probability of correctly deciding a symbol ui approaches a high(1.0) (completely reliable) or low (0.5) (completely unreliable). The code rate, R, approaches the channel capacity, C when the proportion of reliable bits approaches the channel capacity.

III. POLAR ENCODER

The encoder uses a generator matrix to create a new code word from the message signal. The nth Kronecker power of a matrix G2 is used to get the code word.

$$G = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \tag{7}$$

Let us represent the input data as u = (u0, 1,...,uN1) for N = 2n. The corresponding code word is given by the following operation and let it be represented as X = (x0,x1,...,xN1). Then the encoded code word is obtained by Matrix multiplication and modulo2 addition.

For example, let N = 8. The encoder now requires an 8x8 matrix formed by doing repeated Kronecker product of the standard matrix G.

$$G3 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

The matrix G3 is used to create the encoder circuit. As per the concept of channel polarization, the channels are classified into useless and perfect based on a ranking as provided by the information rates of the channels. The useless channels are frozen with bit zeros and message is sent through the perfect channels. The code word X now passes

(8)

 $X = [u0 u1 u2 u3 u4 u5 u6 u7] \pm G3$ Let the frozen bits set be given by F = 0.1.2.4. Then, X = [0.0.0.0.4] $\pm G3$.

through the channel after modulation.

The information set depends on the channel being used. It varies for different channels. Figure 3 shows an encoder for N = 8. The code word is in the bit reversed order.

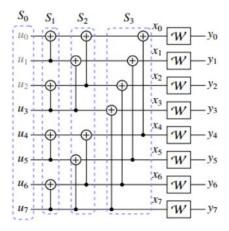


Figure 3 . Polar code Encoder for N =8

IV. FROZEN BIT DETERMINATION

The frozen bit determination can done using an algorithm proposed by Vangala[5]. In this section, a simulation-based method is described for the selection of information bits. It uses the theory behind decoding. As already seen channel polarization constructs the polar code indicating some channels to be more robust and some others to be weaker. The selection of information or frozen bits means to find out the more robust sub-channels. The SC decoding algorithm assumes that each bit being decoded is correct and moves forward. So one bit from the N bits is chosen as the information bit with all the other bits as known

or as frozen. A recursive simulation is performed to find the best set. A series of steps are involved in this with each step dependent on the previous steps. The summarized algorithm for selection is given.

- Initialization- Consider a polar code with length N. Let the number of information bits k = 0, the information set Q = and and the number of elements in Qc be N.
- Code Generation- Take k = k+1. Generate an (N,K,A) polar code using one bit from Ac as an information bit.
- 3) Simulation- Perform Monte Carlo simulations for all the possible codes. Choose from among them the best one. and select the one with best performance. At a specified SNR, (N-K) exhaustive search is performed to estimate the bits. The sets A and A c are then updated with the best code.

An iterative execution of steps 2 and 3 is done so that code rates as desired can be achieved. The bits are selected in an incremental way. The proposed algorithm selects the infor- mation bits in an incremental manner. Multiple bit selection instead of just one at a time can increase the speed reducing the iteration time at the cost some performance loss. Use of field programmable gate arrays also improve the speed of frozen bit determination.

V. DECODER

The principle of decoding lies in decision making of bits at the decoder output from the LLR values of the sent message bits. A number of decoder architectures were proposed like the list decoders. Successive cancellation decoder is widely used among these due to its reduced complexity. A direct mapping of the decoder components would contribute to a complexity of 2N whereas it is proven that SCD has a complexity of just O(NlogN).

A. Algorithm

SCD makes its decisions on bits one by one. so only one decision can be made at a time. To decode the ith bit, it requires LLR of channel output y and the partial modulo sums of previously estimated bits. The rules used for decoding are given below:

- If the ith bit belongs to the frozen bit set, then the estimate ui will be estimated as zero.
- 2) If the ith bit does not belong to the frozen bit set, then the LLR

value of the last stage is compared with a threshold value to estimate the result[7], which is generally zero.

- ui will be estimated to be zero if the LLR Lui is greater than or equal to zero.
- ui will be estimated to be one otherwise.

$$u_{\varepsilon} = \begin{cases} 0, & \text{if } L_{u_{\varepsilon}} \ge 1 \\ 1, & \text{otherwise} \end{cases}$$

Thus a recursive computation as described above results in the estimation of all the N bits sent over the channel. An example for this principle can be illustrated with the help of a length 2 decoder .The input bits u1 and u2 and transformed to x1 and x2, respectively and are transmitted over the channel. The nature of the channel W is assumed to be known. The output of the channel y1 and y2 are now used to compute the LLRs. The are two types of nodes- g and f which are used in the LLR are calculations. The formulae used for LLR calculation throughout this work are given below in the equations 9 to 16.

$$L_f(L_1, L_2) = sign(L_1).sign(L_2).min(|L_1|, |L_2|)$$
 (9)

$$L_g(u_s, L_1, L_2) = L_1.(-1)^{uS} + L_2$$
 (10)

$$sign(L_f) = sign(L_1) \bigoplus sign(L_2)$$
 (11)

$$|L_f| = min(|L_1|, |L_2|)$$
 (12)

$$r = \begin{cases} 1, & \text{if } |L_1|_{\dot{c}}|L_2| \\ 0, & \text{otherwise} \end{cases}$$
 (13)

$$B(i,l) = i/2^l \mod 2 \tag{14}$$

$$sign(L_{i,l}) = \begin{cases} sign(L_1), & \text{if } B(i,l) = 0\\ sign(L_2), & \text{otherwise} \end{cases}$$
 (15)

$$|L_{i,l}| = \begin{cases} |L_1|, & \text{if } B(i,l) = 0\\ |L_2|, & \text{otherwise} \end{cases}$$
 (16)

With the knowledge of Lf and Lg, the estimates ue1 and ue2 are made. Now for any length of data the decoder works in a similar

way. On knowing the LLRs of the encoder outputs and frozen bit set, the decoder makes an estimate the bits that are sent over the channel. Earlier likelihood ratios were used. LLRs are preferred over simple likelihood ratios due to the reduced complexity for implementation and its more accurate calculations.

B. Decoding Of u0

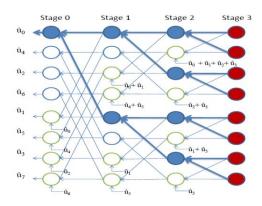


Figure 4 Decoding OF u0

VI. SCD COMPONENTS

An SCD has four major components as shown in the below architecture- processing element, partial sums update logic, memory units and controller. Architecture of SCD is shown in Fig. 5

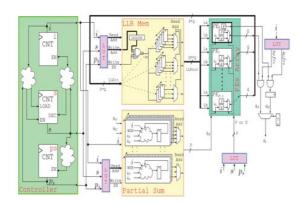


Figure 5.Architecture of an SCD

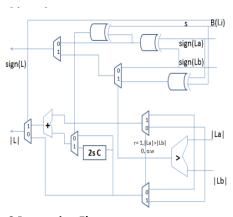


Figure 6 Processing Element

VII. PROCESSING ELEMENT

The processing elements are implemented using the log likelihood ratios Initial architectures involved the direct implementation and hence had more complexity. The processing element is shown in Figure .6 , With a semi- parallel architecture introduced, the complexity was reduced and for an N length decoder it came out that the number of PEs required can be even less than N/2 with resource sharing employed. The entire process can be completed in 2N-2 clock cycles without resource sharing[4]. It gave a throughput of 90 percent for N/2 PEs. The f and g functions are merged into a single unit as shown in figure for hardware implementation ease. The sign and magnitude representation is used for this. The f function computation utilizes an XOR gate and a bit compare and select (CS) operator.

VIII. PARTIAL SUM UPDATION UNIT

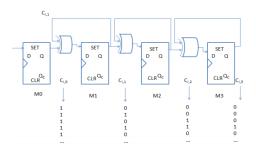


Figure 7. Matrix generation unit

The g node requires partial sums of previously estimated bits for its calculation. This bit represented as us is based on an update logic. The update unit will have (N-1) registers for partial sum storage along with some combinational logic.

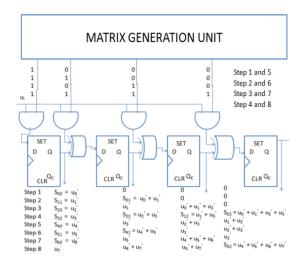


Figure 8. Partial sum Updation unit

IX. RESULTS AND CONCLUSION

The process of polar coding was implemented in MATLAB. For a code length of N =8 and a code rate of k =1/2, a message $u = [\ 0\ 0\ 0\ 1\ 0\ 1\ 0\ 1]$ is to be sent. The generator matrix encodes the signal into the code word X which is modulated before being sent over the channel.

Fig.9 shows that, for an increasing SNR the BER keeps on decreasing as desired. For an increase in the length of sent data, the BER decreases. Similarly the noise power decreases for an increase in SNR. Altogether the desired condition is an increased SNR with lower BER as achieved here. Thus polar codes fall under the category of capacity- achieving codes .Different components of the decoder is implemented in Verilog The most important advantage of polar coding is its reduced complexity. To show the reduced complexity different components used in SCD is implemented in Modelsim.

Each elements combines to get a complete decoder after verification Fig 10, 11,12 shows

the out put of the Processing Element, the matrix generation unit and Partial sum updation unit out put respectively in Verilog. The block diagram of these is shown in figures 6,7 and 8.The main SCD components are processing element, matrix generation unit and Partial sum updation unit. The processing elements are implemented using the log likelihood ratios expressed in equations 9 and 10. The f and g functions are merged into a single unit as shown in figure 6. The f function computation utilizes an XOR gate and a bit compare and select (CS) operator.. The g function implementation uses a signed magnitude adder/subtractor. The sign(Lg) and |Lg| values are calculated on knowing us, sign(L1),sign(L2), |L1| and |L2|. It also depends on the relation between |L1| and |L2|.The g node requires partial sums of previously estimated bits for its calculation. This bit represented as us is based on an update logic. The update unit will have (N-1) registers for partial sum storage along with combinational logic. Now, figure 8 is the actual with the matrix generation incorporated into it for N = 8. The SCD can have a maximum of N/2 g function evaluated in parallel. Hence the PSU will have N/2 bit register to store the partial sums, N/2 AND gates, N/2 DFFs, N/2 XOR gates and a matrix generation unit. The operation of this PSU can be simply reduced to the following concept for any N..

The main contribution of this work are the implementation of polar encoder and decoder in Matlab , detailed analysis of decoder and implementation of various components of SCD in Verilog .

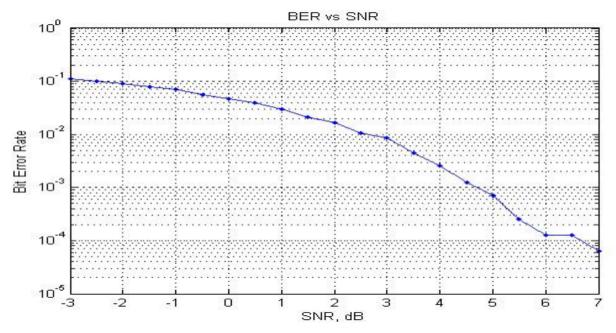


Figure 9 BER VS SNR

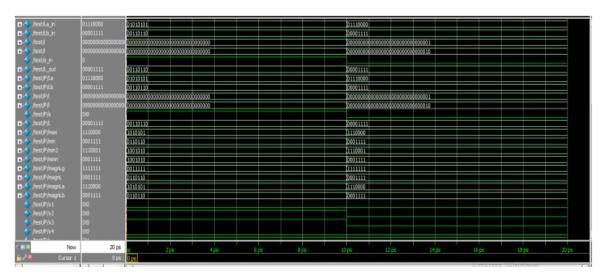


Figure 10 Processing Element Output for N=8 polar code

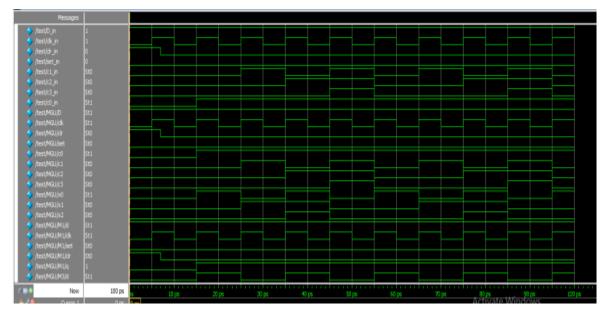


Figure 11 The Matrix Generation Unit for N=8

The main advantages of polar coding scheme are its reduced error and decreased hardware complexity gives an added advantage.

With the discovery of channel polarization, the whole lot of researches began in the field of polar codes. They proved to be the very first capacity achieving codes for binary input symmetric memory-less channels(BMS). They belong to the category of block codes and their reduced complexity[7] make them a potential competent for the existing error correction codes. Being a recently developed error correction code, polar codes have grown out be highly promising in terms of the complexity involved. A low complexity encoding and decoding of O(NlogN) is its most

attractive feature. The concept of channel polarization is highly attractive due to its reliability and simplicity. The future of polar codes is under rigorous research. The proposed 5G technology is all set to replace the current turbo codes with the polar codes due to its tremendous decrease in complexity with a better performance. From the BER vs SNR plot the performance was analyzed. The implementation of individual components of SCD proved enough the reduction in complexity and the ease of processing. Thus, polar codes prove themselves to be the most promising future of error correction codes.

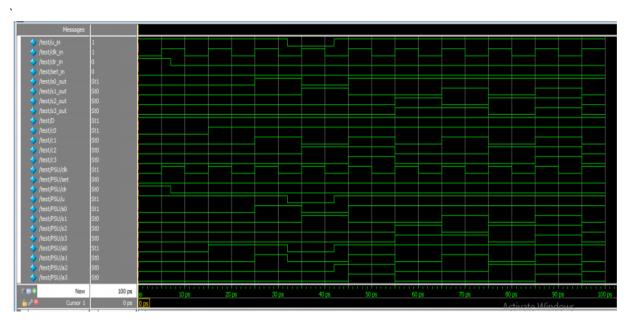


Figure 12 PSU output for N=8 polar codes

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