# CAD For VLSI (CS6230) Final Project

Project Title: P2. Pipelined double precision(fp64) floating point adder Author: HARIHARAN P (EE20B042) AND JAWHAR S (EE20B049) Date: 10 Dec 2023

# Test Cases used Binary value = (-1) Sign bit \* 2 (Exponent – 1023) \* 1.Mantissa

# Positive + positive

1)

# Negative + negative

2)

## **Positive + Negative**

#### **Negative + Positive**

#### -X + +X

# +Infinity + X

# -Infinity + X

#### NAN + X

## +Infinity + -Infinity