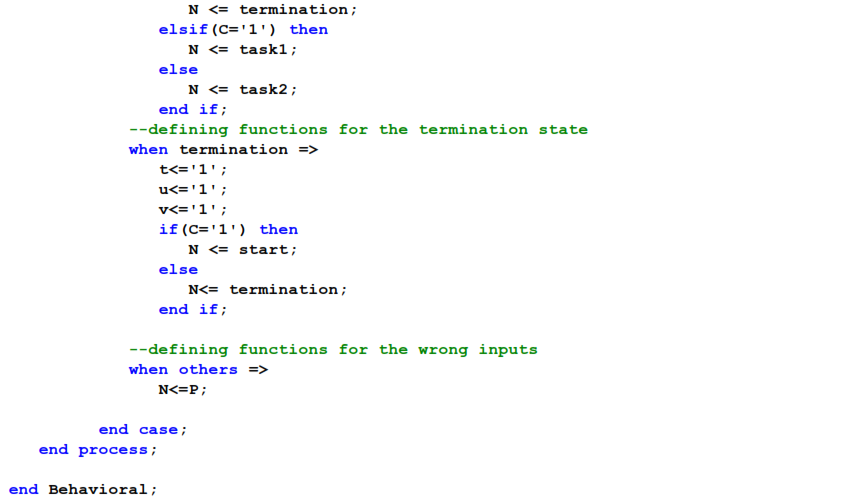
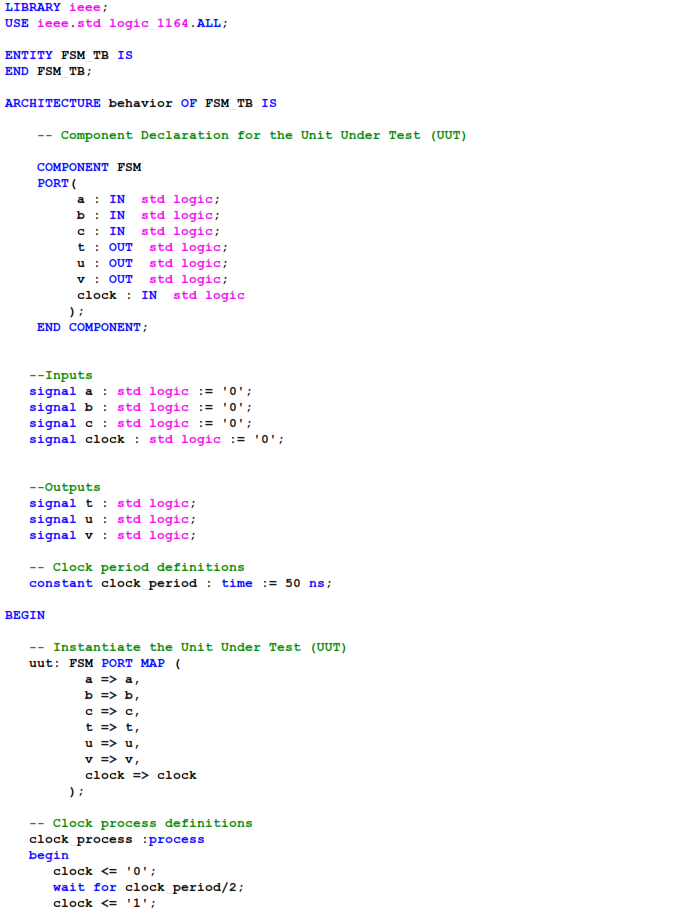
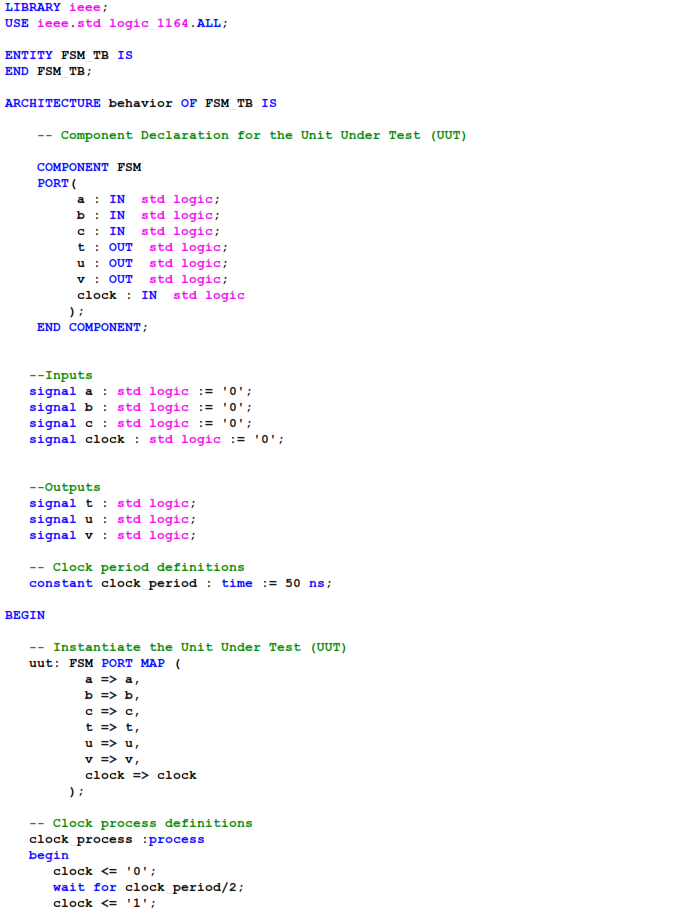
# VHDL code

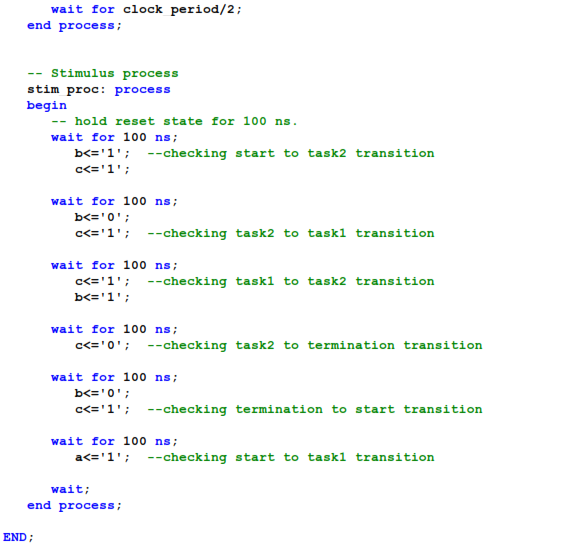
# 



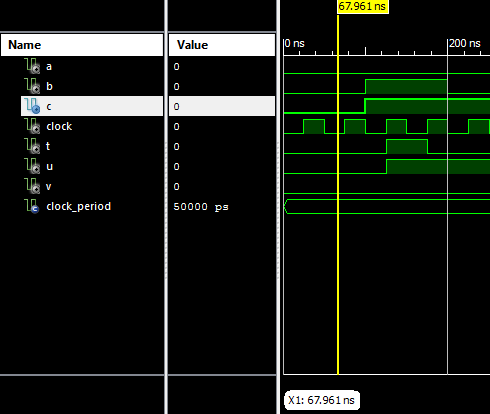
Testbench code





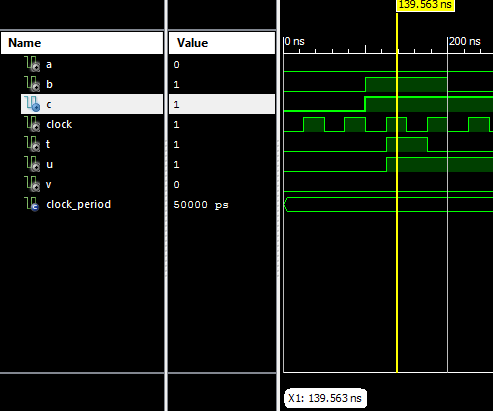


Start to task 2 transition



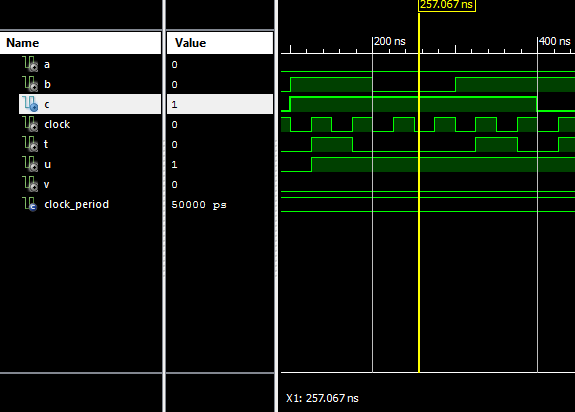
Above figure illustrate the simulation at start state of the design. In here we can see the states are changed from start state to task 2 state when b becomes one (b=1) after the 100ns. As per the above figure and the simulation results we can confirm that the design is performing well at the start to task 2 change.

Task 2 to task 1 transition



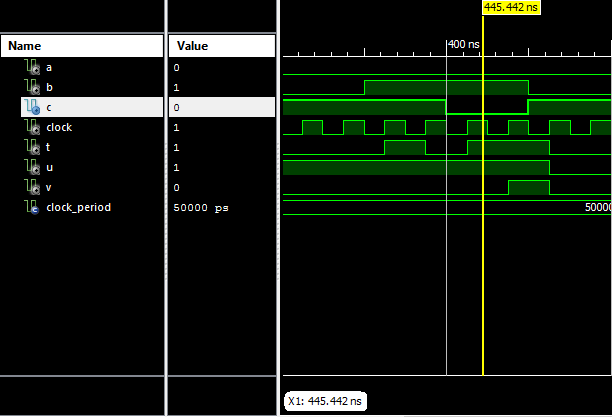
Above figure illustrate the simulation when the output at the task 2 state of the design. In here we can see the states are changed from task 2 to task 1 state because c is one (c=1) at the 175ns. As per the above figure and the simulation results we can confirm that the design is performing well at the task 2 to task 1 change.

Task 1 to task 2 transition



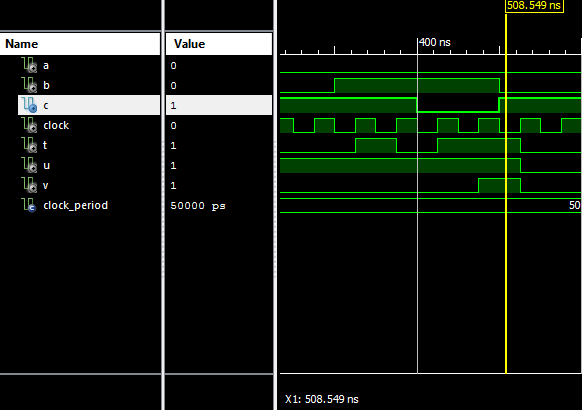
Above figure illustrate the simulation when the output at the task 1 state of the design. In here we can see that the states are changed from task 1 state to task 2 state because b becomes one (b=1) after the 325ns. As per the above figure and the simulation results we can confirm that the design is performing well at the task 1 to task 2 change.

Task 2 to termination transition



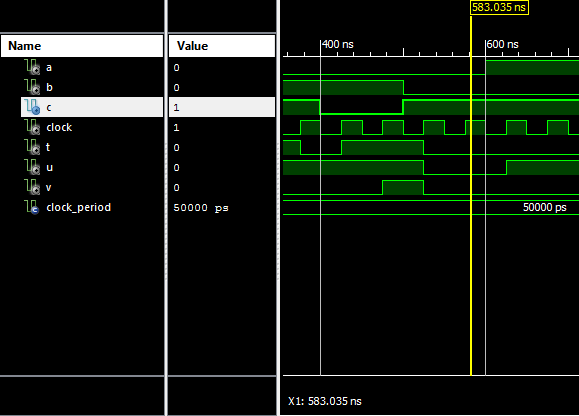
Above figure illustrate the simulation when the output at the task 2 state of the design. In here we can see that the states are changed from task 2 state to termination state because c is Zero (c=0) at the 475ns. Therefore, as per the above figure and the simulation results we can confirm that the design is performing well at the task 2 state to termination state change.

Termination to Start transition



Above figure illustrate the simulation when the output at the termination state of the design. In here we can see that the states are changed from termination state to start state at the 525ns because c is 1 (c=1) at that point. Therefore, as per the above figure and the simulation results we can confirm that the design is performing well at the termination state to start state change.

Start to task 1 transition



Above figure illustrate the simulation when the output at the start state of the design. In here we can see that the states are changed from start state to task 1 state at the 625ns because a is 1 (a=1) at that point. Therefore, as per the above figure and the simulation results we can confirm that the design is performing well at the start state to task 1 state change.