```
1   --------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:   09:49:22 06/25/2021
6   -- Design Name:
7   -- Module Name:   D:/DMU/ADD/Assignment 01/Xilinx file location/USR_4/USR_4_TB.vhd
8   -- Project Name:  USR_4
9   -- Target Device:
10  -- Tool versions:
11  -- Description:
12  --
13  -- VHDL Test Bench Created by ISE for module: USR_4
14  --
15  -- Dependencies:
16  --
17  -- Revision:
18  -- Revision 0.01 - File Created
19  -- Additional Comments:
20  --
21  -- Notes:
22  -- This testbench has been automatically generated using types std_logic and
23  -- std_logic_vector for the ports of the unit under test.  Xilinx recommends
24  -- that these types always be used for the top-level I/O of a design in order
25  -- to guarantee that the testbench will bind correctly to the post-implementation
26  -- simulation model.
27  --------------------------------------------------------------------------------
28  LIBRARY ieee;
29  USE ieee.std_logic_1164.ALL;
30
31  -- Uncomment the following library declaration if using
32  -- arithmetic functions with Signed or Unsigned values
33  --USE ieee.numeric_std.ALL;
34
35  ENTITY USR_4_TB IS
36  END USR_4_TB;
37
38  ARCHITECTURE behavior OF USR_4_TB IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT USR_4
43      PORT(
44           SIR : IN  std_logic;
45           SIL : IN  std_logic;
46           CLK : IN  std_logic;
47           RST : IN  std_logic;
48           D : IN  std_logic_vector(3 downto 0);
49           S : IN  std_logic_vector(1 downto 0);
50           Q : OUT  std_logic_vector(3 downto 0)
51          );
52      END COMPONENT;
53
54
55     --Inputs
56     signal SIR : std_logic := '0';
57     signal SIL : std_logic := '0';
```

```
58      signal CLK : std_logic := '0';
59      signal RST : std_logic := '0';
60      signal D : std_logic_vector(3 downto 0) := (others => '0');
61      signal S : std_logic_vector(1 downto 0) := (others => '0');
62
63      --Outputs
64      signal Q : std_logic_vector(3 downto 0);
65
66      -- Clock period definitions
67      constant CLK_period : time := 10 ns;
68
69   BEGIN
70
71      -- Instantiate the Unit Under Test (UUT)
72      uut: USR_4 PORT MAP (
73             SIR => SIR,
74             SIL => SIL,
75             CLK => CLK,
76             RST => RST,
77             D => D,
78             S => S,
79             Q => Q
80           );
81
82      -- Clock process definitions
83      CLK_process :process
84      begin
85         CLK <= '0';
86         wait for CLK_period/2;
87         CLK <= '1';
88         wait for CLK_period/2;
89      end process;
90
91
92      -- Stimulus process
93      stim_proc: process
94      begin
95
96         --RESET
97         RST<='0';
98         wait for 100 ns;-- HOLD AT SAME STATE FOR 100 NS.
99
100        --HOLD
101        RST<='1';
102        wait for 100 ns;
103        D<="1101";
104        S<="00";
105        wait for 100 ns;-- HOLD SELECTION AT SAME STATE FOR 100 NS.
106
107        --PARALLEL LOADING
108        S<="11";
109        wait for 100 ns;-- HOLD SELECTION AT SAME STATE FOR 100 NS.
110
111        --SHIFT LEFT
112        S<="10";
113        SIL<= '1';
114        wait for 100 ns;-- HOLD SELECTION AT SAME STATE FOR 100 NS.
```

```
115
116         --SHIFT RIGHT
117         S<="01";
118         SIR<= '0';
119
120         wait for 100 ns;-- HOLD SELECTION AT SAME STATE FOR 100 NS.
121
122         wait;
123       end process;
124
125   END;
126
```