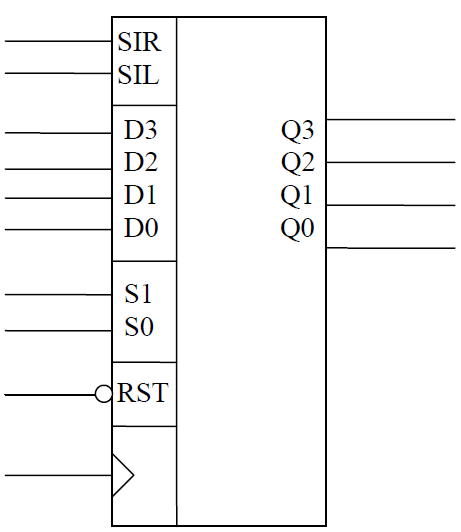
**Assignment 1 Coursework Specification**

|  |  |  |
| --- | --- | --- |
| Module Name: | Advanced Digital Design | |
| Module Code: | ENGD3801 | |
| Title of the Assignment: | Assignment 1 | |
| This coursework item is: | | Summative |
| This coursework will be marked anonymously: | | Yes |
| The module learning outcomes that are assessed by this coursework are:   1. “Knowledge and specialist analytic development techniques in the areas of VLSI design, ASM design and implementation, and VHDL design.” 2. “Development of generic and transferable skills in advanced digital system design methodologies using industry standard design tools.” | | |
| This coursework is: | | Individual |
| This coursework constitutes 16% to the overall module mark. | | |
| Date Set: | by DMU | |
| Date & Time Due: | by Sunday, 7th July 2021 | |
| **When completed you are required to submit the following:**   1. **Submit an electronic copy of your assignment to TURNITIN via Blackboard by the advertised deadline.**   **IMPORTANT: Partial submissions are not acceptable. Failure to submit the electronic copy to Turnitin amounts to a non-submission.** | | |
| **Your marked coursework and feedback will be available to you on:**  If for any reason this is not forthcoming by the due date your module leader will let you know why and when it can be expected | | 25-07-2021 |
| **Late submission of coursework policy:**  Late submissions will be processed in accordance with current University regulations which state:  *“The time period during which a student may submit a piece of work late without authorisation and have the work capped at 40% [50% at PG level] if passed is* ***14 calendar days****. Work submitted unauthorised more than 14 calendar days after the original submission date will receive a mark of 0%. These regulations apply to a student’s first attempt at coursework. Work submitted late without authorisation which constitutes reassessment of a previously failed piece of coursework will always receive a mark of 0%.”* | | |
| **Academic Offences and Bad Academic Practices:**  These include plagiarism, cheating, collusion, copying work and reuse of your own work, poor referencing or the passing off of somebody else's ideas as your own. If you are in any doubt about what constitutes an academic offence or bad academic practice you must check with your tutor. Further information and details of how DSU can support you, if needed, is available at:  <https://www.dmu.ac.uk/current-students/student-support/exams-deferrals-regulations-policies/student-regulations-and-policies/academic-offences.aspx>  and  <https://www.dmu.ac.uk/current-students/student-support/exams-deferrals-regulations-policies/student-regulations-and-policies/bad-academic-practice.aspx> | | |
| Module tutor name: | Mr. Rohan Dharmarathne | |

**Assignment 1**

*Design in VHDL a* ***4-bit universal shift register*** *as presented below:*



SIR – Serial Input Right

SIL – Serial Input Left

D3…,D0 – Parallel Data Inputs

Q3…,Q0 – Data Outputs

RST – Asynchronous Reset Input

S1, S0 – Operation Select Inputs

*The operation of the universal register is described by the following truth table:*

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Action |
| 0 | 0 | Hold |
| 0 | 1 | Shift Left |
| 1 | 0 | Shift Right |
| 1 | 1 | Parallel Load |

**What you should submit**

You should submit a formal report explaining your design and your results. For general guidance on writing (technical) reports please refer to the following link:

[*https://www.theiet.org/media/5182/technical-report-writing.pdf*](https://www.theiet.org/media/5182/technical-report-writing.pdf)

Specifically, your report should contain at least:

1. an introduction including the design brief,
2. a background section,
3. a section explaining how you’ve solved the design task given to you and if applicable why you’ve selected a particular solution out of several possible,
4. the complete listing of the code you’ve written, **bearing in mind good programming and design practice**,
5. the results of the simulations carried out (i.e. suitable, legible, and detailed simulation waveforms)
6. accompanied by detailed comments and explanations, and
7. conclusions (and possible further improvements if applicable). Avoid including simulation waveforms with a black background.

***For full marking details please consult the associated Grading Rubric****.*

Grading Rubric

|  |  |  |
| --- | --- | --- |
| Marks Breakdown | Possible Marks | Your Marks |
| Introduction /Design Brief | /4 |  |
| Background | /6 |  |
| VHDL code for the shift register & design efficiency | /15 |  |
| Comments on the code | /10 |  |
| Detailed simulation results outlining the operation of the shift register | /25 |  |
| Suitable comments for the above simulation waveforms | /25 |  |
| Conclusions | /10 |  |
| Overall layout & presentation | /5 |  |
| TOTAL MARK | /100 |  |