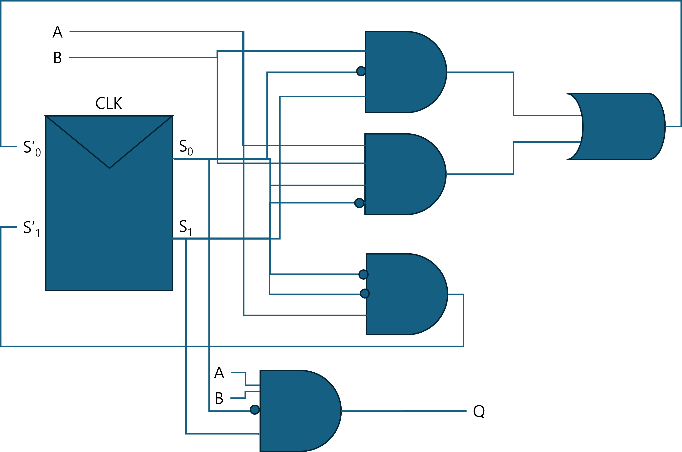
|  |  |  |  |
| --- | --- | --- | --- |
| **Logic Circuit Design Homework #03** | | | |
| Due date | May 10th, 2024 | Instructor | Yoo, Younghwan |
| Student ID | 202355517 | Name | 권민규 |

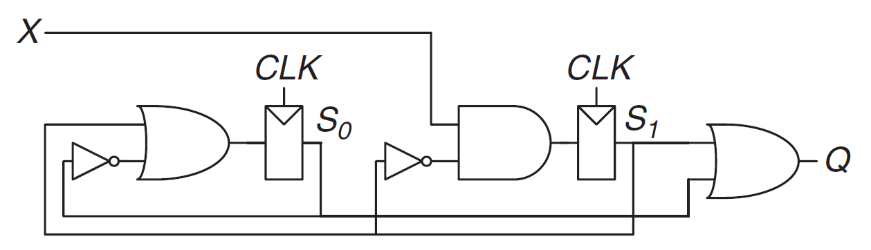
1. Using binary state encodings, complete a state transition table and output table for the following FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.



|  |  |  |
| --- | --- | --- |
| BiNary State encoding |  |  |
| S0 | 0 | 0 |
| S1 | 0 | 1 |
| S2 | 1 | 0 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Current State | | Input | | Next State | | Output |
|  |  | A | B |  |  | Q |
| 0 | **0** | 0 |  | **0** | **0** | 0 |
| 0 | **0** | 1 |  | **0** | **1** | 0 |
| 0 | **1** |  | 0 | **0** | **0** | 0 |
| 0 | **1** |  | 1 | **1** | **0** | 0 |
| 1 | **0** | 0 | 0 | **0** | **0** | 0 |
| 1 | **0** | 0 | 1 | **0** | **0** | 0 |
| 1 | **0** | 1 | 0 | **0** | **0** | 0 |
| 1 | **0** | 1 | 1 | **1** | **0** | 1 |



2. Analyze the circuit in the figure. Write a state transition table and an output table; and sketch the FSM for the circuit. The reset state is .

|  |  |  |
| --- | --- | --- |
| BiNary State encoding |  |  |
| S0 | 0 | 0 |
| S1 | 0 | 1 |
| S2 | 1 | 0 |
| S3 | 1 | 1 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Current State | | Input | Next State | | Output |
|  |  | X |  |  | Q |
| 0 | **0** | 0 | **0** | **0** | 0 |
| 0 | **0** | 1 | **1** | **0** | 0 |
| 0 | **1** | 0 | **0** | **0** | 1 |
| 0 | **1** | 1 | **1** | **0** | 1 |
| 1 | **0** | 0 | **0** | **1** | 1 |
| 1 | **0** | 1 | **0** | **1** | 1 |
| 1 | **1** | 0 | **0** | **0** | 1 |
| 1 | **1** | 1 | **0** | **0** | 1 |

