

زمانبندی حافظه ها





مشخصات غیر زمانی ۸۰۸۶

8086

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-1.0V to +7V
Power Dissipation.....	2.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS (8086: TA = 0°C to 70°C, VCC = 5V ±10%)

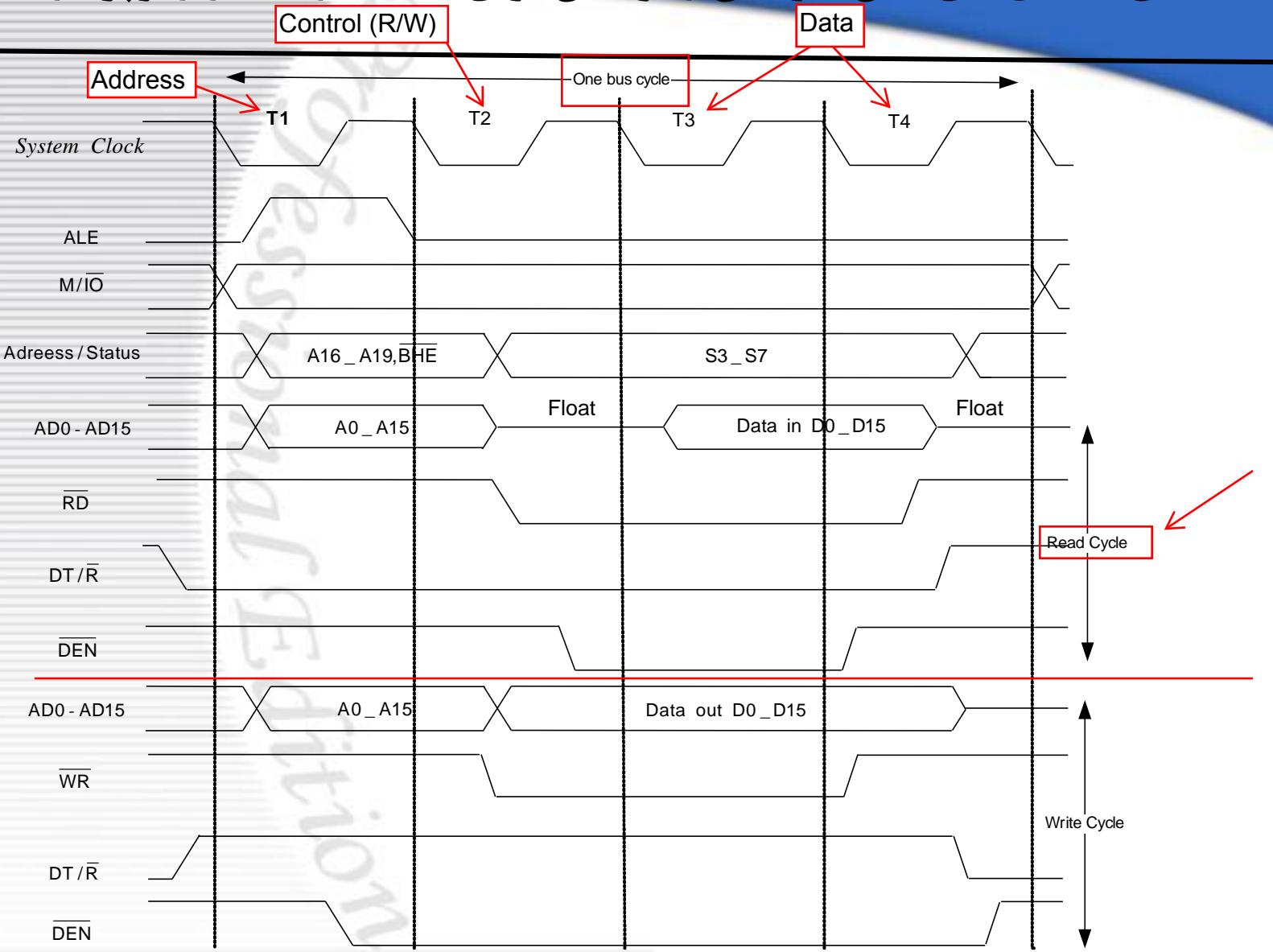
(8086-1: TA = 0°C to 70°C, VCC = 5V ±5%)
(8086-2: TA = 0°C to 70°C, VCC = 5V ±5%)

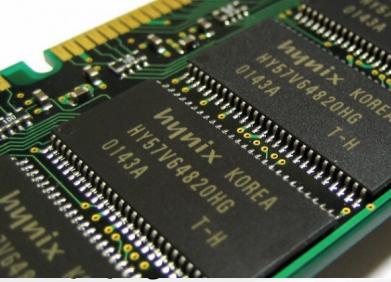
Symbol	Parameter	Min	Max	Units	Test Conditions
V _{IL}	Input Low Voltage	-0.5	+0.8	V	(Note 1)
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.5	V	(Notes 1, 2)
V _{OL}	Output Low Voltage		0.45	V	I _{OL} = 2.5 mA
V _{OH}	Output High Voltage	2.4		V	I _{OH} = - 400 μA
I _{CC}	Power Supply Current: 8086 8086-1 8086-2		340 360 350	mA	T _A = 25°C
I _{LI}	Input Leakage Current		± 10	μA	0V ≤ V _{IN} ≤ V _{CC} (Note 3)
I _{LO}	Output Leakage Current		± 10	μA	0.45V ≤ V _{OUT} ≤ V _{CC}
V _{CL}	Clock Input Low Voltage	-0.5	+0.6	V	
V _{CH}	Clock Input High Voltage	3.9	V _{CC} + 1.0	V	
C _{IN}	Capacitance of Input Buffer (All input except AD ₀ -AD ₁₅ , RQ/GT)		15	pF	f _c = 1 MHz
C _{IO}	Capacitance of I/O Buffer (AD ₀ -AD ₁₅ , RQ/GT)		15	pF	f _c = 1 MHz

NOTES:

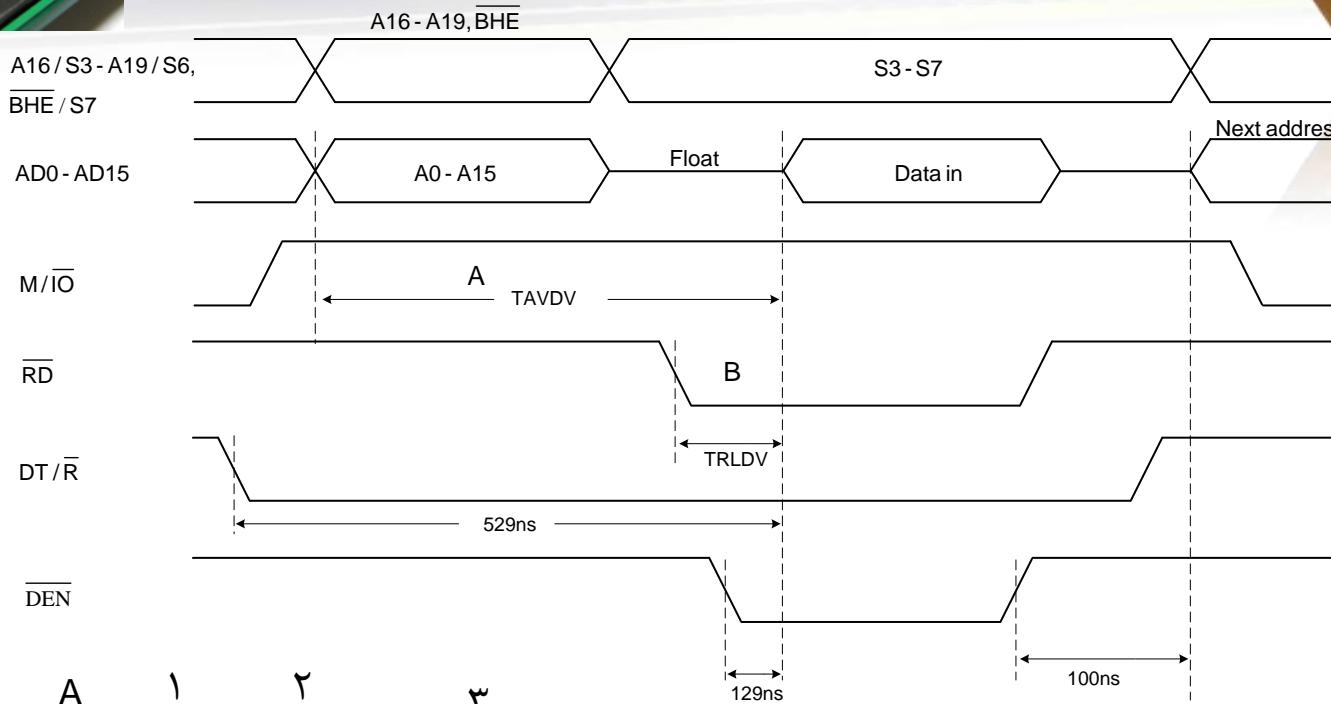
1. V_{IL} tested with MN/MX Pin = 0V, V_{IH} tested with MN/MX Pin = 5V. MN/MX Pin is a Strap Pin.
2. Not applicable to RQ/GT0 and RQ/GT1 (Pins 30 and 31).
3. HOLD and HLDA I_{LI} min = 30 μA, max = 500 μA.

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زمان‌بندی حافظه در سیکل خواندن (مد مینیمم)



$$TAVDV = 3 \times TCLCL - TCLAV_{max} - TDVCL_{min} = 3 \times 200\text{ns} - 110\text{ns} - 30\text{ns} = 460\text{ns} \text{ (8086)}$$

$$TRLDV = 2 \times TCLCL - TCLRL_{max} - TDVCL_{min} = 2 \times 200\text{ns} - 165\text{ns} - 30\text{ns} = 205\text{ns} \text{ (8086)}$$

B 1 4 3

TAVDV: Address Access Time

TCLCL: Clock cycle periode

TCLAV: Address Valid Delay

TDVCL: Data Setup Time

TRLDV: Read Access Time

TCLRL:RD Active Delay



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A.C. CHARACTERISTICS (8086: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$)

(8086-1: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

(8086-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	8086		8086-1		8086-2		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	500	100	500	125	500	ns	
TCLCH	CLK Low Time	118		53		68		ns	
TCHCL	CLK High Time	69		39		44		ns	
TCH1CH2	CLK Rise Time			10		10		ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time			10		10		ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		5		20		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TR1VCL	RDY Setup Time into 8284A (See Notes 1, 2)	35		35		35		ns	
TCLR1X	RDY Hold Time into 8284A (See Notes 1, 2)	0		0		0		ns	
TRYHCH	READY Setup Time into 8086	118		53		68		ns	
TCHRYX	READY Hold Time into 8086	30		20		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		-10		-8		ns	
THVCH	HOLD Setup Time	35		20		20		ns	
TINVCH	INTR, NMI, TEST Setup Time (See Note 2)	30		15		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		12	ns	From 2.0V to 0.8V



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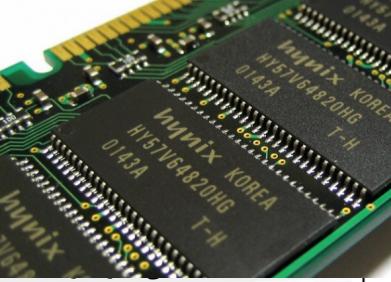
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	8086		8086-1		8086-2		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
TCLAV	Address Valid Delay	10	110	10	50	10	60	ns	$*C_L = 20-100 \text{ pF}$ for all 8086 Outputs (In addition to 8086 selfload)
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	10	40	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH-20		TCLCH-10		TCLCH-10		ns	
TCLLH	ALE Active Delay		80		40		50	ns	
TCHLL	ALE Inactive Delay		85		45		55	ns	
TLLAX	Address Hold Time	TCHCL-10		TCHCL-10		TCHCL-10		ns	
TCLDV	Data Valid Delay	10	110	10	50	10	60	ns	
TCHDX	Data Hold Time	10		10		10		ns	
TWHDX	Data Hold Time After WR	TCLCH-30		TCLCH-25		TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	10	50	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	45	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	50	10	70	ns	
TAZRL	Address Float to READ Active	0		0		0		ns	
TCLR _L	RD Active Delay	10	165	10	70	10	100	ns	
TCLR _H	RD Inactive Delay	10	150	10	60	10	80	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		TCLCL-35		TCLCL-40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	60	10	100	ns	
TRLRH	RD Width	2TCLCL-75		2TCLCL-40		2TCLCL-50		ns	
TWLWH	WR Width	2TCLCL-60		2TCLCL-35		2TCLCL-40		ns	
TAVAL	Address Valid to ALE Low	TCLCH-60		TCLCH-35		TCLCH-40		ns	
TOLOH	Output Rise Time		20		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0V to 0.8V

NOTES:

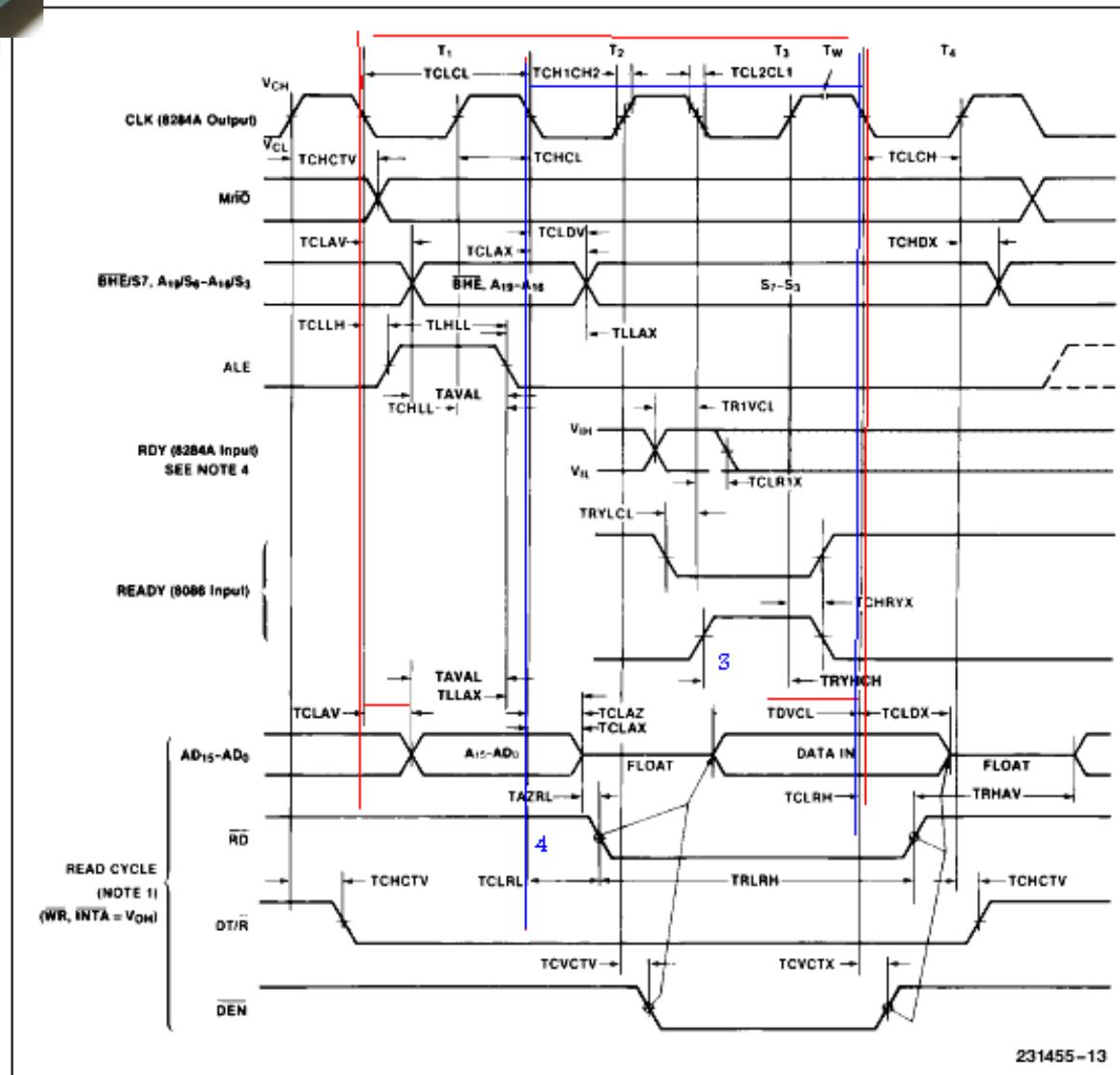
1. Signal at 8284A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3).



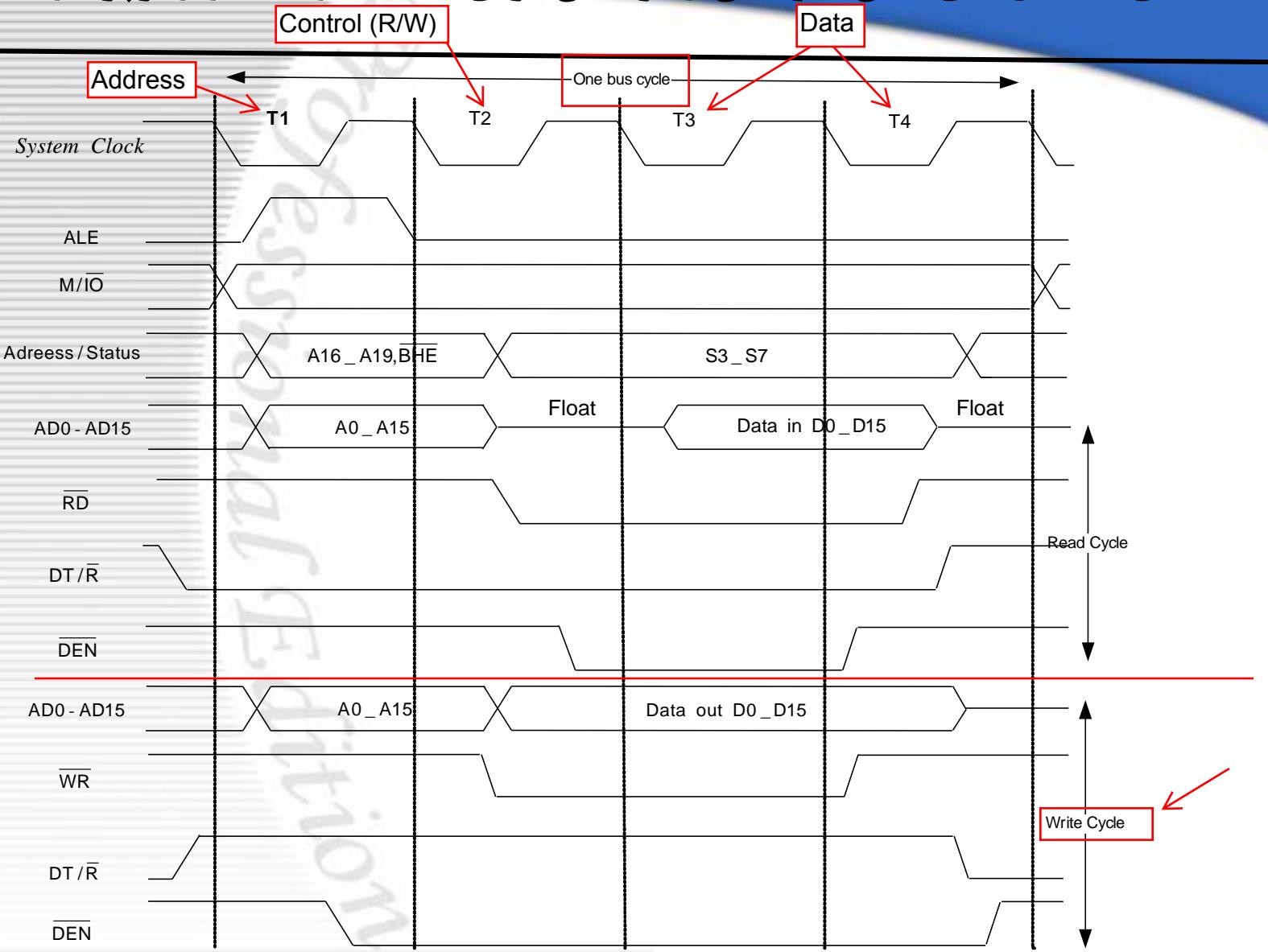
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MINIMUM MODE

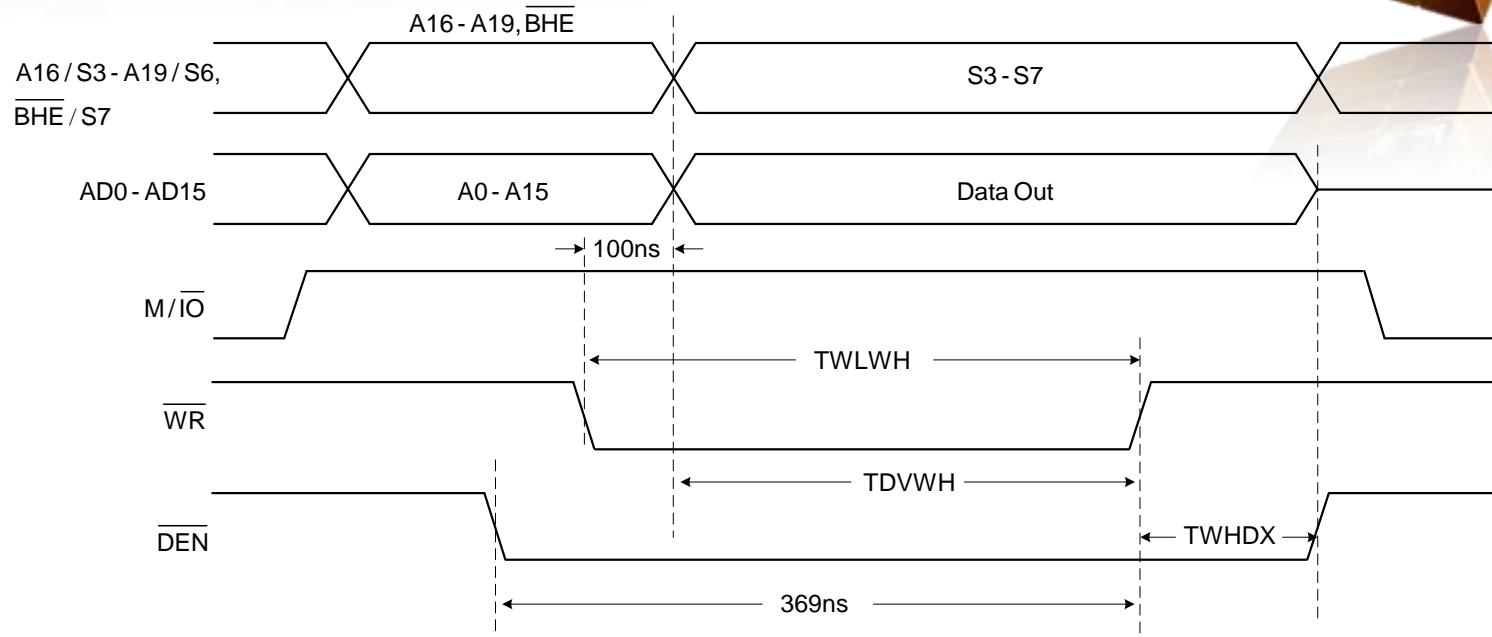


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$$DT / \bar{R} = V_{OH}$$

$$TWLWH = 2TCLCL - 60\text{ns} = 2 \times 200\text{ns} - 60\text{ns} = 340\text{ns} \quad (8086)$$

$$TDVWH = 2TCLCL - TCLDV_{max} + TCVCTX_{min} = 2 \times 200\text{ns} - 110\text{ns} + 10\text{ns} = 300\text{ns} \quad (8086)$$

$$TWHDX = TCLCH - 30\text{ns} = 118\text{ns} - 30\text{ns} = 88\text{ns} \quad (8086)$$

TCVCTX: Control Inactive Delay

TCLCL: Clock cycle periode

TCLDV: Data Valid Delay

TCVCT: Control Active Dealy 1

TCLCH: Clock Low Time

TWHDX: Data Hold Time After Write



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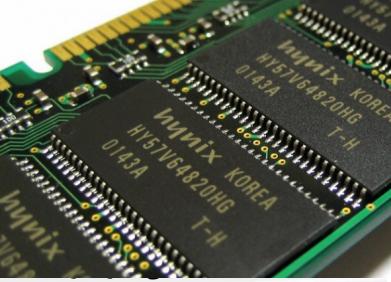
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

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TCVCTV	Control Active Delay 1	10	110	10	50	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	45	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	50	10	70	ns	
TAZRL	Address Float to READ Active	0		0		0		ns	
TCLRL	RD Active Delay	10	165	10	70	10	100	ns	
TCLRH	RD Inactive Delay	10	150	10	60	10	80	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		TCLCL-35		TCLCL-40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	60	10	100	ns	
TRLRH	RD Width	2TCLCL-75		2TCLCL-40		2TCLCL-50		ns	
TWLWH	WR Width	2TCLCL-60		2TCLCL-35		2TCLCL-40		ns	
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MINIMUM MODE (Continued)

