LTspice Basic Simulation Exercises

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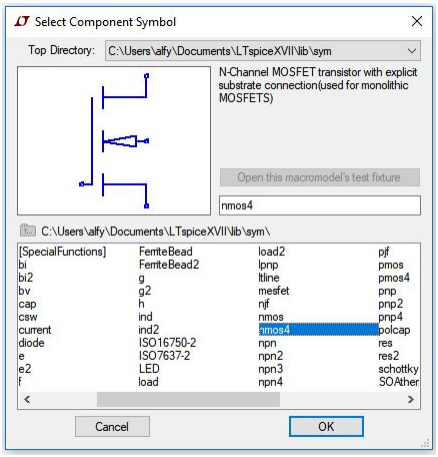
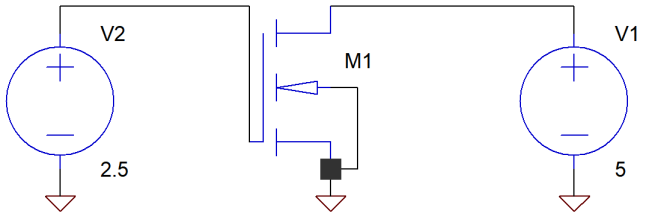
MOSFET Model

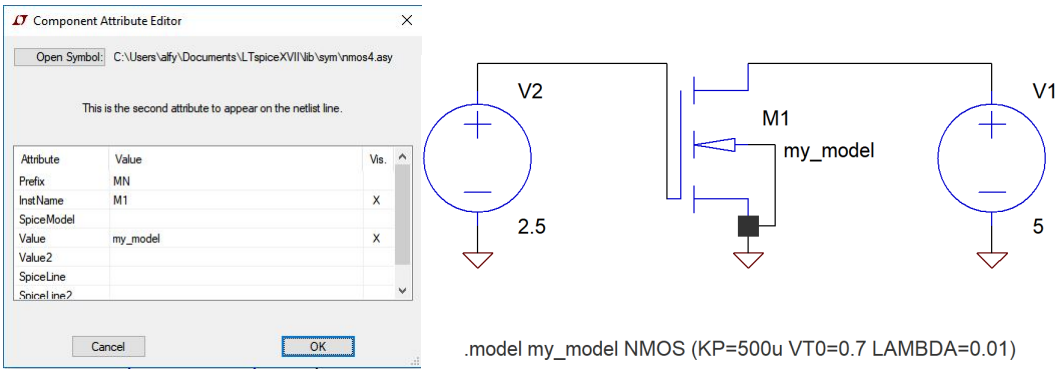
- Use the *Add Component* icon and search for *nmos4* to add an n-channel MOSFET.



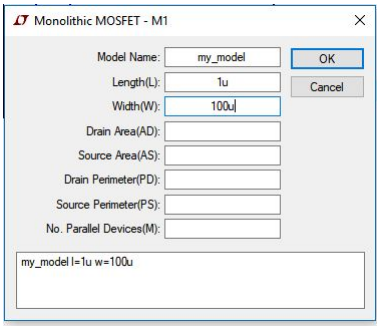
- Draw the following circuit.



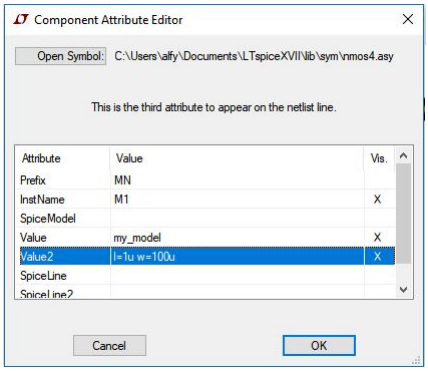
- We will first create a model for a MOSFET and simulate it. Hold *Ctrl* and right-click the MOSFET. Under value, type *my_model*. Now, we define the characteristics of the MOSFET using a spice directive. Add the directive *.model my_model NMOS (KP=500u VT0=0.7 LAMBDA=0.01)*. This defines an NMOS model called *my_model* with $\mu_n C_{ox} = 500\mu A/V^2$, $V_T = 0.7V$ and $\lambda = 0.01$

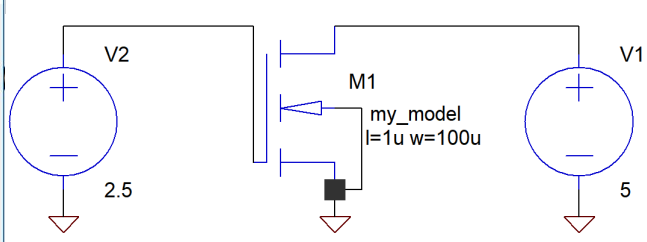


- Right-click the MOSFET and enter its length and width.



- We would like the width and length information to be visible on the schematic. Hold *Ctrl* and right-click the MOSFET. Double click under the column *Visible* to make *Value2* also visible.





.model my_model NMOS (KP=500u VT0=0.7 LAMBDA=0.01)

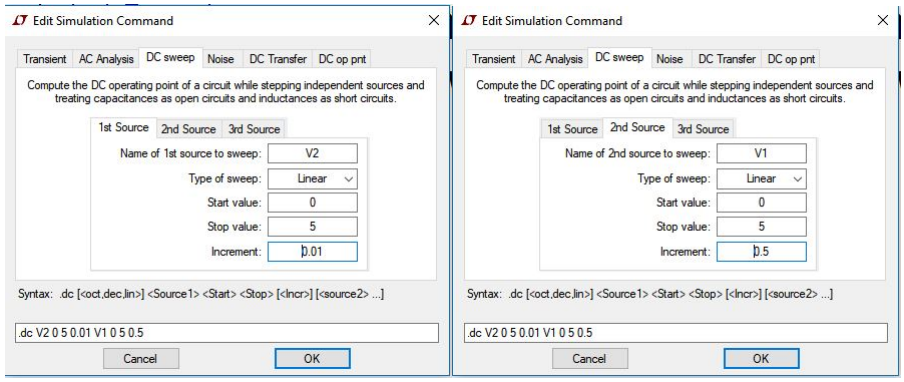
- Now run a DC operating point simulation to see the nodal voltages and device currents.

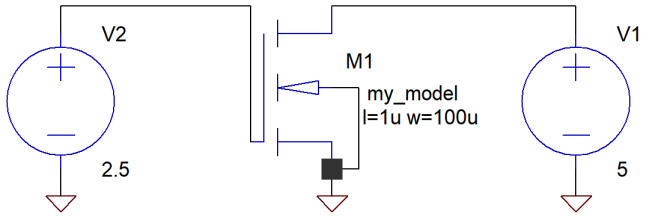
```
--- Operating Point ---

V(n002):        5             voltage
V(n001):        2.5           voltage
Id(M1):         0.08505       device_current
Ig(M1):         0             device_current
Ib(M1):         -5.01e-012    device_current
Is(M1):         -0.08505      device_current
I(V2):          0             device_current
I(V1):          -0.08505      device_current
```

- After running a DC operating point simulation, go to *View* menu and click on *Spice Error Log*. Here, we can find the calculated small signal parameters of all the mosfets in the schematic. Note that since we have created a simple MOSFET model (*my_model*) without specifying any parameters for the intrinsic capacitances, the default value is taken (zero capacitance).

```
                    --- MOSFET Transistors ---
Name:           m1
Model:      my_model
Id:         8.51e-02
Vgs:        2.50e+00
Vds:        5.00e+00
Vbs:        0.00e+00
Vth:        7.00e-01
Vdsat:      1.80e+00
Gm:         9.45e-02
Gds:        8.10e-04
Gmb:        0.00e+00
Cbd:        0.00e+00
Cbs:        0.00e+00
Cgsov:      0.00e+00
Cgdov:      0.00e+00
Cgbov:      0.00e+00
Cgs:        0.00e+00
Cgd:        0.00e+00
Cgb:        0.00e+00
```

- To probe the $I_D - V_{GS}$ characteristics, we need to sweep both the voltage sources. Enter the following details in the simulation command window.

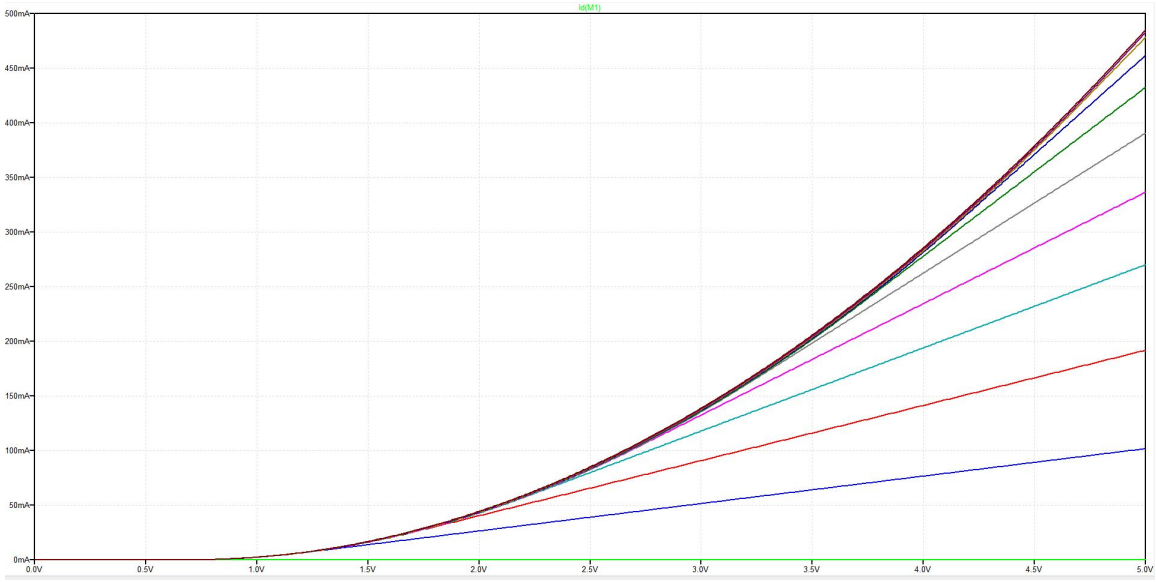




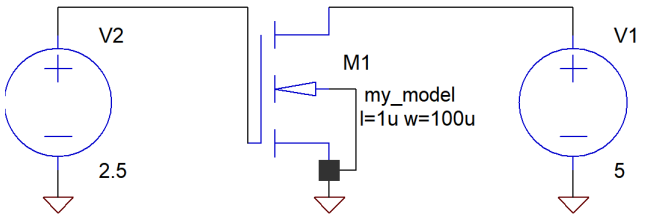
.dc V2 0 5 0.01 V1 0 5 0.5

.model my_model NMOS (KP=500u VT0=0.7 LAMBDA=0.01)

- Probe the current through the drain.

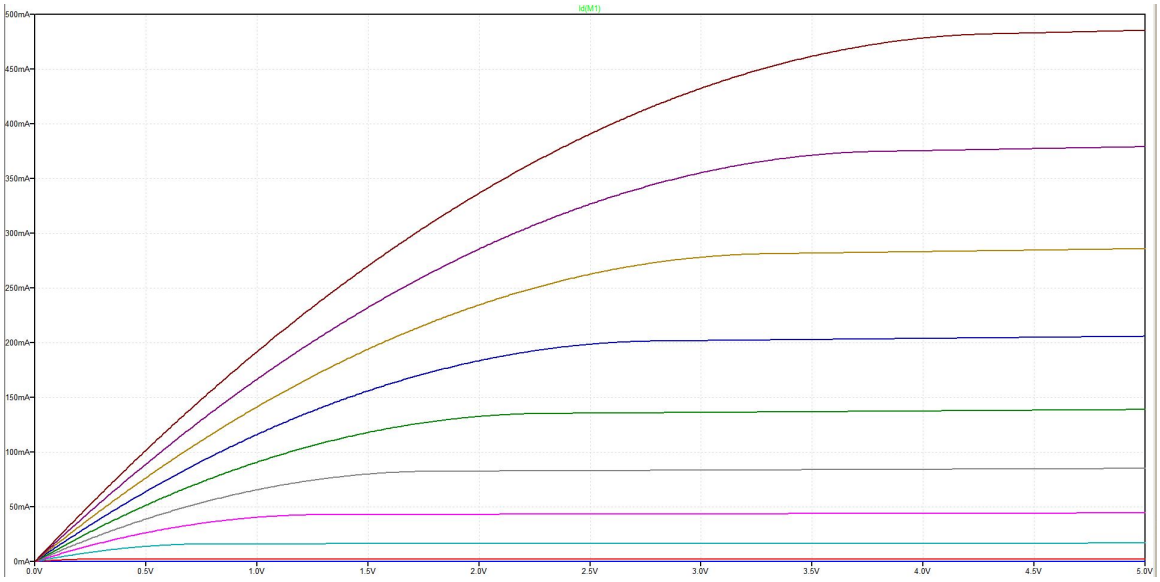


- Interchange the order in which the voltage sources are swept to get the $I_D - V_{DS}$ characteristics. (Notice the change in the *.dc* directive)



.dc V1 0 5 0.01 V2 0 5 0.5

.model my_model NMOS (KP=500u VT0=0.7 LAMBDA=0.01)



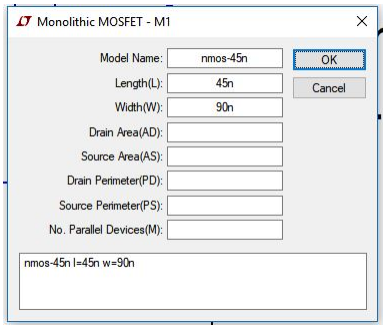
We get the expected curves of a long channel MOSFET.

- Here, we have used a simplified model for the MOSFET. LTspice can also simulate more complex MOSFET models. Let us use the Predictive Technology Model (PTM) which can be downloaded from `http://ptm.asu.edu/`. Navigate to *Latest Models* and download the *45nm PTM HP model.* Save the file as *45nm_HP.txt*
- The name of the default n-channel MOSFET model is *nmos* (We have used *my_model*). The name of the model in the PTM file is also *nmos*. To avoid confusion, use a text editor to open *45nm_HP.txt* and change the name to *nmos-45n*.

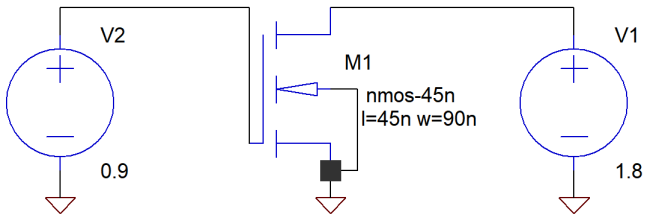
Change `.model nmos nmos level = 54` to `.model nmos-45n nmos level = 54`

Do the same for *pmos* and change it to *pmos-45n*.

- Now to add the model file to this schematic, first save the model file in the same folder as the schematic. Use the spice directive *.include 45nm_HP.txt* to add the file.
- Right-click the MOSFET in the schematic and change the model name to *nmos-45n*. Change the width and length also.



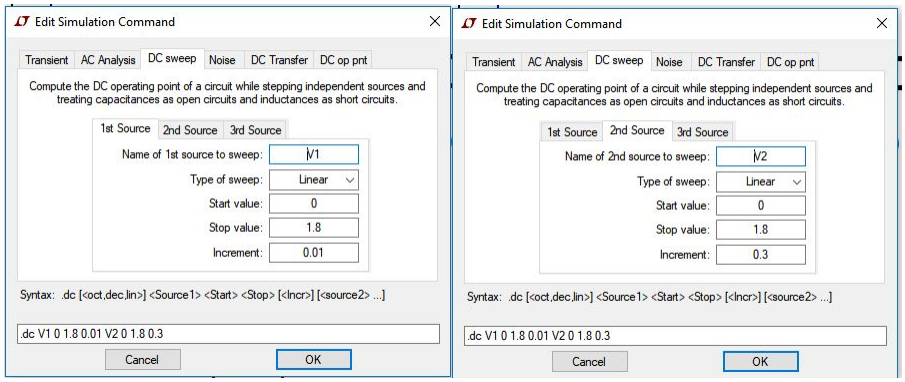
- Change the DC voltages as follows and run a DC operating point simulation. View the small signal parameters.



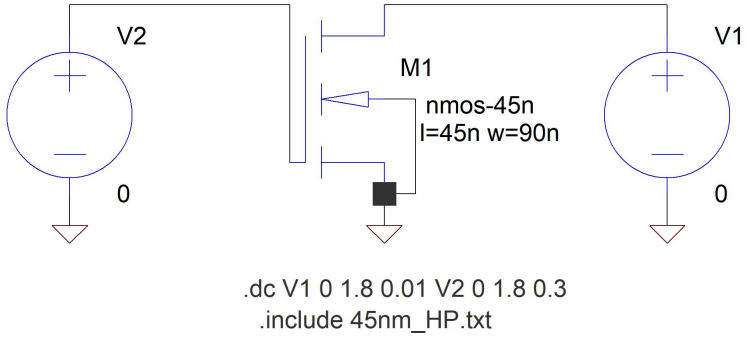
.include 45nm_HP.txt

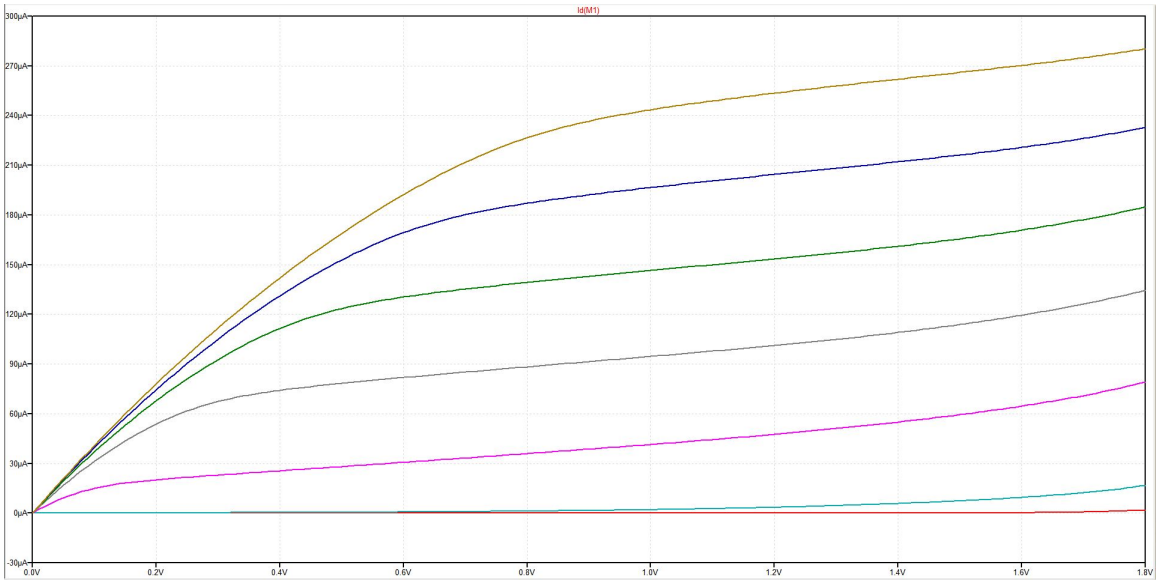
```
--- Operating Point ---

V(n002):        1.8             voltage
V(n001):        0.9             voltage
V(m1#dbody):    8.16609e-007    voltage
V(m1#sbody):    8.16595e-007    voltage
Id(M1):         0.000134572     device_current
Ig(M1):         3.18757e-011    device_current
Ib(M1):         -4.35518e-007   device_current
Is(M1):         -0.000134137    device_current
I(V2):          -3.18758e-011   device_current
I(V1):          -0.000134572    device_current

--- BSIM4 MOSFETS ---

Name:       m1
Model:      nmos-45n
Id:         1.35e-04
Vgs:        9.00e-01
Vds:        1.80e+00
Vbs:        0.00e+00
Vth:        2.37e-01
Vdsat:      3.89e-01
Gm:         1.77e-04
Gds:        8.60e-05
Gmb         4.41e-05
Cbd:        3.20e-17
Cbs:        7.20e-17
```

- Note that this PTM model file also models the intrinsic capacitances of the MOSFET, as well as a lot of other effects.
- Perform a DC sweep to get the $I_D - V_{DS}$ curves.



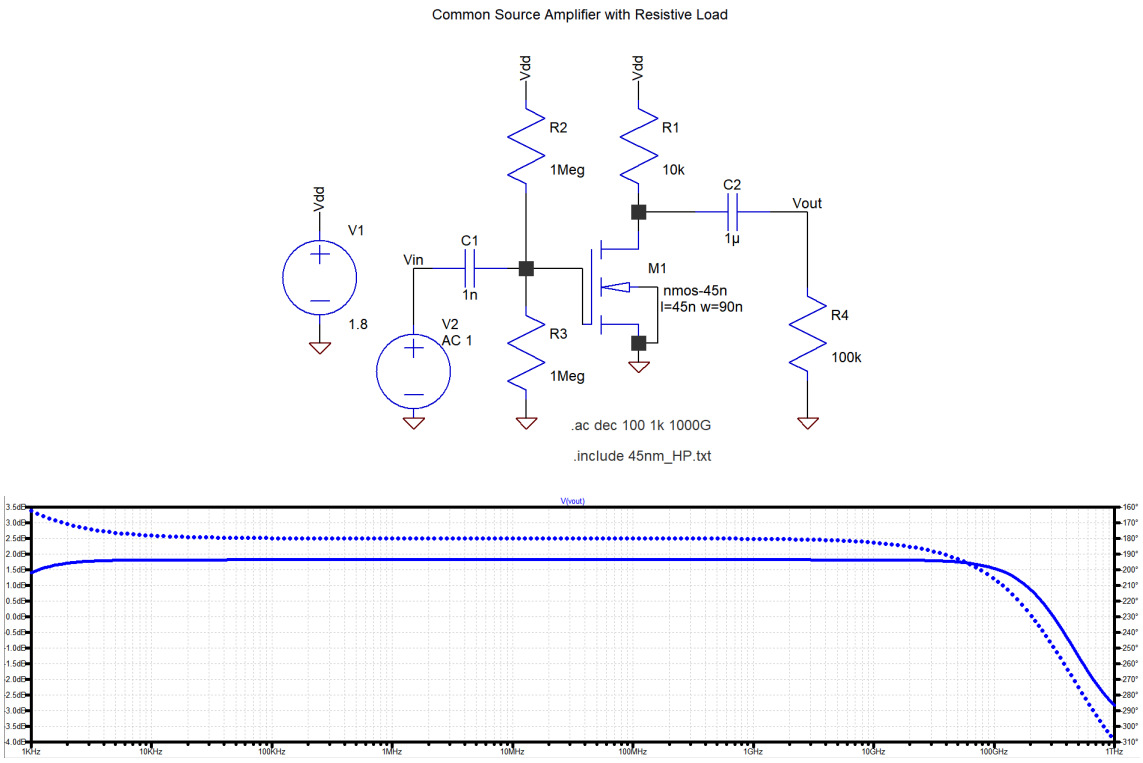
- Run the simulation and probe the drain current





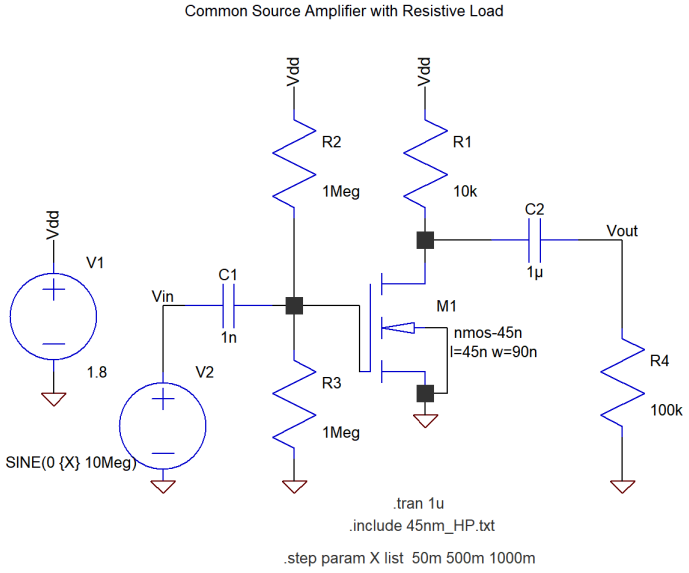
We see the effects of small geometry in the $I_D - V_{DS}$ curves.

- Now, draw the following circuit. This is a common source amplifier with resistive load. Run an AC simulation and probe *Vout*.

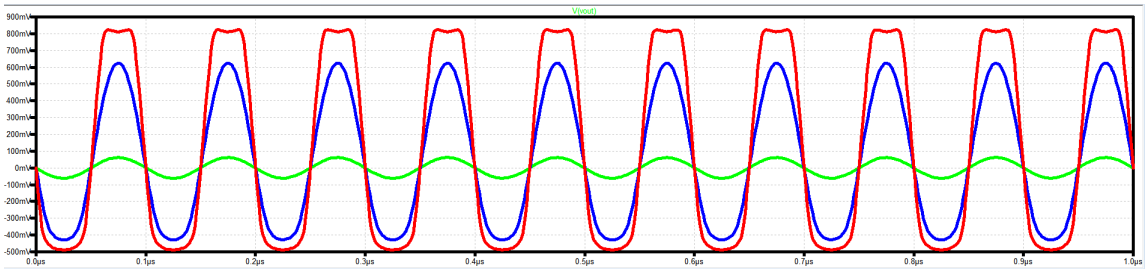


- Note that AC analysis is done by linearizing the circuit about its DC operating point. Hence, the amplitude of the input voltage does not matter. Scaling the input voltage simply linearly scales all other AC voltages/currents. Since the input amplitude is $1V$, probing output voltage directly gives the circuit gain. We note that at very low frequencies ($<10kHz$), the gain drops. This is due to the finite AC coupling capacitors used. Ignoring these frequencies, the DC gain of this circuit is about $1.82dB$. The 3dB bandwidth is about $625GHz$.

- Now, do a transient simulation for different amplitudes of input sinusoidal voltages.

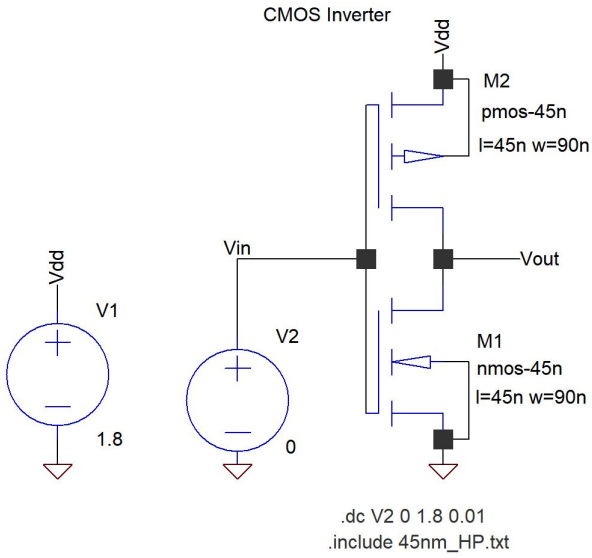


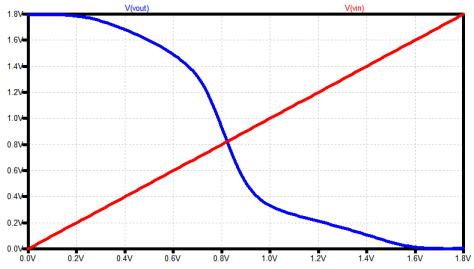
- Probe *Vout*



Notice that the output for an input with amplitude $50mV$ is not distorted a lot. The output amplitude for $50mV$ input is about $61.8mV$. This corresponds to a gain of $1.84dB$, which is close to what we got using AC analysis. However, when the amplitude is $500mV$, the MOSFET goes into triode and we see that the gain is much lesser than the gain in saturation (observe the output at the maximum and minimum value). At $1000mV$, the device also goes into cutoff. Notice that at cutoff, the output is effectively clipped, while at triode there is a relatively soft clipping.

- Now draw the following circuit. This is a cmos inverter. Run a DC sweep simulation to get the Voltage Transfer Characteristics (VTC) of the inverter.





- For the MOSFET sizes chosen, the trip point of the inverter is about $822mV$.