LTspice Basic Simulation Exercises

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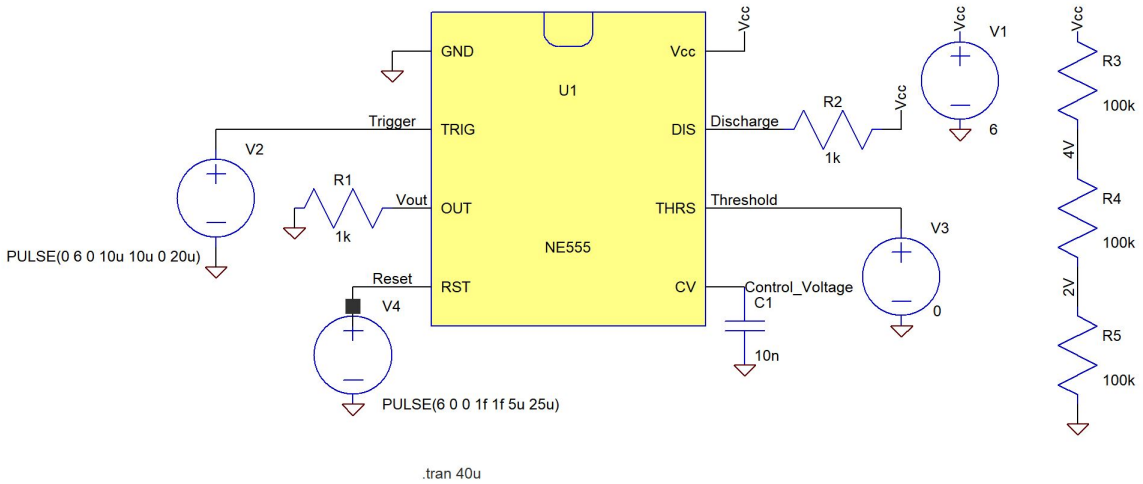
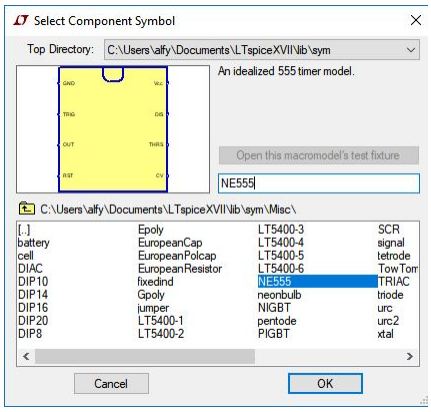
555 Timer

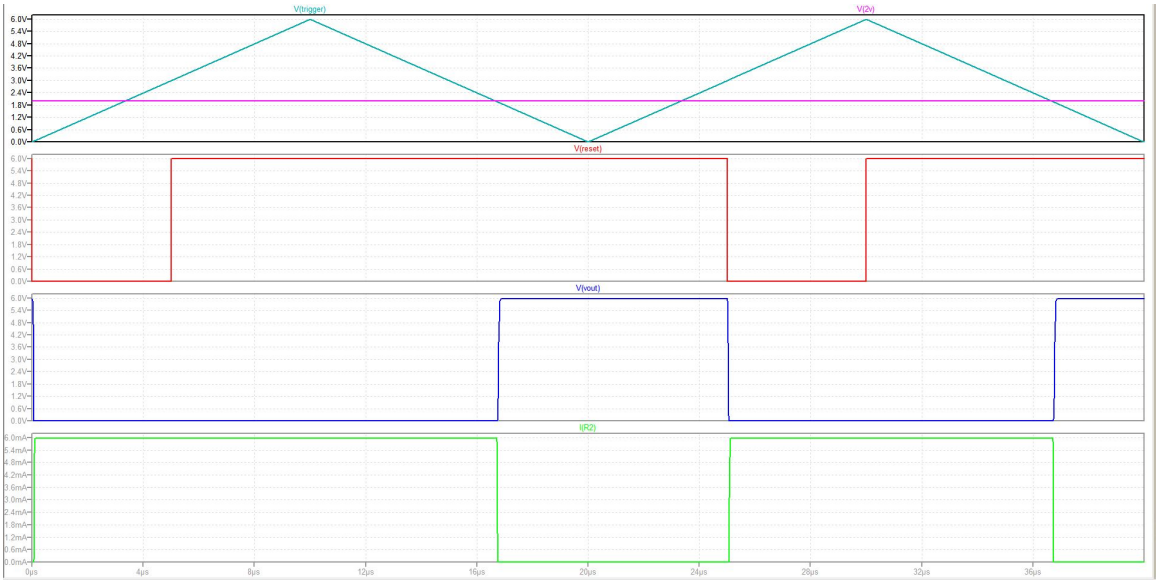
- Create a new schematic and draw the following circuit.



- Use the *Add Component* icon and search for *NE555* to add the 555 Timer.

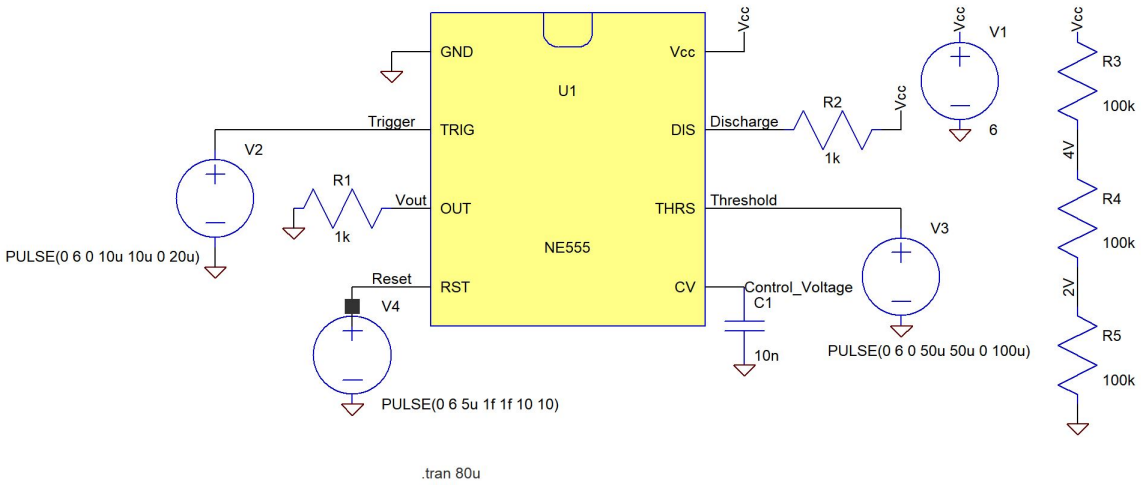


- We make this circuit to illustrate the operation of the 555 Timer. The voltage divider circuit in the right is for convenience during interpretation of the waveforms. Also note that the supply voltage used here is $6V$. Set up the voltage sources as shown in the schematic. Probe *Vout, Trigger, Reset* and current through *R2*. Probe $2V$ along with *Trigger*.

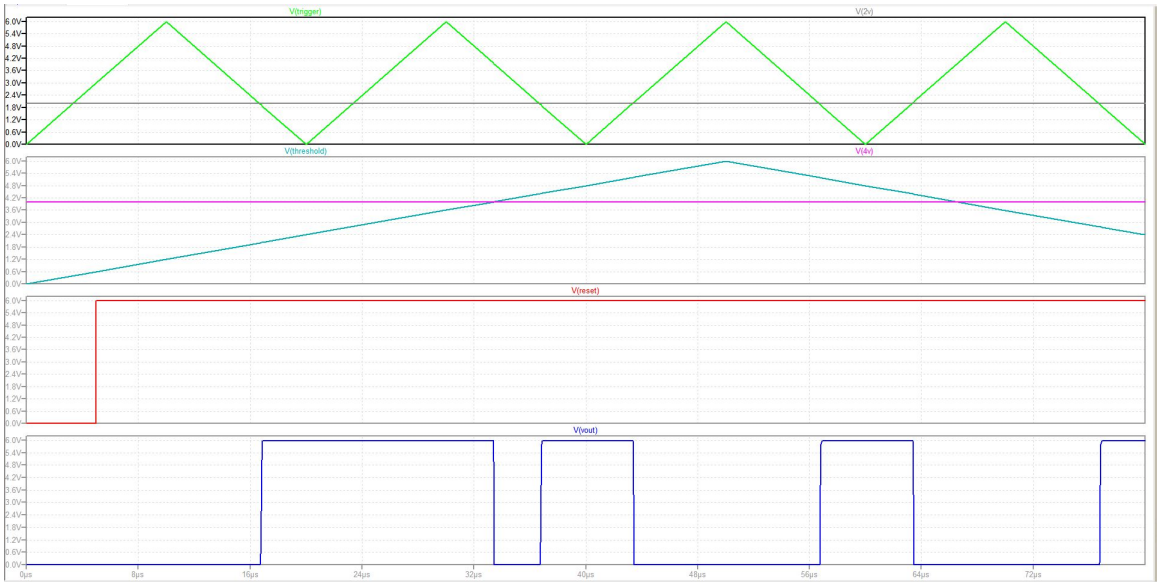


Notice that when *reset* is held low, *Vout* is always low $(0 - 5\mu s)$. When *reset* is held high, *Vout* goes high if the voltage at *trigger* is less than $2V$ (one third of Vcc) $(\sim 16.8\mu s)$. *Vout* continues to stay high until *reset* is pulled low again $(25\mu s)$. Note that when *Vout* is high, even if the voltage at *Trigger* goes above $2V$, *Vout* is still high. $(\sim 23.4\mu s)$. Also note that the *discharge* pin effectively sinks current when *Vout* is low, and is at high impedance when *Vout* is high.

- Now, draw the following circuit.



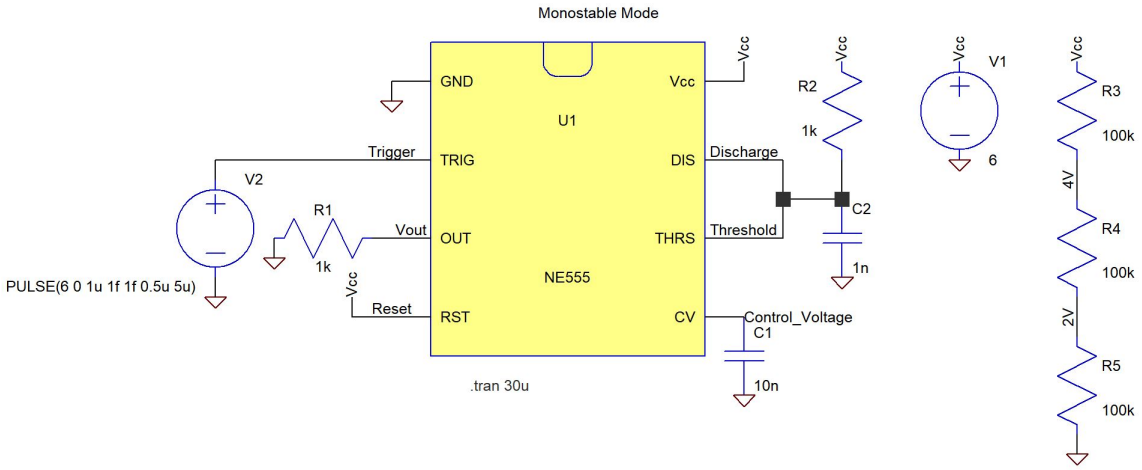
- Probe *Vout, Trigger, Reset* and *Threshold.* Probe $2V$ along with *Trigger* and $4V$ along with *Threshold.*



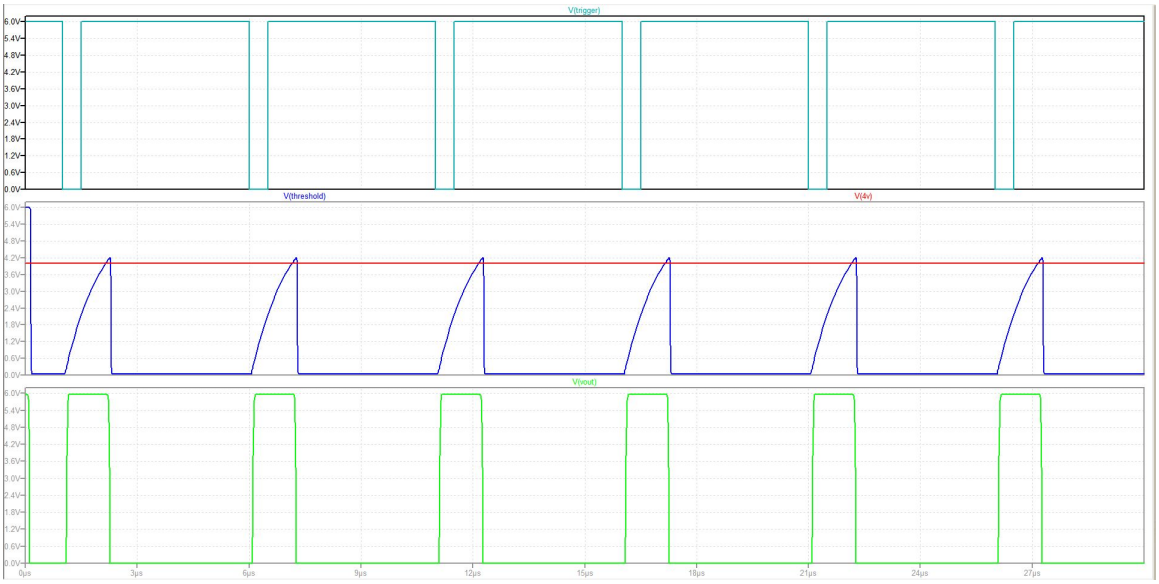
Initially *reset* is held low and *Vout* is low. Once *reset* goes high ($5\mu s$) and the voltage at *trigger* goes below 2V,($\sim 16.8\mu s$) *Vout* goes high. *Vout* continues to be high even after the voltage at *trigger* goes above 2V($\sim 23.4\mu s$). When the voltage at *threshold* goes above $4V$ (two thirds of Vcc), *Vout* goes low($\sim 33.4\mu s$). *Vout* goes high again when the voltage at *trigger* goes below 2V($\sim 36.8\mu s$) even though the voltage at *threshold* is still above $4V$. At $\sim 43.4\mu s$, the voltage at *trigger* goes above $2V$. Here *Vout* goes low as the voltage at *threshold* is already above $4V$.

- So far we have tried to understand the operation of the 555 Timer using a black box approach. Go through a block diagram of the 555 Timer to gain more insight as to how the above graphs were generated. Basically, there is a flip flop which is set by a comparator output of $(\frac{Vcc}{3} - V_{Trigger})$ and reset by a comparator output of $(V_{Threshold} - \frac{2Vcc}{3})$ and an active low external reset pin. Note that the external reset pin overrides the set input of the flip flop which overrides the reset connected to the comparator. The discharge pin is an open collector output. The voltages $\frac{Vcc}{3}$ and $\frac{2Vcc}{3}$ are generated through a voltage divider. This can be manipulated through the *Control_ Voltage* pin. However, we do not use it in these examples. We instead connect it to a capacitor to stabilize the voltage divider.

- Draw the following schematic and run a transient simulation.

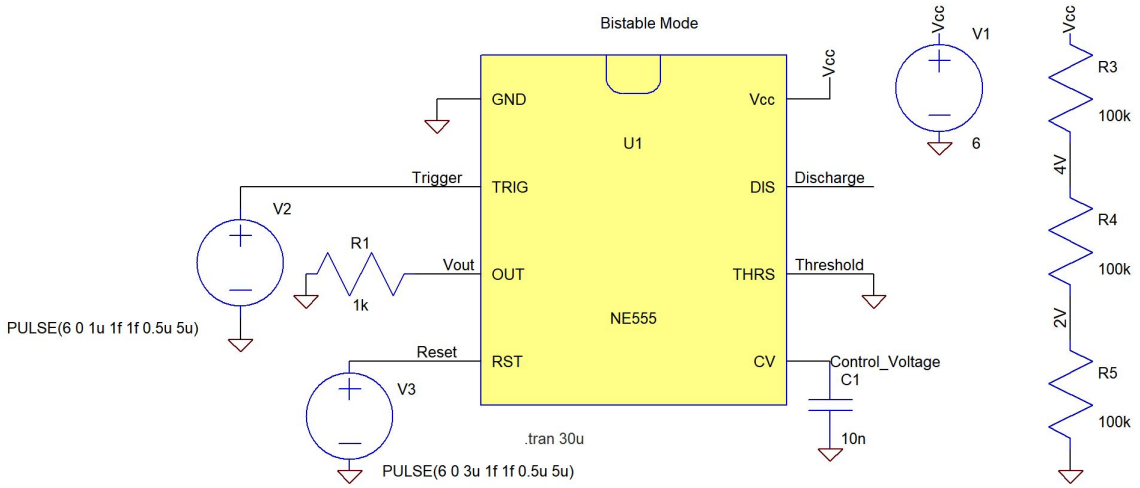


- Probe *Trigger*, *Threshold/Discharge* and *Vout*. Probe $4V$ along with *Threshold/Discharge*.



Initially, *Trigger* is at $6V$ and *Vout* is low. Hence the *discharge* pin forces the voltage at *threshold* to be at $0V$ (it sinks current through the resistor). When a short pulse is given to *trigger*, *Vout* is set (since voltage at *Trigger* will go below $2V$). Now, the *discharge* pin is at high impedance. This will cause the capacitor to get charged and the voltage at *Threshold* to rise. It will eventually rise to $4V$, which will cause *Vout* to become low, and the *discharge* pin will immediately discharge the capacitor and force the voltage at *threshold* to become $0V$. And this repeats when the next pulse is given to *Trigger*.

- Here, the 555 Timer was used in *Monostable Mode* which essentially implies that there is only one stable mode. When *Vout* is made to go high (due to a pulse on *Trigger*), it will eventually become low.
- Draw the following circuit and run a transient simulation.



- Probe *Trigger*, *Reset* and *Vout*.

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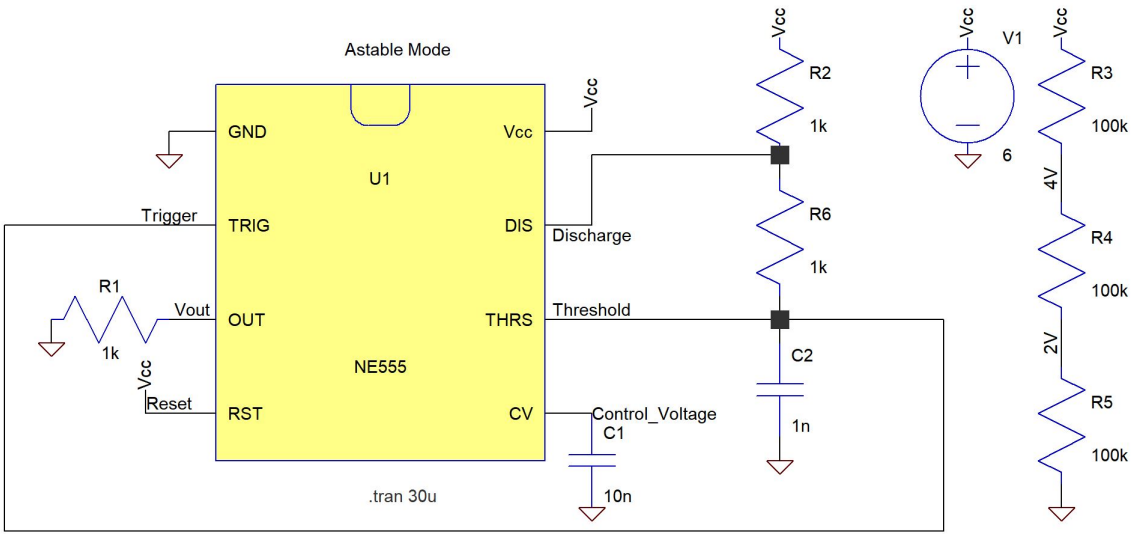
Note that *Threshold* is grounded. Now, when a pulse is given to *Trigger*, *Vout* becomes high. It stays high until a pulse is given to *reset*, which forces *Vout* to become low.

- Here, the 555 Timer was used in *Bistable Mode* which essentially implies that there are two stable modes. When *Vout* is made to go high (due to a pulse on *Trigger*), it will remain high. When *Vout* is made to go low (due to a pulse on *Reset*), it will remain low.
- Draw the following circuit and run a transient simulation.



- Probe *Trigger* / *Threshold*, *Discharge* and *Vout*. Probe $2V$ and $4V$ along with *Trigger* / *Threshold*.

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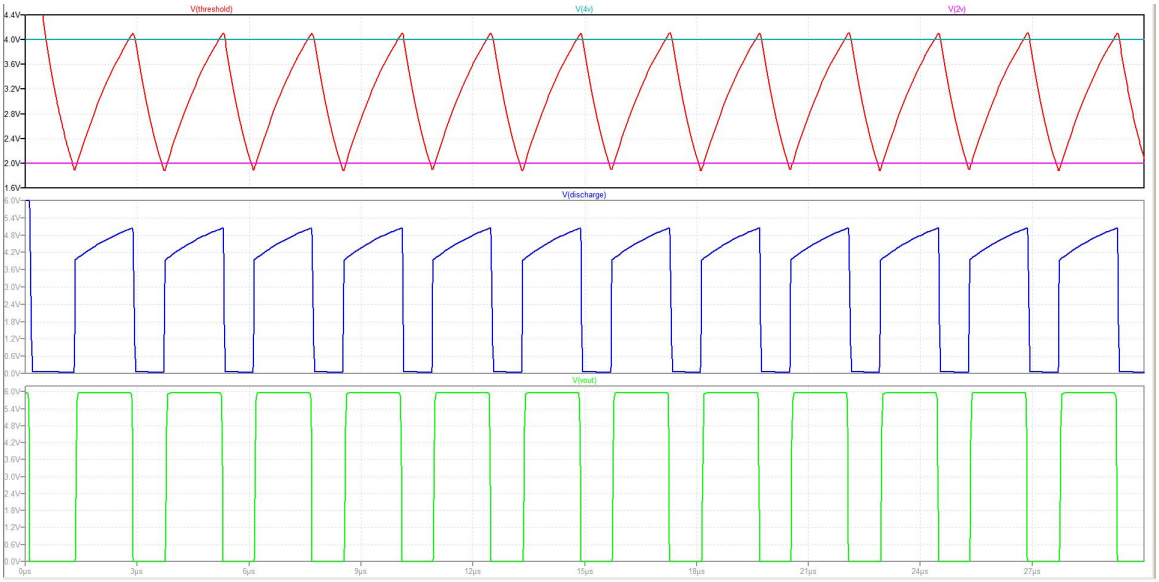

Initially, let us assume that the capacitor was discharged. Now the voltage at *Trigger* and *Threshold* will be $0V$. This will set *Vout* and cause *discharge* to go to high impedance. Now the capacitor will charge through *R2* and *R6*. Eventually, the capacitor voltage will cross $2V$ (nothing happens) and then $4V$. When the capacitor is charged to $4V$, the *threshold* pin will cause *Vout* to go low. This will cause the *discharge* pin to go to ground, discharging the capacitor through *R6*. Eventually, the capacitor voltage will fall to 2V, causing the *trigger* pin to set *Vout*. This will again force the *discharge* pin to high impedance, causing the capacitor to charge through *R2* and *R6*. This cycle continues.

- Here, the 555 Timer was used in *Astable Mode* which essentially implies that there are no stable modes. *Vout* keeps on switching between high and low.