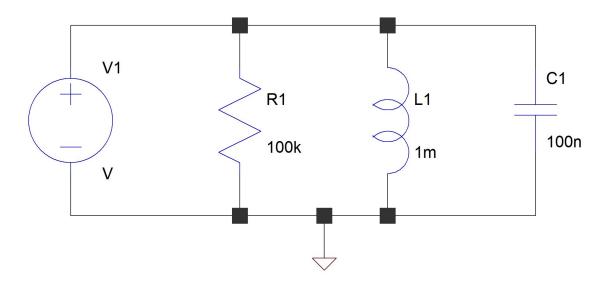
LTspice Basic Simulation Exercises

Alfred Festus Davidson alfy7.github.io

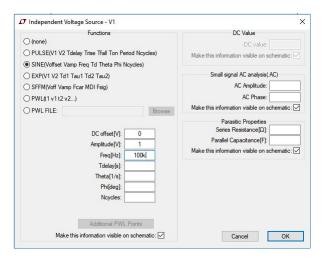
December 1, 2017

RLC Circuits

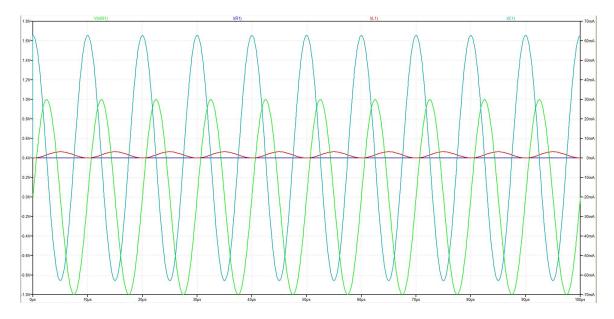
ullet Create a new schematic and draw the following circuit. Inductors can be added either using the shortcut key L or its icon ullet



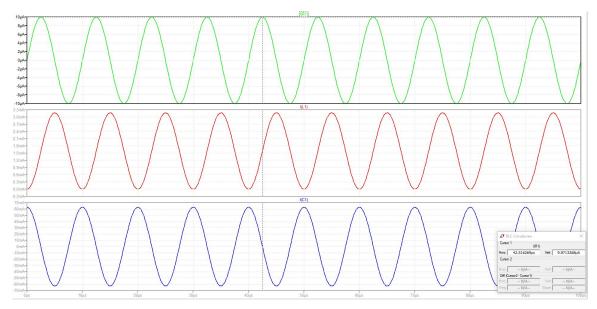
• This is a parallel RLC circuit. One interesting idea that can be captured by this circuit is the phase relation between voltage and current through a resistor, capacitor and inductor. This circuit applies the same voltage to all 3 components. If we apply a sinusoidal voltage, we can see the phase of current through each of the components. To set voltage source V1 as a sinusoidal voltage source, right-click it and enter the following parameters after choosing SINE mode.



• Run a transient simulation for upto $100\mu s$

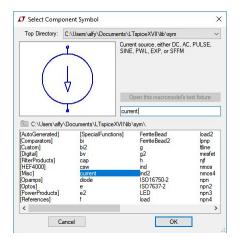


Add plot panes so that the phase relation can be seen clearly

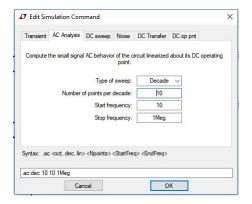


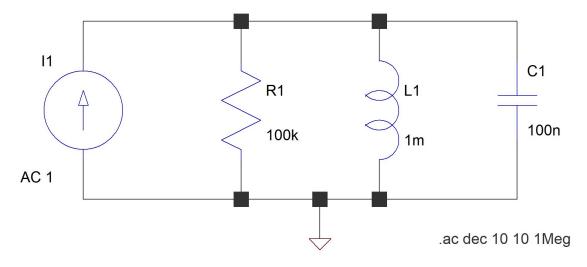
Here, as you can see, when the same voltage is applied across a resistor, inductor and capacitor, the inductor current lags behind the resistor current (peak of the waveform in inductor current appears after corresponding peak in resistor current waveform) while the capacitor current leads the resistor current. (peak of the waveform in capacitor current appears before corresponding peak in resistor current waveform) Further, you can see that the inductor and capacitor currents are completely out of phase. You can also plot the applied voltage in another plot pane to see the relation with the phase of the voltage.

• The parallel RLC circuit can show the phenomena of resonance. At resonance, the impedance (magnitude) offered by the this RLC combination is maximum. Hence, on applying a sinusoidal current through this circuit, we will see that the voltage peaks at resonance. Add a current source using the Add Component icon and searching for current. Rotate the current source appropriately before placing it.

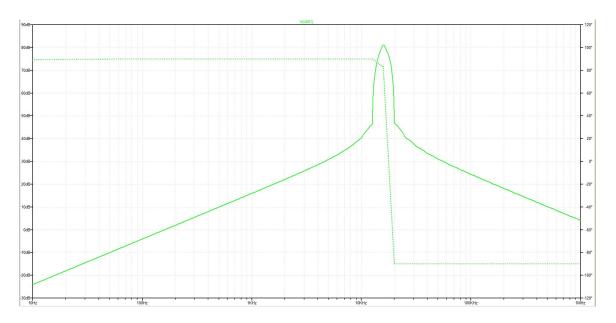


• Run an AC Analysis simulation to get the bode plot.

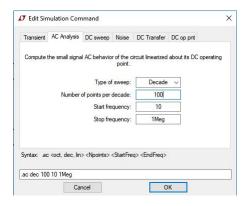


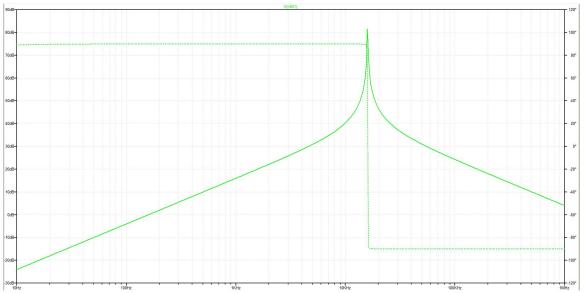


• Probe the voltage at the top node



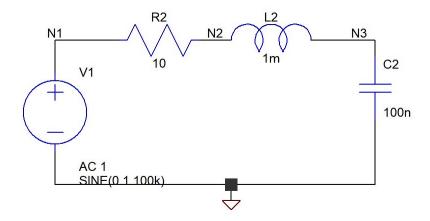
We see a distorted waveform. This is due to the fact that the resolution of the plot displayed does not capture resonance completely, which happens in a very narrow band in this case. Increase the *number of points per decade* to get a more accurate graph



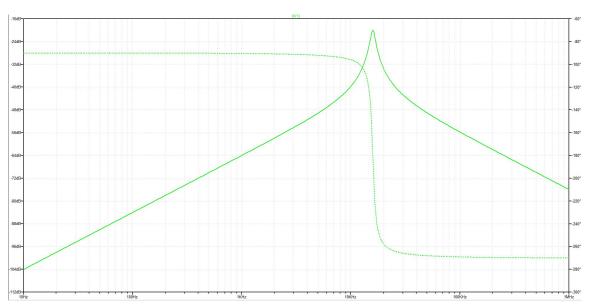


Here we see the characteristic resonance peak and the sudden drop in phase.

• Now draw the following circuit. This is a series RLC circuit which shows minimum impedance (magnitude) at resonance. So we excite this circuit with a voltage source to see the peak in the current drawn by the circuit at resonance. (Note the change in resistor value from the previous circuit)

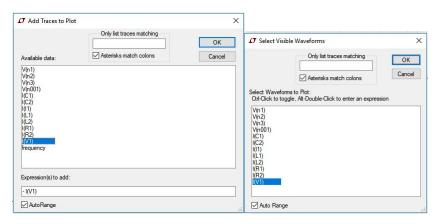


• Run the same AC Analysis simulation (with increased number of points per decade) and probe the current through the voltage source.

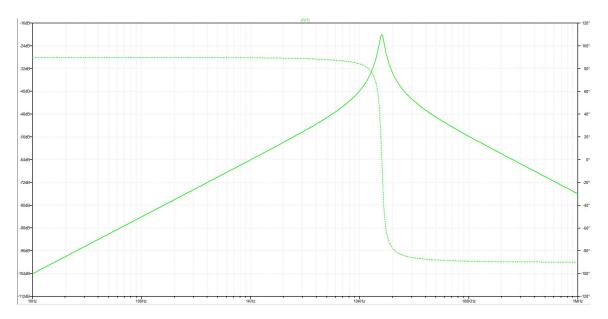


We find that the phase plot is incorrect. This is due to the fact that we have plotted the current entering the voltage source and not the current leaving it (or rather we need the current drawn by the RLC circuit)

• One way to fix this is by first deleting the trace and then in the $Add\ Trace$ dialog box (Right click the plot pane), use the expression editor to type -I(V1). To delete a trace, right click the plot pane, click $View->Visible\ Traces$ and toggle off the traces you do not want to view.

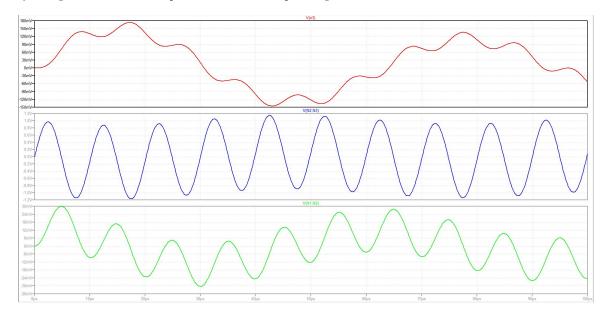


.



Now, the waveform is the expected characteristic graph of a series RLC circuit.

• We can also use this circuit to see the phase relation between the voltages across a resistor, capacitor and inductor when the same current flows through them. Set up the current source to give a sinusoid of amplitude 1mA and frequency 100kHz. Run a transient simulation for upto $100\mu s$. One way to plot the voltage across an element (or voltage between any two nodes) is by clicking on the first node, holding the Ctrl key and then clicking on the next node. Another way to do the same is by using the $Add\ Trace$ expression editor and plotting the difference between the two nodes.

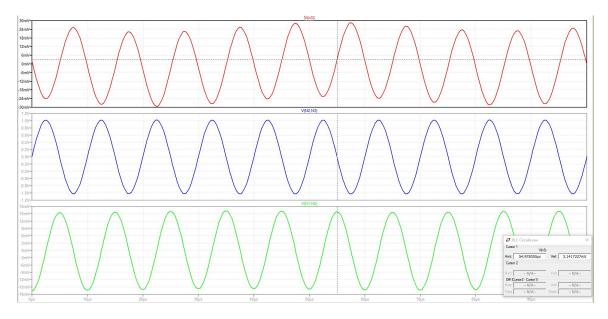


We see that the transient response of the circuit has not died down. Note that we are plotting the actual response of the circuit, which contains both transient and steady state components, but we want to see the sinusoidal steady state response only (because all these phase relations and phasor analysis is only valid for the steady state response)

• We edit the simulation command such that LTspice runs the simulation for a longer time but starts obtaining the waveform only during the end of the simulation. Note that even now LTspice will display the total response, but now the transients will have become insignificant compared to the steady state response.

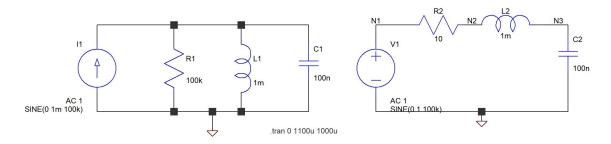
Transient	AC Analysis	DC sweep	Noise	DC Transfer	DC op pnt
	Perf	om a non-lin	ear, time	-domain simulat	ion.
				Stop time:	1100u
		Time	e to start	saving data:	1000u
			Maximu	ım Timestep:	
	Start e	external DC s	upply vo	tages at 0V:]
	Stop sim	nulating if stea	ady state	is detected:	
	Don't reset T	=0 when ste	ady state	is detected:	
		Step the	load cu	rrent source:]
		Skip initial op	erating p	oint solution:	
Syntax: .tra	ın <tprint> <t:< td=""><td>stop> [<tstar< td=""><td>t> [<tma< td=""><td>xstep>]] [<optio< td=""><td>on> [<option>]]</option></td></optio<></td></tma<></td></tstar<></td></t:<></tprint>	stop> [<tstar< td=""><td>t> [<tma< td=""><td>xstep>]] [<optio< td=""><td>on> [<option>]]</option></td></optio<></td></tma<></td></tstar<>	t> [<tma< td=""><td>xstep>]] [<optio< td=""><td>on> [<option>]]</option></td></optio<></td></tma<>	xstep>]] [<optio< td=""><td>on> [<option>]]</option></td></optio<>	on> [<option>]]</option>
ran 0 1100	Ou 1000u				
	C	ncel		0	V

• Now, run the simulation.



Here, as you can see, when the same current is passed through a resistor, inductor and capacitor, the voltage across the inductor leads the voltage across the resistor (peak of the waveform of the voltage across the inductor appears before corresponding peak in the voltage across the resistor) while the voltage across the capacitor lags behind the voltage across the resistor. (peak of the waveform of the voltage across the capacitor appears after corresponding peak in the voltage across the resistor) Further, you can see that the voltage across the inductor and capacitor are completely out of phase. You can also plot the applied current in another plot pane to see the relation with the phase of the current.

• The final schematic is shown below.



• As a side note, the voltage and current sources can be made to generate a wide variety of waveforms including triangle wave, saw-tooth wave and others.