RTL Report

Testbench	Pass (Pass/Failed)
Clock Cycle	4 (ns)
Total Time	2068 (ns)

Synthesis Report

Testbench	Pass (Pass/Failed)
Clock Cycle	4 (ns)
Cell Area	121588.156675(Please report **Total cell area**)
Total Time	2068 (ns)
Area*Time	251444308

APR Report

Testbench	Pass (Pass/Failed)
Clock Cycle	4 (ns)
Cell Area	143182.480 (Please report **Total area of Core)**
Total Time	2324 (ns)
Area*Time	332756083.5

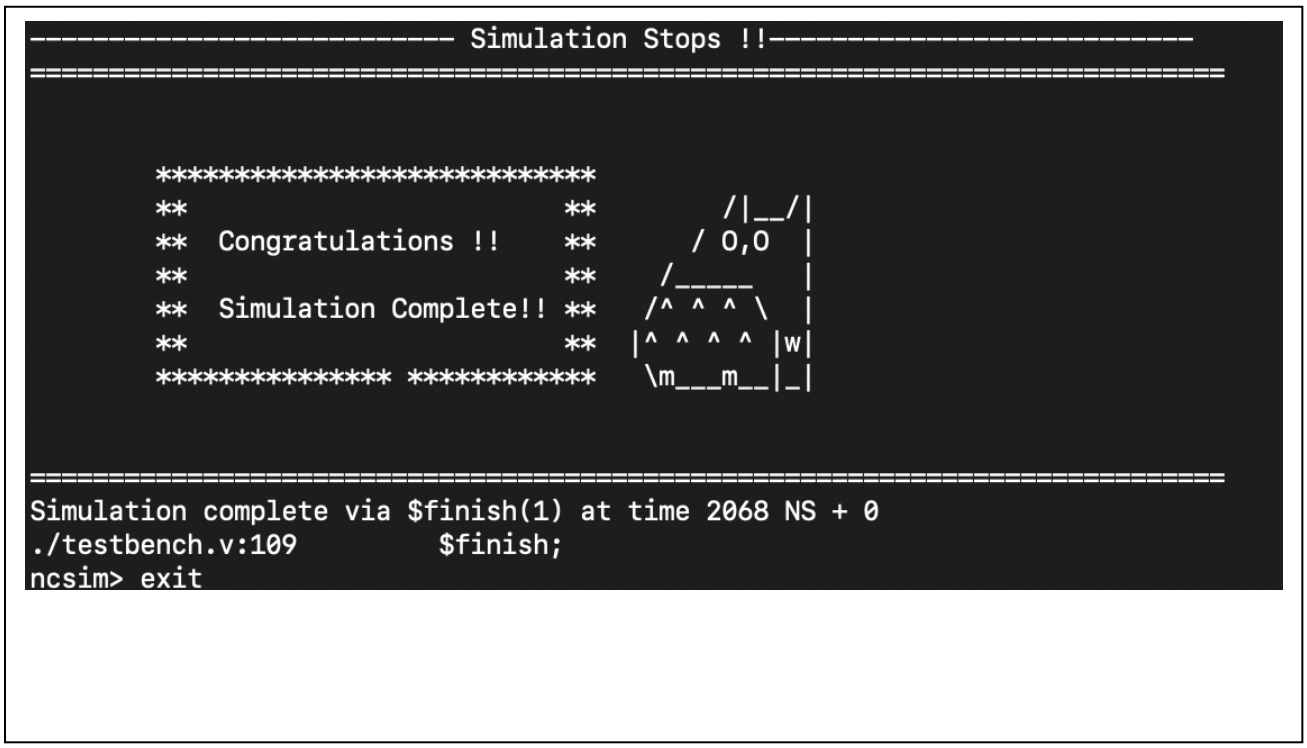
How to report area in Design Vision?

➔ report_area > autoseller_area.txt, find **Total cell area.**

How to report area in Innovus?

➔ File > Report > Summary > choose Text only, file name: **summaryReport.rpt**>OK, find **Total area of Core.**

RTL Simulation Result (截圖)



Synthesis Simulation Result (截圖)

Synthesis Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : SET
Version: N-2017.09-SP2
Date   : Tue May 25 09:56:43 2021
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: cir_reg[9] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: min_reg[3][0][0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  SET                tsmc13_wl10           slow

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              1.00       1.00
  cir_reg[9]/CK (DFFRX4)                   0.00 #     1.00 r
  cir_reg[9]/Q (DFFRX4)                    0.37       1.37 f
  U3294/Y (BUFX20)                         0.10       1.46 f
  U5077/Y (NAND2X1)                        0.10       1.56 r
  U5076/Y (CLKBUFX3)                       0.34       1.90 r
  U4887/Y (XNOR2X1)                        0.30       2.21 f
  U4741/Y (NOR2X1)                         0.19       2.40 r
  U2318/Y (CLKBUFX3)                       0.34       2.73 r
  U3006/Y (INVX3)                          0.24       2.97 f
  U4869/Y (OAI21XL)                        0.49       3.46 r
  U4868/Y (OAI21XL)                        0.19       3.64 f
  U2479/Y (OAI2BB1X2)                      0.31       3.95 r
  U2480/Y (CLKINVX1)                       0.40       4.35 f
  U4647/Y (OAI22XL)                        0.40       4.76 r
  min_reg[3][0][0]/D (DFFRX1)              0.00       4.76 r
  data arrival time                                   4.76

  clock clk (rise edge)                    4.00       4.00
  clock network delay (ideal)              1.00       5.00
  clock uncertainty                       -0.10       4.90
  min_reg[3][0][0]/CK (DFFRX1)             0.00       4.90 r
  library setup time                      -0.14       4.76
  data required time                                  4.76
  -----------------------------------------------------------
  data required time                                  4.76
  data arrival time                                  -4.76
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

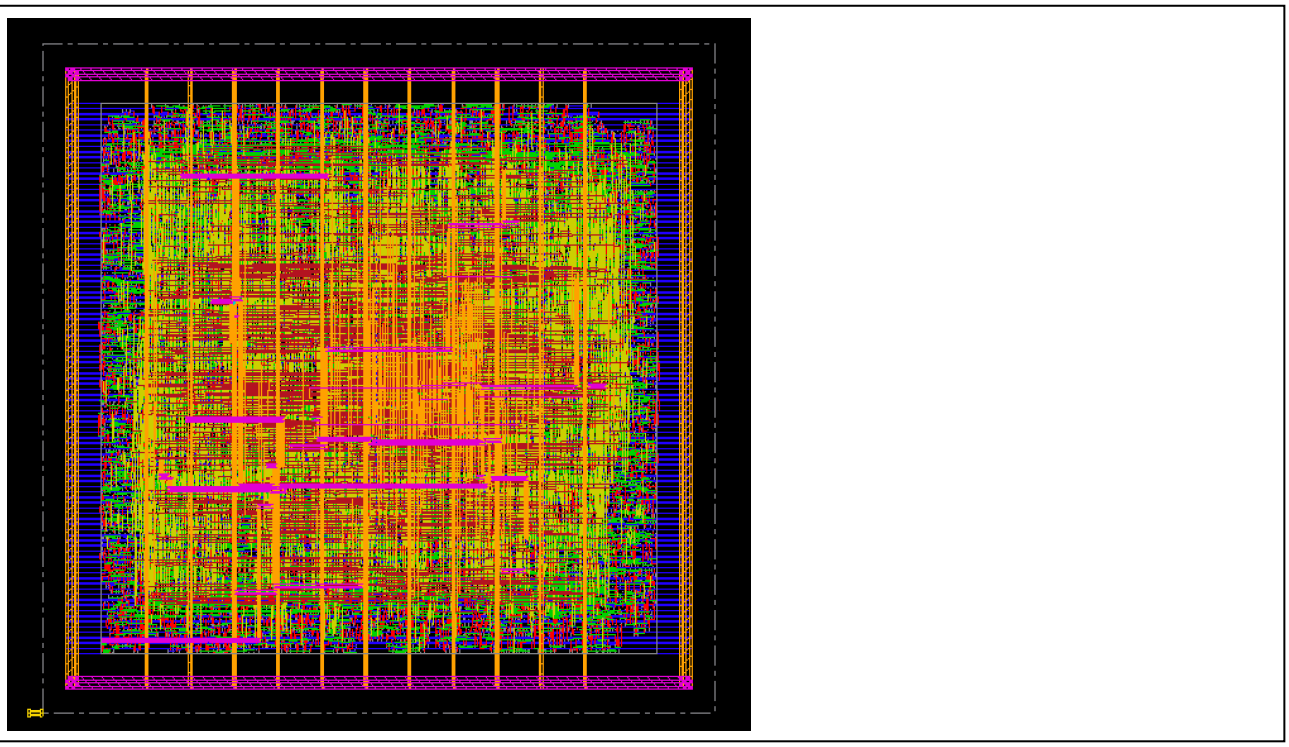
Synthesis Area Report

```
****************************************
Report : area
Design : SET
Version: N-2017.09-SP2
Date   : Tue May 25 09:56:20 2021
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         3533
Number of nets:                         11878
Number of cells:                         8024
Number of combinational cells:           6623
Number of sequential cells:              1301
Number of macros/black boxes:               0
Number of buf/inv:                        697
Number of references:                     195

Combinational area:              85346.970354
Buf/Inv area:                     3861.584948
Noncombinational area:           36241.186321
Macro/Black Box area:                0.000000
Net Interconnect area:          968291.590881

Total cell area:                121588.156675
Total area:                    1089879.747556
```

Synthesis Power Report

```
Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
SET                   tsmc13_wl10       slow


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   9.6806 mW   (73%)
  Net Switching Power  =   3.5423 mW   (27%)
                         ---------
Total Dynamic Power    =  13.2230 mW  (100%)

Cell Leakage Power     =  29.8165 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           8.2617           0.6431        9.6455e+06            8.9144  (  67.26%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational      1.4190           2.8992        2.0171e+07            4.3383  (  32.74%)
--------------------------------------------------------------------------------------------------
Total              9.6806 mW        3.5423 mW     2.9816e+07 pW        13.2528 mW
```

APR NanoRoute Innovus Result (截圖)



APR Simulation Result (截圖)

```
---------------------------- Simulation Stops !!----------------------------
================================================================================



        ****************************
        **                        **        /|__/|
        **  Congratulations !!    **      / O,O  |
        **                        **    /_____   |
        **  Simulation Complete!! **   /^ ^ ^ \  |
        **                        **  |^ ^ ^ ^ |w|
        ********************** ***********   \m___m__|_|


================================================================================
Simulation complete via $finish(1) at time 2324 NS + 0
./testbench.v:109         $finish;
ncsim> exit
```