Design Short Summary for B07505005/黃郁棻 B07505033/呂昕玲

請填寫 Pass/Failed

16x16 RTL	64x64 RTL	16x16 SYN	64x64 SYN	16x16 APR	64x64 APR
Pass	Pass	Pass	Pass	Pass	Pass

以下請 report testbench16.v 的資料(包括截圖)

RTL Report

Clock Cycle	7.5 (ns)
Total Time	439,260 (ns)

Synthesis Report

Clock Cycle	7.5 (ns)
Cell Area	96799.325752 (Please report **Total cell area**)
Total Time	439,261.116 (ns)
Area*Time	42,520,179,860

APR Report

Clock Cycle	7.5 (ns)
Cell Area	102037.504 (Please report **Total area of Core)**
Total Time	439,261.785 (ns)
Area*Time	44,821,176,140

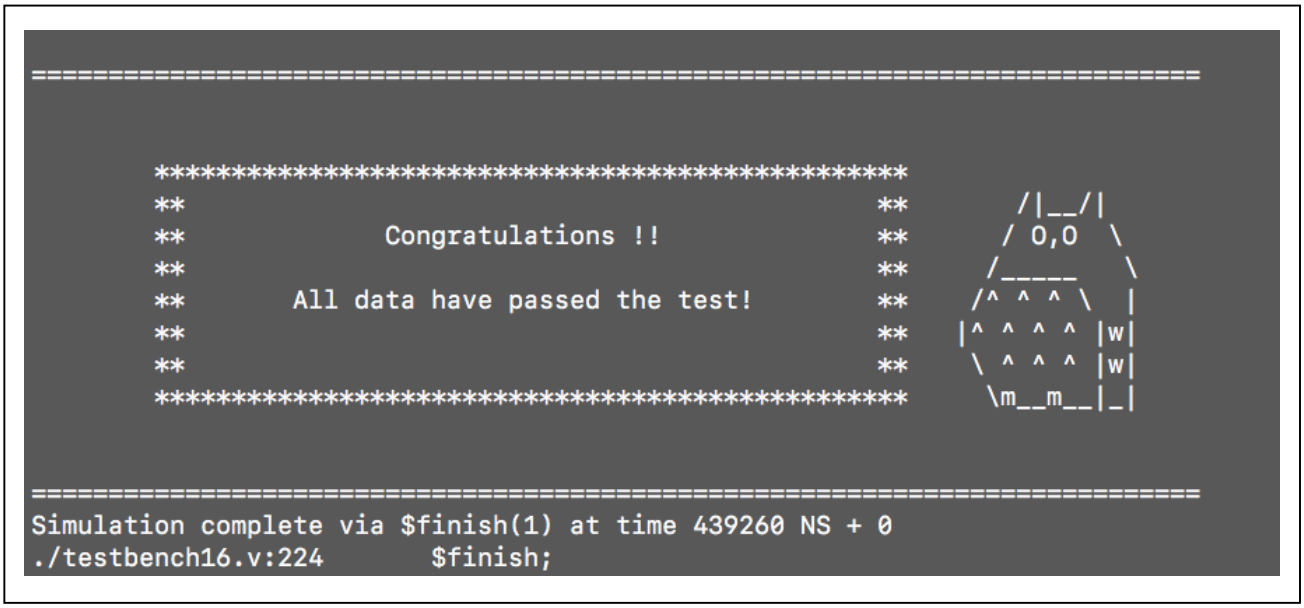
How to report area in Design Vision?

➔ report_area > autoseller_area.txt, find **Total cell area.**

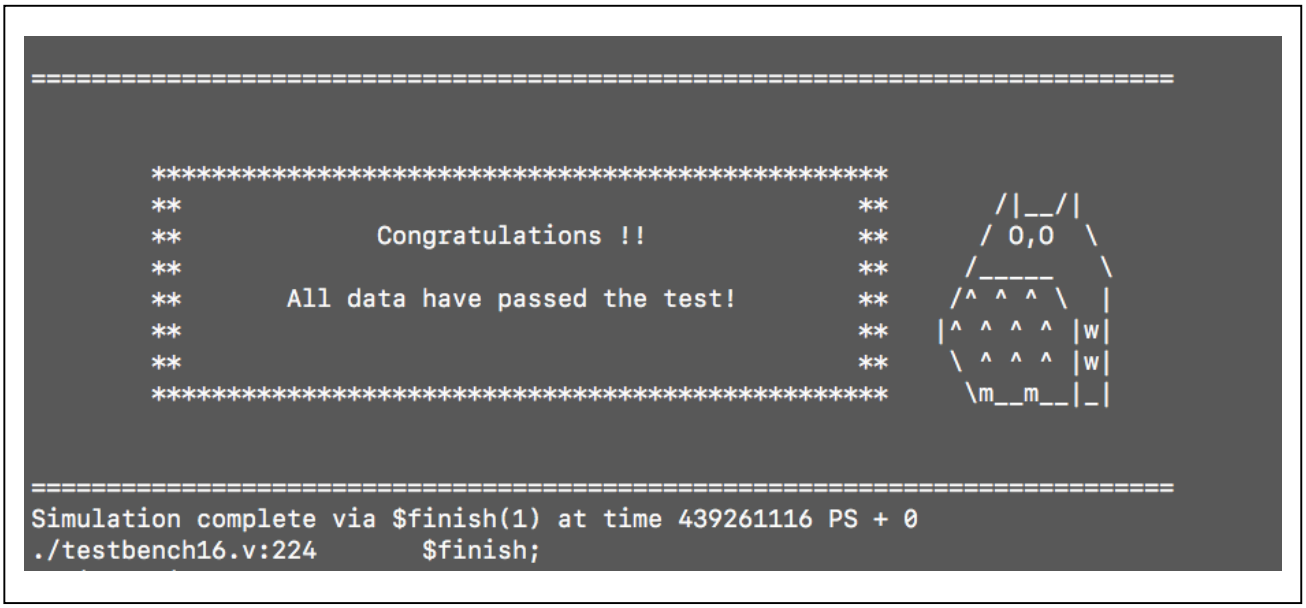
How to report area in Innovus?

➔ File > Report > Summary > choose Text only, file name: **summaryReport.rpt**>OK, find **Total area of Core.**

RTL Simulation Result (截圖)



Synthesis Simulation Result (截圖)



Synthesis Timing Report

```
wo_dout_reg[1]/D (DFFRX1)                0.00       7.67 f
data arrival time                                   7.67

clock clk (rise edge)                    7.50       7.50
clock network delay (ideal)              0.50       8.00
clock uncertainty                       -0.10       7.90
wo_dout_reg[1]/CK (DFFRX1)               0.00       7.90 r
library setup time                      -0.23       7.67
data required time                                  7.67
-----------------------------------------------------------
data required time                                  7.67
data arrival time                                  -7.67
-----------------------------------------------------------
slack (MET)                                         0.00
```

Synthesis Area Report

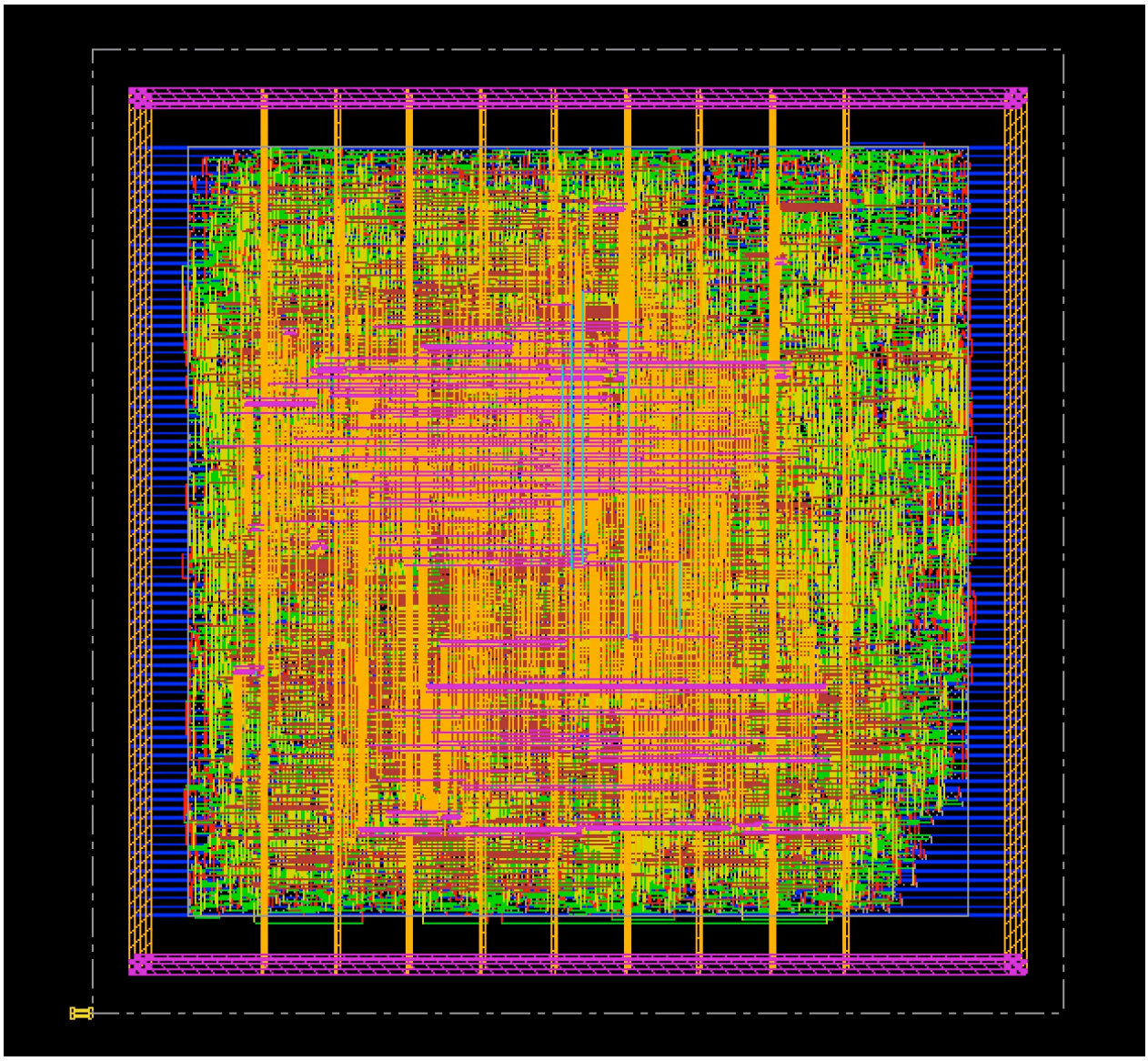
```
Combinational area:              42983.260547
Buf/Inv area:                     5857.727341
Noncombinational area:           53816.065205
Macro/Black Box area:                0.000000
Net Interconnect area:          892924.590973

Total cell area:                 96799.325752
Total area:                     989723.916724
```

Synthesis Power Report

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	4.5893	3.1882e-02	4.9502e+07	4.6707	(86.76%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	8.8074e-02	0.5995	2.5428e+07	0.7130	(13.24%)	
Total	4.6773 mW	0.6314 mW	7.4930e+07 pW	5.3837 mW		

APR NanoRoute Innovus Result (截圖)



APR Simulation Result (截圖)