Lab 3 Specifications

Lab-specific Specifications

Proficiency

\Box Circuit correctly reads inputs from 4×4 keypad.	
\square Dual seven-segment display shows the last two hexadecimal digits p	pressed.
\square Most recent numeric entry is shown on the right.	
□ Design does not lock up when multiple buttons are pressed at once the current values on the display and functions properly again where released.)	
☐ Design only registers first button press if additional buttons are holding down one button.	pressed down while
☐ Each button press registered only once (e.g., no switch bouncing)	
$\hfill \square$ Seven segment displays are same brightness regardless of how many nated.	segments are illumi-
\square Design has no latches.	
\square Design has no tristate buffers.	
\square Report includes state transition diagram illustrating the operation	of the system.
Excellence	
☐ Design uses synchronizers on asynchronous inputs to mitigate meta	stability.
☐ Keypad and seven-segment display are aligned in the same orienta the numbers on both are facing the same direction).	_
☐ State transition diagram is completely specified (i.e., all transitions specified, output conditions specified in each state)	s between states are
☐ Report includes state transition table to document the next tate are each state based on the current state and inputs.	ad output values for
\square Report explains tradeoffs between the chosen design decisions and al	ternatives (e.g., why
did you select a certain switch debouncing strategy and what are the	ne tradeoffs between
your chosen method and others?).	

General Specifications

Proficiency

Genera	al Schematic Specifications
□ A □ C □ N □ A	All pin names labeled All pin numbers labeled Crossing wires clearly identified as junction or unconnected Neat layout (e.g., clear organization and spacing) All parts labeled with part number All component values present
\mathbf{Block}	Diagram
	Block diagram present with one block per SystemVerilog module Each block includes all input and output signals
HDL .	& Code Specifications
Genera	al Formatting
□ I □ N (l	Descriptive filename (e.g., lab2_jb.sv) Descriptive variable names Neat formatting (e.g., standard indentation, consistent formatting for variable names kebab-case/snake_case/camelCase/PascalCase)) Descriptive and clear function/module names
Commo	ents
	Comments to indicate the purpose of each function/module
Lab W	Vriteup/Summary
d d d E d F S P V d V d	Brief (e.g., 3-5 sentence) description of the main goals of the assignment and what was lone. Explanation of design approach. How did you go about designing and implementing the lesign? Explanation of testing approach. How did you verify your design was behaving as expected? Statement of whether the design meets all the requirements. If not, list the shortcomings Number of hours spent working on the lab are included. Vriteup contains minimal spelling or grammar issues and any errors do not significantly letract from clarity of the writeup.
	Optional) List commments or suggestions on what was particularly good about the ssignment or what you think needs to change in future versions.

Excellence

General Schematic Specifications

☐ Standard symbols used for all components where applicable
☐ Signals "flow" from left to right where possible (e.g., inputs on left hand side, outputs on right hand side)
9
☐ Title block with author name, title, and date
HDL & Code Specifications
General Formatting
\square Name, email, and date at the top of every file
☐ Comment at the top of each source code file to describe what is in it
☐ Clear and organized hierarchy (e.g., deliniation between top level modules and submodules)
Testbenches
☐ Testbenches written for each individual module to demonstrate proper operation
☐ Testbench output included in the report
Lab Writeup/Summary
☐ Writeup is free of spelling and grammar issues