

## **Lab 7 Specifications**

### **Lab-specific Specifications**

#### **Proficiency**

- ☐ AES core simulation testbench passes
- ☐ AES SPI simulation testbench passes

#### **Excellence**

- ☐ Design fits on FPGA hardware
- ☐ SPI communication is displayed on logic analyzer
- ☐ System fully operational (sends data from MCU to FPGA and FPGA sends the correct data back again).

## General Specifications

### Proficiency

#### General Schematic Specifications

- ☐ All pin names labeled
- ☐ All pin numbers labeled
- ☐ Crossing wires clearly identified as junction or unconnected
- ☐ Neat layout (e.g., clear organization and spacing)
- ☐ All parts labeled with part number
- ☐ All component values present

#### Block Diagram

- ☐ Block diagram present with one block per SystemVerilog module
- ☐ Each block includes all input and output signals

#### HDL & Code Specifications

##### *General Formatting*

- ☐ Descriptive filename (e.g., `lab2_jb.sv`)
- ☐ Descriptive variable names
- ☐ Neat formatting (e.g., standard indentation, consistent formatting for variable names (kebab-case/snake\_case/camelCase/PascalCase ))
- ☐ Descriptive and clear function/module names

##### *Comments*

- ☐ Comments to indicate the purpose of each function/module

#### Lab Writeup/Summary

- ☐ Brief (e.g., 3-5 sentence) description of the main goals of the assignment and what was done.
- ☐ Explanation of design approach. How did you go about designing and implementing the design?
- ☐ Explanation of testing approach. How did you verify your design was behaving as expected?
- ☐ Statement of whether the design meets all the requirements. If not, list the shortcomings.
- ☐ Number of hours spent working on the lab are included.
- ☐ Writeup contains minimal spelling or grammar issues and any errors do not significantly detract from clarity of the writeup.
- ☐ (Optional) List comments or suggestions on what was particularly good about the assignment or what you think needs to change in future versions.

## **Excellence**

### **General Schematic Specifications**

- ☐ Standard symbols used for all components where applicable
- ☐ Signals “flow” from left to right where possible (e.g., inputs on left hand side, outputs on right hand side)
- ☐ Title block with author name, title, and date

### **HDL & Code Specifications**

#### *General Formatting*

- ☐ Name, email, and date at the top of every file
- ☐ Comment at the top of each source code file to describe what is in it
- ☐ Clear and organized hierarchy (e.g., deliniation between top level modules and submodules)

#### *Testbenches*

- ☐ Testbenches written for each individual module to demonstrate proper operation
- ☐ Testbench output included in the report

### **Lab Writeup/Summary**

- ☐ Writeup is free of spelling and grammar issues