E155 Course Syllabus

Contact Information

Item	Information
Instructors:	Prof. Josh Brake
Lab Assistant(s):	Kavi Dey, Neil Chulani, Henry Merilees
Web page:	https://hmc-e155.github.io/
Lab Checkoff Sheet:	Sheet Link
Email list:	eng-155 [at] g.hmc.edu
Discord Server:	See email for invite

Be sure to join the class Discord and check it regularly as it will be the main source of course-related communication for this semester.

Course Schedule

Name	**Info**
Lecture	TR 1:15 - 2:30 pm
Lab Checkoff	TR afternoons by signup in the Digital Lab (PA B183)
Office Hours	TBD

You will be working on labs on your own time and it is not required that you attend the entire scheduled lab period. Instead, sign up for a time to get your lab checked off. Please sign up for a time during your lab section. If you are unable to find a spot that works for you, see if you can swap with one of your classmates. If you are still having trouble finding a time that works for you, reach out and let me know.

"Office hours" is code for "come hang out." You are encouraged to attend office hours to ask questions, get help with your labs, talk about careers and graduate school, or chat about

something on your mind (whether it is related to this class, academics, or anything else). In addition to things related to Engineering, embedded systems, digital electronics, and microcontrollers, a short (but not comprehensive!) list of things I enjoy talking about are sports (MLB: NY Mets; NFL: Tennessee Titans), running/biking/hiking, life design, time management, or books/essays I'm reading. I am available more often than not, so try dropping me a line via Discord or email if you are having a problem with your lab or want to set up a time. You may also contact the lab assistant(s) for questions when I am not available.

In broad strokes, MicroPs can be divided into two halves. The first half of the class focuses on giving you fundamental embedded systems concepts in lecture which you learn by experience through seven, hands-on labs. These labs are designed to be loosely structured design projects – you will be given information about the required specifications and some pointers on how to get started, but much of the development process is left open to you. The second half of the class is mainly focused on the project. The project gives you the opportunity to demonstrate independent and creative mastery of embedded system design in teams of two. The specific project task is very open-ended; the only requirement is that the project does something fun or useful and that it meaningfully uses both the FPGA and MCU. In addition to having a series of design review checkpoints, you will give a mid-project presentation to the class and a final presentation of your project when finished. The content of the lectures in the second half of the class focuses on exposing you to more advanced embedded systems concepts and exploring a range of various types of external hardware that may be useful to use in your project.

Week #	Monday Date	Tuesday's Class	Thursday's Class	Due
1	8/26	Intro & Analog Behavior of Digital Systems	Combinational and Sequential Logic	Git & Quarto Portfolio Setup
2	9/2	Verilog Coding	Synchronous Design	Lab 1
3	9/9	FPGA Documentation	C Programming on an MCU	Lab 2
4	9/16	Clock Configuration	Timers	Lab 3
5	9/23	Interrupts	Serial Interfaces Overview & SPI	Lab 4
6	9/30	TBD	TBD	
7	10/7	Project Kickoff	UART and the IoT	Lab 5
8	10/14	Happy Fall Break! **No Class**	Proposal Debriefs	Project Proposal

Week #	Monday Date	Tuesday's Class	Thursday's Class	Due
9	10/21	Advanced Encryption Standard (AES)	Graphics and Displays	Lab 6
10	10/28	Motors and Speakers	Direct Memory Access	Lab 7
11	11/4	Design Review Presentations	Design Review Presentations	Design Review Presentation & Memo
12	11/11	Introduction to Real Time Operating Systems	Project Status Report and Demo	Project Status Reports & Demo
13	11/18	The Fast Fourier Transform (FFT)	Connectors	
14	11/25	Emerging Topics in Embedded Systems	Happy Thanksgiving! **No class**	
15	12/2	Guest Lecture: Ben Chelf	TBD	Project Checkoffs, Report, Demo Day

Course Learning Objectives

The overarching goal of this course is to take you from a basic familiarity and knowledge of digital design with field gate programmable arrays (FPGAs) and microcontrollers programming and expand your capabilities to design, build, and test embedded systems.

The learning goals for the course are divided into two main categories: technical and professional. The technical learning goals describe the technical skills you will acquire as you complete the course. The professional learning goals articulate how this course will help you to grow as a person and develop the character traits that will help you to thrive as you take the skills you learn in this class beyond the walls of Harvey Mudd.

Technical Learning Goals

By the end of this course you should be able to:

- Design and implement combinational and sequential circuits on an FPGA.
- Use an ARM-based microcontroller to interface with the real world via sensors and actuators.
- Build an embedded system project of your own design from the ground up.
- Select appropriate embedded hardware for a given design challenge.
- Effectively and efficiently debug electrical systems with measurement tools such as an oscilloscope and logic analyzer.
- Read and understand complicated datasheets at a level that enables you to incorporate them into your designs.

Professional Learning Goals

By the end of this course you should be able to:

- Communicate technical results with clarity and in a professional manner through oral presentations and written reports.
- Communicate your work with a wide variety of audiences, including technical experts, your peers, and the general public.
- Articulate how you have developed character strengths throughout the semester.

Teaching Philosophy

The ultimate goal for this course is to help you to master the material and become skilled embedded systems developers who understand how to build a system from a set of requirements and specifications and to verify that the system meets those specifications.

Here are a few of the main pedagogical concepts that you can expect to see in this course.

- **Transparent Teaching** – you should not have to guess what you are supposed to get out of a given activity or assignment in this class. I strive to be as transparent about why we are doing what we are doing. This is most clearly articulated through explicit learning goals that accompany each lecture, lab, or project. If the purpose of anything we do in this class is ever unclear, please ask me and I will be happy to clarify it.
- **Psychological Safety** – A psychologically safe environment is one where each person feels able to share their questions, concerns, or mistakes without feeling embarrassed or looked down upon by others. Building a psychologically safe classroom is a joint venture which I expect each of you to join with me in pursuing.
- **A Growth Mindset** – growth can only happen when you reach the end of what you already know. Each of you coming into this class will have different levels of experience with the types of skills that are useful in this class like working with embedded systems, programming, debugging, design, etc. My goal as an instructor is to take you from wherever you are and bring you as far along in your journey as possible. To do that, I

encourage each of you to ask questions and push yourself to the edge of your knowledge. It can be frustrating or embarrassing to have questions that you feel you should already have the answer to. You should take these moments as opportunities to ask questions and fill the gaps in your knowledge. In the end, having a growth mindset is strongly linked with deep curiosity about what you are learning and a realization that while being honest about the limits of your understanding might be challenging, embracing that discomfort allows you to grow and improve quickly.

- **Frequent, Low-stakes Testing** – Research has shown that having frequent opportunities to assess your knowledge is a powerful way to learn and correct any misconceptions. One way that this will take place is through regular in-class quizzes and activities.
- **Interleaving** – The scheduling of the material is arranged in such a way that you will return to many similar concepts throughout the semester with some time in between. The goal of this is to have you return to familiar concepts after some time away so that you reinforce the material after working on something else. This has been shown to improve long-term retention of the material (see *Small Teaching* by James Lang if you are curious in learning more).

Recommended Texts

I assume you have a solid grasp of digital design at the level of E85; review Digital Design and Computer Architecture, ARM Edition (link) if you feel rusty on a topic. We will not be closely following a textbook, but you may find The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors by Joseph Yiu to be a helpful, comprehensive reference for the microcontroller. An electronic version of the book is available through the library (link).

Lab Kit

While there is not a textbook to purchase, you will need to buy a lab kit. The fee is $75 in Claremont Cash, and should be paid by filling out the Google Form (link) which authorizes Sydney Torrey in the Engineering office to charge your Claremont Cash account. Once you have paid for your kit via the form, see Sam Abdelmuati in the stockroom to pick up your kit. If you cook your board this semester, you can buy and rebuild a replacement, but ask the instructor for help troubleshooting first. You'll also check out a large breadboard from the stockroom, and will need to return it at the end of the semester.

The kit fee can be waived in cases of financial hardship. To request a waiver fill out the form here (link). Course instructors will not know about waiver requests.

Lab Access

The Digital Lab (Parson B183) is available for you to use when working on your labs. The current door code will be shared privately. There are Windows PCs available with SEGGER Embedded Studio and Lattice Radiant installed along with the drivers required to program your board. The lab also has the electronics assembly equipment needed to solder, oscilloscopes and power supplies at the lab stations, and a lab cabinet with various resistors and some of the parts like wires, seven-segment LEDs, and transistors you will need for some of your labs. You are welcome to use these while working on your lab, but please make sure to return the components to the lab cabinet when you are done.

In addition, the software we will be using for programming the MCU (SEGGER Embedded Studio for ARM) and FPGA (Lattice Radiant) are free and supported on a variety of platforms if you wish to download them on your personal computer. SEGGER Embedded Studio is supported on Windows, MacOS, and Linux and Lattice Radiant is supported on Windows and Linux. If you are running MacOS, you can download and virtualize Windows using VMWare Fusion Pro under a Personal Use License for free. More details and download links can be found here (link).

Grading

The grading for this class is based on a variation of specifications-grading and may be a bit different than what you have seen in other classes. The grade you earn in the class will be determined based the number of deliverables you successfully complete and the level of polish to which you complete them across three different bundles:

1. Labs
2. Project
3. In-class reflections

Each assignment will contain a list of specifications (or specs) for two levels of completeness: proficiency and excellence. The list of specifications are designed to be aligned with the learning goals for the assignment. The proficiency specifications will indicate the level of completeness that demonstrates that you have achieved a level of comfort with the material in the assignment such that you would be able to implement the learning outcomes in a different setting. Excellence specs are above and beyond proficiency specs. Meeting the excellence specs for an assignment indicates that you have not only achieved the basic level of expected knowledge of the material, but have truly understood and are able to apply the techniques with deftness.

The table below describes the levels that you need to meet in each bundle (i.e., column) in order to earn the grade in the respective row. To earn the grade in a given row, you must meet **all** the criteria in that row. In other words, to get a B, you must complete the following:

- All 7 labs to the proficiency specs and 5 of those labs must meet the excellence specs.
- All 5 project elements must meet proficiency specs and 4 of them must meet the excellence specs.

Grade	Labs	Project
F	$P < 5$	$P < 4$
D	$P \geq 5$, $E \geq 1$	$P \geq 4$
C	$P \geq 6$, $E \geq 2$	$P \geq 4$, $E \geq 2$
B	$P = 7$, $E \geq 5$	$P = 5$, $E \geq 4$
A	$P = 7$, $E = 7$	$P = 5$, $E = 5$

Performance on the labs and project is weighted equally. +/- grades will be assigned for situations in which your performance falls between the conditions for each row.

In addition to the labs and projects, you will also write short (2-3 paragraph) reflections each week as a way of helping you to catalog your growth in the class. These informal reflections are designed to be published as blog posts on your portfolio website and along with your in-class participation on short quizzes can help to boost your grade in the class by up to half a letter grade (e.g., from a B- to a B or B+ to an A-). As one example, if you meet the requirements for an A in the labs bundle but the requirements for a B in the project bundle, you can expect to earn either a B+ or A-. In these situations, your in-class participation is a contributing factor to split the difference between the - of the higher tier and the + of the lower tier.

Course Policies & Honor Code

This section articulates a number of policies for the course. The goal of theses policies is to create the most effective learning experience for you in this course. If you have questions about any of these policies or the motivation behind them, I would be glad to discuss more with you. Please find me sometime after class or in office hours!

Communication Policy

Please note that I do not always respond immediately to messages. In particular I typically do not check email or Discord between 6:00 pm and 6:00 am on weeknights, and I typically do not check these at all on weekends. In addition, Friday is my off-campus consulting day which means that I may be slow to respond to messages then.

That said, I do my best to do meet the following:

- Messages sent on a weekday other than Friday (i.e., Monday-Thursday) before 4:00 pm PT will get a response the same day.

- Messages sent after 4:00 pm PT Sunday-Wednesday will get a response the next day.
- Messages sent after 4:00 pm PT on Fridays or on the weekend will get a response the following Monday.

Collaboration Policy

Your peers are an excellent source of support and can be a great help as you complete MicroPs. With that said, it is important that each student in the class do the work for themselves to develop their own expertise. The collaboration policy for MicroPs is as follows:

> **i** Collaboration Policy
>
> You **should**:
>
> - Discuss high level questions about the approach to the lab **after** you have spent time developing your own initial approach.
> - Ask for feedback on your Verilog code **after** both you and the person you are asking to review your code have made a significant attempt on your own.
> - List on your lab writeup any people that have reviewed your work or for whom you have reviewed work.
> - Ask the instructor any question you think might be inappropriate to discuss with a peer.
>
> You may **not**:
>
> - Pair program.
> - Use code that you have not personally typed (e.g., do not copy-paste code from any source). Note that this policy does not apply to the portions of your lab where you are encouraged to use AI.
> - Directly copy code from any other person.
> - Use any source code in your project without citation (e.g., if you use a module from a textbook or another online source, be sure to cite it in the comments of your code.).

AI Policy

AI tools like ChatGPT are an emerging and active area of research and development. The generative AI tools available today are significantly better than those available even six months ago. Although there are no guarantees in life, it is reasonable to assume that they will continue to improve as they are further refined, even as laws of diminishing returns inevitably come into play.

Experiencing this rapidly evolving field in real time is exciting, but it also presents some challenges for teaching and learning. Some have argued that generative AI democratizes expertise, but in truth what it democratizes is the *appearance* of expertise, not the expertise itself. As we think about generative AI tools like large language models (LLMs) and their place in education, we need to be careful to keep our principles and values clearly in view at all times. What is the goal of the work we are doing together?

From a practical point of view, it is prudent to ask the question about how the continued development of AI will impact the value of this knowledge and skill. It is hard to believe that AI will not significantly change the nature of work in the course of your careers. It is highly likely that there is a future where some of the skills you learn today are no longer relevant, in the same way that we no longer use slide rules to make calculations. For example, it has become clear that LLMs can be a significant aid when programming.

While we look toward the future and anticipate many changes, we must be careful not to discard the foundational skills and knowledge that will allow us to leverage the capabilities of whatever innovation is on the horizon. Not only that, but we must also not forget that our knowledge and skill is built on the foundation of our character; those things that define who we are as people and shape our deepest values for who we want to be and the world we want to be a part of.

On the question of how to engage generative AI, I encourage us all to embrace a posture of curiosity and critical exploration. To turn a blind eye to an innovation of such magnitude is to surrender one's agency to shape its trajectory. How to engage AI wisely through this lens will vary based on the situation. For example, some of your classes and professors will urge you to avoid using generative AI tools altogether. Instead of responding with an attitude of suspicion or assuming that they have made this decision out of fear, I would urge you to engage with a posture of humility and curiosity, seeking to understand the reasons behind their policy and how the decision aligns with the goals they are trying to guide you and your classmates toward.

Other professors may have a more or less welcoming approach to these new tools, encouraging or even requiring that you experiment with them in their classes. Once again, I would encourage you to engage with curiosity and seek to understand the values that motivate their decision.

Following the public release of ChatGPT in late 2022, large language models (LLMs) hit the mainstream and have been the subject of robust conversations about how educators and students should approach these tools. AI tools, whether in the form of an LLM or something else, are likely to have an impact on your career and work as an engineer. In this class, we will be approaching AI tools with a posture of cautious engagement. The guiding principle for the use of AI tools is that these tools must be used in the spirit of the assignment.

Using AI in MicroPs

In MicroPs this fall we will adopt the following policies for generative AI use:
You **should**:

- **Use AI on the AI prototypes throughout the course.** Each lab this fall will include a section describing a generative AI experiment. For the tasks in these sections you are required to leverage generative AI. As you embrace AI, I would encourage you to reflect on your experience using it and on its impact on your skill development. Your reflections on these AI experiments each week are a great topic to discuss in your weekly reflections.

You should **not**:

- **Use generative AI to directly generate any code on the main lab design challenges.** Learning how to write Verilog and C code is a core learning objective in this class. The best way to learn how to evaluate the quality of LLM-generated code is by first writing a large quantity of it for yourself.
- **Use generative AI to generate any of your technical documentation.** Thinking is writing, and learning how to articulate what you've done and what it means matters. Outsourcing this task to an LLM will not help you to better understand the work you are doing. As noted above, you may use spellcheckers, but you must not use tools which will rewrite sentences for you or generate text (e.g., Google's "Help Me Write" feature)

Once the labs finish, we will revisit this policy for the project phase of the class to decide collectively how we may want to revise our approach to generative AI. The results of your weekly AI prototypes and reflections about them will provide a healthy foundation from which we can discuss!

Honor Code Violations

Students in this class are expected to follow the HMC honor code. An honor code policy appears below and prescribes behavior that is considered honorable, so read those maxims and follow them closely. Any honor code violations will be handled through JB.

If you believe you have violated the honor code in any way, please take the initiative to self report so that we can come up with a fair and just path forward together.

Honor Code Policy

1. All students enrolled in this course are bound by the HMC Honor Code. More information on the HMC Honor Code can be found in the HMC Student Handbook.
2. It is your responsibility to determine whether your actions adhere to the HMC Honor Code. If this document does not clarify the legitimacy of a particular action, you should contact the course instructor and request clarification.
3. Work you submit for individual assignments should be your own, and you should complete all assignments based on your own understanding of the underlying material. If you work with, or receive help from, another individual on an assignment, provide a written acknowledgement in complete sentences that includes the person's name and the nature of the help.
4. This document is not meant to be an exhaustive list of every possible Honor Code violation. Infractions not explicitly mentioned here may still violate the Honor Code.
5. **Boundaries of Collaboration.** Verbal collaboration with other students on individual assignments is encouraged **after** you have given serious thought to each component yourself. However, all submitted written work should be written by yourself individually, and not a collaborative effort or copied from a common source (e.g., a chalkboard). It is **not** acceptable to work on labs in lockstep with another classmate.
6. **Use of Computer Software.** The use of graphing calculators and computer software to aid in course work is acceptable, as long as it does not substitute for an understanding of the course material.
7. **Use of Web Resources.** The use of Internet resources to aid in course work is acceptable, as long it does not substitute for an understanding of the course material. Plagiarism and direct copying from online (or any other) sources is strictly prohibited.
8. **Use of Your Own Work from Previous Semesters.** If you have previously attempted this course, you may resubmit your work from previous semesters as this semester's coursework, as long as you understand the underlying material.
9. **Use of Other Course Resources from Previous Semesters.** You may not reference assignments (labs, problem sets, activities) of this course from previous semesters.
10. **Retention of Course Resources.** Assignments and exams from this course may not be committed to dorm repositories or otherwise used to help future students.

Inclusiveness and Harassment

We do difficult work in this class and everyone should feel comfortable engaging with the material. We explicitly want you to feel safe doing this work, so it is worth stating that the instructors are committed to making the class a safe space for everyone regardless of race, gender, ethnicity, sexual orientation, religion, and academic history. If you feel that you are experiencing a hostile environment, speak to an instructor immediately.

Educational Accessibility

HMC is committed to providing an inclusive learning environment and support for all students. Students with a disability (including mental health, chronic or temporary medical conditions) who may need some accommodation in order to fully participate in this class are encouraged to contact Educational Accessibility Services at ability@g.hmc.edu to request accommodations. Students from the other Claremont Colleges should contact their home college's disability resources officer.