Lab 5 Specifications

Lab-specific Specifications

Proficiency

- ☐ Design measures and displays speed of motor in units of rev/s with an update rate of at least 1 Hz.
- ☐ Measured speed matches true motor speed and direction (calculations should be provided in the report to verify this).
- ☐ Code uses interrupts (rather than polling or timers) to detect encoder pulses.
- ☐ Interrupt code does not miss any encoder pulses at normal speed.
- ☐ Motor speed is reported as zero when it is not spinning

Excellence

- ☐ Design uses all edges of encoder pulses to achieve highest resolution measurement.
- ☐ MCU does not miss any pulses at high speed and outputs a non-zero velocity at low speeds.
- ☐ Report compares the performance of interrupt based code to manual polling at high speeds.
- ☐ Report includes flowchart illustrating main steps of the program and function calls.

General Specifications

Schematic Specifications

Proficiency

- ☐ All pin names labeled
- ☐ All pin numbers labeled
- ☐ Crossing wires clearly identified as junction or unconnected
- ☐ Neat layout (e.g., clear organization and spacing)
- ☐ All parts labeled with part number
- ☐ All component values present

Block Diagram

- ☐ Block diagram present with one block per SystemVerilog module
- ☐ Each block includes all input and output signals

Excellence

General Schematic Specifications

- ☐ Standard symbols used for all components where applicable
- ☐ Signals "flow" from left to right where possible (e.g., inputs on left hand side, outputs on right hand side)
- ☐ Title block with author name, title, and date

HDL & Code Specifications

Proficiency

- ☐ Descriptive filename that matches module name (e.g., `lab2_jb.sv`)
- ☐ One module per file
- ☐ Descriptive variable names
- ☐ Neat formatting (e.g., standard indentation, consistent formatting for variable names (kebab-case/snake_case/camelCase/PascalCase))
- ☐ Descriptive and clear function/module names
- ☐ Comments to indicate the purpose of each function/module

Excellence

- ☐ Name, email, and date at the top of every file
- ☐ Comment at the top of each source code file to describe what is in it
- ☐ Clear and organized hierarchy (e.g., delineation between top level modules and submodules)
- ☐ Testbenches written for each individual module to demonstrate proper operation
- ☐ Testbench output for each module included in the report

Writeup/Summary

Proficiency and Excellence

- ☐ Statement of whether the design meets all the requirements. If not, list the shortcomings.
- ☐ Number of hours spent working on the lab are included.
- ☐ Writeup contains minimal spelling or grammar issues and any errors do not significantly detract from clarity of the writeup.
- ☐ AI prototype attempted and some reflection is recorded.
- ☐ (Optional) List comments or suggestions on what was particularly good about the assignment or what you think needs to change in future versions.

Comments

Add specific notes here about the assignment.