Lab 2 Specifications

Lab-specific Specifications

Proficiency

- ☐ HDL design includes only a single seven-segment decoder module.
- ☐ Sum of the numbers on the two displays is correctly displayed for all inputs
- ☐ Seven segment displays are same brightness regardless of how many segments are lit
- ☐ Resistors are in series with FPGA pins so that they correctly limit current

Excellence

- ☐ No noticeable bleeding of the digits between displays
- ☐ No flickering on the individual digits
- ☐ Current draw/sink on all FPGA pins are below the currents specified in the recommended operating conditions. Claims are backed up by calculations and reference to the appropriate items on the datasheet.
- ☐ Digits on the seven-segment display are upright to the viewer.

General Specifications

Schematic Specifications

Proficiency

- ☐ All pin names labeled
- ☐ All pin numbers labeled
- ☐ Crossing wires clearly identified as junction or unconnected
- ☐ Neat layout (e.g., clear organization and spacing)
- ☐ All parts labeled with part number
- ☐ All component values present

Block Diagram

- ☐ Block diagram present with one block per SystemVerilog module
- ☐ Each block includes all input and output signals

Excellence

General Schematic Specifications

- ☐ Standard symbols used for all components where applicable
- ☐ Signals "flow" from left to right where possible (e.g., inputs on left hand side, outputs on right hand side)
- ☐ Title block with author name, title, and date

HDL & Code Specifications

Proficiency

- ☐ Descriptive filename that matches module name (e.g., `lab2_jb.sv`)
- ☐ One module per file
- ☐ Descriptive variable names
- ☐ Neat formatting (e.g., standard indentation, consistent formatting for variable names (kebab-case/snake_case/camelCase/PascalCase))
- ☐ Descriptive and clear function/module names
- ☐ Comments to indicate the purpose of each function/module

Excellence

- ☐ Name, email, and date at the top of every file
- ☐ Comment at the top of each source code file to describe what is in it
- ☐ Clear and organized hierarchy (e.g., delineation between top level modules and submodules)
- ☐ Testbenches written for each individual module to demonstrate proper operation
- ☐ Testbench output for each module included in the report

Writeup/Summary

Proficiency and Excellence

- ☐ Statement of whether the design meets all the requirements. If not, list the shortcomings.
- ☐ Number of hours spent working on the lab are included.
- ☐ Writeup contains minimal spelling or grammar issues and any errors do not significantly detract from clarity of the writeup.
- ☐ AI prototype attempted and some reflection is recorded.
- ☐ (Optional) List comments or suggestions on what was particularly good about the assignment or what you think needs to change in future versions.

Comments

Add specific notes here about the assignment.