Project Final Checkoff Specs

Proficiency

- ☐ Project meets most of of the specifications as laid out in the proposal with explanations for any specifications that weren't met.
- ☐ System operates without any major bugs (e.g., doesn't freeze in operation)
- ☐ Document listing each spec from the proposal along with a short (e.g., 3-5 sentence) summary explaining whether the spec was met or not.
- ☐ Technical documentation (e.g., schematics, code, block diagrams) available for review at checkoff.
- ☐ Verilog HDL is functional and cleanly formatted
- ☐ MCU C code is functional and cleanly formatted

Excellence

- ☐ Project meets **all** the specifications as laid out in the proposal.
- ☐ Project is polished (e.g., wires are hidden, any physical interfaces are well-designed and reliable, clean user interface)
- ☐ Verilog code is efficient and demonstrates best coding practices (e.g., modularity, test-benches were appropriate, etc.)
- ☐ C code is efficient and well organized (e.g., code encapsulated in functions and custom libraries as appropriate)