Lab 1 Specifications

Lab-specific Specifications

Proficiency

- ☐ Development board is fully assembled (e.g., all parts soldered)
- ☐ Verilog module to control LEDs and a 7-segment display written
- ☐ FPGA programmed with Verilog code.
- ☐ 7-segment display can display all sixteen hexadecimal digits from `0x0` through `0xF`
- ☐ All digits are unique (e.g., `0x6` and `0xb` are different shapes)
- ☐ DIP switches to control the display are arranged so that each adjacent switch controls the next bit. (e.g., the switch for bit 0 is next to the switch for bit 1, which is next to the switch for bit 2, etc.)
- ☐ LEDs display the specified logic operations properly.

Excellence

- ☐ Calculations provided to demonstrate that the current draw for each segment in the seven-segment display is within recommended operating conditions.
- ☐ QuestaSim simulation with automatic testbenches for each module to demonstrate that the design is working properly.
- ☐ All digits are equally bright, regardless of the number of segments illuminated.

General Specifications

Schematic Specifications

Proficiency

- ☐ All pin names labeled
- ☐ All pin numbers labeled
- ☐ Crossing wires clearly identified as junction or unconnected
- ☐ Neat layout (e.g., clear organization and spacing)
- ☐ All parts labeled with part number
- ☐ All component values present

Excellence

- ☐ Standard symbols used for all components where applicable
- ☐ Signals "flow" from left to right where possible (e.g., inputs on left hand side, outputs on right hand side)
- ☐ Title block with author name, title, and date

Block Diagram (Required for labs 1, 2, 3 and 7)

Proficiency and Excellence

- ☐ Block diagram present with one block per SystemVerilog module
- ☐ Each block includes all input and output signals

HDL & Code Specifications

Proficiency

- ☐ Descriptive filename that matches module name (e.g., `lab2_jb.sv`)
- ☐ One module per file
- ☐ Descriptive variable names
- ☐ Neat formatting (e.g., standard indentation, consistent formatting for variable names (kebab-case/snake_case/camelCase/PascalCase))
- ☐ Descriptive and clear function/module names
- ☐ Comments to indicate the purpose of each function/module

Excellence

- ☐ Name, email, and date at the top of every file
- ☐ Comment at the top of each source code file to describe what is in it
- ☐ Clear and organized hierarchy (e.g., delineation between top level modules and submodules)
- ☐ Testbenches written for each individual module to demonstrate proper operation
- ☐ Testbench output for each module included in the report

Writeup/Summary

Proficiency and Excellence

- ☐ Statement of whether the design meets all the requirements. If not, list the shortcomings.
- ☐ Number of hours spent working on the lab are included.
- ☐ Writeup contains minimal spelling or grammar issues and any errors do not significantly detract from clarity of the writeup.
- ☐ AI prototype attempted and some reflection is recorded.
- ☐ (Optional) List comments or suggestions on what was particularly good about the assignment or what you think needs to change in future versions.

Comments

Add specific notes here about the assignment.