Project Final Checkoff Specs

Proficiency

Project meets most of of the specifications as laid out in the proposal with explanations or any specifications that weren't met.
system operates without any major bugs (e.g., doesn't freeze in operation)
Document listing each spec from the proposal along with a short (e.g., 3-5 sentence) ummary explaining whether the spec was met or not.
Cechnical documentation (e.g., schematics, code, block diagrams) available for review at heckoff.
Verilog HDL is functional and cleanly formatted
ACU C code is functional and cleanly formatted
ence
Project meets all the specifications as laid out in the proposal.
Project is polished (e.g., wires are hidden, any physical interfaces are well-designed and eliable, clean user interface)
Verilog code is efficient and demonstrates best coding practices (e.g., modularity, test- penches were appropriate, etc.)
C code is efficient and well organized (e.g., code encapsulated in functions and custom abraries as appropriate)