# FPGA Documentation

Lecture 05

Josh Brake
Harvey Mudd College

# Outline

- Documentation Overview
- FPGA documentation Bingo
- Manual design mapping exercise
- Quick basic testbench review

# Learning Objectives

By the end of this lecture you should be able to…

- Find basic specs in the FPGA documentation to answer questions about your system like DC logic levels, max clock speed, etc.
- Determine the number of logic cells required by simple Verilog modules.
- Recall how to write a Verilog testbench

# Lattice iCE40UP Documentation

Documentation

| Quick Reference | Technical Resources | Information Resources | Downloads |
|---|---|---|---|
| Key Documents | Reference Design | Product Brochure | IBIS Model |
| Data Sheet | Product Change Notification | Quality Assurance | |
| Application Note | Schematic | White Paper | |
| Pin & Package | | | |
| User Manual | | | |

| TITLE | NUMBER | VERSION | DATE | FORMAT | SIZE |
|---|---|---|---|---|---|
| iCE40 UltraPlus Family Data Sheet | FPGA-DS-02008 | 2.0 | 9/20/2021 | PDF | 1.1 MB |
| Memory Usage Guide for iCE40 Devices | FPGA-TN-02002 | 1.7 | 10/14/2020 | PDF | 954.3 KB |
| iCE40 I2C and SPI Hardened IP Usage Guide | FPGA-TN-02010 | 1.7 | 9/11/2020 | PDF | 1.3 MB |
| iCE40 SPRAM Usage Guide | FPGA-TN-02022 | 1.3 | 4/16/2021 | PDF | 912.9 KB |
| iCE40 Hardware Checklist | FPGA-TN-02006 | 2.0 | 3/10/2022 | PDF | 355.4 KB |
| iCE40 Oscillator Usage Guide | FPGA-TN-02008 | 1.7 | 1/25/2021 | PDF | 675 KB |
| iCE40 sysCLOCK PLL Design and User Guide | FPGA-TN-02052 | 1.4 | 4/30/2022 | PDF | 1.3 MB |
| iCE40 LED Driver User Guide | FPGA-TN-02021 | 1.5 | 11/29/2021 | PDF | 2 MB |

# Lattice iCE40UP Documentation

- Info on FPGA chip itself
  - DC logic levels
  - Timing information
  - Package dimensions
  - Pinout information
  - Block diagrams of internal components


**iCE40 UltraPlus Family Data Sheet**

**Data Sheet**

FPGA-DS-02008-2.0


**Package Diagrams**

**Data Sheet**

FPGA-DS-02053-6.8

# UPduino Documentation

Specs specific to the UPduino board

- Schematics
- Supporting hardware
- Programming instructions

## UPduino Documentation

### tinyVision.ai

#### UPDuino v3.0: PCB Design Files, Designs, Documentation

The UPDuino v3.0 is a small, low-cost FPGA board. The board features an on-board FPGA programmer, flash and LED with _all_ FPGA pins brought out to easy to use 0.1" header pins for fast prototyping.

The tinyVision.ai UPduino v3.0 Board Features:

- Lattice UltraPlus ICE40UP5K FPGA with 5.3K LUTs, 1Mb SPRAM, 120Kb DPRAM, 8 Multipliers
- FTDI FT232H USB to SPI Device
- _ALL_ 32 FPGA GPIO on 0.1" headers
- _ALL_ FTDI pins brought to test points
- 4MB SPI Flash
- RGB LED
- On board 3.3V and 1.2V Regulators, can supply 3.3V to your project
- Open source schematic and layout using KiCAD design tools
- Integrated into the open source APIO toolchain

# FPGA Documentation Bingo

# Manual Design Mapping

Going from Verilog HDL to logic cells

- 2-input AND: _____
- 4-input AND: _____
- 5-input AND: _____
- 16-input AND: _____
- Arbitrary function of 5 inputs: _____
- Arbitrary function of 6 inputs: _____

  _____
- 2 inverters: _____
- Divide by 3 counter: _____

# Wrap up

- FPGA documentation contains important information like logic levels and timing specs
- Learning to navigate the documentation is a skill that must be practiced. Try to browse instead of search.
- As a hardware designer, you should be able to explain how many logic cells

# Announcements/Reminders