Lab 3 Specifications

Lab-specific Specifications

Proficiency

\Box Circuit correctly reads inputs from 4×4 keypad.	
\square Dual seven-segment display shows the last two hexadecimal digits p	pressed.
\square Most recent numeric entry is shown on the right.	
□ Design does not lock up when multiple buttons are pressed at once the current values on the display and functions properly again where released.)	
☐ Design only registers first button press if additional buttons are holding down one button.	pressed down while
☐ Each button press registered only once (e.g., no switch bouncing)	
$\hfill \square$ Seven segment displays are same brightness regardless of how many nated.	segments are illumi-
\square Design has no latches.	
\square Design has no tristate buffers.	
\square Report includes state transition diagram illustrating the operation	of the system.
Excellence	
☐ Design uses synchronizers on asynchronous inputs to mitigate meta	stability.
☐ Keypad and seven-segment display are aligned in the same orienta the numbers on both are facing the same direction).	_
☐ State transition diagram is completely specified (i.e., all transitions specified, output conditions specified in each state)	s between states are
☐ Report includes state transition table to document the next tate are each state based on the current state and inputs.	ad output values for
\square Report explains tradeoffs between the chosen design decisions and al	ternatives (e.g., why
did you select a certain switch debouncing strategy and what are the	ne tradeoffs between
your chosen method and others?).	

General Specifications

Schematic Specifications

Proficiency
 □ All pin names labeled □ All pin numbers labeled □ Crossing wires clearly identified as junction or unconnected □ Neat layout (e.g., clear organization and spacing) □ All parts labeled with part number □ All component values present
Block Diagram
\Box Block diagram present with one block per System Verilog module \Box Each block includes all input and output signals
Excellence
General Schematic Specifications
 □ Standard symbols used for all components where applicable □ Signals "flow" from left to right where possible (e.g., inputs on left hand side, outputs on right hand side) □ Title block with author name, title, and date
HDL & Code Specifications
Proficiency
 □ Descriptive filename that matches module name (e.g., lab2_jb.sv) □ One module per file □ Descriptive variable names □ Neat formatting (e.g., standard indentation, consistent formatting for variable names (kebab-case/snake_case/camelCase/PascalCase)) □ Descriptive and clear function/module names □ Comments to indicate the purpose of each function/module

Excellence
\square Name, email, and date at the top of every file
\square Comment at the top of each source code file to describe what is in it
□ Clear and organized hierarchy (e.g., delineation between top level modules and submodules)
☐ Testbenches written for each individual module to demonstrate proper operation
\square Testbench output for each module included in the report
Writeup/Summary
Proficiency and Excellence
☐ Statement of whether the design meets all the requirements. If not, list the shortcomings.
□ Number of hours spent working on the lab are included.
□ Writeup contains minimal spelling or grammar issues and any errors do not significantly detract from clarity of the writeup.

□ (Optional) List comments or suggestions on what was particularly good about the as-

Comments

Add specific notes here about the assignment.

 \square AI prototype attempted and some reflection is recorded.

signment or what you think needs to change in future versions.