

Hardware released under CERN OHL version 1.2  
<http://www.ohwr.org/projects/cernohl/wiki>

Changed by HMLAB under CERN OHL version 1.2  
<http://www.hm-lab.com/hm-core>

Name: <b>HM-CORE</b>			OPEN SOURCE HARDWARE Designed by Trenz Electronic and changed by HMLAB For more information, please visit: <a href="http://www.hm-lab.com/hm-core">www.hm-lab.com/hm-core</a>
Size: <b>A4</b>	Number:	Revision: <b>A</b>	
Date: <b>4/1/2018</b>	Time: <b>3:48:09</b>	Sheet <b>1</b> of <b>12</b>	

U1A

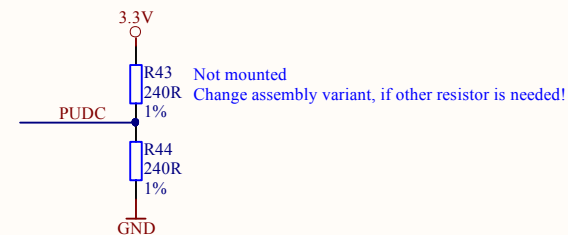
**BANK 34**

IO_L1P_T0_34	G11	AMUX_S1	Analog MUX
IO_L1N_T0_34	H12	AMUX_S2	Analog MUX
IO_L2P_T0_34	G12	AMUX_S0	Analog MUX
IO_L2N_T0_34	H13	BDBUS0	FTDI PORT B
IO_L3P_T0_DQS_PUDC_B_34	G14		PUDC
IO_L3N_T0_DQS_34	H14	BDBUS1	FTDI PORT B
IO_L4P_T0_34	I15	BDBUS2	FTDI PORT B
IO_L4N_T0_34	K15	BDBUS4	FTDI PORT B
IO_L5P_T0_34	I13	B34_L5_P	NC
IO_L5N_T0_34	I14	BDBUS3	FTDI PORT B
IO_L6P_T0_34	H11	FPGA_LED	FPGA LED
IO_L6N_T0_VREF_34	I11	B34_L6_N	NC
IO_L7P_T1_34	N13	BCBUS3	FTDI PORT B
IO_L7N_T1_34	N14	BCBUS1	FTDI PORT B
IO_L8P_T1_34	L15	BDBUS5	FTDI PORT B
IO_L8N_T1_34	M15	BDBUS7	FTDI PORT B
IO_L9P_T1_DQS_34	L14	BDBUS6	FTDI PORT B
IO_L9N_T1_DQS_34	M14	BCBUS0	FTDI PORT B
IO_L10P_T1_34	K13		NC
IO_L10N_T1_34	L13		NC
IO_L11P_T1_SRCC_34	K11		NC
IO_L11N_T1_SRCC_34	K12		NC
IO_L12P_T1_MRCC_34	L12		NC
IO_L12N_T1_MRCC_34	M12	B34_L12_N	NC
IO_L13P_T2_MRCC_34	N11	RXD	DIGITAL HEADER
IO_L13N_T2_MRCC_34	N12	D2	DIGITAL HEADER
IO_L13N_T2_MRCC_34	P15	BCBUS2	FTDI PORT B
IO_L15P_T2_DQS_34	R15	BCBUS4	FTDI PORT B
IO_L15N_T2_DQS_34	P11	D12	DIGITAL HEADER
IO_L16P_T2_34	R11	D11	DIGITAL HEADER
IO_L16N_T2_34	R12	D13	DIGITAL HEADER
IO_L17P_T2_34	R13	SDA	DIGITAL HEADER
IO_L17N_T2_34	P13	SCL	DIGITAL HEADER
IO_L18P_T2_34	P14	BCBUS7	FTDI PORT B
IO_L18N_T2_34	M9	B34_L19_P	NC
IO_L19P_T3_34	N9	B34_L19_N	NC
IO_L19N_T3_VREF_34	R7	D4	DIGITAL HEADER
IO_L20P_T3_34	R8	D6	DIGITAL HEADER
IO_L20N_T3_34	M10	B34_L21_P	NC
IO_L21P_T3_DQS_34	M11	TXD	DIGITAL HEADER
IO_L21N_T3_DQS_34	N7	D3	DIGITAL HEADER
IO_L22P_T3_34	N8	D7	DIGITAL HEADER
IO_L22N_T3_34	P8	D5	DIGITAL HEADER
IO_L23P_T3_34	P9	D8	DIGITAL HEADER
IO_L23N_T3_34	P10	D10	DIGITAL HEADER
IO_L24P_T3_34	R10	D9	DIGITAL HEADER
IO_L24N_T3_34			

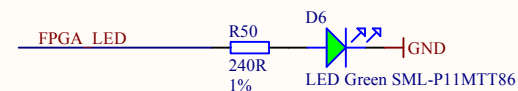
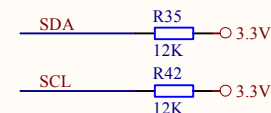
XC7Z7010-CLG225

B34

①



Not mounted

Name: **HM-CORE FPGA B34**Size: **A4**

Number:

Revision: **A**

Date: 4/1/2018

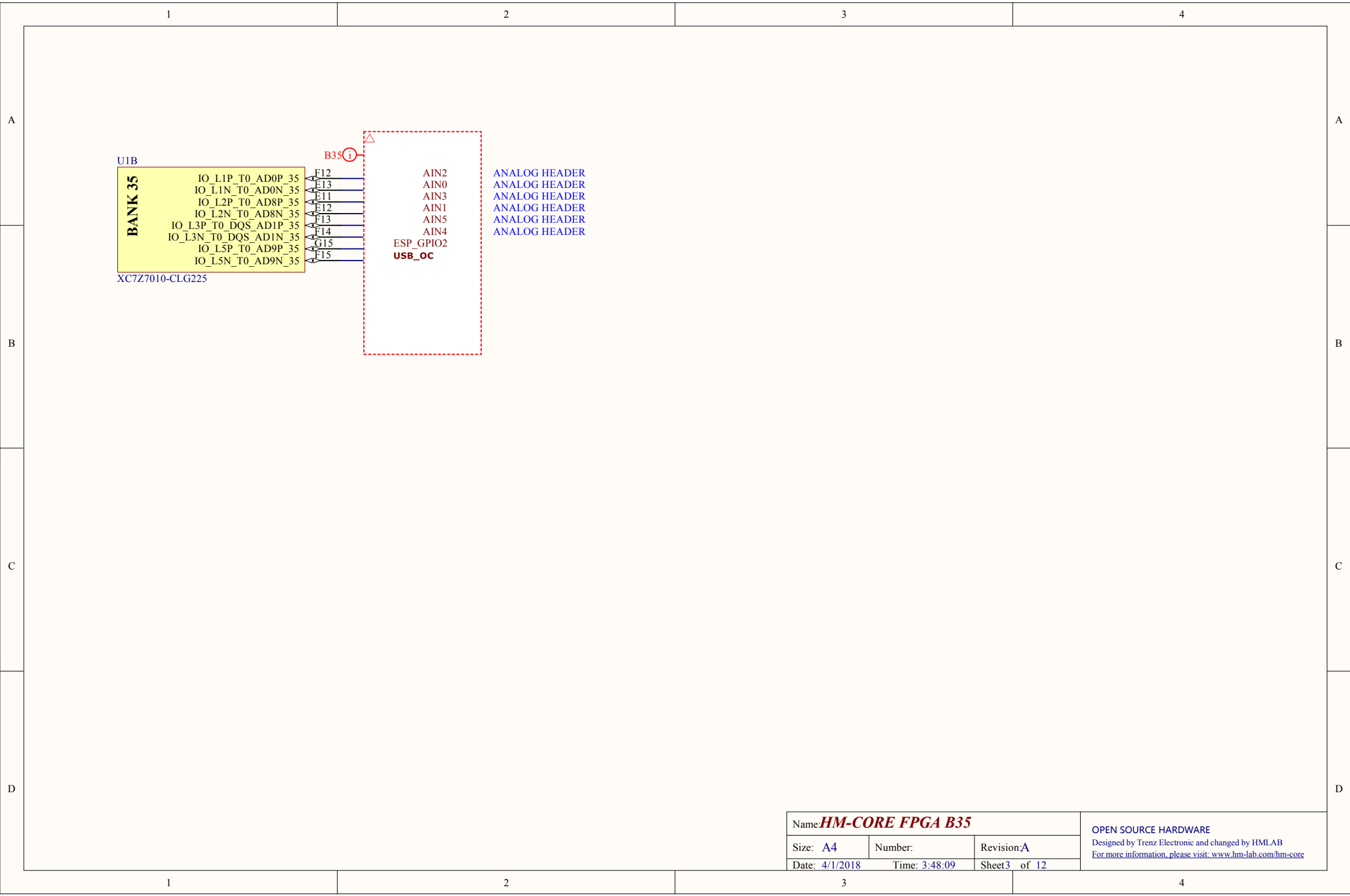
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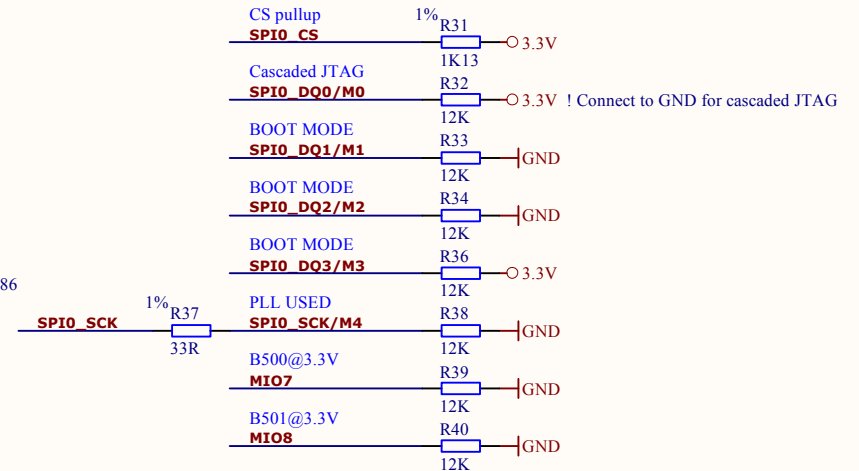
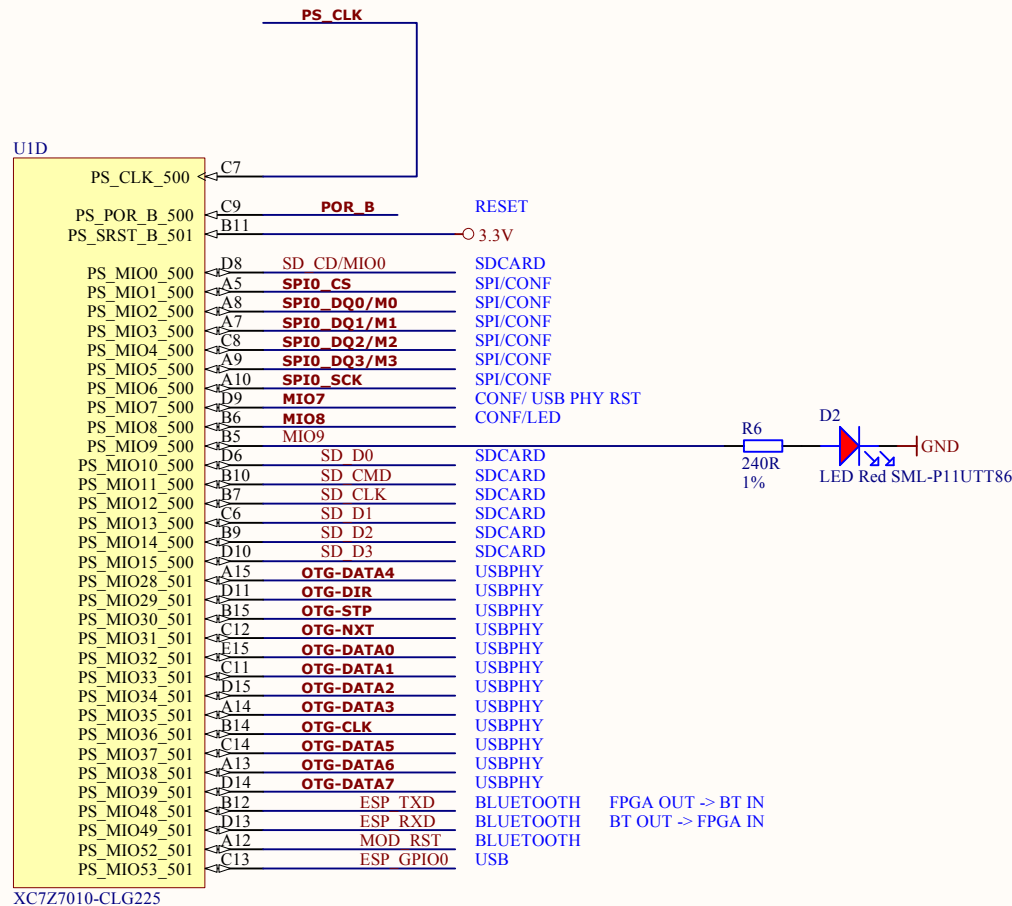
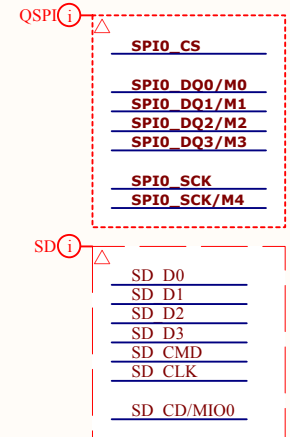
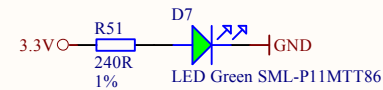
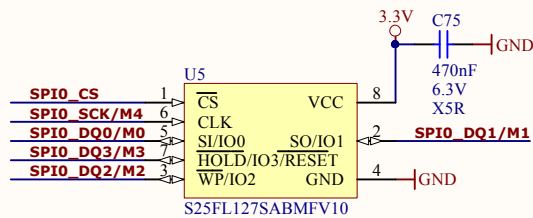
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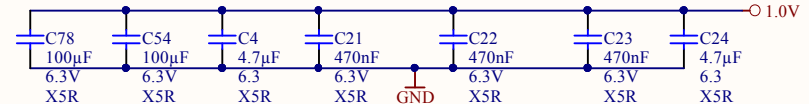
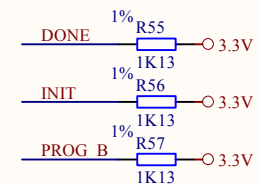
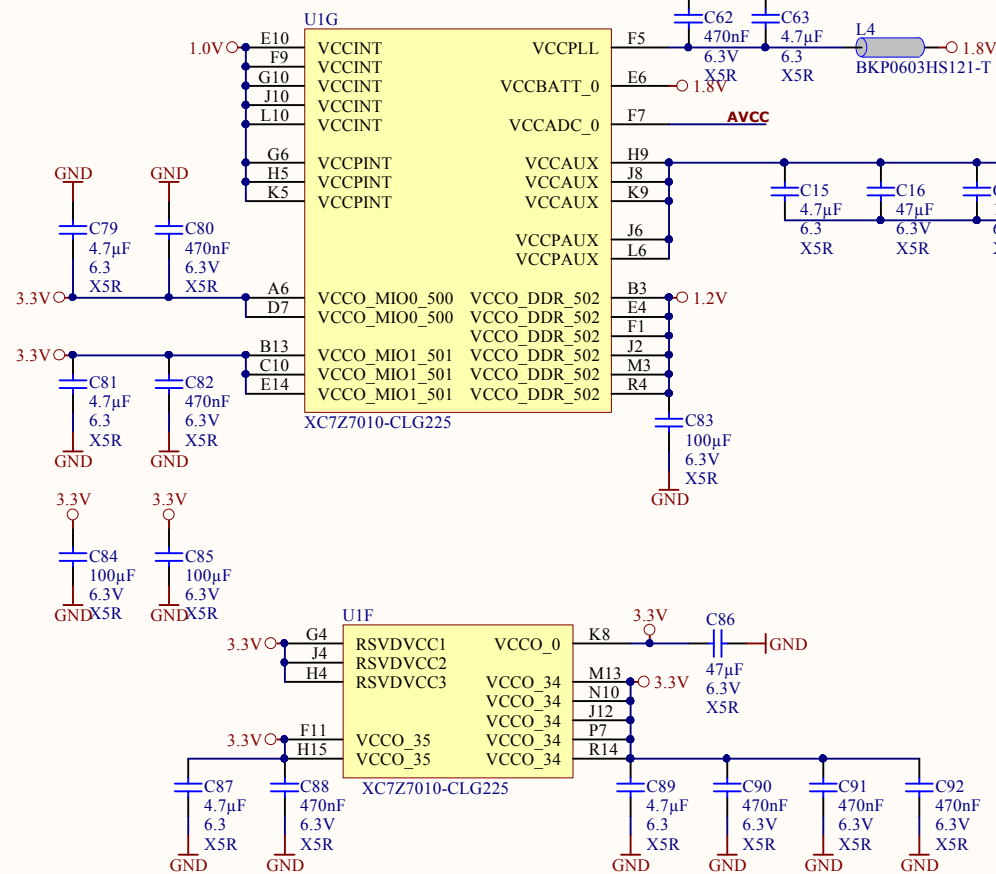
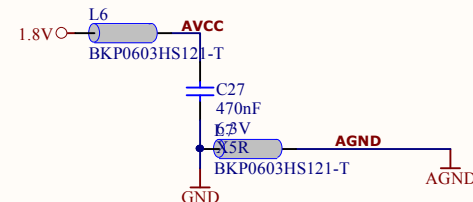
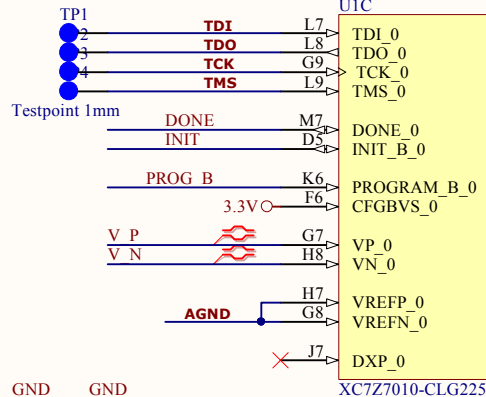
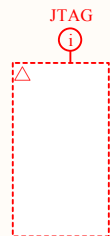
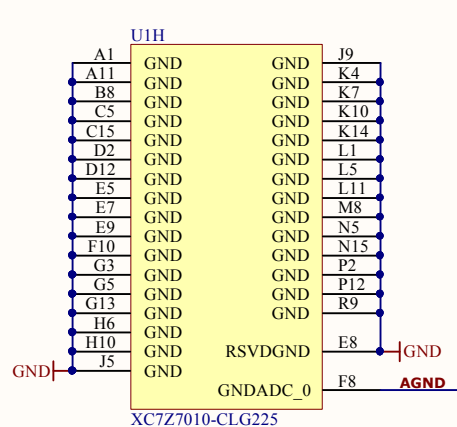
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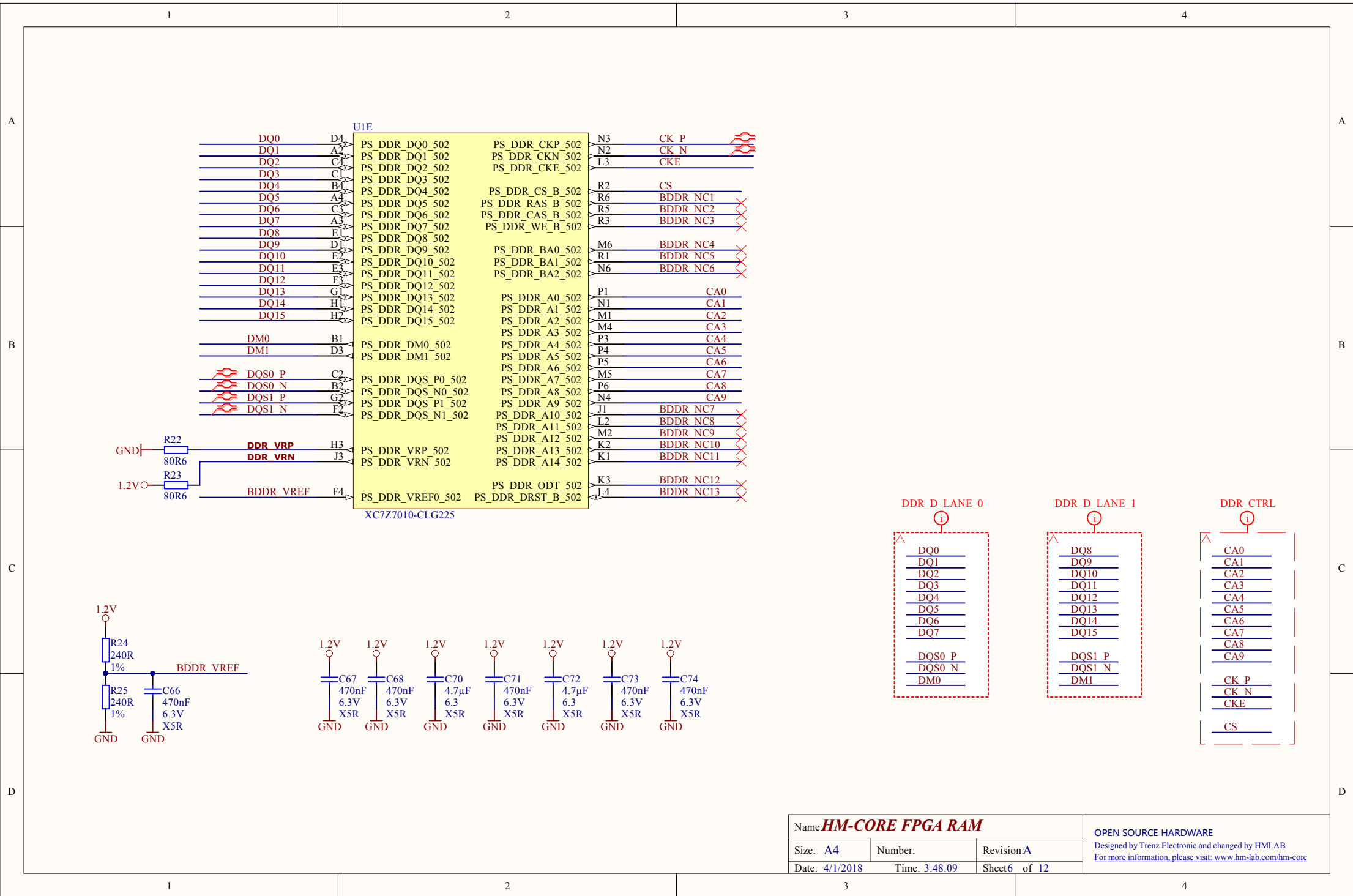




Name: <i><b>HM-CORE FPGA MIO</b></i>			OPEN SOURCE HARDWARE Designed by Trenz Electronic and changed by HMLAB <u>For more information, please visit: <a href="http://www.hm-lab.com/hm-core">www.hm-lab.com/hm-core</a></u>
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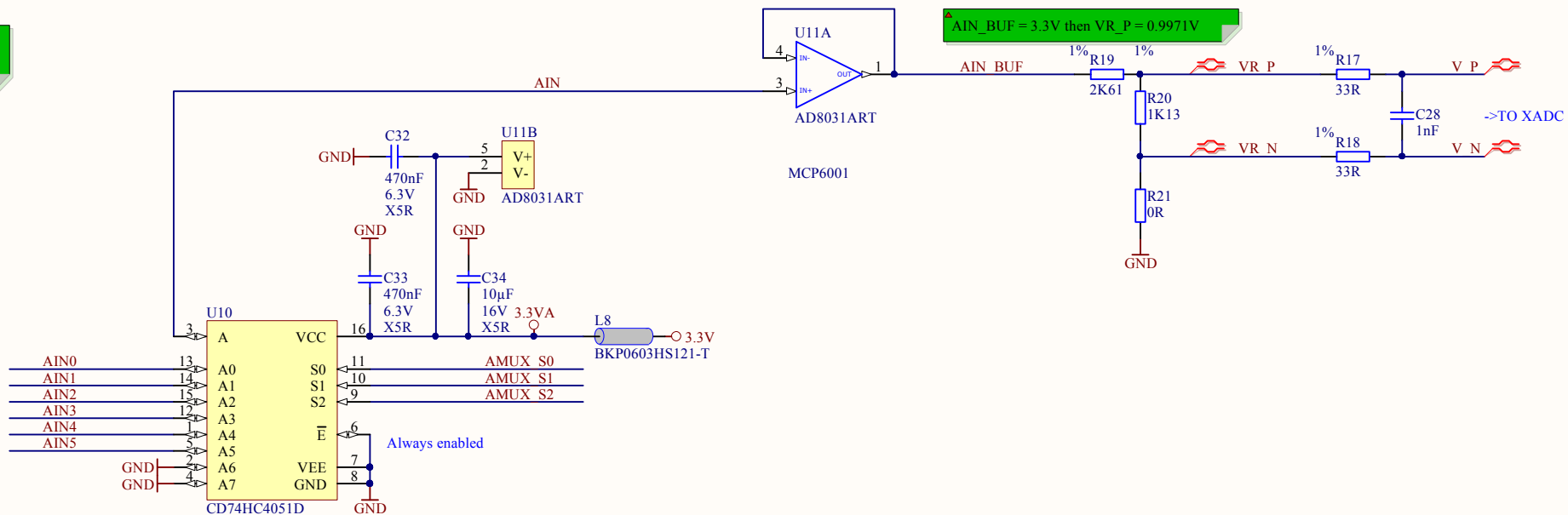


Name: <b>HM-CORE FPGA PWR</b>			OPEN SOURCE HARDWARE Designed by Trenz Electronic and changed by HMLAB For more information, please visit: <a href="http://www.hm-lab.com/hm-core">www.hm-lab.com/hm-core</a>
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Default:  
 \* AMUX disabled  
 \* Digital buffers disabled

->FROM AD HEADER



Name: **HM-CORE Analog Input**

Size: **A4**

Number:

Revision: **A**

Date: **4/1/2018**

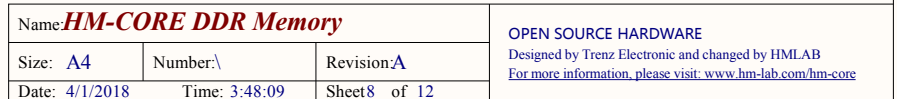
Time: **3:48:09**

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A

B

C

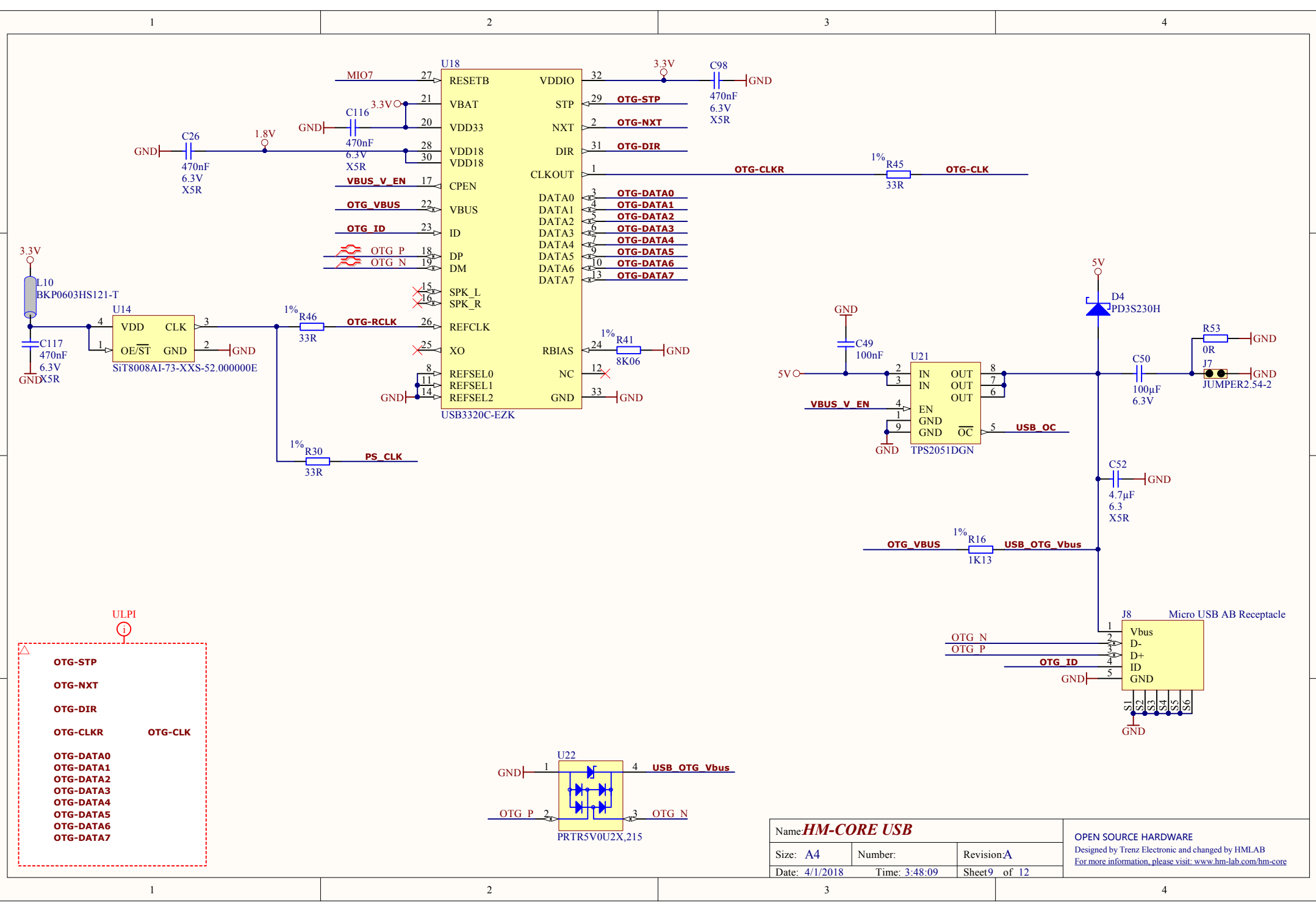
D

A

B

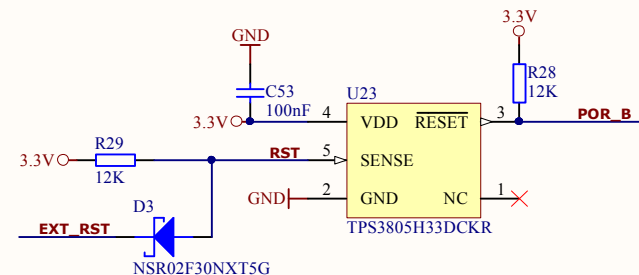
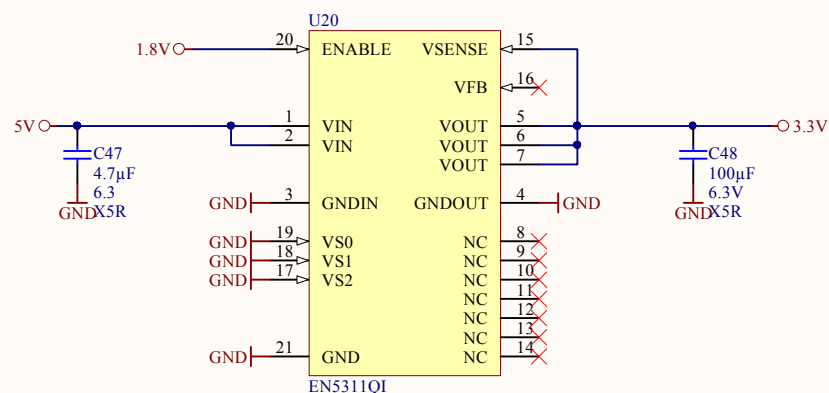
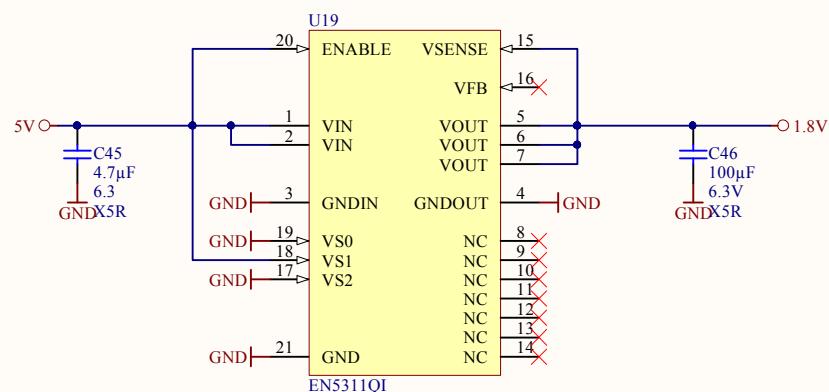
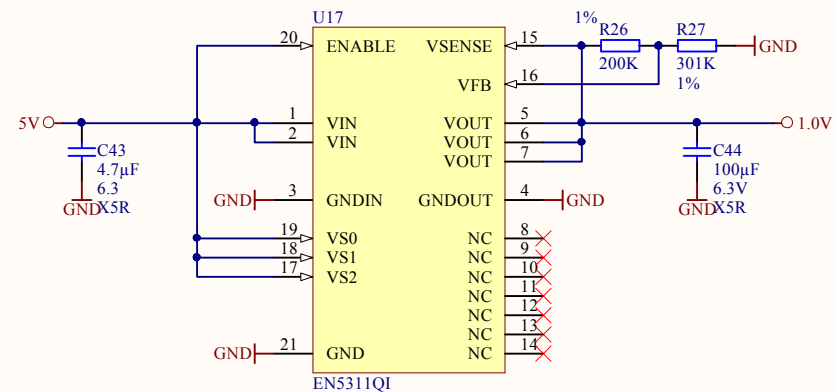
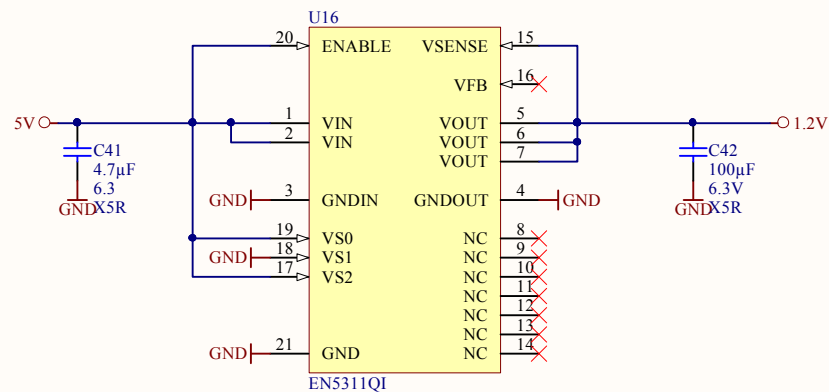
C

D



Name: <b><i>HM-CORE USB</i></b>			OPEN SOURCE HARDWARE Designed by Trenz Electronic and changed by HMLAB <u>For more information, please visit: <a href="http://www.hm-lab.com/hm-core">www.hm-lab.com/hm-core</a></u>
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Name: **HM-CORE PowerSupply**

Size: **A4**

Number:

Revision: **A**

Date: 4/1/2018

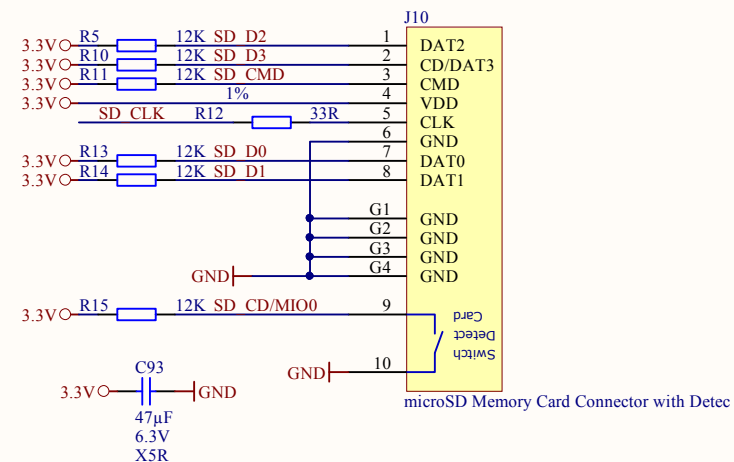
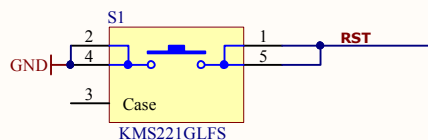
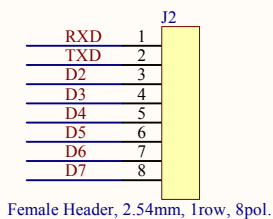
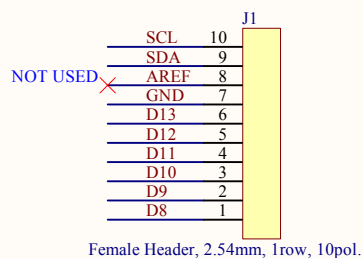
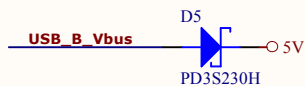
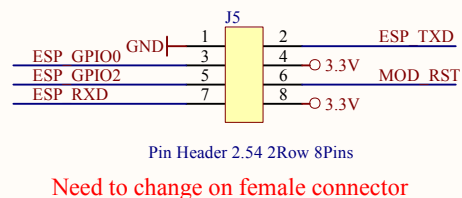
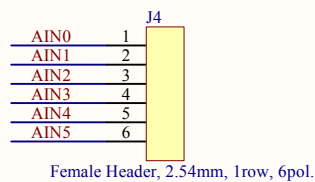
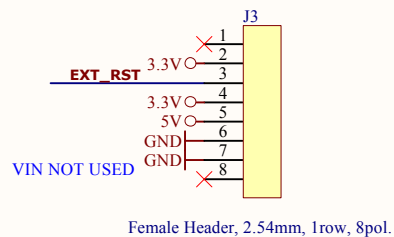
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Name: <i>HM-CORE Connectors</i>			OPEN SOURCE HARDWARE Designed by Trenz Electronic and changed by HMLAB <a href="http://www.hm-lab.com/hm-core">For more information, please visit: www.hm-lab.com/hm-core</a>
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