CMOSTEK CMT2281F2

240 – 960 MHz SoC OOK Receiver

Features

- High-Performance RISC CPU
  - PIC16-like Instruction-set
  - Only 37 instructions to learn:
    - All Single-Cycle Except Branches
  - Operating speed:
    - Up to 16 MHz Clock
    - 125nsinstruction cycle
    - F_{SYS} = 8MHz @ 2.0V~5.0V
    - F_{SYS} = 16MHz @ 2.7V~5.0V
  - Interrupt capability
  - 8-level deep hardware stack
  - 2048 Words Flash / 128B SRAM / 256B EEPROM
  - 2 x 8-bit timers/counters with programmable prescaler
  - 8 I/O pins with individual direction control:
    - Interrupt-on-pin change
    - Individually programmable weak pull-ups
    - Push-pull output except PA5
- High-Performance OOK Receiver
  - All Features Configurable
  - Frequency Range: 300 to 960 MHz
  - OOK Modulation
  - Symbol Rate up to 40 kbps
  - Sensitivity: -109 dBm @ 3kbps, 0.1%BER
  - Maximum input signal: +10 dBm
  - Image rejection ratio: 30dB
  - Receive bandwidth: 120/240/330/400KHz(option)
- Supply Voltage:
  - 2.0 to 3.6 V or 3.0 to 5.0 V
- FCC / ETSI Compliant
- RoHS Compliant
- 16-pin SOP Package

Applications

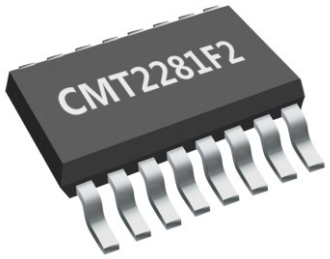
- Remote Keyless Entry (RKE)
- Garage and gate door openers
- Home/Building Automation and Security
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Consumer Electronics Applications

Descriptions

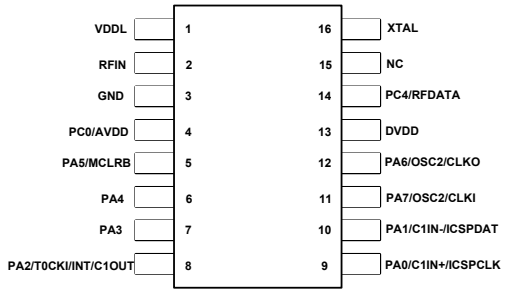
The CMT2281F2 devices are fully integrated, highly flexible, high performance, SoC OOK receiver with embedded RISC microcontroller core for various 300 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The CMT2281F2 uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the BOM counts. The device sensitivity is up to -109 dBm. The device operates from 2.0 V to 5.0 V. Its low power design enables superior operation life for battery powered application. The CMT2281F2 receiver together with CMOSTEK NextGenRF™ transmitter enables a highly flexible, low cost RF link.

Ordering Information

Part Number	Frequency	Package Option	MOQ
CMT2281F2-ESR	433.92 MHz	T&R	2,500 pcs
CMT2281F2-ESB	433.92 MHz	Tube	1,000 pcs
More Ordering Info: See Page 25			



SOP16



CMT2281F2

Typical Application

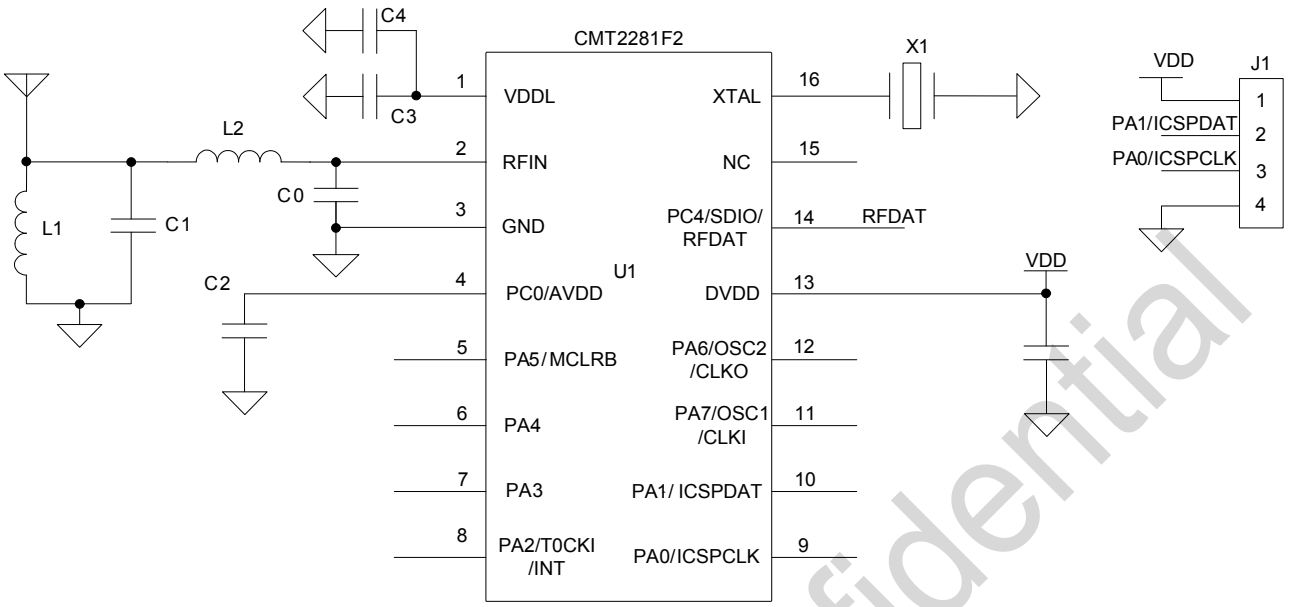


Figure 1. CMT2281F2 Typical Application

Note:

1. When Pin4 and Pin1 are open-circuit, supply voltage range is 3.0 to 5.0 V.
2. When Pin4 and Pin1 are short-circuit, supply voltage range is 2.0 to 3.6 V.

Table 1.BOM of 315/433.92 MHz Application

Designator	Descriptions	Value 315MHz	Value 433.92MHz	Unit	Manufacturer
U1	CMT2281F2, 240 – 960 MHz SoC OOK Receiver		-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	19.7029	27.1412	MHz	EPSON
L1	±10%, 0603 multi-layer chip inductor	62	36	nH	Sunlord
L2	±10%, 0603 multi-layer chip inductor	68	36	nH	Sunlord
C0	±0.25 pF, 0402 NP0, 50 V	3	3	pF	
C1	±0.25 pF, 0402 NP0, 50 V	12	10	pF	
C2	±20%, 0603 X7R, 25 V	0.1		uF	
C3	±0.25 pF, 0603 NP0, 50 V	470		pF	
C4	±20%, 0603 X7R, 25 V	0.1		uF	
C5	±20%, 0603 X7R, 25 V	4.7		uF	

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
BW	Bandwidth
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
GFSK	Gauss Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
LDO	Low Drop-Out
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PN	Phase Noise
RBW	Resolution Bandwidth
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
TBD	To Be Determined
Tx	Transmission, Transmitter
Typ	Typical
XO/XOSC	Crystal Oscillator
XTAL	Crystal

Table of Contents

1. Electrical Characteristics

When V_{DD} = 5.0 V, T_{OP} = 25 ℃, F_{RF} = 433.92 MHz, OOK modulation, the sensitivity is measured by receiving a PN9 sequence and matching to 50Ω according to the 0.1%BER standard.

1.1 Recommended Operating Conditions

Table 2. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}	When the Pin1 and Pin4 are open-circuit	3.0		5.5	V
		When the Pin1 and Pin4 are short-circuit	2.0		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

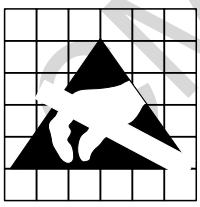
1.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}	Pin1 and Pin4 are open-circuit	-0.3	5.5	V
		Pin1 and Pin4 are short-circuit	-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} +0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Receiver Specifications

Table 4. Receiver Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range	F_{RF}	F_{XTAL} = 19.7029MHz		315		MHz
		F_{XTAL} = 27.1412MHz		433.92		MHz
		See “AN200 CMT2281F2 User Guide”	300		960	MHz
Symbol Rate	SR	OOK	0.5		40	ksps
Sensitivity	S_{315}	F_{RF} = 315 MHz, DR = 3 kbps, BER = 0.1%		-109		dBm
	$S_{433.92}$	F_{RF} = 433.92 MHz, DR = 3 kbps, BER = 0.1%		-109		dBm
Saturation input signal level	P_{LVL}			10		dBm
Working current	I_{DD315}	F_{RF} = 315 MHz, RF only, MCU Sleep		4.2		mA
	$I_{DD433.92}$	F_{RF} = 433.92 MHz, RF only, MCU Sleep		4.5		mA
Sleep Current	I_{SLEEP}	See “AN200 CMT2281F2 User Guide”	155		655	uA
Power Off Current	I_{SHUT}	PC0/AVDD = 0(Output), MCU Sleep		1		uA
Frequency synthesizer settle time	T_{LOCK}	Start from XOSC stability		150		us
Anti blocking	BI	±1 MHz, continuous wave interference		32		dBm
		±2 MHz, continuous wave interference		42		
		±10 MHz, continuous wave interference		61		dBm
Input 3rd order intercept point	IIP3	FDEV = 1 MHz and 2 MHz double tone test, maximum system gain setting		-23		dBm
Receiver bandwidth	BW_{315}	F_{RF} = 315 MHz		240		kHz
	$BW_{433.92}$	F_{RF} = 433.92 MHz		330		kHz
Receiver startup time [1]	$T_{START-UP}$	From power up to receiving		4.5+T_{XTAL}		ms

Notes:

[1.]T_{XTAL} is the oscillation time of crystal, which is related to the crystal itself and has nothing to do with the chip.

1.4 RF Crystal Oscillator

Table 5. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency	$F_{XTAL315}$			26.25		MHz
	$F_{XTAL433.92}$			26.2982		MHz
	$F_{XTAL868}$			26.303		MHz
Crystal Tolerance[1]				±20		ppm
Load Capacitance	C_{LOAD}			15		pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[2]	t_{XTAL}			400		us

Notes:

[1]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[2]. This parameter is to a large degree crystal dependent.

1.5 Internal High Frequency Oscillator

Table 6. IHRC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
IHRC Frequency	F_{IHRC}	3.3V, 27℃		15.99		MHz
Temperature-dependent		-20℃~ +80℃, 3.3V		4.2%/100℃		
Voltage-dependent		2~3.6V		±3		%/V
Setup Time				2.2	10	us
Leakage Current				0.8	2	nA
Triming Range		Step 0.625%		±20%		

1.6 Internal Low Frequency Oscillator

The ILRC support two frequency: 32KHz or 256KHz. It can be selected by LFMOD in OSCCON register, 0 is the 32KHz, and the 1 is the 256KHz.

Table 7. ILRC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ILRC Frequency	F_{ILRC}	2.5V, 25℃, 32K		32.3		KHz
		2.5V, 25℃, 256K		258.5		KHz
Temperature-dependent		-20℃~ +80℃, 2.5V		22.3%/100℃		
Voltage-dependent		2~3.6V		±11.1		%/V
Setup Time		2.5V, 25℃		4.6	10	us
Leakage Current		Disable		0.15	1	nA

1.7 LVD/LVR

Table 8. LVD/LVR Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVD Voltage				2.0		V
				2.2		
				2.8		
LVR delay				125	157	us

1.8 POR

Table 9. POR Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POR Current	I_{POR}	3.3V		50		nA
Temperature-dependent		3.3V		2.0		V

1.9 I/O PAD

Table 10. I/OPAD Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage	VIL				0.3	VDD
Input High Voltage	VIH		0.7			VDD
Output High Current	I_{OH}	3.3V, 25℃		10		mA
Output Low Current	I_{OL}	3.3V, 25℃		15		mA
Weak Pull-up		3.3V		41.7		KΩ

1.10 MCU Supply Current

Table 11. Supply Current

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Mode		3.3V, F_{SYS} = 2MHz		310		uA
		3.3V, F_{SYS} = 32KHz		50		uA
Sleep Mode with WDT_ON		3.3V		3		uA
Sleep Mode with WDT_OFF		3.3V		0.8		uA
Sleep Mode with LVD_ON		3.3V		15		uA

Notes:
1. All the IO is input mode, and with pull-down resistance.
2.Comparator is disable, CM<2:0> = 111

2. Pin Descriptions

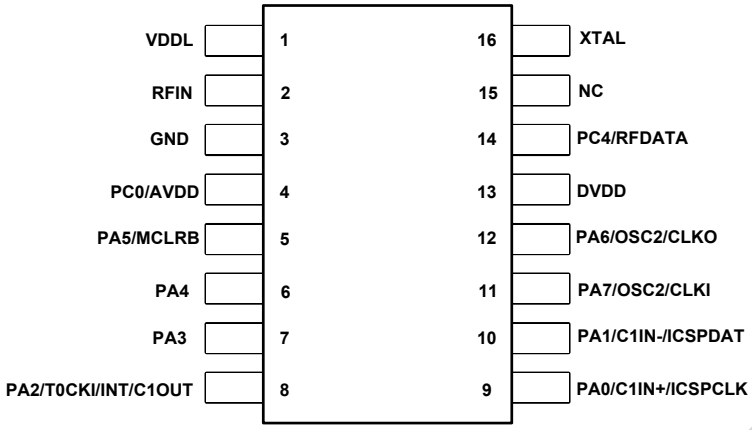


Figure 2. CMT2281F2 Pin Assignments

Table 12. CMT2281F2 Pin Descriptions

Pin Number	Name	I/O	Descriptions	
1	VDDL	O	RF power supply output	
2	RFIN	I	The RF signal is input to the LNA	
3	GND	I	Ground	
4	PC0/AVDD	IO	PC0	PORTC I/O
			AVDD	RF power supply input
5	PA5/MCLRB	I	PA5	PORTA input with pull-up and interrupt-on-change
			MCLRB	Master Clear w/internal pull-up
6	PA4	IO	PORTA I/O w/programmable pull-up and interrupt-on-change	
7	PA3	IO	PORTA I/O w/programmable pull-up and interrupt-on-change	
8	PA2/T0CKI/INT	IO	PA2	PORTA I/O w/programmable pull-up and interrupt-on-change
			T0CKI	Timer0 clock input
			INT	External Interrupt
9	PA0/ICSPCLK	IO	PA0	PORTA I/O w/programmable pull-up and interrupt-on-change
			ICSPCLK	Serial Programming and debugging Data I/O
10	PA1/ICSPDAT	IO	PA1	PORTA I/O w/programmable pull-up and interrupt-on-change
			ICSPDAT	Serial Programming and debugging Clock
11	PA7/OSC1/CLKI	IO	PA7	PORTA I/O w/programmable pull-up and interrupt-on-change
			OSC1	Crystal/Resonator
			CLKI	External clock input/RC oscillator connection
12	PA6/OSC2/CLKO	IO	PA6	PORTA I/O w/programmable pull-up and interrupt-on-change
			OSC2	Crystal/Resonator
			CLKO	Clock output
13	DVDD	I	MCU power supply input	
14	PC4/RFDAT	IO	PC4	PORTC I/O
			RFDAT	RF received signal data output
15	NC	--		
16	XTAL	I	single-ended crystal oscillator input or external reference clock input	

Pin Number	Name	I/O	Descriptions	
Internal pin	PC2/SCLK	IO	PC2	PORTC I/O
			SCLK	RF's serial interface clock input
	PC3/CSB	IO	PC3	PORTC I/O
			CSB	RF's serial interface select enable input

3. Typical Performance Characteristics

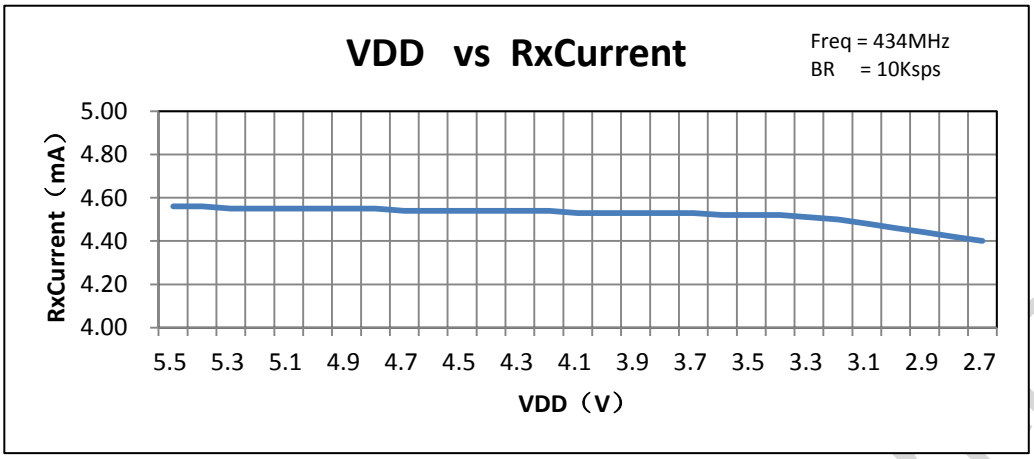


Figure 3. Rx Current vs. Supply Voltage

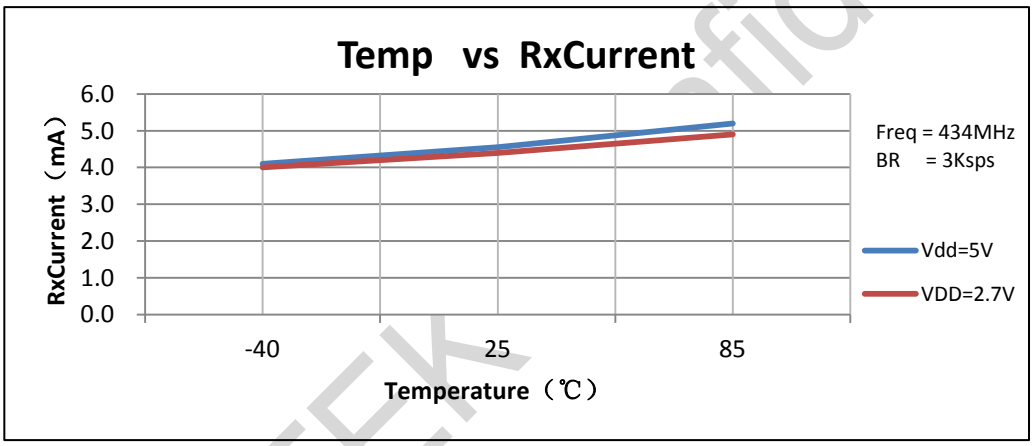


Figure 4. Rx Current vs. Working Temperature

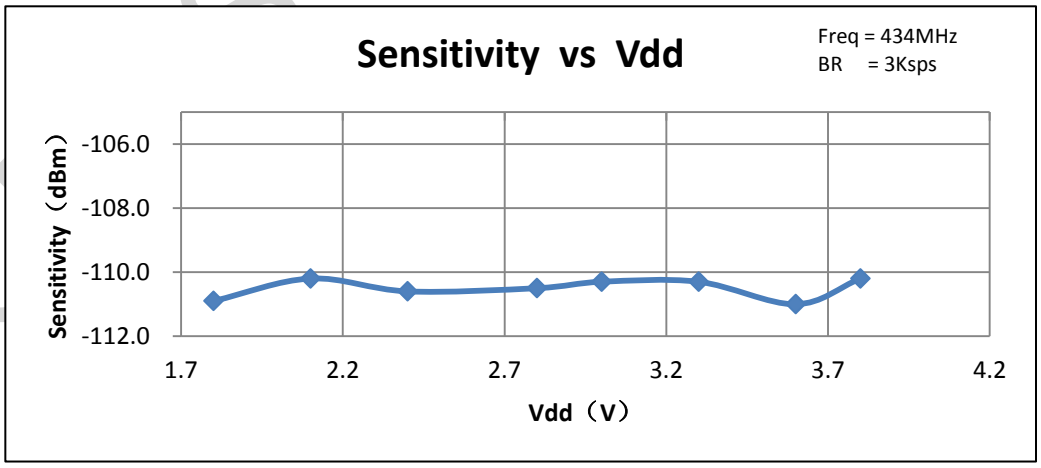


Figure 5. Sensitivity vs. Supply Voltage

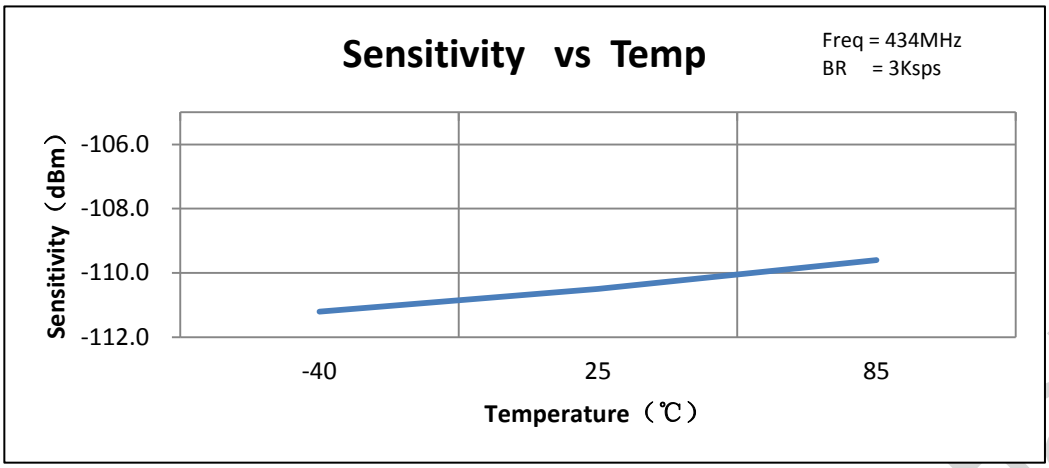


Figure 6. Sensitivity vs Working Temperature

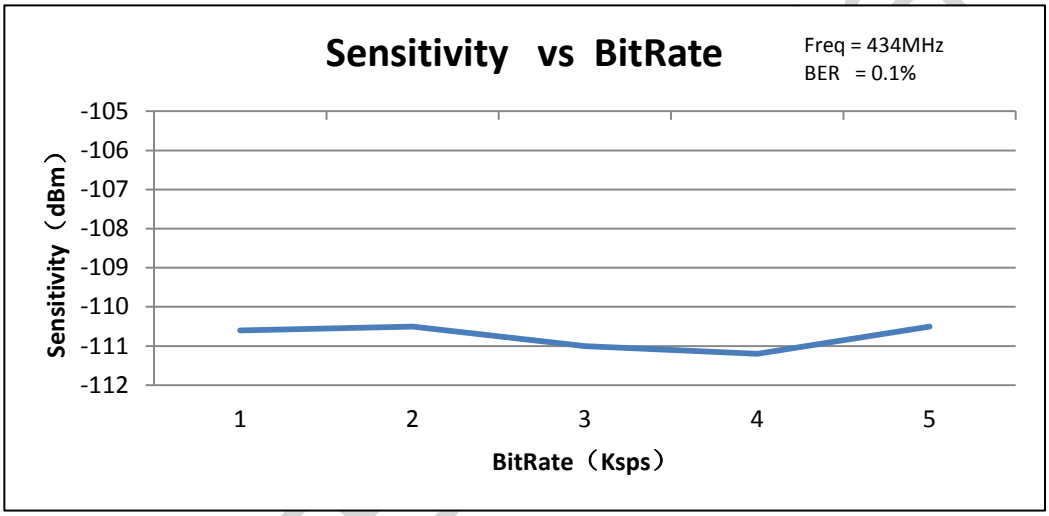


Figure 7. Sensitivity vs Bit Rate

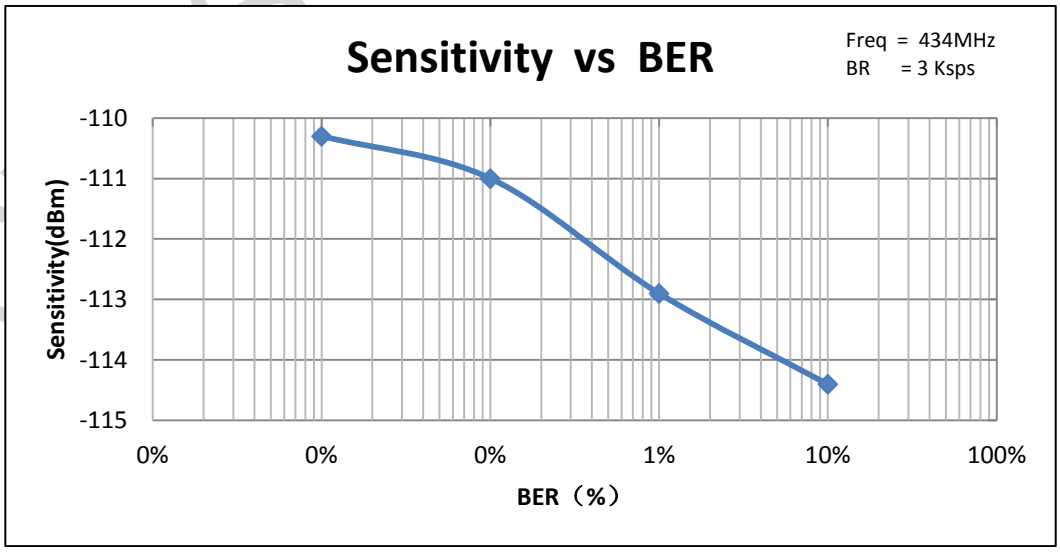


Figure 8. Sensitivity vs Bit Error Rate

4. Functional Descriptions

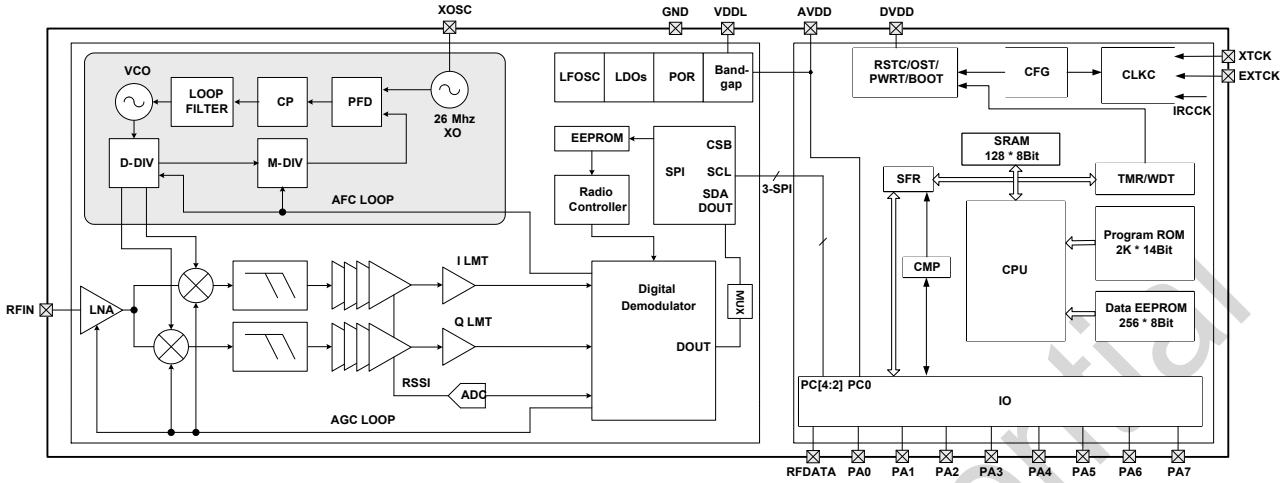


Figure 9. CMT2281F2 Functional Block Diagram

4.1 Overview

The CMT2281F2 devices are fully integrated, highly flexible, high performance, SoC OOK receiver with an embedded RISC microcontroller designed for various 240 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF^{TM} family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design. CMT2281F2 supports two kinds of voltage, which can be used in the application of 5V system, and also can be chosen as the application of 3V system.

The RF part of CMT2281F2 uses LNA+MIXER+IFFILTER+LIMITTER+PLL's low intermediate frequency structure to achieve the wireless reception function below Sub-1G frequency. The analog front-end is responsible for mixing RF signals into intermediate frequency, and converting the real time RSSI into the 8-bit digital signal through SAR-ADC, and sending them to the interior to do the OOK demodulation and correlation processing. At the same time, the internal circuit will mix the intermediate frequency signal down to the zero frequency (Baseband) and do a series of filtering and judging process, while AGC dynamically control the analog front-end. Finally, the original signal is demodulated and output through the DATA pin(Pin14 PC4/RFDAT).

The RISC microcontroller has 2048-word flash program space. Up to 8 I/O are supported with their functions customized by the user program. RF Frequency, Bandwidth, Symbol Rate and other product features can be programmed into the registers. This saves the cost and simplifies the product development and manufacturing effort. Alternatively, in stock products of 433.92 MHz is available for immediate demands. The CMT2281F2 can operates from 3.0 to 5.0V, as well as operates from 2.0 to 3.6V, depended on Pin1 and Pin4 are open-circuit or short-circuit. The device together with CMOSTEK NextGenRF^{TM} receiver enables a highly flexible, low cost RF link.

4.2 Demodulation, Frequency and Symbol Rate

The CMT2281F2 supports OOK demodulation with the symbol rate up to 40 kbps. The CMT2281F2 continuously covers the frequency range from 300 to 960 MHz, including the license free ISM frequency band around 315 MHz, 433.92 MHz, 868.35 MHz and 915 MHz.

Table 13. Demodulation, Frequency and Symbol Rate

Parameter	Value	Unit
Demodulation	OOK	-
Frequency	300 to 960	MHz
OOK Symbol Rate	0.5 to 40	kbps

4.3 RF Front-end and Automatic Gain Control

CMT2281F2 is an OOK modulated receiver with the low intermediate frequency architecture. The receiver's RF front-end consists of a low noise amplifier (LNA), an I/Q mixer (Mixer), an intermediate frequency filter (IF Filter), and a wideband power detector (WB Power Detector). The RF front-end amplifies and converts the RF input signals from the antenna to the intermediate frequency for the further processing.

With the help of the broadband power detector and RF attenuation network of RF front-end, the automatic gain control (AGC) loop can adjust the RF front-end gain. The chip can also achieve the best system linearity, selectivity and sensitivity even under the condition of strong interference outside the band.

With only one low-cost matching circuit, the LNA input can be matched to 50Ω or other types of antennas.

4.4 Intermediate Frequency (IF) Filter

The signal from the RF front-end is filtered by an integrated 3rd order band pass image rejection filter. When the device operates at 433.92 MHz, the intermediate frequency bandwidth is 330 kHz. The center frequency and bandwidth will be adjusted automatically according to the selected crystal frequency.

4.5 Received Signal Strength Indicator

The output signal of the IF filter is amplified by the cascade I/Q logarithmic amplifier, and then sent to the demodulator for demodulation. I/Q dual logarithmic amplifiers include the received signal strength indicator (RSSI). The indicator generates the DC level in proportion to the input signal level within the I/Q path. The sum of levels of these two paths is used as an indication of the received signal strength, with a dynamic range of more than 66dB.

4.6 Successive Approximation Register

The 8-bit SAR-ADC in the RF part of CMT2281F2 transforms the RSSI output into the digital signal for OOK demodulation.

4.7 Crystal Oscillator

CMT2281F2 uses a single ended crystal oscillator circuit with the required load capacitance integrated within the chip. The recommended crystal is 19.7029MHz/27.1412MHz, with an accuracy of + 20 ppm, an equivalent resistance (ESR) <60 and a load capacitance (CLOAD) of 15pF. In order to save the external load capacitance, the load capacitance required by the crystal oscillation is integrated in the CMT2281F2 chip.

If there is a suitable clock source (RCLK) in the application system, which can be used as the reference clock of CMT2281F2, the user can drive the XTAL pin of the chip through the DC blocking capacitor. This will save one crystal and further reduce the system cost. The recommended RCLK peak to peak value is between 0.3V to 0.7V (at the XTAL pin).

4.8 Frequency Synthesizer

The frequency synthesizer is used to generate the local oscillator (LO) frequency required for the I/Q mixer. By the 19.7029 MHz or 27.1412 MHz reference clock provided by a crystal or external clock source, the frequency synthesizer can generate the 315MHz/433.92MHz working frequency. The internal high performance VCO operates at the 2 x LO frequency without the external inductor. The chip can work stably in various conditions when it is powered up, and further save the system power consumption and stray radiation.

For more the detail about how to use CMT2281F2, please see “AN200 CMT2281F2 User Guide”.

5. RISC Microcontroller Core

The embedded high-performance RISC Microcontroller has the following features:

High-Performance RISC CPU

- 2048 words Flash ROM, 128B SRAM
- 256B EEPROM
- All single-cycle instructions except branches
- Operating Speed
  - DC - 16MHz oscillator
  - 125 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Multiplexed MCLRB/Input Pin

Peripheral Features

- 8 I/O Pins
  - Individual Direction Control
  - Interrupt-on-Pin Change
  - Individual Programmable Weak Pull-ups
- Timer0: 8-bit timer with 3-bit prescaler
- Timer2: 8-bit timer with 3-bit prescaler
- Watchdog timer with on-chip RC oscillator

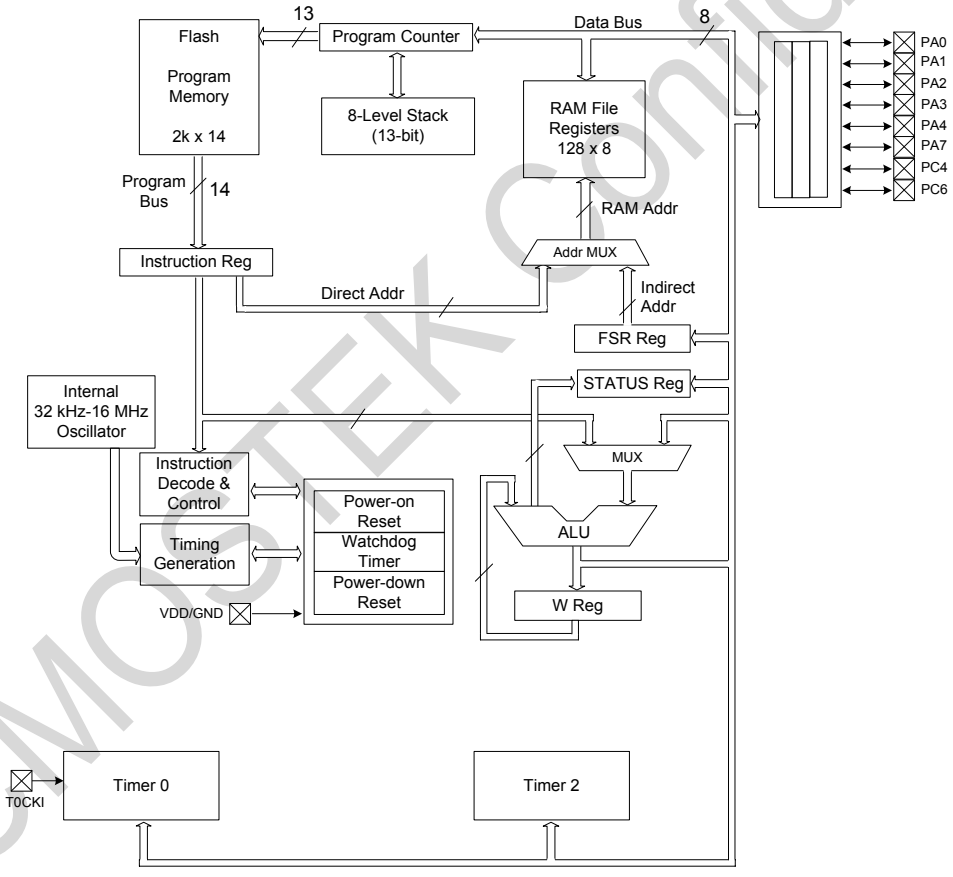


Figure 10. Microcontroller Core Block Diagram

5.1 Memory Organization

5.1.1 Program Memory Organization

The CMT2281F2 device has 2k x 14 (0000h-07FFh) space for program memory. Accessing a location above these boundaries will cause a wrap-around within the first 2k x 14 space. The Reset Vector is at 0000h and the Interrupt Vector is at 0004h (see figure below).

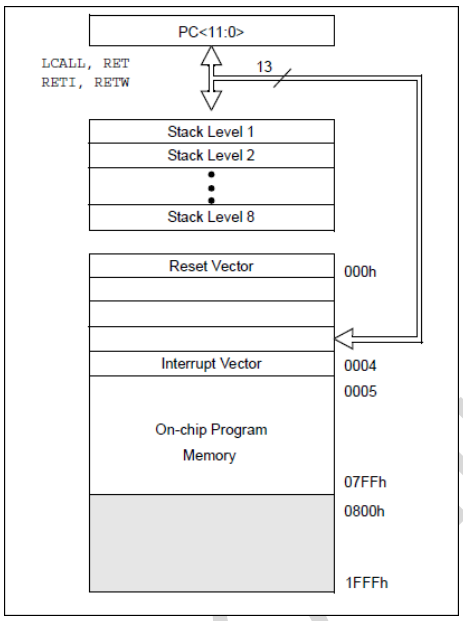


Figure 112. Program Memory Map and Stack

5.1.2 Data Memory Organization

The data memory (see figure 11) is partitioned into two banks: The General-Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when being read. PAGE(STATUS<5>) is the bank select bit.

- PAGE0 = 0 Bank 0 is selected.
- PAGE0 = 1 Bank 1 is selected.

5.1.2.1 General Purpose Register File

The register file is organized as 64 x 8 in the CMT2281F2. Each register is accessed, either directly or indirectly, through the FSR.

5.1.2.2 Special Function Register File

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device. These registers are static RAM. The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

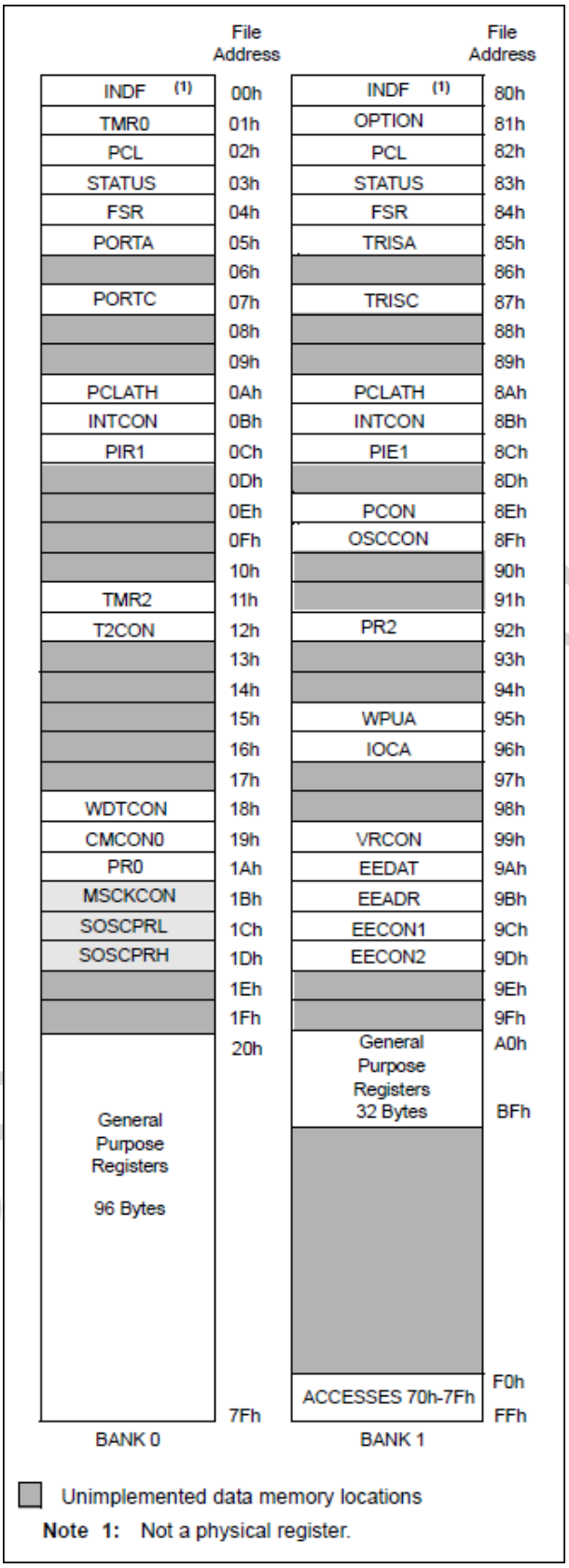


Figure 123. Data Memory Map of the CMT2281F2

Table 14. CMT2281F2 Special Registers Summary Bank0

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
0	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
1	TMR0	Timer0 Module's register, Timer0<7:0>								xxxx xxxx
2	PCL	Program Counter's (PC) Least Significant Byte, PC<7:0>								0000 0000
3	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
4	FSR	Indirect Data Memory Address Pointer								
5	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00x0 0000
6										---- ----
7	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	0000 0000
8										---- ----
9										---- ----
A	PCLATH	-	-	-	Write Buffer for upper 5 bits of Program Counter, PC<13:8>					---0 0000
B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-	00-0 000-
D										---- ----
E										---- ----
F										---- ----
10										---- ----
11	TMR2	Timer2 Module register, Timer2<7:0>								0000 0000
12	T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000
13										---- ----
14										---- ----
15										---- ----
16										---- ----
17										---- ----
18	WDTCON	-	-	-	WDTPS<3:0>				SWDTEN	---0 1000
19	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>			0000 0000
1A	PR0	PR0<7:0>								1111 1111
1B	MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-	---0 -00-
1C	SOSCPPRL	SOSCPR<7:0>								1111 1111
1D	SOSCPRH	-	-	-	-	SOSCPR<11:8>				---- 1111
1E										---- ----
1F										---- ----

Table 15. CMT2281F2 Special Function Registers Summary Bank1

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
80	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
81	OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL	Program Counter's (PC) Least Significant Byte, PC<7:0>								0000 0000
83	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
84	FSR	Indirect Data Memory Address Pointer								
85	TRISA	TRISA<7:6>		--	TRISA<4:0>					11x1 1111
86										---- ----
87	TRISC	TRISC<7:0>								1111 1111
88										---- ----
89										---- ----
8A	PCLATH	-	-	-	Write Buffer for upper 5 bits of Program Counter, PC<13:8>					---0 0000
8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
8C	PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-	00-0 000-
8D										---- ----
8E	PCON							/POR	/BOR	---- --qq
8F	OSCCON	LFMOD	IRCF[2:0]			OSTS	HTS	LTS	SCS	0101 x000
90										---- ----
91										0000 0000
92	PR2	PR2[7:0], Timer2 period register								1111 1111
93										---- ----
94										---- ----
95	WPUA	WPUA<7:6>		-	WPUA<4:0>					11-1 1111
96	IOCA	IOCA<7:0>								---- ----
97										---- ----
98										---- ----
99	VRCON	VREN	-	VRR	-	VR<3:0>				0-0- 0000
9A	EEDAT	EEDAT<7:0>								0000 0000
9B	EEADR	EEADR<7:0>								0000 0000
9C	EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD	--00 x0-0
9D	EECON2	-	-	-	-	-	-	-	WR	---- ---0
9E										---- ----
9F										---- ----

5.2 Port A

There have 8 general purpose I/O pins available, PA0~PA7, as shown in the table below. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Table 16. Mapping from the GPIOs to the Pinouts

GPIO	Pinout
PA0	PA0/ICSPCLK
PA1	PA1/ICSPDAT
PA2	PA2
PA3	PA3
PA4	PA4
PA5	PA5/MCLRB
PA6	PA6/OSC2/CLKO
PA7	PA7/OSC1/CLKI

5.2.1 PORTA and the CPIOA Registers

PORTA is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin as input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin as output (i.e., put the contents of the output latch on the selected pin). The exception is PA5, which is input only and its TRISA bit will always read as '1'.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; this value is modified and then written to the PORT data latch. PA5 reads '0' when MCLRE = 1.

5.2.2 Additional Pin Functions

Every PORTA pin on the CMT2281F2 has an interrupt-on-change(IOC) option and every PORTA pin has a pull-up option.

5.2.2.1 Pull-up

Each of the PORTA pinshas an individually configurable internal pull-up. Control bits WPUA enable or disable each pull-up.

5.2.2.2 Interrupt-On-Change

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits IOCA enable or disable the interrupt function for each pin. The interrupt-on-change is disabled on a Power-on Reset. For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set, the PORTA Change Interrupt Flag bit (PAIF) in the INTCON register. This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt by:

1) Any read or write of PORTA. This will end the mismatch condition, then.
2) Clear the flag bit PAIF.

A mismatch condition will continue to set flag bit PAIF. Reading PORTA will end the mismatch condition and allow flag bit PAIF to be cleared. The latch holding the last read value is not affected by a MCLR nor BOD Reset. After these resets, the PAIF flag will continue to be set if a mismatch is present.

5.3 PORTC

PORTC is a general purpose I/O port consisting of 8 bidirectional pins. The pins can be configured for either digital I/O, but only PC0 and PC4 has been pin out. PC0 is connected to the RF's AVDD, PC4 is connected to the SPI's SDIO, as well as RFDATA. PC2 is connected to the RF's SCLK, PC3 is connected to the RF's CSB, but both this two pins are inside in the chip,

are not pin out, and are used to configuration the RF parameters.

Table 17. Mapping from the SPI

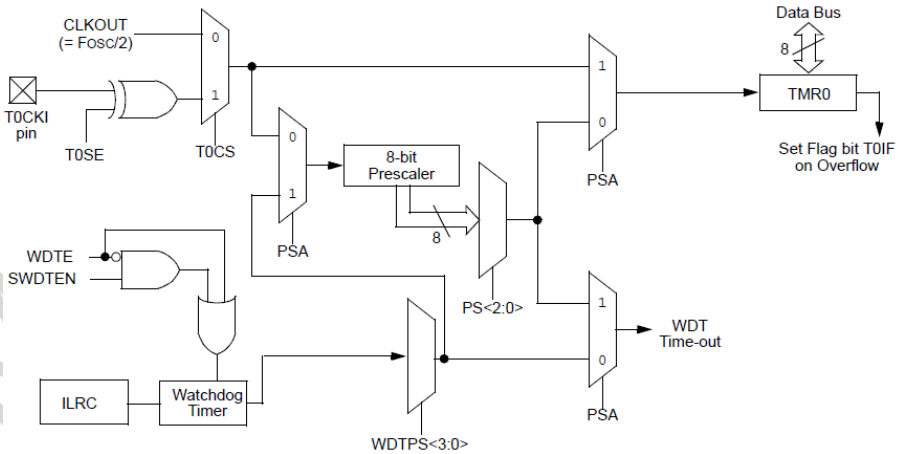
GPIO	RF Part	Pinout
PC0	AVDD	PC0/AVDD
PC1	--	×
PC2	SCLK	×
PC3	CSB	×
PC4	SDIO/RFDATA	PC4/RFDAT
PC5	--	×
PC6	--	×
PC7	--	×

5.4 Timer0 Module

The Timer0 module timer/counter has the following features.

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 13 is a block diagram of the Timer0 module and the prescaler shared with the WDT.



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the Option register, WDTPS<3:0> are bits in the WDTCON register.

Figure 134. Block Diagram of the Timer0/WDT Prescaler

5.4.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit(OPTION<5>). In Timer mode, the Timer0module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is in habited for the following two instruction cycles. The

user can work around this by writing an adjusted value to theTMR0 register.

Counter mode is selected by setting the T0CS bit(OPTION<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin PA2/T0CKI. The incrementing edge is determined by the source edge (T0CE) control bit(OPTION<4>). Clearing the T0CE bit selects the rising edge.

5.4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit(INTCON<2>) must be cleared in software by theTimer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt can not wake the processor from Sleep, since the timer is shutoff during Sleep.

5.4.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 andQ4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least $2T_{OSC}$(and a small RC delay of 20 ns) and low for at least $2T_{OSC}$(and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

5.4.4 Prescaler

An 8-bit counter is available as a prescaler for theTimer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this Datasheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (OPTION<2:0>). The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRR 1, STWR 1,BSR 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

5.5 Timer2 Module

Figure 14 shows the basic block diagram of the Timer2 module.

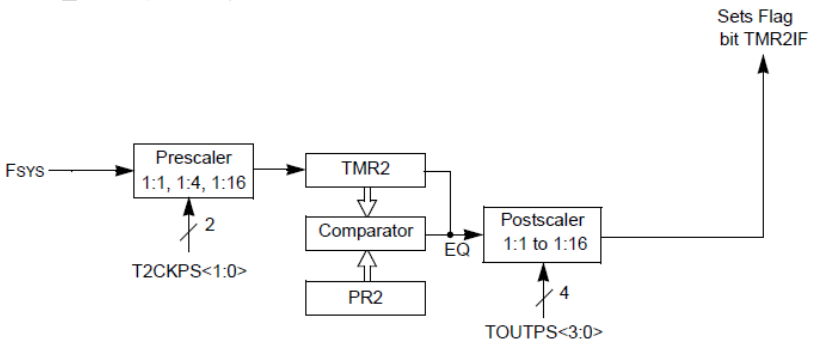


Figure 14. Timer2 Block Diagram

6. Ordering Information

Table 18. CMT2281F2 Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2281F2-ESR[1]	240 – 960 MHz SoC OOK Receiver	SOP16	Tape & Reel	2.0 to 3.6 V, -40 to 85 ℃	2,500
CMT2281F2-ESB[1]	240 – 960 MHz SoC OOK Receiver	SOP16	Tube	2.0 to 3.6 V, -40 to 85 ℃	1,000

Notes:

[1]. "E" stands for extended industrial product grade, which supports the temperature range from -40 to +85 ℃.
"S" stands for the package type of SOP16.
"R" stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 2,500 pcs. "B" stands for the tube package option, with the MOQ of 1,000 pcs.

Visit www.cmostek.com/products to know more about the product and product line.
Contact sales@cmostek.com or your local sales representatives for more information.

7. Package Outline

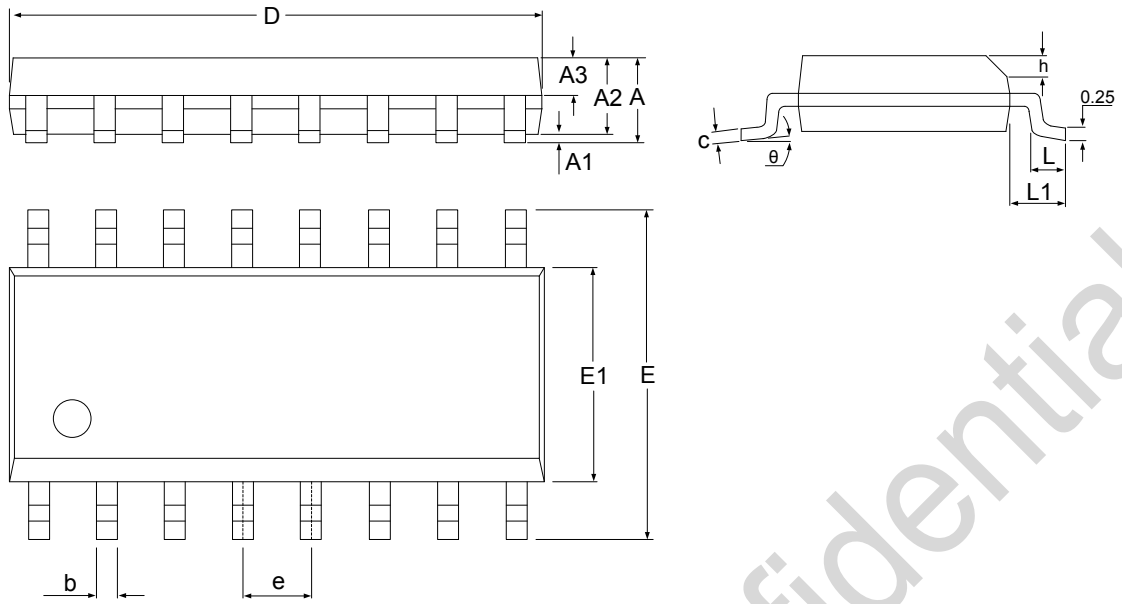


Figure 15.16-Pin SOP Package

Table 19.16-Pin SOP Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
C	0.21	-	0.26
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 BSC		
θ	0	-	8°

8. Top Marking

8.1 CMT2281F2 Top Marking

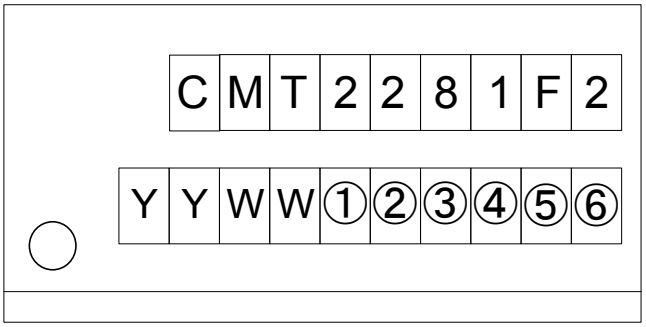


Figure 16. CMT2281F2 Top Marking

Table 20. CMT2281F2 Top Marking Explanation

Mark Method :	Laser
Pin 1 Mark :	Circle's diameter = 1 mm.
Font Size :	0.35 mm, right-justified.
Line 1 Marking :	CMT2281F2 represents part number CMT2281F2
Line 2 Marking :	YYWW is the Date code assigned by the assembly house. YY represents the last two digits of the mold year and WW represents the workweek. ①②③④⑤⑥is the internal tracking number.

9. Other Documentations

Table 21. Other Documentations for CMT2281F2

Brief	Name	Descriptions
AN200	CMT2281F2 User Guide	Details of using the CMT2281F2
AN204	CMT2281F2/CMT2280F2/CMT2189B/CMT2189C IDE Guide	Details of using the IDE

10. Document Change List

Table 22. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.8	All	Initial Released	2018-1-1

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