CMT4502

Bluetooth Low Energy (BLE) System on Chip

主要功能

- ARM® Cortex™-M0 32 位处理器
- 存储器
  - 512KB 系统闪存
  - 128KB ROM
  - 138KB SRAM，睡眠模式下所有数据恒常保持
  - 8 通道 DMA
- 33/19 通用 I/O 引脚
  - 所有引脚均可设置为串行接口和可编辑的 IO MUX 函数映射
  - 所有引脚均可设置为唤醒状态
  - 共 18 个针脚可触发中断
  - 3 个 QDEC 解码器
  - 6 通道 PWM
  - 2 通道 PDM
  - 2 通道 I2C
  - 2 通道 SPI
  - 1 通道 UART
  - JTAG
- 支持 DMIC/AMIC 麦克风功能
- 支持低噪声 PGA 的 3/8 通道 12 位 ADC
- 4 通道 24 位时钟，1 个监视时钟
- 实时计数器(RTC)
- 电源、时钟复位控制器
- 弹性电源管理
  - 供电电压范围：1.8V-3.6V
  - 嵌入式降压型 DC-DC
  - 嵌入式 LDOs
  - 电源监视器：支持低电量检测
- 能量功耗
  - 睡眠模式，只通过 IO 唤醒的电流量：0.7uA
  - 睡眠模式，可以通过 32KHz RTC 唤醒的电流量：2uA
  - RX 模式下，系统峰值电流为 6.7mA
  - TX 0dBm 发射功率下，系统峰值电流为 6.7mA
- RC 振荡器硬件校准
  - 32KHz RC RTC 振荡器自动校准精度为±500ppm
  - 32MHz RC HCLK 振荡器自动校准精度为 3%
- 高速数据吞吐量
  - 支持 BLE 2Mbps 协议
  - 支持数据长度扩展（DLE）功能
  - 最高数据吞吐量达 1.6Mbps(DLE+2Mbps)
- 支持 SIG-Mesh 多种特性
  - Friend 节点
  - LowPower 节点
  - Proxy 节点
  - Relay 节点
- 2.4 GHz 收发器
  - 支持 BLE5.0 RF PHY 1Mbps/2Mbps
  - 接收灵敏度：BLE 1Mbps 数据速率：-97dBm
  - 发射功率：-20dBm 至 10dBm， 3dBm 步进
  - 单针天线：无需射频匹配或 RX/TX 切换
  - RSSI ： 1dB 分辨率
- AES-128 硬件加密
- 工作温度：-40℃ ~ 85℃
- RoHS 程序包：QFN32/QFN48
- 应用场景：智能穿戴设备、蓝牙室内导航、智能家居、智能楼宇、医疗健康、运动健身、智能工业、零售支付、信息安全、数据传输、远程控制、个人外设以及物联网（IoT）

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版本更新日志

修改时间	版本号	详细信息
2019.05	1.0	
2020.05	1.1	1. 添加了“GPIO 电气特性”的相关内容 2. 在首页添加了“能量功耗”栏目 3. 在首页添加了“RC 振荡器硬件校准”的精度信息 4. 添加了“DMIC/AMIC 数据通道”的相关内容
2021.07	1.2	更正了“CMT4502(QFN32)引脚功能”的表格信息，分别是：Pin2，3，4，5，7，8
2023.05	1.3	更正了 125K 500K Coded PHY，UART 硬件流控，I2S 等功能描述信息

目录

1 简介

CMT4502 是一款超低功耗物联网蓝牙无线通信芯片，搭载 32 位 ARM®Cortex™-M0 CPU，配备 138K SRAM/Retention SRAM，具有超低功耗、高性能和无线多模的特点，支持安全性、应用和无线更新的 BLE 功能。同时，其串行外围设备 IO 和集成应用程序 IP 也将为客户带来低成本的优势。

CMT4502 支持 BLE5.0 高速数据吞吐，包括 BLE 2Mbps 协议和长度扩展功能；支持蓝牙 Sig-Mesh 协议的多种特性: Friend/LowPower/ProxyRelay 节点，能够提供 BLE5.0 的完整协议功能支持。

2 产品概述

2.1 框图

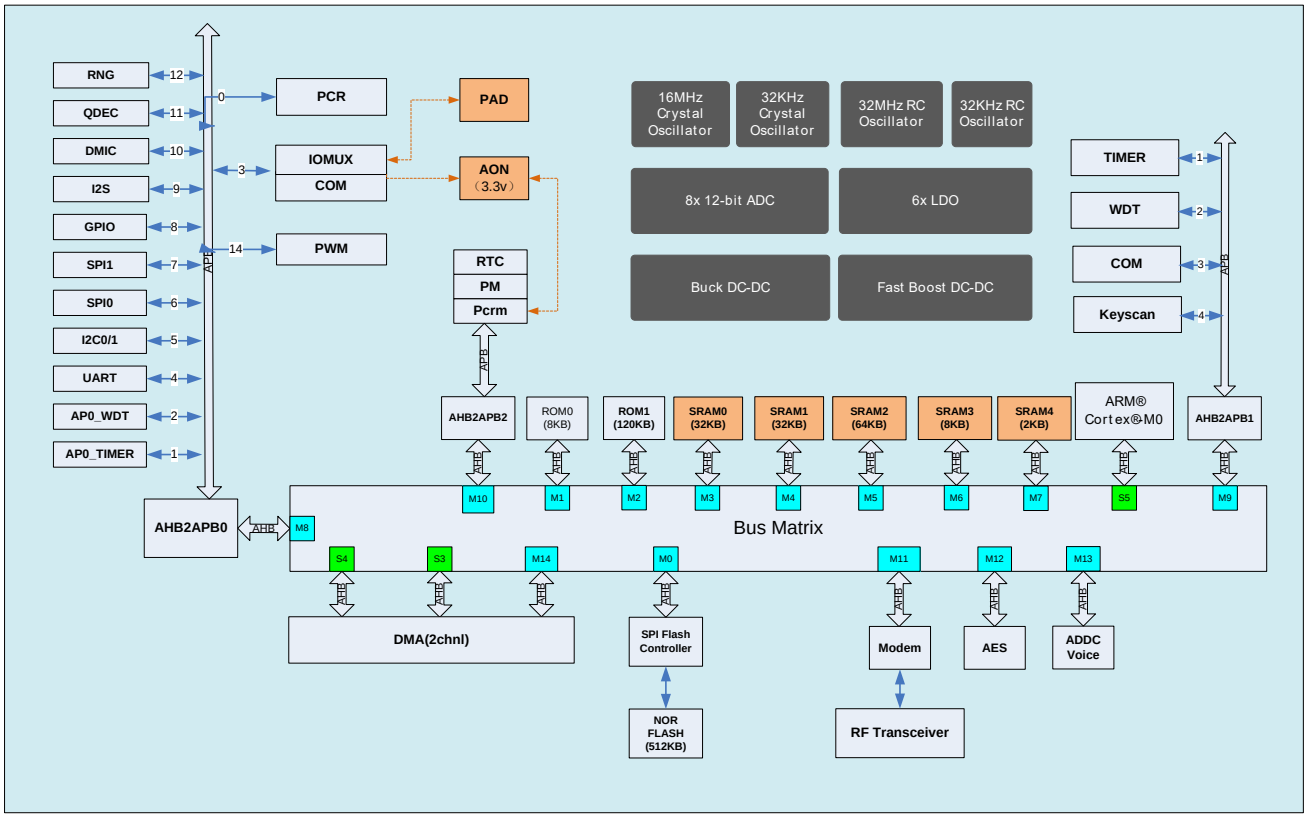


图 1：CMT4502 框图

2.2 引脚的分配与功能

本节将阐述不同封装形式下的引脚分配及其功能。

2.2.1 CMT4502 (QFN32)

2.2.1.1 引脚分配

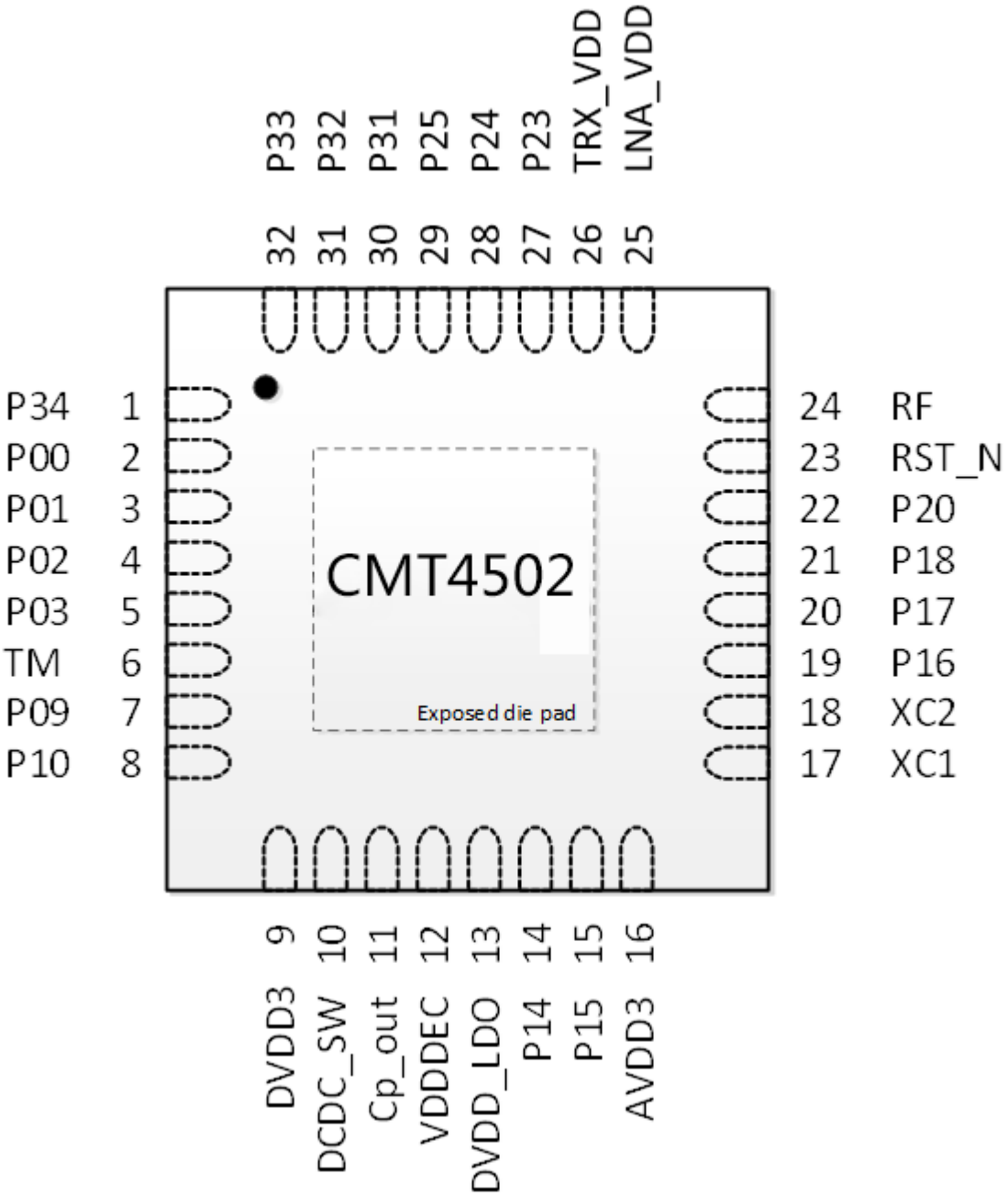


图 2：引脚分配 - CMT4502 QFN32 封装形式

2.2.1.2 引脚功能

Pin	Pin name	Description
1	P34	all functions configurable *Note: Not support interrupt and ADC function
2	P00	all functions configurable/ JTAG_TDO *Note: Not support ADC function
3	P01	all functions configurable/ JTAG_TDI *Note: Not support ADC function
4	P02	all functions configurable/ JTAG_TMS *Note: Not support ADC function
5	P03	all functions configurable/ JTAG_TCK *Note: Not support ADC function
6	TM	Test_Mode
7	P09	all functions configurable *Note: Not support ADC function
8	P10	all functions configurable *Note: Not support ADC function
9	DVDD3	3V power supply for digital IO, DCDC, Charge pump
10	DCDC_SW	Buck dcdc output
11	cp_out	charge pump output
12	VDDDEC	1.2V VDD_CORE, digital LDO output
13	DVDD_LDO	digital LDO input
14	P14	all functions configurable/AIO<3>
15	P15	all functions configurable/AIO<4>
16	AVDD3	3V power supply for analog IO, bg, rcosc, etc
17	XC1	16M crystal input
18	XC2	16M crystal output
19	P16	all functions configurable/AIO<5>/32K crystal input
20	P17	all functions configurable/AIO<6>/32k crystal output
21	P18	all functions configurable/ JTAG_TDO *Note: Not support interrupt function
22	P20	all functions configurable/AIO<9>/Micphone bias output
23	RST_N	reset pin
24	RF	RF antenna
25	LNA_VDD	LNA_VDD
26	TRX_VDD	TRX_VDD
27	P23	all functions configurable *Note: Not support interrupt and ADC function
28	P24	all functions configurable/test_mode_select[0] *Note: Not support interrupt and ADC function
29	P25	all functions configurable/test_mode_select[1] *Note: Not support interrupt and ADC function
30	P31	all functions configurable *Note: Not support interrupt and ADC function
31	P32	all functions configurable *Note: Not support interrupt and ADC function
32	P33	all functions configurable *Note: Not support interrupt and ADC function

表 1：引脚功能 - CMT4502 QFN32 封装形式

2.2.2 CMT4502 (QFN48)

2.2.2.1 引脚分配

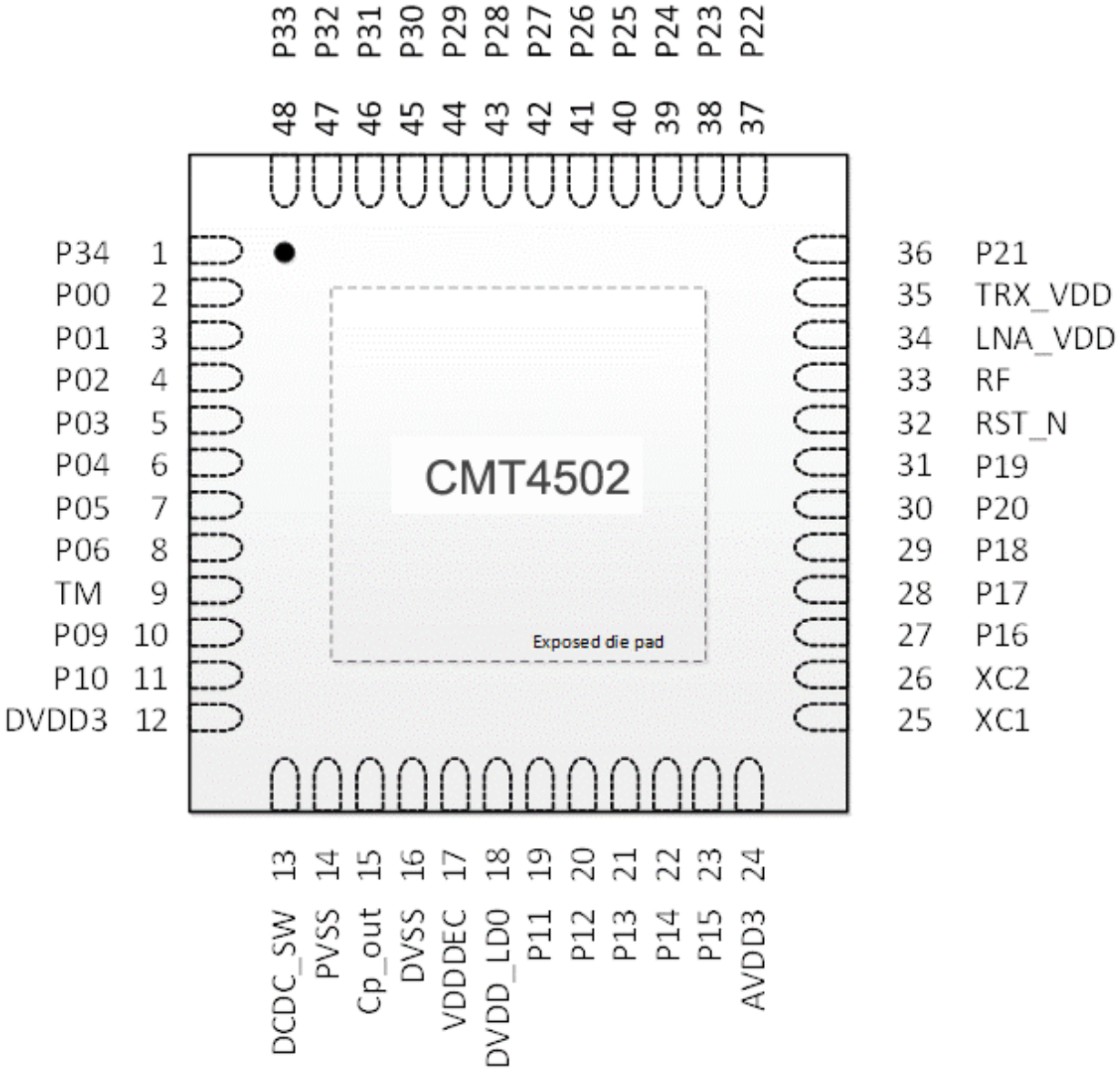


图 4：引脚分配 – CMT4502 QFN48 封装形式

2.2.2.2 引脚功能

Pin	Pin name	Description
1	P34	all functions configurable *Note: Not support interrupt and ADC function
2	P00	all functions configurable/ JTAG_TDO *Note: Not support ADC function
3	P01	all functions configurable/ JTAG_TDI *Note: Not support ADC function
4	P02	all functions configurable/JTAG_TMS *Note: Not support ADC function
5	P03	all functions configurable/JTAG_TCK *Note: Not support ADC function
6	P04	all functions configurable *Note: Not support ADC function
7	P05	all functions configurable *Note: Not support ADC function
8	P06	all functions configurable *Note: Not support ADC function
9	TM	Test_Mode
10	P09	all functions configurable *Note: Not support ADC function
11	P10	all functions configurable *Note: Not support ADC function
12	DVDD3	3V power supply for digital IO, DCDC, Charge pump
13	DCDC_SW	Buck dcdc output
14	PVSS	Buck dcdc and charge pump power vss
15	cp_out	charge pump output
16	DVSS	digital vss
17	VDDDEC	1.2V VDD_CORE, digital LDO output
18	DVDD_LDO	digital LDO input
19	P11	all functions configurable/AIO<0>
20	P12	all functions configurable/AIO<1>
21	P13	all functions configurable/AIO<2>
22	P14	all functions configurable/AIO<3>
23	P15	all functions configurable/AIO<4>
24	AVDD3	3V power supply for analog IO, bg, rcosc, etc
25	XC1	16M crystal input
26	XC2	16M crystal output
27	P16	all functions configurable/AIO<5>/32K crystal input
28	P17	all functions configurable/AIO<6>/32k crystal output
29	P18	all functions configurable/AIO<7>/PGA differential positive input *Note: Not support interrupt function

30	P20	all functions configurable/AIO<9>/Micphone bias output *Note: Not support interrupt function
31	P19	all functions configurable/AIO<8>/PGA differential negative input *Note: Not support interrupt function
32	RST_N	reset pin
33	RF	RF antenna
34	LNA_VDD	LNA_VDD
35	TRX_VDD	TRX_VDD
36	P21	all functions configurable *Note: Not support interrupt function and ADC function
37	P22	all functions configurable *Note: Not support interrupt function and ADC function
38	P23	all functions configurable *Note: Not support interrupt function and ADC function
39	P24	all functions configurable/test_mode_select[0] *Note: Not support interrupt function and ADC function
40	P25	all functions configurable/test_mode_select[1] *Note: Not support interrupt function and ADC function
41	P26	all functions configurable *Note: Not support interrupt function and ADC function
42	P27	all functions configurable *Note: Not support interrupt function and ADC function
43	P28	all functions configurable *Note: Not support interrupt function and ADC function
44	P29	all functions configurable *Note: Not support interrupt function and ADC function
45	P30	all functions configurable *Note: Not support interrupt function and ADC function
46	P31	all functions configurable *Note: Not support interrupt function and ADC function
47	P32	all functions configurable *Note: Not support interrupt function and ADC function
48	P33	all functions configurable *Note: Not support interrupt function and ADC function

表 3：引脚功能 – CMT4502 QFN48 封装形式

3 系统模块

CMT4502 的框图请参阅**图 1**。

3.1 CPU

CMT4502 搭载 ARM Cortex-M0 CPU。其 CPU、内存和所有外围设备均由 AMBA 总线结构连接。

ARM®Cortex™-M0 CPU 具有 16 位指令集和 32 位扩展(Thumb-2®技术)功能，可以在占用很小内存的情况下提供高密度代码。其采用的单周期 32 位乘子、3 级流水线和嵌套向量中断控制器

(NVIC)，使程序执行变得更加简单高效。

ARM®Cortex™-M0 CPU 将作为 BLE 调制解调器的总控制器，运行所有程序。

该 CPU 的主要特性如下：

- 处理器核心速率高达 48Mhz
  - 低门数，高效能
  - ARMv6M 构架，Thumb ISA，无 ARM ISA
  - 无缓存，无 TCM
  - 多达 32 个嵌入式 NVIC 中断装置
  - 系统定时器
  - 支持睡眠/深度睡眠模式
  - 支持低功耗 WFI 和 WFE
- 4 个 32 位通用定时器和 1 个监视定时器(WDT)
- 用于引导和协议栈的 120kb ROM
- 用于程序和数据保留的 138kb SRAM
- 用于外设和寄存器的 AHB 至 APB 桥接端口
- 时钟和复位控制器
- AHB 调试端口和 DAP ROM
- APB 接口可连接至 BLE 调制解调器
- 动态和静态时钟门控
- 无痕使用

上述某些特性与 AP 子系统共享。

3.2 存储器

CMT4502 共有 128KB 的 ROM，138KB 的 SRAM 和高达 512KB 闪存。这些内存的物理地址空间如图 3 所示。

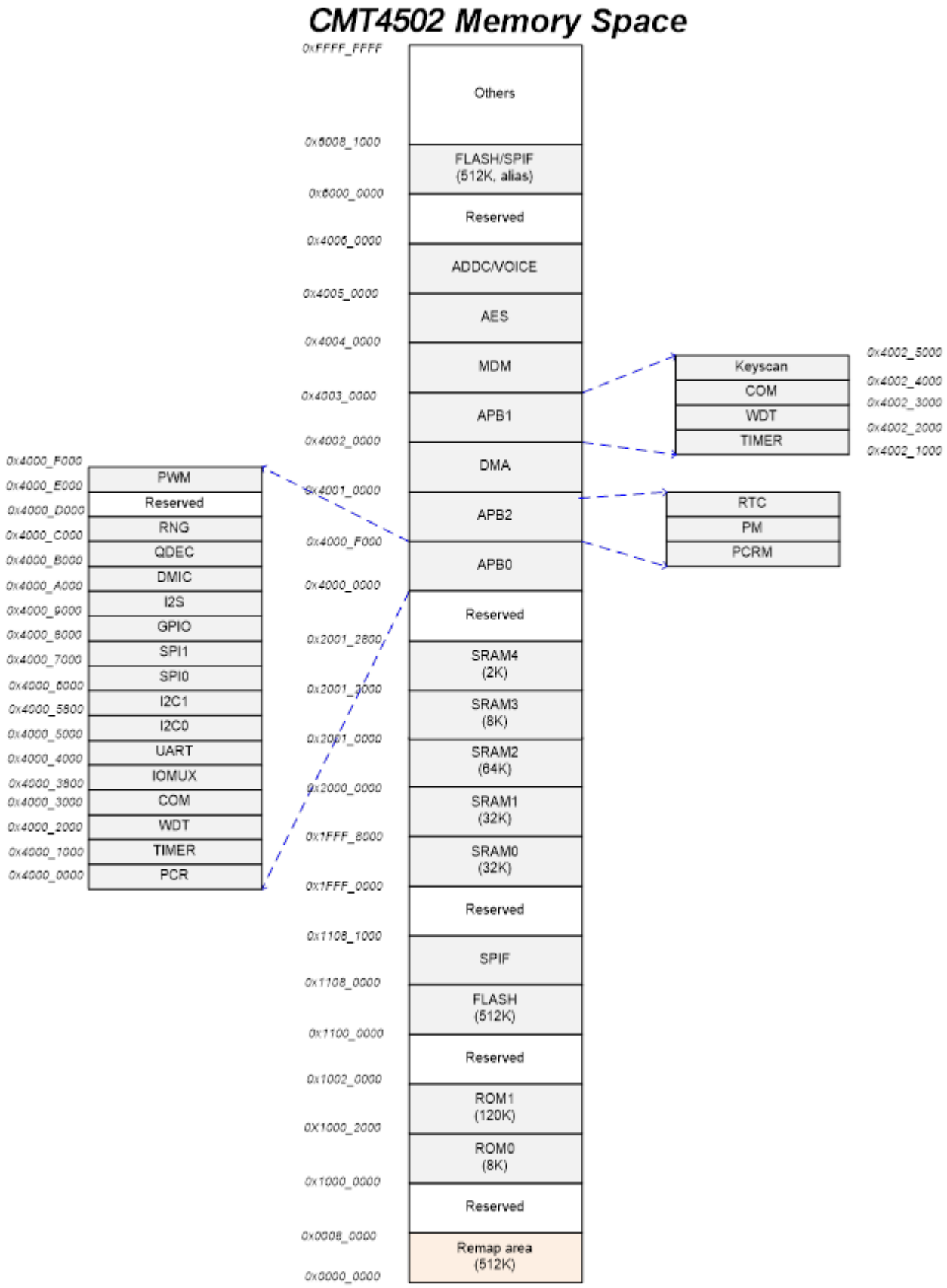


图 3：CMT4502 的存储空间

3.2.1 ROM

CMT4502 共有 2 个 ROM。

	SIZE	CONTENT
ROM0	8KB	Reserved
ROM1	120KB	Boot ROM for M0. Protocol stack. Common peripheral drivers.

表 2：ROM 列表

3.2.2 SRAM

CMT4502 的 SRAM 分为 5 个区块，各个区块都具备可进行单独配置的数据保留能力，且所有区块均可用于储存程序或数据。

	SIZE	CONTENT
SRAM0	32KB	
SRAM1	32KB	
SRAM2	64KB	
SRAM3	8KB	
SRAM4	2KB	

表 3：SRAM 列表

3.2.3 FLASH

CMT4502 利用 FLASH 实现非易失性程序和数据存储功能，FLASH 的大小为 256KB 或 512KB，支持 2 线读取。

3.2.4 内存地址映射

Name	Size（KB）	Master	Physical Address	CM4 Alias	M0 Remap		
					0	1	2
ROM0	8	M0	1000_0000~1000_1FFF	0x0			
ROM1	120	M0	1000_2000~1001_FFFF		0x0		
RAM0	32	M0	1FFF_0000~1FFF_7FFF				
RAM1	32	M0	1FFF_8000~1FFF_FFFF				
RAM2	64	M0	2000_0000~2000_FFFF			0x0	
RAM3	8	M0	2001_0000~2001_1FFF				
RAM4	2	M0	2001_2000~2001_27FF				
FLASH	512	M0	1100_0000~1107_FFFF				0x0
			6000_0000~6007_FFFF				

表 4：内存地址映射

3.3 引导和执行模式

引导期间，ROM1 将转化为 0x0 地址，M0 将从 ROM1 开始执行程序。

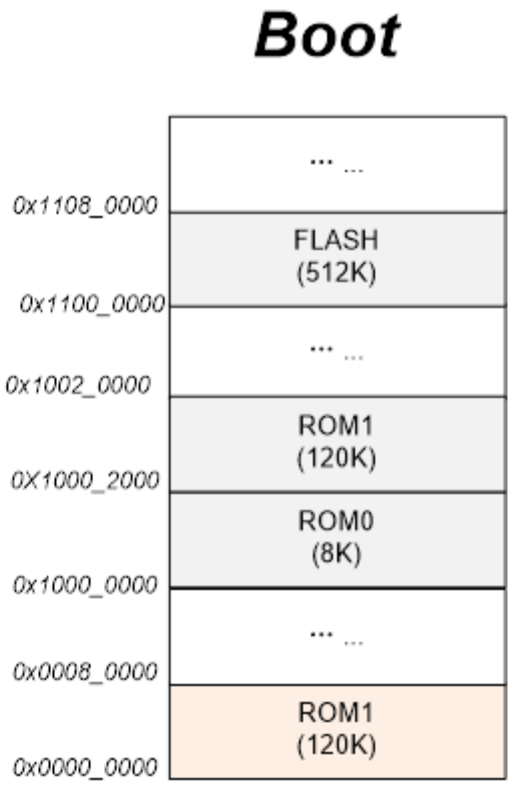


图 4：CMT4502 引导模式

3.3.1 镜像模式

镜像模式与芯片的变化无关，任何芯片的变化都可以使用镜像模式来执行。在镜像模式下，程序将从 FLASH 被复制到 SRAM，随即在 SRAM 中执行。对于 M0 处理器而言，其中一个 SRAM 区块必须转换为 0x0 地址。

3.3.2 FLASH 模式

FLASH 模式与芯片的变化无关，任何芯片的变化都可以使用 FLASH 模式来执行。在 FLASH 模式下，程序将在 FLASH 中执行。对于 M0 处理器而言，FLASH 必须转换为 0x0 地址。

3.3.3 引导装载程序

ROM 中的引导加载程序的基本结构如下所示。FLASH 中的内容需进行特别定义，以保证引导加载程序能够识别 FLASH 内容是否有效，如下面的案例所示。如果 FLASH 是有效的，ROM 引导加载程序将以正常模式启动芯片，并开始执行程序；如果 FLASH 无效，引导加载程序将进入 FLASH 编程模式。

Address	Variable	Content
0	PRODUCT_MODE	Identify the chip mode
4	CODE_BASE	The base address of the code
8	CODE_LEN	The length of the code
C	BOOT_MODE	Identify mirror or FLASH mode

表 5：Flash 内容设置案例

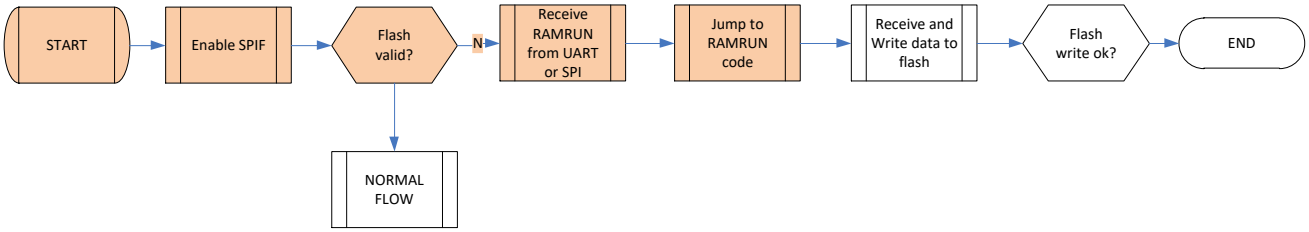


图 5：引导装载程序流程图

3.4 电源、时钟和复位(PCR)

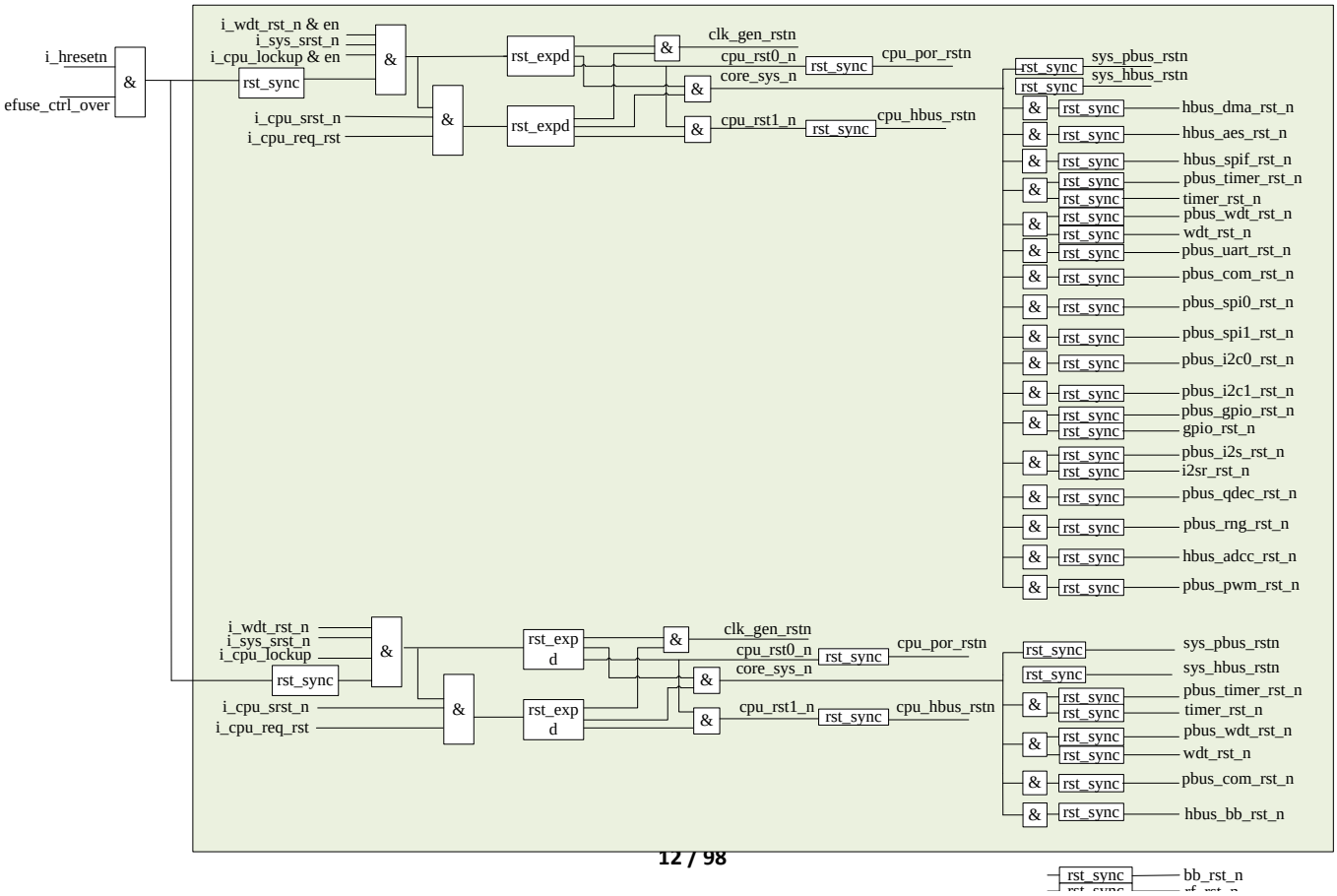


图 6：CMT4502 的电源、时钟和复位示意图

3.5 电源管理

CMT4502 的电源管理系统具有极高的灵活性。除了系统休眠模式和关机模式之外，还具有诸如 CPU、无线信号收发、外围设备等节能且独立的功能控制模块。系统正常运行时，所有的功能模块将根据所需的应用程序功能独立启动。

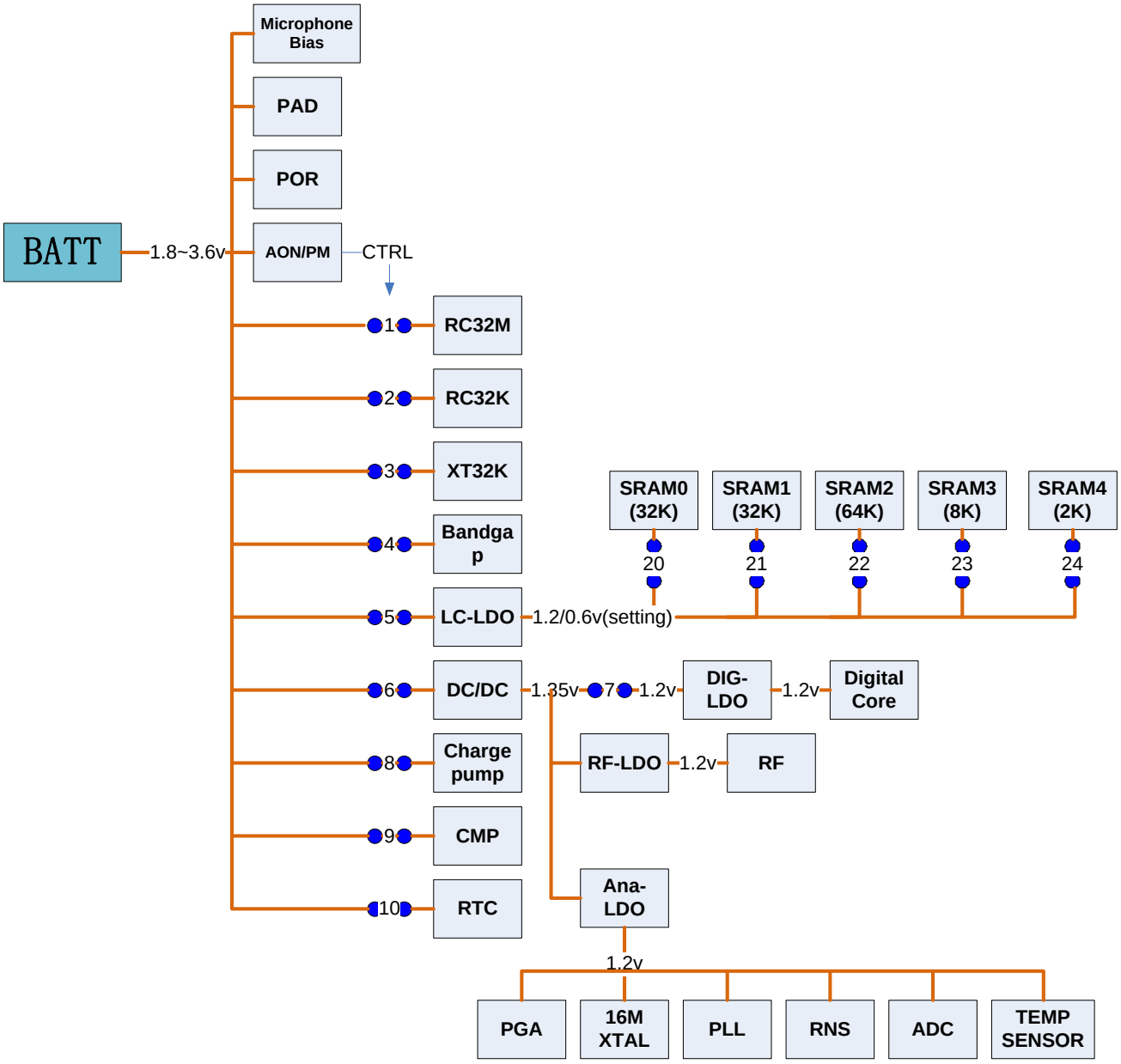


图 7：电源系统

下表将展示正常、睡眠和关机 3 个模式。用户可根据自身需求切换这些模式。

Switch	Normal	Sleep	Off
1RC32M	On	Off	Off
2RC32K	On	Optional	Off
3XT32K	On	Optional	Off
4bandgap	On	Off	Off
5LC-LDO	On	on	Off
6DC/DC	On	Off	Off
7DIG-LDO	On	Off	Off
8charge pump	On	Off	Off
9CMP	On	Optional	Off
10RTC	On	Optional	Off
20SRAM-32K	1.2v	0.6v	0
21SRAM-32K	1.2v	0.6v	0
22SRAM-64K	1.2v	0.6v	0
23SRAM-8K	1.2v	0.6v	0
24SRAM-2K	1.2v	0.6v	0

表 6：不同电源模式下的 FLASH 开关

3.6 低功耗功能

3.6.1 操作和睡眠状态

3.6.1.1 正常状态

3.6.1.2 钟门状态

CPU 执行 WFI/WFE 后即进入钟门状态。从钟门状态中唤醒之后，CPU 将从其上次中止的地方开始，继续执行程序。唤醒手段包括“中断”和“事件”两种。这些唤醒手段将由软件根据应用程序配置。

3.6.1.3 系统休眠状态

唤醒手段包括：

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 系统关闭状态

唤醒手段包括：

- IOs
- RESET
- UVLO reset

3.6.2 状态切换

3.6.2.1 进入钟门状态并唤醒

CPU 执行 WFI/WFE。

3.6.2.2 进入睡眠/关机状态并唤醒

PM 寄存器将识别 CPU 当前处于镜像模式还是休眠前的 FLASH 模式，并记录下重新映射和向量的内容。CPU 将配置相应的 PM 缓存，以使芯片进入休眠或关闭模式。唤醒后，芯片进入启动引导模式，在 RON 中执行开机代码。ROM 代码将在休眠/关机前检查引导模式和重新映射信息，执行相应配置，随后开始执行程序。

3.7 中断

Interrupt Name	M0 Interrupt Number
Reserved	0
Reserved	1
cp_timer_irq	2
cp_wdt_irq	3
bb_irq	4
kscan_irq	5
rtc_irq	6
Reserved	7
Reserved	8
timer_irq	9
wdt_irq	10
uart_irq	11
i2c0_irq	12
i2c1_irq	13
spi0_irq	14
spi1_irq	15
gpio_irq	16
i2s_irq	17
spif_irq	18

dmac_intr	19
dmac_inttc	20
dmac_interr	21
fpidc	22
fpdzc	23
fpioc	24
fpufc	25
fpofc	26
fpixc	27
aes_irq	28
adcc_irq	29
qdec_irq	30
rng_irq	31

表 7：中断图示

3.8 时钟管理

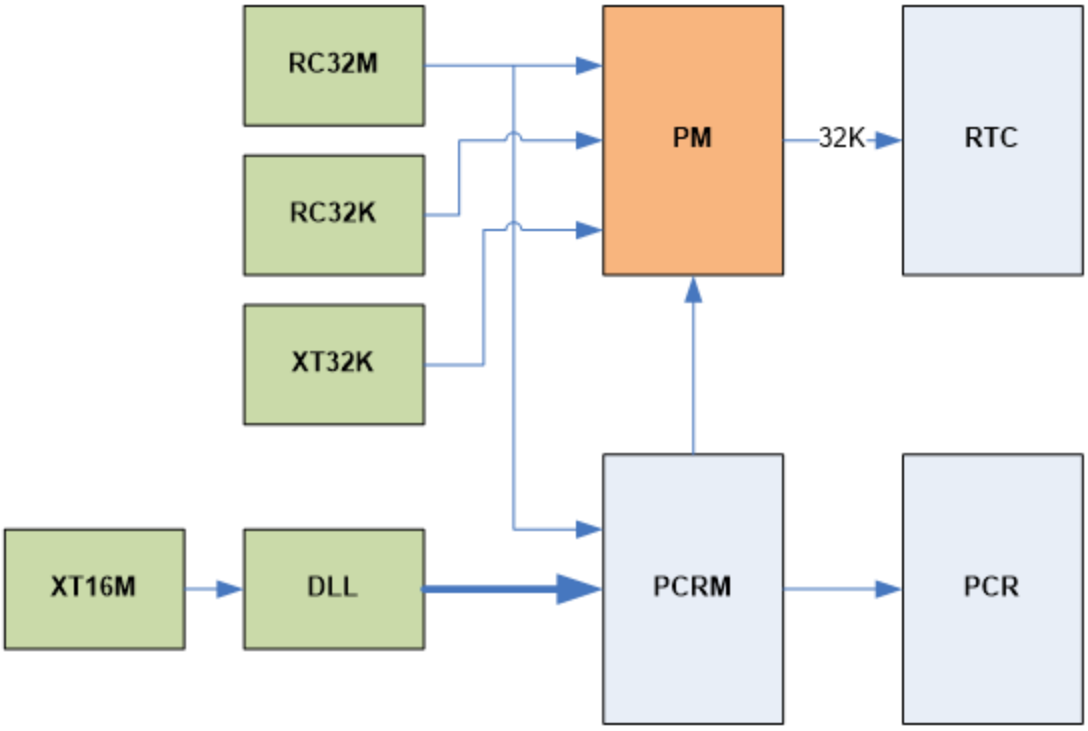


图 8：时钟管理图示

两个晶体时钟源：16MHz 晶体振荡器(XT16M)和 32.768kHz 晶体振荡器(XT32k)，其中 32.768k 晶体振荡器处于备用状态。芯片上的 RC 振荡器也有两个：32MHz RC 振荡器(RC32M)和 32kHz RC 振荡器(RC32k)，二者均可根据 16MHz 晶体振荡器进行校准。若未安装 32.768kHz 晶体振荡器，RC32k 振荡器将会被周期性校准并用于 RTC。若处于 XT16M 晶体振荡器启动前的初始或唤醒状态，RC32M 将作为主时钟使用。芯片上的 DLL 可以根据 XT16M 时钟源生成频率更高的时

钟，如 32/48/64/96MHz。

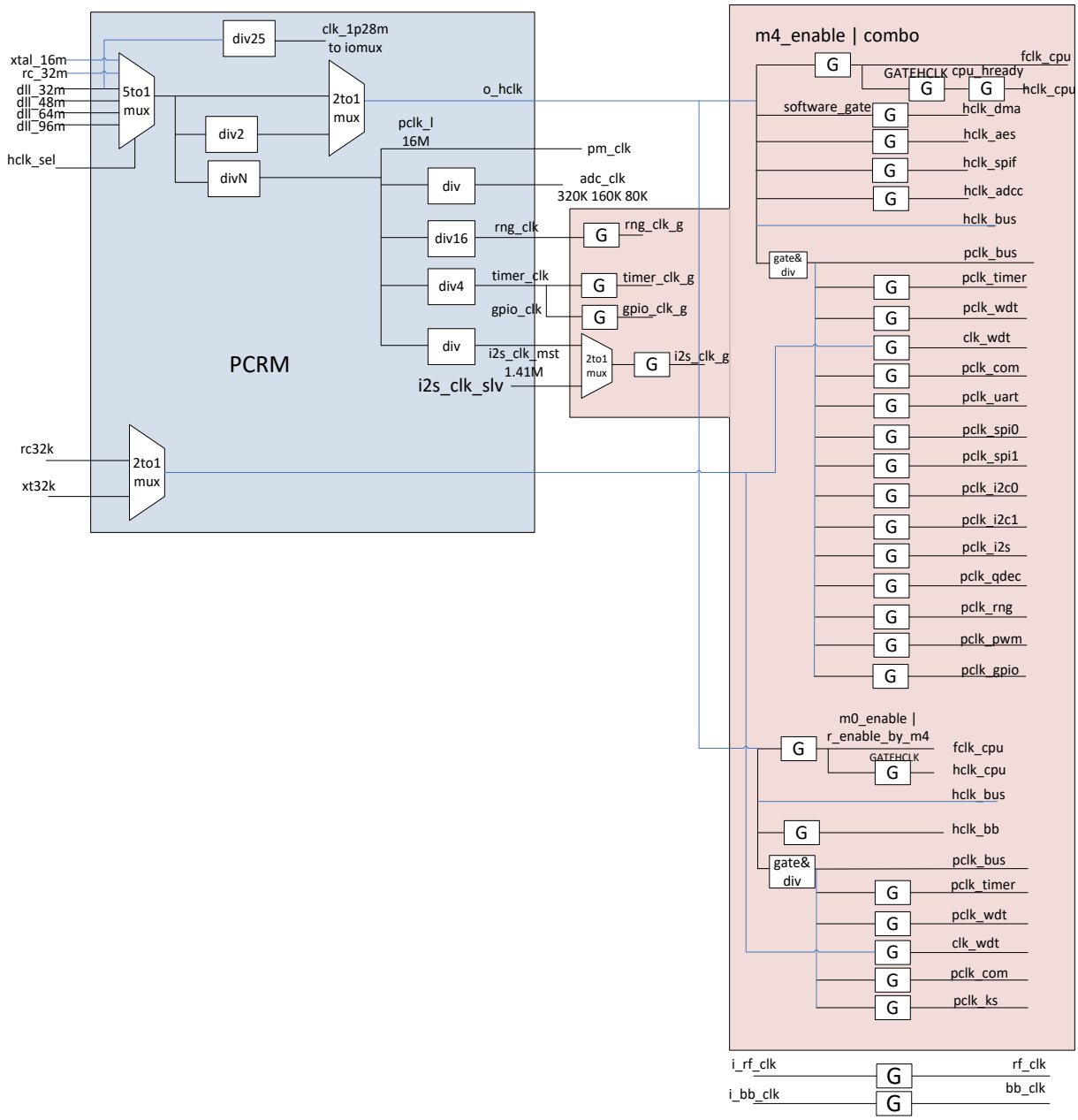


图 9：时钟结构图

3.9 IOMUX

IOMUX 提供了一种灵活的 I/O 配置，因为大多数外围设备的端口都可以配置并映射到任何物理 I/O 触点（甚至是模具边界）上。这些外围模块包括 I2C 0-1、UART、PWM 0-5、SPI 0-1、正交解码器等。然而，对于其他特定用途的外设，它们的 IOs 映射在启用时是固定的，这些专用外设包括 JTAG、analog_ios、GPIOs 和按键扫描。

图 10 是 IOMUX 的逻辑图。

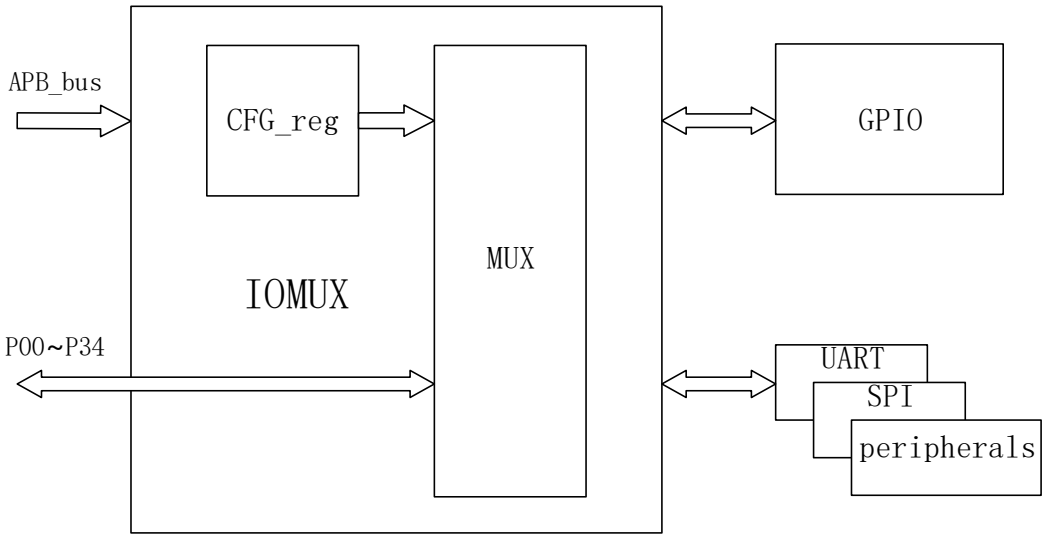


图 10：IOMUX 逻辑结构图

从 P00 到 P07，再从 P09 到 P34，共有 34 个可配置的触点。P08 被标记为用于测试模式的 TM 引脚。下表展示了可以通过 IOMUX 映射的外围模块 IOs 映射。这些外围模块包括 I2C 0-1、UART、PWM 0-5、SPI 0-1、正交解码器、1.28MHz 时钟和 dmic_out。

Signal Name	IO	FULLMUX
iic0_scl	B	0
iic0_sda	B	1
iic1_scl	B	2
iic1_sda	B	3
uart_tx	O	8
uart_rx	I	9
pwm0	O	10
pwm1	O	11
pwm2	O	12
pwm3	O	13
pwm4	O	14
pwm5	O	15
spi_0_sck	B	16
spi_0_ssn	B	17
spi_0_tx	O	18
spi_0_rx	I	19
spi_1_sck	B	20
spi_1_ssn	B	21
spi_1_tx	O	22
spi_1_rx	I	23

chax	I	24
chbx	I	25
chix	I	26
chay	I	27
chby	I	28
chiy	I	29
chaz	I	30
chbz	I	31
chiz	I	32
clk_1p28m	O	33
adcc_dmic_out	I	34

表 8：通过 IOMUX 映射的外围 IOs

另一方面，也有一些特殊用途的外设，仅当 IOs 和某些固定的物理触点对应时，才能使用它们的功能。这些特殊用途的外设包括：JTAG、模拟 I/Os （ADC 输入）、GPIO 和按键扫描。当它们被启用时，其 IOs 将根据下表映射到物理触点处（默认启用 JTAG）

QFN48	QFN32					Name
0	√	GPIO_P00	jtag_dout	GPIO		mk_in[0]
1	√	GPIO_P01	jtag_din	GPIO		mk_out[0]
2	√	GPIO_P02	jtag_tm	GPIO		mk_in[1]
3	√	GPIO_P03	jtag_clk	GPIO		mk_out[1]
4		GPIO_P04	GPIO			mk_out[9]
5		GPIO_P05	GPIO			mk_in[10]
6		GPIO_P06	GPIO			mk_out[10]
7		GPIO_P07	GPIO			mk_in[11]
8	√	TEST_MODE				
9	√	GPIO_P09	GPIO			mk_out[4]
10	√	GPIO_P10	GPIO			mk_in[4]
11		GPIO_P11	GPIO		analog_io[0]	mk_out[11]
12		GPIO_P12	GPIO		analog_io[1]	mk_in[12]
13		GPIO_P13	GPIO		analog_io[2]	mk_out[12]
14	√	GPIO_P14	GPIO		analog_io[3]	mk_out[2]
15	√	GPIO_P15	GPIO		analog_io[4]	mk_in[2]
16	√	GPIO_P16	XTALI(ANA)	GPIO		mk_out[16]
17	√	GPIO_P17	XTALO(ANA)	GPIO		mk_out[17]
18	√	GPIO_P18	GPIO		analog_io[7]	mk_in[5]
19		GPIO_P19	GPIO		analog_io[8]	mk_in[13]
20	√	GPIO_P20	GPIO		analog_io[9]	mk_out[5]
21		GPIO_P21	GPIO			mk_out[13]
22		GPIO_P22	GPIO			mk_in[14]
23	√	GPIO_P23	GPIO			mk_in[6]
24	√	GPIO_P24	GPIO			mk_out[3]
25	√	GPIO_P25	GPIO			mk_in[3]
26		GPIO_P26	GPIO			mk_out[14]
27		GPIO_P27	GPIO			mk_in[9]

28		GPIO_P28	GPIO		mk_out[8]
29		GPIO_P29	GPIO		mk_in[15]
30		GPIO_P30	GPIO		mk_out[15]
31	√	GPIO_P31	spi_t_ssn	GPIO	mk_out[7]
32	√	GPIO_P32	spi_t_rx	GPIO	mk_in[7]
33	√	GPIO_P33	spi_t_tx	GPIO	mk_out[6]
34	√	GPIO_P34	spi_t_sck	GPIO	mk_in[8]

表 9：通过 IOMUX 映射的用于特殊用途的外围 IOs

上表中，第一列是当没有选择 IOMUX 函数，也没有启用模拟 IO、GPIO<0:3>、key scan 等专用外设时，默认状态下的 IO 映射。在此模式下，JTAG 将使用 pin<0:3>。

当启用模拟 IOs 时，<11:15>，<18:20>的引脚将连接到内部模拟 IOs。具体而言，analog_io<0:4><9>连接到 ADC 输入，analog_io<7,8>连接到 PGA 输入。

在 JTAG 模式下，JTAG 测试模式的数据输出将映射到 P00；JTAG 测试模式的数据输入将映射到 P01；JTAG 测试模式的模式控制输入将映射到 P02；JTAG 测试模式的时钟输入将映射到 P03。

3.9.1 寄存器注册表

详细的 IOMUX 和物理 IO 控件相关信息如下所示。

Base address: 4000_3800

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x0			**r_analog_io**	
[31:10]	RW	22'h0	reserved	
[9:0]	RW	10'h60	r_analog_io_en	Analog IO enable
0xc			**full_mux0**	**register description**
[31:0]	RW	32'h0	r_func_io_en[31:0]	full mux enable. [8] must set to 0
0x10			**full_mux1**	**register description**
[31:3]	RW	29'h0	reserved	
[2:0]	RW	3'h0	r_func_io_en[34:32]	full mux enable
0x14			**gpio_papb**	**register description**
[31:17]	RW	15'h0	reserved	
[16]	RW	1'h0	r_gpio_pb_16_en	gpio_16 enable
[15]	RW	1'h0	r_gpio_pb_15_en	gpio_15 enable
[14]	RW	1'h0	r_gpio_pb_14_en	gpio_14 enable
[13]	RW	1'h0	r_gpio_pb_13_en	gpio_13 enable
[12:4]	RW	9'h0	reserved	
[3]	RW	1'h0	r_gpio_pa_03_en	gpio_03 enable
[2]	RW	1'h0	r_gpio_pa_02_en	gpio_02 enable

[1]	RW	1'h0	r_gpio_pa_01_en	gpio_01 enable
[0]	RW	1'h0	r_gpio_pa_00_en	gpio_00 enable
0x18			**func_io0**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io03_sel	pad 3 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io02_sel	pad 2 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io01_sel	pad 1 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io00_sel	pad 0 full mux function select
0x1c			**func_io1**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io07_sel	pad 7 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io06_sel	pad 6 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io05_sel	pad 5 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io04_sel	pad 4 full mux function select
0x20			**func_io2**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io11_sel	pad 11 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io10_sel	pad 10 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io09_sel	pad 9 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io08_sel	pad 8 full mux function select. not used. can delete
0x24			**func_io3**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io15_sel	pad 15 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io14_sel	pad 14 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io13_sel	pad 13 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io12_sel	pad 12 full mux function select
0x28			**func_io4**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io19_sel	pad 19 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io18_sel	pad 18 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io17_sel	pad 17 full mux function select
[7:6]	RW	2'h0	reserved	

[5:0]	RW	6'h0	r_func_io16_sel	pad 16 full mux function select
0x2c			**func_io5**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io23_sel	pad 23 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io22_sel	pad 22 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io21_sel	pad 21 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io20_sel	pad 20 full mux function select
0x30			**func_io6**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io27sel	pad 27 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io26_sel	pad 26 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io25_sel	pad 25 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io24_sel	pad 24 full mux function select
0x34			**func_io7**	**register description**
[31:30]	RW	2'h0	reserved	
[29:24]	RW	6'h0	r_func_io31sel	pad 31 full mux function select
[23:22]	RW	2'h0	reserved	
[21:16]	RW	6'h0	r_func_io30_sel	pad 30 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io29_sel	pad 29 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io28_sel	pad 28 full mux function select
0x38			**func_io8**	**register description**
[31:22]	RW	10'h0	reserved	
[21:16]	RW	6'h0	r_func_io34_sel	pad 34 full mux function select
[15:14]	RW	2'h0	reserved	
[13:8]	RW	6'h0	r_func_io33_sel	pad 33 full mux function select
[7:6]	RW	2'h0	reserved	
[5:0]	RW	6'h0	r_func_io32_sel	pad 32 full mux function select
0x4C			**key_scan_in_en**	**register description**
[31:16]	RW	16'h0	reserved	
[15:0]	RW	16'h0	r_kscan_in_en	key scan in enable
0x50			**key_scan_out_en**	**register description**
[31:18]	RW	14'h0	reserved	
[17:0]	RW	18'h0	r_kscan_out_en	key scan out enable

表 10：IOMUX 注册表

3.9.2 寄存器注册表

物理 IO 控件相关信息如下所示。

Base address: 4000_F000

0xF008			IOCTL0
[31 : 30]	RW	2'd0	
[29 : 28]	RW	2'b0	pull up/down control of pin 09 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[27]	RW	1'b0	wake up polarity select of pin 09 0: active POSEDGE 1: active NEGEDGE
[26 : 24]	RW	3'b110	P08 is used for test mode config pin
[23 : 22]	RW	2'b0	pull up/down control of pin 07 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[21]	RW	1'b0	wake up polarity select of pin 07 0: active POSEDGE 1: active NEGEDGE
[20 : 19]	RW	2'b0	pull up/down control of pin 06 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[18]	RW	1'b0	wake up polarity select of pin 06 0: active POSEDGE 1: active NEGEDGE
[17 : 16]	RW	2'b0	pull up/down control of pin 05 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[15]	RW	1'b0	wake up polarity select of pin 05 0: active POSEDGE 1: active NEGEDGE
[14 : 13]	RW	2'b0	pull up/down control of pin 04 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down

[12]	RW	1'b0	wake up polarity select of pin 04 0: active POSEDGE 1: active NEGEDGE
[11 : 10]	RW	2'b11	pull up/down control of pin 03 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[9]	RW	1'b0	wake up polarity select of pin 03 0: active POSEDGE 1: active NEGEDGE
[8 : 7]	RW	2'b0	pull up/down control of pin 02 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[6]	RW	1'b0	wake up polarity select of pin 02 0: active POSEDGE 1: active NEGEDGE
[5 : 4]	RW	2'b0	pull up/down control of pin 01 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[3]	RW	1'b0	wake up polarity select of pin 01 0: active POSEDGE 1: active NEGEDGE
[2 : 1]	RW	2'b0	pull up/down control of pin 00 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[0]	RW	1'b0	wake up polarity select of pin 00 0: active POSEDGE 1: active NEGEDGE
0xF00C			**IOCTL1**
[31 : 30]	RW	2'd0	
[29 : 28]	RW	2'b0	pull up/down control of pin 19 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down

[27]	RW	1'b0	wake up polarity select of pin 19 0: active POSEDGE 1: active NEGEDGE
[26 : 25]	RW	2'b0	pull up/down control of pin 18 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[24]	RW	1'b0	wake up polarity select of pin 18 0: active POSEDGE 1: active NEGEDGE
[23 : 22]	RW	2'b0	pull up/down control of pin 17 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[21]	RW	1'b0	wake up polarity select of pin 17 0: active POSEDGE 1: active NEGEDGE
[20 : 19]	RW	2'b0	pull up/down control of pin 16 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[18]	RW	1'b0	wake up polarity select of pin 16 0: active POSEDGE 1: active NEGEDGE
[17 : 16]	RW	2'b0	pull up/down control of pin 15 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[15]	RW	1'b0	wake up polarity select of pin 15 0: active POSEDGE 1: active NEGEDGE
[14 : 13]	RW	2'b0	pull up/down control of pin 14 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[12]	RW	1'b0	wake up polarity select of pin 14 0: active POSEDGE

			1: active NEGEDGE
[11 : 10]	RW	2'b0	pull up/down control of pin 13 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[9]	RW	1'b0	wake up polarity select of pin 13 0: active POSEDGE 1: active NEGEDGE
[8 : 7]	RW	2'b0	pull up/down control of pin 12 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[6]	RW	1'b0	wake up polarity select of pin 12 0: active POSEDGE 1: active NEGEDGE
[5 : 4]	RW	2'b0	pull up/down control of pin 11 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[3]	RW	1'b0	wake up polarity select of pin 11 0: active POSEDGE 1: active NEGEDGE
[2 : 1]	RW	2'b0	pull up/down control of pin 10 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[0]	RW	1'b0	wake up polarity select of pin 10 0: active POSEDGE 1: active NEGEDGE
0xF010			**IOCTL2**
[31 : 30]	RW	2'd0	
[29 : 28]	RW	2'b0	pull up/down control of pin 29 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[27]	RW	1'b0	wake up polarity select of pin 29 0: active POSEDGE

			1: active NEGEDGE
[26 : 25]	RW	2'b0	pull up/down control of pin 28 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[24]	RW	1'b0	wake up polarity select of pin 28 0: active POSEDGE 1: active NEGEDGE
[23 : 22]	RW	2'b0	pull up/down control of pin 27 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[21]	RW	1'b0	wake up polarity select of pin 27 0: active POSEDGE 1: active NEGEDGE
[20 : 19]	RW	2'b0	pull up/down control of pin 26 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[18]	RW	1'b0	wake up polarity select of pin 26 0: active POSEDGE 1: active NEGEDGE
[17 : 16]	RW	2'b11	pull up/down control of pin 25 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[15]	RW	1'b0	wake up polarity select of pin 25 0: active POSEDGE 1: active NEGEDGE
[14 : 13]	RW	2'b11	pull up/down control of pin 24 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[12]	RW	1'b0	wake up polarity select of pin 24 0: active POSEDGE 1: active NEGEDGE
[11 : 10]	RW	2'b0	pull up/down control of pin 23

			00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[9]	RW	1'b0	wake up polarity select of pin 23 0: active POSEDGE 1: active NEGEDGE
[8 : 7]	RW	2'b0	pull up/down control of pin 22 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[6]	RW	1'b0	wake up polarity select of pin 22 0: active POSEDGE 1: active NEGEDGE
[5 : 4]	RW	2'b0	pull up/down control of pin 21 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[3]	RW	1'b0	wake up polarity select of pin 21 0: active POSEDGE 1: active NEGEDGE
[2 : 1]	RW	2'b0	pull up/down control of pin 20 00: floating, no pull up and pull down 01: weak pull up 10: strong pull up 11: pull down
[0]	RW	1'b0	wake up polarity select of pin 20 0: active POSEDGE 1: active NEGEDGE

表 11：物理 IO 控件注册表

3.10 GPIO

常规的 I/Os 是一种可以映射到物理 I/O 并通过软件进行编辑的外围设备。该 GPIO 共有两个端口。其中，端口 A 设有 18 位双向行，如 GPIO_PORTA[17:0]；端口 B 设有 17 位双向行，如 PIO_PORTB[16:0]。当所有的 GPIOs 均被启用时，如上文的 IOMUX 表中所述，默认设置 P00 至 P17 连接到端口 A；P18 至 P34 连接到端口 B。

通过选择输入或输出方向，所有的端口 A 和端口 B 引脚都可以配置为双向串行接口，其对应的数据可以从寄存器读取或写入寄存器。所有的端口 A 和端口 B 引脚都可用于唤醒，但只有 18 个端口 A 的引脚可用于中断操作。也只有端口 A 引脚支持脱扣功能。
通过调控电阻回复到默认状态的方式，每个 GPIO 引脚都可以调整至 AVDD33 或初始状态。

更多详细信息，请参阅 software SDK 文档文件夹中的“CMT45xx GPIO 应用说明”文档。

#	QFN48	QFN32	Default MODE	Default IN_OUT	IRQ	Wakeup	ANA_IO
0	GPIO_P00	√	jtag_dout	OUT	√	√	
1	GPIO_P01	√	jtag_din	IN	√	√	
2	GPIO_P02	√	jtag_tm	IN	√	√	
3	GPIO_P03	√	jtag_clk	IN	√	√	
4	GPIO_P04		GPIO	IN	√	√	
5	GPIO_P05		GPIO	IN	√	√	
6	GPIO_P06		GPIO	IN	√	√	
7	GPIO_P07		GPIO	IN	√	√	
8	TEST_MODE	√					
9	GPIO_P09	√	GPIO	IN	√	√	
10	GPIO_P10	√	GPIO	IN	√	√	
11	GPIO_P11		GPIO	IN	√	√	ADC_CH1N_P11
12	GPIO_P12		GPIO	IN	√	√	ADC_CH1P_P12
13	GPIO_P13		GPIO	IN	√	√	ADC_CH2N_P13
14	GPIO_P14	√	GPIO	IN	√	√	ADC_CH2P_P14
15	GPIO_P15	√	GPIO	IN	√	√	ADC_CH3N_P15
16	GPIO_P16	√	XTALI(ANA)	ANA	√	√	
17	GPIO_P17	√	XTALO(ANA)	ANA	√	√	
18	GPIO_P18	√	GPIO	IN		√	
19	GPIO_P19		GPIO	IN		√	
20	GPIO_P20	√	GPIO	IN		√	ADC_CH3P_P20
21	GPIO_P21		GPIO	IN		√	
22	GPIO_P22		GPIO	IN		√	
23	GPIO_P23	√	GPIO	IN		√	
24	GPIO_P24	√	GPIO	IN		√	
25	GPIO_P25	√	GPIO	IN		√	
26	GPIO_P26		GPIO	IN		√	
27	GPIO_P27		GPIO	IN		√	
28	GPIO_P28		GPIO	IN		√	
29	GPIO_P29		GPIO	IN		√	

30	GPIO_P30		GPIO	IN	√
31	GPIO_P31	√	**spi_t_ssn**	IN	√
32	GPIO_P32	√	**spi_t_rx**	IN	√
33	GPIO_P33	√	**spi_t_tx**	OUT	√
34	GPIO_P34	√	**spi_t_sck**	IN	√

表 12：CMT45xx GPIO 应用说明

3.10.1 寄存器注册表

GPIOs 相关信息如下所示。

Base address: 0x4000_8000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			**gpio_swporta_dr**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RW	18'b0	Port A Data Register	Values written to this register are output on the I/O signals for Port A
0x04			**gpio_swporta_ddr**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RW	18'b0	Port A Data Direction Register	Values written to this register independently control the direction of the corresponding data bit in Port A 1'b0: Input 1'b1: Output
0x08			**gpio_swporta_ctl**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Port A Data Source	The data and control source for a signal can come from either software or hardware 1'b0: Software mode 1'b1: Hardware mode
0x0c			**gpio_swportb_dr**	
[31:15]	RO	15'b0	Reserved	Reserved
[16:0]	RW	17'b0	Port B Data Register	Values written to this register are output on the I/O signals for Port B
0x10			gpio_swportb_ddr	
[31:15]	RO	15'b0	Reserved	Reserved
[16:0]	RW	17'b0	Port B Data Direction Register	Values written to this register independently control the direction of the corresponding data bit in Port B 1'b0: Input 1'b1: Output
0x14			**gpio_swportb_ctl**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Port B Data Source	The data and control source for a signal can come from either software or hardware 1'b0: Software mode 1'b1: Hardware mode
0x30			**gpio_inten**	

[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RW	18'b0	Interrupt enable	Allows each bit of Port A to be configured for interrupts 1'b0: Configure Port A bit as normal GPIO signal 1'b1: Configure Port A bit as interrupt
0x34			**gpio_intmask**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RW	18'b0	Interrupt mask	Controls whether an interrupt on Port A can create an interrupt for the interrupt controller by not masking it 1'b0: Interrupt bits are unmasked 1'b1: Mask interrupt
0x38			**gpio_inttype_level**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RW	18'b0	Interrupt level	Controls the type of interrupt that can occur on Port A 1'b0: Level-sensitive 1'b1: Edge-sensitive
0x3c			**gpio_int_polarity**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RW	18'b0	Interrupt polarity	Controls the polarity of edge or level sensitivity that can occur on input of Port A 1'b0: Active-low or falling-edge 1'b1: Active-high or rising-edge
0x40			**gpio_intstatus**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RO	18'b0	Interrupt status	Interrupt status of Port A
0x44			**gpio_raw_intstatus**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RO	18'b0	Raw interrupt status	Raw interrupt of status of Port A
0x48			**gpio_debounce**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	RW	18'b0	Debounce enable	Controls whether an external signal that is the source of an interrupt needs to be debounced to remove any spurious glitches 1'b0: No debounce 1'b1: Enable debounce
0x4c			**gpio_porta_eoi**	
[31:18]	RO	14'b0	Reserved	Reserved
[17:0]	WO	18'b0	Clear interrupt	Controls the clearing of edge type interrupts from Port A 1'b0: No interrupt clear 1'b1: Clear interrupt
0x50			**gpio_ext_porta**	
[31:18]	RO	14'b0	Reserved	Reserved

[17:0]	RO	18'b0	External Port A	When Port A is configured as Input, then reading this location reads the values on the signal. When the data direction of Port A is set as Output, reading this location reads the data register for Port A
0x54			**gpio_ext_portb**	
[31:17]	RO	15'b0	Reserved	Reserved
[16:0]	RO	17'b0	External Port B	When Port B is configured as Input, then reading this location reads the values on the signal. When the data direction of Port B is set as Output, reading this location reads the data register for Port B
0x60			**gpio_ls_sync**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Synchronization level	Writing a 1 to this register results in all level-sensitive interrupts being synchronized to pclk_intr 1'b0: No synchronization to pclk_intr 1'b1: Synchronize to pclk_intr
0x64			**gpio_id_code**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RO	16'b0	GPIO ID code	This is a user-specified code that a system can read. It can be used for chip identification, and so on
0x6c			**gpio_ver_id_code**	
[31:0]	RO	32'b0	GPIO Component Version	ASCII value for each number in the version
0x74			**gpio_config_reg1**	
[31:21]	RO	11'b0	Reserved	Reserved
[20:16]	RO	5'b0x0f	ENCODED_ID_WIDTH	The value of this register is equal to GPIO_ID_WIDTH-1
[15]	RO	1'b0	GPIO_ID	The value of this register is derived from the GPIO_ID configuration parameter 1'b0: Exclude 1'b1: Include
[14]	RO	1'b0	ADD_ENCODED_PARAMS	The value of this register is derived from the GPIO_ADD_ENCODED_PARAMS configuration parameter 1'b0: False 1'b1: True
[13]	RO	1'b0	DEBOUNCE	The value of this register is derived from the GPIO_DEBOUNCE configuration parameter 1'b0: Exclude 1'b1: Include
[12]	RO	1'b0	PORTA_INTR	The value of this register is derived from the GPIO_PORTA_INTR configuration parameter 1'b0: Exclude 1'b1: Include
[11]	RO	1'b0	Reserved	Reserved
[10]	RO	1'b0	Reserved	Reserved
[9]	RO	1'b0	HW_PORTB	The value of this register is derived from the

				GPIO_HW_PORTB configuration parameter 1'b0: Exclude 1'b1: Include
[8]	RO	1'b0	HW_PORTA	The value of this register is derived from the GPIO_HW_PORTA configuration parameter 1'b0: Exclude 1'b1: Include
[7]	RO	1'b0	Reserved	Reserved
[6]	RO	1'b0	Reserved	Reserved
[5]	RO	1'b0	PORTB_SINGLE_CTL	The value of this register is derived from the GPIO_PORTB_SINGLE_CTL configuration parameter 1'b0: False 1'b1: True
[4]	RO	1'b0	PORTA_SINGLE_CTL	The value of this register is derived from the GPIO_PORTA_SINGLE_CTL configuration parameter 1'b0: False 1'b1: True
[3:2]	RO	2'b0x2	NUM_PORTS	The value of this register is derived from the GPIO_NUM_PORT configuration parameter 2'b00 1 2'b01 2 2'b10 3 2'b11 4
[1:0]	RO	2'b0x2	APB_DATA_WIDTH	The value of this register is derived from the GPIO_APB_DATA_WIDTH configuration parameter 2'b00 8 bits 2'b01 16 bits 2'b10 32 bits 2'b11 Reserved
0x70			**gpio_config_reg2**	
[31:10]	RO	22'b0	Reserved	Reserved
[9:5]	RO	5'b0x0f	ENCODED_ID_PWIDTH_B	The value of this register is equal to GPIO_PWIDTH_B-1
[4:0]	RO	5'b0x11	ENCODED_ID_PWIDTH_A	The value of this register is equal to GPIO_PWIDTH_A-1

表 13：GPIOs 注册表

3.10.2 电气特性

TA = 25℃, VDD = 3V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

表 14：电气特性

4 外设模块

4.1 2.4GHz 无线通信

2.4 GHz 射频收发器多用于全球 ISM 2.4 至 2.4835 GHz 频段的作业之中。无线调制模式和可配置的分组结构使其能够在符合蓝牙®低能耗(BLE)协议的情况下实现交互操作。

- 通用调制格式
  - 具有可配置高斯滤波器的 FSK（可配置调制指数）
  - 半正弦形态的 OQPSK
  - 无线数据传输
  - 传输速率：1Mbps/2Mbps
- 输出功率为-20dBm 至+10dBm 的可编辑发射机，3dB 步进
- RSSI 功能（1 dB 分辨率，±2 dB 精度）
- 接收器灵敏度
  - -97dBm@1Mbps BLE
  - -94dBm@2Mbps BLE
- 嵌入式射频变压器
- 带相位调制的集成 FRAC-N 合成器

4.2 时钟/计数器

此处可以附加一个 24 位的系统时钟，以扩展处理器和 NVIC 的功能。若如此，扩展的 NVIC 功能如下：

- 24 位系统时钟
- 额外的可配置高优先级系统时钟中断装置
- 更多信息请参见 ARMv7-M ARM

通用时钟已包含在设计之中，上述时钟将采用美国新思科技公司的产品 DW_apb_timer。输入时钟将以 4MHz 的速率运行。

4.2.1 寄存器注册表

时钟的相关信息如下所示，且同一时钟有两种模式。

Base address: Timer setA: 4000_1000, timer_setB: 4002_1000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			**Timer1LoadCount**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RW	24'b0	Timer1 Load Count Register	Value to be loaded into Timer1
0x04			**Timer1CurrentValue**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RO	24'b0	Timer1 Current Value Register	Current Value of Timer1
0x08			**Timer1ControlReg**	
[31:3]	RO	29'b0	Reserved	Reserved
[2]	RW	1'b0	Timer Interrupt Mask	Timer interrupt mask for Timer1 1'b0: not masked 1'b1: masked
[1]	RW	1'b0	Timer Mode	Timer mode for Timer1 1'b0: free-running mode 1'b1: user-defined count mode
[0]	RW	1'b0	Timer Enable	Timer enable bit for Timer1 1'b0: disable 1'b1: enable
0x0c			**Timer1EOI**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer1 End of-Interrupt Register	Reading from this register returns all zeroes (0) and clears the interrupt from Timer1
0x10			**Timer1IntStatus**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer1 Interrupt Status Register	Contains the interrupt status for Timer1
0x14			**Timer2LoadCount**	

[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RW	24'b0	Timer2 Load Count Register	Value to be loaded into Timer2
0x18			**Timer2CurrentValue**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RO	24'b0	Timer2 Current Value Register	Current Value of TimerN
0x1c			**Timer2ControlReg**	
[31:3]	RO	29'b0	Reserved	Reserved
[2]	RW	1'b0	Timer Interrupt Mask	Timer interrupt mask for Timer2 1'b0: not masked 1'b1: masked
[1]	RW	1'b0	Timer Mode	Timer mode for Timer2 1'b0: free-running mode 1'b1: user-defined count mode
[0]	RW	1'b0	Timer Enable	Timer enable bit for Timer2 1'b0: disable 1'b1: enable
0x20			**Timer2EOI**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer2 End of-Interrupt Register	Reading from this register returns all zeroes (0) and clears the interrupt from Timer2
0x24			**Timer2IntStatus**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer2 Interrupt Status Register	Contains the interrupt status for Timer2
0x28			**Timer3LoadCount**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RW	24'b0	Timer3 Load Count Register	Value to be loaded into Timer3
0x2c			**Timer3CurrentValue**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RO	24'b0	Timer3 Current Value Register	Current Value of TimerN
0x30			**Timer3ControlReg**	
[31:3]	RO	29'b0	Reserved	Reserved
[2]	RW	1'b0	Timer Interrupt Mask	Timer interrupt mask for Timer3 1'b0: not masked 1'b1: masked
[1]	RW	1'b0	Timer Mode	Timer mode for Timer3 1'b0: free-running mode 1'b1: user-defined count mode
[0]	RW	1'b0	Timer Enable	Timer enable bit for Timer3 1'b0: disable 1'b1: enable
0x34			**Timer3EOI**	

[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer3 End of-Interrupt Register	Reading from this register returns all zeroes (0) and clears the interrupt from Timer3
0x38			**Timer3IntStatus**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer3 Interrupt Status Register	Contains the interrupt status for Timer3
0x3c			**Timer4LoadCount**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RW	24'b0	Timer4 Load Count Register	Value to be loaded into Timer4
0x40			**Timer4CurrentValue**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:0]	RO	24'b0	Timer4 Current Value Register	Current Value of Timer4
0x44			**Timer4ControlReg**	
[31:3]	RO	29'b0	Reserved	Reserved
[2]	RW	1'b0	Timer Interrupt Mask	Timer interrupt mask for Timer4 1'b0: not masked 1'b1: masked
[1]	RW	1'b0	Timer Mode	Timer mode for Timer4 1'b0: free-running mode 1'b1: user-defined count mode
[0]	RW	1'b0	Timer Enable	Timer enable bit for Timer4 1'b0: disable 1'b1: enable
0x48			**Timer4EOI**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer4 End of-Interrupt Register	Reading from this register returns all zeroes (0) and clears the interrupt from Timer4
0x4c			**Timer4IntStatus**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	Timer4 Interrupt Status Register	Contains the interrupt status for Timer4
0xa0			**TimersIntStatus**	
[31:4]	RO	28'b0	Reserved	Reserved
[3:0]	RO	4'b0	Timers Interrupt Status Register	Contains the interrupt status of all timers in the component 0: either timer_intr or timer_intr_n is not active after masking 1: either timer_intr or timer_intr_n is active after masking
0xa4			**TimersEOI**	
[31:4]	RO	28'b0	Reserved	Reserved
[3:0]	RO	4'b0	Timers End of-Interrupt Register	Reading this register returns all zeroes (0) and clears all active interrupts
0xa8			**TimersRawIntStatus**	

[31:4]	RO	28'b0	Reserved	Reserved
[3:0]	RO	4'b0	Timers Raw Interrupt Status Register	The register contains the unmasked interrupt status of all timers in the component 0: either timer_intr or timer_intr_n is not active prior to masking 1: either timer_intr or timer_intr_n is active prior to masking
0xac		**TimersRawIntStatus**		
[31:0]	RO	32'b0	Timers Component Version	Current revision number of the DW_apb_timers component

表 14：计时器注册表

4.3 实时计数器

实时计数器（RTC）模块提供了一个通用的低频时钟源低功耗定时器。RTC 拥有一个 24 位计数器、一个 12 位(1/X)预分频器、具有捕获/比较寄存器，和一个 tick 事件生成器用于低功耗、无 tick 的 RTOS 应用实现。

4.3.1 寄存器注册表

RTC 相关信息如下所示。

Base address: 4000_F000

0xF024			**RTCCTL**
[31 : 24]	RW	8'h0	
[23]	RW	1'b0	Counter overflow event enable. 1'b0: disable 1'b1: enable
[22]	RW	1'b0	Comparator 2 event enable. 1'b0: disable 1'b1: enable
[21]	RW	1'b0	Comparator 1 event enable. 1'b0: disable 1'b1: enable
[20]	RW	1'b0	Comparator 0 event enable. 1'b0: disable 1'b1: enable
[19]	RW	1'b0	RTC tick event enable. 1'b0: disable 1'b1: enable
[18]	RW	1'b0	Counter overflow interrupt enable. 1'b0: disable

			1'b1: enable
[17]	RW	1'b0	Comparator 2 interrupt enable. 1'b0: disable 1'b1: enable
[16]	RW	1'b0	Comparator 1 interrupt enable. 1'b0: disable 1'b1: enable
[15]	RW	1'b0	Comparator 0 interrupt enable. 1'b0: disable 1'b1: enable
[14]	RW	1'b0	RTC tick interrupt enable. 1'b0: disable 1'b1: enable
[13 : 2]	RW	12'h0	12bit prescaler for RTC counter frequency (32768/(PRESCALER+1)).Can be written only when RTC is stopped.
[1]	RW	1'b0	RTC counter clear bit. Write 1'b1 will clear RTC counter and after one clock this bit will return to 1'b0.
[0]	RW	1'b0	RTC run/stop control. 1'b0: stop 1'b1: run
0xF028			**RTCCNT**
[31 : 24]	RO	8'h0	
[23 : 0]	RO	24'h0	Writing32'h5A5AA5A5 can trigger the overflow task that sets the RTC counter value to 24'hFFFFF0 to allow SW test of the overflow condition. Reading can read the value of RTC counter (low 24 bits).
0xF02C			**RTCCC0**
[31 : 24]	RW	8'h0	
[23 : 0]	RW	24'h0	Compare value of comparator 0
0xF030			**RTCCC1**
[31 : 24]	RW	8'h0	
[23 : 0]	RW	24'h0	Compare value of comparator 1
0xF034			**RTCCC2**
[31 : 24]	RW	8'h0	
[23 : 0]	RW	24'h0	Compare value of comparator 2
0xF038			**RTCFLAG**
[31 : 4]	R	28'h0	
[3]	RO	1'b0	Overflow result flag.
[2]	RO	1'b0	Compare result flag of comparator 2.
[1]	RO	1'b0	Compare result flag of comparator 1.
[0]	RO	1'b0	Compare result flag of comparator 0.

表 15：RTC 注册表

4.4 AES-ECB 加密

ECB 加密模块支持 128 位的 AES 加密，它可以用于一系列加密函数，如哈希生成、数字签名和用于数据加密/解密的密钥流生成。

4.4.1 寄存器注册表

AES-ECB 加密模块的相关信息如下所示。

Base address:4004_0000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00				**AES layer enable register**
[31:1]	—	31'b0	reserved	
[0]	RW	1'b0	Enable	Setting this bit to “1” will enable AES to do TX/RX
0x04				**AES layer control register**
[31:17]	—	15'b0	reserved	
[16]	RW	1'b0	Fifo out/in（PDU）	if pdu is little-endian set 0;if pdu is big-endian set 1
[15:12]	—	4'b0	reserved	
[11:8]	RW	4'b0	Enginne revert	[11]:data out: if it is little-endian set 0 if it is big-endian set 1 [10]:xor data :1 [9]: key : if it is little-endian set 0 if it is big-endian set 1 [8]:data if it is little-endian set 0 if it is big-endian set 1
[7:5]	—	3'b0	reserved	
[4]	RW	1'b0	Aes_single mode	Aes single mode
[3]	RW	1'b0	Code_mode	Encript /decript
[2:0]	—	3'b0	reserved	
0x08				**AES reserved register**
[31:0]	—	32'b0	reserved	
0x0c				**AES plen & aad register**
[31:16]	—	16'b0	reserved	
[15:8]	RW	8'b0	plen	Packet length
[7:0]	RW	8'b0	aad	aad
0x10				**AES interrupt mask register**
[31:4]	—	28'b0	reserved	

[3:0]	RW	4'b0	Aes interupt enable	[0]: encript done;[1]: decript failed;[2[: decript ok;[3] single mode done
0x14				**AES interrupt status register**
[31:4]	—	28'b0	reserved	
[3:0]	RO	4'b0	Aes interupt status	[0]: encript done;[1]: decript failed;[2[: decript ok;[3] single mode done
0x18				**AES reserved register**
[31:0]	—	32'b0	reserved	
0x1C				**AES reserved register**
[31:0]	—	32'b0	reserved	
0x20				**AES key0 register**
[31:0]	RW	32'b0	Key0[31:0]	Key[31:0]
0x24				**AES key1 register**
[31:0]	RW	32'b0	Key1[31:0]	Key[63:32]
0x28				**AES key2 register**
[31:0]	RW	32'b0	Key2[31:0]	Key[95:64]
0x2C				**AES key3 register**
[31:0]	RW	32'b0	Key3[31:0]	Key[127:96]
0x30				**AES nonce0 register**
[31:0]	RW	32'b0	Nonce0[31:0]	Single mode:data_in[31;0];ECB-CCM:Nonce[31:0]
0x34				**AES nonce1 register**
[31:0]	RW	32'b0	Nonce1[31:0]	Single mode:data_in[31;0];ECB-CCM:Nonce[63:32]
0x38				**AES nonce2 register**
[31:0]	RW	32'b0	Nonce2[31:0]	Single mode:data_in[31;0];ECB-CCM:Nonce[95:64]
0x3C				**AES nonce3 register**
[31:0]	RW	32'b0	Nonce3[31:0]	Single mode:data_in[31;0];ECB-CCM:Nonce[127:96]
0x50				**AES data out 0(single mode) register**
[31:0]	RO	32'b0	Data_o0[31:0]	Data_out[31:0]
0x54				**AES data out 1(single mode) register**
[31:0]	RO	32'b0	Data_o1[31:0]	Data_out[63:32]
0x58				**AES data out 2(single mode) register**
[31:0]	RO	32'b0	Data_o2[31:0]	Data_out[95:64]
0x5C				**AES data out 3(single mode) register**
[31:0]	RO	32'b0	Data_o3[31:0]	Data_out[127:96]
0x100				**AES memory (0x0100~0x01FC)**
[31:0]	RW	32'b0	memory write	Writing offset address 0x100~0x1FC will write data into aes memory

表 16: AES-ECB 注册表

4.5 随机数发生器（RNG）

随机数发生器(RNG)根据内部热噪声产生真实的非确定性随机数，这些随机数可用于加密目的。RNG 不需要种子值。

4.6 监视时钟(WDT)

使用低频时钟源(LFCLK)的倒计时监视时钟为防止应用程序锁定提供了可配置的强有力保护措施。当低功耗程序的 CPU 进入长时间休眠状态或调试器强制停止 CPU 时，监视时钟将停止工作。

4.7 SPI

SPI 接口支持 3 个串行同步协议，分别是 SPI、SSP 和 Microwire 串行协议。SPI 包含一个 SPI 主机和一个 SPI 副机，它们在逻辑上是互斥的，每次只能启动一个区块。主机和副机的操作模式由 COM 区块中的 PERI_MASTER_SELECT 寄存器控制。

bit	Reset value	Definition
1	0	SPI1 is master mode when set
0	0	SPI0 is master mode when set

表 17: PERI_MASTER_SELECT 的寄存器定位
(base address = 0x4000_302C)

4.7.1 寄存器注册表

SPI0 和 SPI1 的配置寄存器相关信息如下所示。

Base address: SPI0: 4000_6000; SPI1: 4000_7000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			CTRLR0	
[31:16]	RO	16'b0	Reserved	Reserved
[15:12]	RW	4'b0	CFS	Control Frame Size.Selects the length of the control word for the Microwire frame format
[11]	RW	1'b0	SRL	Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input 1'b0: Normal Mode Operation 1'b1: Test Mode Operation
[10]	RW	1'b0	SLV_OE	Slave Output Enable 1'b0: Slave txd is enabled 1'b1: Slave txd is disabled
[9:8]	RW	2'b0	TMOD	Transfer Mode. Selects the mode of transfer for serial communication. 2'b00: Transmit & Receive 2'b01: Transmit Only 2'b10: Receive Only 2'b11: EEPROM Read
[7]	RW	1'b0	SCPOL	Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock 1'b0: Inactive state of serial clock is low 1'b1: Inactive state of serial clock is high

[6]	RW	1'b0	SCPH	Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal 1'b0: Serial clock toggles in middle of first data bit 1'b1: Serial clock toggles at start of first data bit
[5:4]	RW	2'b0	FRF	Frame Format. Selects which serial protocol transfers the data 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11: Reserved
[3:0]	RW	4'b0x7	DFS	Data Frame Size. Selects the data frame length
0x04			**CTRLR1**	**DW_apb_ssi is configured as a master device**
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	NDF	Number of Data Frames
0x08			**SSIENR**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	SSI_EN	This register enables and disables the DW_apb_ssi 1'b0: disable 1'b1: enable
0x0c			**MWCR**	
[31:3]	RO	29'b0	Reserved	Reserved
[2]	RW	1'b0	MHS	Microwire Handshaking 1'b0: disabled 1'b1: enabled
[1]	RW	1'b0	MDD	Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used
[0]	RW	1'b0	MWMOD	Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential 1'b0: non-sequential transfer 1'b1: sequential transfer
0x10			**SER**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	SER	Slave Select Enable Flag 1'b0: non-sequential transfer 1'b1: sequential transfer
0x14			**BAUDR**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	SCKDV	SSI Clock Divider
0x18			**TXFTLR**	
[31:3]	RO	29'b0	Reserved	Reserved
[2:0]	RW	3'b0	TFT	Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt
0x1c			**RXFTLR**	
[31:3]	RO	29'b0	Reserved	Reserved

[2:0]	RW	3'b0	RFT	Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt
0x20			**TXFLR**	
[31:4]	RO	28'b0	Reserved	Reserved
[3:0]	RO	4'b0	TXTFL	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO
0x24			**RXFLR**	
[31:4]	RO	28'b0	Reserved	Reserved
[3:0]	RO	4'b0	RXTFL	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO
0x28			**SR**	
[31:7]	RO	25'b0	Reserved	Reserved
[6]	RO	1'b0	DCOL	Data Collision Error 1'b0: No error 1'b1: Transmit data collision error
[5]	RO	1'b0	TXE	Transmission Error.Set if the transmit FIFO is empty when a transfer is started 1'b0: No error 1'b1: Transmission error
[4]	RO	1'b0	RFF	Receive FIFO Full 1'b0: not full 1'b1: full
[3]	RO	1'b0	RFNE	Receive FIFO Not Empty 1'b0: empty 1'b1: not empty
[2]	RO	1'b1	TFE	Transmit FIFO Empty 1'b0: not empty 1'b1: empty
[1]	RO	1'b1	TFNF	Transmit FIFO Not Full 1'b0: full 1'b1: not full
[0]	RO	1'b0	BUSY	SSI Busy Flag 1'b0: DW_apb_ssi is idle or disabled 1'b1: DW_apb_ssi is actively transferring data
0x2c			**IMR**	
[31:6]	RO	26'b0	Reserved	Reserved
[5]	RW	1'b1	MSTIM	Multi-Master Contention Interrupt Mask 1'b0: masked 1'b1: not masked
[4]	RW	1'b1	RXFIM	Receive FIFO Full Interrupt Mask 1'b0: masked 1'b1: not masked
[3]	RW	1'b1	RXOIM	Receive FIFO Overflow Interrupt Mask 1'b0: masked 1'b1: not masked
[2]	RW	1'b1	RXUIM	Receive FIFO Underflow Interrupt Mask 1'b0: masked

				1'b1: not masked
[1]	RW	1'b1	TXOIM	Transmit FIFO Overflow Interrupt Mask 1'b0: masked 1'b1: not masked
[0]	RW	1'b1	TXEIM	Transmit FIFO Empty Interrupt Mask 1'b0: masked 1'b1: not masked
0x30			**ISR**	
[31:6]	RO	26'b0	Reserved	Reserved
[5]	RO	1'b0	MSTIS	Multi-Master Contention Interrupt Status 1'b0: not active 1'b1: active
[4]	RO	1'b0	RXFIS	Receive FIFO Full Interrupt Status 1'b0: not active 1'b1: active
[3]	RO	1'b0	RXOIS	Receive FIFO Overflow Interrupt Status 1'b0: not active 1'b1: active
[2]	RO	1'b0	RXUIS	Receive FIFO Underflow Interrupt Status 1'b0: not active 1'b1: active
[1]	RO	1'b0	TXOIS	Transmit FIFO Overflow Interrupt Status 1'b0: not active 1'b1: active
[0]	RO	1'b0	TXEIS	Transmit FIFO Empty Interrupt Status 1'b0: not active 1'b1: active
0x34			**RISR**	
[31:6]	RO	26'b0	Reserved	Reserved
[5]	RO	1'b0	MSTIR	Multi-Master Contention Raw Interrupt Status 1'b0: not active 1'b1: active
[4]	RO	1'b0	RXFIR	Receive FIFO Full Raw Interrupt Status 1'b0: not active 1'b1: active
[3]	RO	1'b0	RXOIR	Receive FIFO Overflow Raw Interrupt Status 1'b0: not active 1'b1: active
[2]	RO	1'b0	RXUIR	Receive FIFO Underflow Raw Interrupt Status 1'b0: not active 1'b1: active
[1]	RO	1'b0	TXOIR	Transmit FIFO Overflow Raw Interrupt Status 1'b0: not active 1'b1: active
[0]	RO	1'b0	TXEIR	Transmit FIFO Empty Raw Interrupt Status 1'b0: not active 1'b1: active
0x38			**TXOICR**	

[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	TXOICR	Clear Transmit FIFO Overflow Interrupt
0x3c			**RXOICR**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	RXOICR	Clear Receive FIFO Overflow Interrupt
0x40			**RXUICR**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	RXUICR	Clear Receive FIFO Underflow Interrupt
0x44			**MSTICR**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	MSTICR	Clear Multi-Master Contention Interrupt
0x48			**ICR**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	ICR	Clear Interrupts
0x4c			**DMACR**	
[31:2]	RO	30'b0	Reserved	Reserved
[1]	RW	1'b0	TDMAE	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel 1'b0: disable 1'b1: enable
[0]	RW	1'b0	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel 1'b0: disable 1'b1: enable
0x50			**DMATDLR**	
[31:3]	RO	29'b0	Reserved	Reserved
[2:0]	RW	3'b0	DMATDL	Transmit Data Level
0x54			**DMARDLR**	
[31:3]	RO	29'b0	Reserved	Reserved
[2:0]	RW	3'b0	DMARDL	Receive Data Level
0x58			**IDR**	
[31:0]	RO	32'b0	IDCODE	Identification Code
0x5c			**SSI_COMP_VERSION**	
[31:0]	RO	32'b0	SSI_COMP_VERSION	Contains the hex representation of the Synopsys component version
0x60~0x9c			**DR**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	DR	Data Register Read: Receive FIFO buffer Write: Transmit FIFO buffer
0xf4			**RSVD_0**	
[31:0]	RW	32'b0	Reserved	Reserved location for future use
0xf8			**RSVD_1**	
[31:0]	RW	32'b0	Reserved	Reserved location for future use
0xfc			**RX_SAMPLE_DLY**	
[31:8]	RO	24'b0	Reserved	Reserved

[7:0]	RW	8'b0	RSD	Receive Data (rxd) Sample Delay.This register is used to delay the sample of the rxd input signal

表 18：SPI0 和 SPI1 的配置寄存器

4.8 I2C (共有 I2c0, I2c1 两个独立实体)

此 I2C 区块支持 100Khz 和 400Khz 模式，同时支持 7 位地址和 10 位地址，且双线均包含内置的可配置脉冲抑制功能。

4.8.1 寄存器注册表

12C 的相关信息如下所示。

Base address: I2C0: 4000_5000, I2C1: 4000_5800

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			I2C Control Register	
[31:7]	RO	25'b0	Reserved	Reserved
[6]	RW	1'b0	IC_SLAVE_DISABLE	This bit controls whether I2C has its slave disabled 1'b0: slave is enabled 1'b1: slave is disabled
[5]	RW	1'b1	IC_RESTART_EN	Determines whether RESTART conditions may be sent when acting as a master 1'b0: disable 1'b1: enable
[4]	RW	1'b1	IC_10BITADDR_MASTER	Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master 1'b0: 7-bit addressing 1'b1: 10-bit addressing
[3]	RW	1'b1	IC_10BITADDR_SLAVE	When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses 1'b0: 7-bit addressing 1'b1: 10-bit addressing
[2:1]	RW	2'b11	SPEED	These bits control at which speed the DW_apb_i2c operates 2'b01: standard mode 2'b10: fast mode 2'b11: high speed mode
[0]	RW	1'b0	MASTER_MODE	This bit controls whether the DW_apb_i2c master is enabled 1'b0: enable 1'b1: disable
0x04			I2C Target Address Register	
[31:13]	RO	19'b0	Reserved	Reserved
[12]	RW	1'b1	IC_10BITADDR_MASTER	This bit controls whether the DW_apb_i2c

				starts its transfers in 7-or 10-bit addressing mode when acting as a master 1'b0: 7-bit addressing 1'b1: 10-bit addressing
[11]	RW	1'b0	SPECIAL	This bit indicates whether software performs a General Call or START BYTE command 1'b0: ignore bit 10 GC_OR_START and use IC_TAR normally 1'b1: perform special I2C command as specified in GC_OR_START bit
[10]	RW	1'b0	GC_OR_START	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c 1'b0: General Call Address 1'b1: START BYTE
[9:0]	RW	10'b0x055	IC_TAR	This is the target address for any master transaction
0x08			**IC_SAR**	
[31:10]	RO	22'b0	Reserved	Reserved
[9:0]	RW	10'b0x055	IC_SAR	The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used
0x0c			**IC_HS_MADDR**	
[31:3]	RO	29'b0	Reserved	Reserved
[2:0]	RW	3'b1	IC_HS_MAR	This bit field holds the value of the I2C HS mode master code
0x10			**IC_DATA_CMD**	
[31:11]	RO	21'b0	Reserved	Reserved
[10]	WO	1'b0	RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1
[9]	WO	1'b0	STOP	This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1
[8]	WO	1'b0	CMD	This bit controls whether a read or a write is performed 1'b0: Read 1'b1: Write
[7:0]	RW	8'b0	DAT	This register contains the data to be transmitted or received on the I2C bus
0x14			**IC_SS_SCL_HCNT**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	IC_SS_SCL_HCNT	This register must be set before any I2C bus

				transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed
0x18			**IC_SS_SCL_LCNT**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	IC_SS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed
0x1c			**IC_FS_SCL_HCNT**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	IC_FS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed
0x20			**IC_SS_SCL_LCNT**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	IC_FS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed
0x24			**IC_HS_SCL_HCNT**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	IC_HS_SCL_HCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed
0x28			**IC_HS_SCL_LCNT**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b0	IC_HS_SCL_LCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed
0x2c			**IC_INTR_STAT**	
[31:12]	RO	20'b0	Reserved	Reserved
[11]	RO	1'b0	R_GEN_CALL	Set only when a General Call address is received and it is acknowledged
[10]	RO	1'b0	R_START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface
[9]	RO	1'b0	R_STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface
[8]	RO	1'b0	R_ACTIVITY	This bit captures DW_apb_i2c activity and stays set until it is cleared
[7]	RO	1'b0	R_RX_DONE	When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte
[6]	RO	1'b0	R_TX_ABRT	This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the

				transmit FIFO
[5]	RO	1'b0	R_RD_REQ	This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c
[4]	RO	1'b0	R_TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register
[3]	RO	1'b0	R_TX_OVER	Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register
[2]	RO	1'b0	R_RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register
[1]	RO	1'b0	R_RX_OVER	Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device
[0]	RO	1'b0	R_RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register
0x30			**IC_INTR_MASK**	
[31:12]	RW	20'b0	Reserved	Reserved
[11]	RW	1'b1	R_GEN_CALL	mask R_GEN_CALL interrupt status bits
[10]	RW	1'b0	R_START_DET	mask R_START_DET interrupt status bits
[9]	RW	1'b0	R_STOP_DET	mask R_STOP_DET interrupt status bits
[8]	RW	1'b0	R_ACTIVITY	mask R_ACTIVITY interrupt status bits
[7]	RW	1'b1	R_RX_DONE	mask R_RX_DONE interrupt status bits
[6]	RW	1'b1	R_TX_ABRT	mask R_TX_ABRT interrupt status bits
[5]	RW	1'b1	R_RD_REQ	mask R_RD_REQ interrupt status bits
[4]	RW	1'b1	R_TX_EMPTY	mask R_TX_EMPTY interrupt status bits
[3]	RW	1'b1	R_TX_OVER	mask R_TX_OVER interrupt status bits
[2]	RW	1'b1	R_RX_FULL	mask R_RX_FULL interrupt status bits
[1]	RW	1'b1	R_RX_OVER	mask R_RX_OVER interrupt status bits
[0]	RW	1'b1	R_RX_UNDER	mask R_RX_UNDER interrupt status bits
0x34			**IC_RAW_INTR_STAT**	
[31:12]	RO	20'b0	Reserved	Reserved
[11]	RO	1'b0	GEN_CALL	Set only when a General Call address is received and it is acknowledged
[10]	RO	1'b0	START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface
[9]	RO	1'b0	STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface
[8]	RO	1'b0	ACTIVITY	This bit captures DW_apb_i2c activity and stays set until it is cleared
[7]	RO	1'b0	RX_DONE	When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte

[6]	RO	1'b0	TX_ABRT	This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO
[5]	RO	1'b0	RD_REQ	This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c
[4]	RO	1'b0	TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register
[3]	RO	1'b0	TX_OVER	Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register
[2]	RO	1'b0	RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register
[1]	RO	1'b0	RX_OVER	Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device
[0]	RO	1'b0	RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register

0x38			**IC_RX_TL**	
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0	RX_TL	Receive FIFO Threshold Level
0x3c			**IC_TX_TL**	
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0	TX_TL	Transmit FIFO Threshold Level
0x40			**IC_CLR_INTR**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_INTR	Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register
0x44			**IC_CLR_RX_UNDER**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_RX_UNDER	Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register
0x48			**IC_CLR_RX_OVER**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_RX_OVER	Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register
0x4c			**IC_CLR_TX_OVER**	
[31:1]	RO	31'b0	Reserved	Reserved

[0]	RO	1'b0	CLR_TX_OVER	Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register
0x50			**IC_CLR_RD_REQ**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_RD_REQ	Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register
0x54			**IC_CLR_TX_ABRT**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_TX_ABRT	Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register
0x58			**IC_CLR_RX_DONE**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_RX_DONE	Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register
0x5c			**IC_CLR_ACTIVITY**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_ACTIVITY	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set
0x60			**IC_CLR_STOP_DET**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_STOP_DET	Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register
0x64			**IC_CLR_START_DET**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_START_DET	Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register
0x68			**IC_CLR_GEN_CALL**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RO	1'b0	CLR_GEN_CALL	Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register
0x6c			**IC_ENABLE**	
[31:2]	RO	30'b0	Reserved	Reserved
[1]	RW	1'b0	ABORT	When set, the controller initiates the transfer abort 1'b0: ABORT not initiated or ABORT done 1'b1: ABORT operation in progress
[0]	RW	1'b0	ENABLE	Controls whether the DW_apb_i2c is enabled 1'b0: disable

				1'b1: enable
0x70			**IC_STATUS**	
[31:7]	RO	25'b0	Reserved	Reserved
[6]	RO	1'b0	SLV_ACTIVITY	Slave FSM Activity Status 1'b0: in IDLE state 1'b1: not in IDLE state
[5]	RO	1'b0	MST_ACTIVITY	Master FSM Activity Status 1'b0: in IDLE state 1'b1: not in IDLE state
[4]	RO	1'b0	RFF	Receive FIFO Completely Full 1'b0: not full 1'b1: full
[3]	RO	1'b0	RFNE	Receive FIFO Not Empty 1'b0: empty 1'b1: not empty
[2]	RO	1'b1	TFE	Transmit FIFO Completely Empty 1'b0: not empty 1'b1: empty
[1]	RO	1'b1	TFNF	Transmit FIFO Not Full 1'b0: full 1'b1: not full
[0]	RO	1'b0	ACTIVITY	I2C Activity Status
0x74			**IC_TXFLR**	
[31:4]	RO	28'b0	Reserved	Reserved
[3:0]	RO	4'b0	TXFLR	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO
0x78			**IC_RXFLR**	
[31:4]	RO	28'b0	Reserved	Reserved
[3:0]	RO	4'b0	RXFLR	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO
0x7c			**IC_RXFLR**	
[31:16]	RO	16'b0	Reserved	Reserved
[15:0]	RW	16'b1	IC_SDA_HOLD	Sets the required SDA hold time in units of ic_clk period
0x80			**IC_TX_ABRT_SOURCE**	
[31:24]	RO	8'b0	TX_FLUSH_CNT	This field preserves the TXFLR value prior to the last TX_ABRT event
[23:17]	RO	7'b0	Reserved	Reserved
[16]	RO	1'b0	ABRT_USER_ABRT	This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1])
[15]	RO	1'b0	ABRT_SLVRD_INTX	When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register
[14]	RO	1'b0	ABRT_SLV_ARBLOST	Slave lost the bus while transmitting data to a remote master
[13]	RO	1'b0	ABRT_SLVFLUSH_TXFIFO	Slave has received a read command and some data exists in the TX FIFO so the slave

				issues a TX_ABRT interrupt to flush old data in TX FIFO
[12]	RO	1'b0	ARB_LOST	Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration
[11]	RO	1'b0	ABRT_MASTER_DIS	User tries to initiate a Master operation with the Master mode disabled
[10]	RO	1'b0	ABRT_10B_RD_NORSTRT	The restart is disabled(IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode
[9]	RO	1'b0	ABRT_SBYTE_NORSTRT	The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte
[8]	RO	1'b0	ABRT_HS_NORSTRT	The restart is disabled(IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode
[7]	RO	1'b0	ABRT_SBYTE_ACKDET	Master has sent a START Byte and the START Byte was acknowledged (wrong behavior)
[6]	RO	1'b0	ABRT_HS_ACKDET	Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior)
[5]	RO	1'b0	ABRT_GCALL_READ	DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1)
[4]	RO	1'b0	ABRT_GCALL_NOACK	DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call
[3]	RO	1'b0	ABRT_TXDATA_NOACK	This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s)
[2]	RO	1'b0	ABRT_10ADDR2_NOACK	Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave
[1]	RO	1'b0	ABRT_10ADDR1_NOACK	Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave
[0]	RO	1'b0	ABRT_7B_ADDR_NOACK	Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave
0x84			**IC_SLV_DATA_NACK_ONLY**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	NACK	Generate NACK 1'b0: generate NACK after data byte received

				1'b1: generate NACK/ACK normally
0x88			**IC_DMA_CR**	
[31:2]	RO	30'b0	Reserved	Reserved
[1]	RW	1'b0	TDMAE	Transmit DMA Enable 1'b0: disable 1'b1: enable
[0]	RW	1'b0	RDMAE	Receive DMA Enable 1'b0: disable 1'b1: enable
0x8c			**IC_DMA_TDLR**	
[31:3]	RO	29'b0	Reserved	Reserved
[2:0]	RW	3'b0	DMATDL	Transmit Data Level
0x90			**IC_DMA_RDLR**	
[31:3]	RO	29'b0	Reserved	Reserved
[2:0]	RW	3'b0	DMARDL	Receive Data Level
0x94			**IC_SDA_SETUP**	
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0x64	SDA_SETUP	SDA Setup
0x98			**IC_ACK_GENERAL_CALL**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b1	ACK_GEN_CALL	ACK General Call
0x9c			**IC_ENABLE_STATUS**	
[31:3]	RO	31'b0	Reserved	Reserved
[2]	RO	1'b0	SLV_RX_DATA_LOST	Slave Received Data Lost
[1]	RO	1'b0	SLV_DISABLED_WHILE_BUSY	Slave Disabled While Busy (Transmit, Receive)
[0]	RO	1'b0	IC_EN	ic_en Status 1'b0: DW_apb_i2c is deemed completely inactive 1'b1: DW_apb_i2c is deemed to be in an enabled state
0xa0			**IC_FS_SPKLEN**	
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0xff	IC_FS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation
0xa4			**IC_HS_SPKLEN**	
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0xff	IC_HS_SPKLEN	This register must be set before any I2C bus transaction can take place to ensure stable operation
0xf4			**IC_COMP_PARAM_1**	
[31:24]	RO	8'b0	Reserved	Reserved
[23:16]	RO	8'b0	TX_BUFFER_DEPTH	The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter 8'b0x00: Reserved 8'b0x01: 2 8'b0x02: 3

				… 8'b0xff: 256
[15:8]	RO	8'b0	RX_BUFFER_DEPTH	The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. For a description of this parameter 8'b0x00: Reserved 8'b0x01: 2 8'b0x02: 3 … 8'b0xff: 256
[7]	RO	1'b0	ADD_ENCODED_PARAMS	The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. 1'b0: False 1'b1: True
[6]	RO	1'b0	HAS_DMA	The value of this register is derived from the IC_HAS_DMA coreConsultant parameter 1'b0: False 1'b1: True
[5]	RO	1'b0	INTR_IO	The value of this register is derived from the IC_INTR_IO coreConsultant parameter 1'b0: Individual 1'b1: Combined
[4]	RO	1'b0	HC_COUNT_VALUES	The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter 1'b0: False 1'b1: True
[3:2]	RO	2'b0	MAX_SPEED_MODE	The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter 2'b00: Reserved 2'b01: Standard 2'b10: Fast 2'b11: High
[1:0]	RO	2'b0	APB_DATA_WIDTH	The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter 2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits 2'b11: Reserved
0xf8			**IC_COMP_VERSION**	
[31:0]	RO	32'b0	IC_COMP_VERSION	Specific values for this register are described in the Releases Table in the AMBA 2 release notes
0xfc			**IC_COMP_TYPE**	
[31:0]	RO	32'b0	IC_COMP_TYPE	This assigned unique hex value is constant

	and is derived from the two ASCII letters "DW" followed by a 16-bit unsigned number

表 19：I2C 注册表

4.9 UART

通用异步收发器提供快速、全双工、高达 1Mbps 波特率的异步串行通信，同时还支持第 9 位数据的奇偶校验和生成。

每个 UART 接口所使用的 GPIOs 均可从设备上的任何 GPIO 中选择，并且是独立可配置的。这不仅增加了设备引脚的灵活性，也使得电路板空间和信号路由的利用更具效率。

4.9.1 寄存器注册表

UART 的相关信息如下所示。

Base address: 4000_4000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			**RBR(Receive Buffer Register)**	**LCR[7] bit = 0**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RO	8'b0	Receive Buffer Register	LSR[0] bit = 1,The data in this register is valid
0x00			**THR(Transmit Holding Register)**	**LCR[7] bit = 0**
[31:8]	WO	24'b0	Reserved	Reserved
[7:0]	WO	8'b0	Transmit Holding Register	LSR[5] bit = 1,The data should only be written to the THR
0x00			**DLL(Divisor Latch Low)**	**1.When UART_16550 == YES,Then LCR[7] bit = 1 2.When UART_16550 == NO,Then LCR[7] bit = 1,USR[0] = 0**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0	Divisor Latch (low)	baud rate = (serial clock freq) / (16 * divisor)
0x04			**DLH(Divisor Latch High)**	**1.When UART_16550 == YES,Then LCR[7] bit = 1 2.When UART_16550 == NO,Then LCR[7] bit = 1,USR[0] = 0**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0	Divisor Latch (high)	baud rate = (serial clock freq) / (16 * divisor)
0x04			**IER(Interrupt Enable Register)**	**LCR[7] bit = 0**
[31:8]	RO	24'b0	Reserved	Reserved
[7]	RW	1'b0	PTIME	This is used to enable/disable the generation of THRE Interrupt

				1'b0: disable 1'b1: enable
[6:4]	RO	3'b0	Reserved	Reserved
[3]	RW	1'b0	EDSSI	This is used to enable/disable the generation of Modem Status Interrupt 1'b0: disable 1'b1: enable
[2]	RW	1'b0	ELSI	This is used to enable/disable the generation of Receiver Line Status Interrupt 1'b0: disable 1'b1: enable
[1]	RW	1'b0	ETBEI	This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt 1'b0: disable 1'b1: enable
[0]	RW	1'b0	ERBFI	This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled) 1'b0: disable 1'b1: enable
0x08			**IIR(Interrupt Identity Register)**	
[31:8]	RO	24'b0	Reserved	Reserved
[7:6]	RO	2'b0	FIFOSE	This is used to indicate whether the FIFOs are enabled or disabled 2'b00: disable 2'b11: enable
[5:4]	RO	2'b0	Reserved	Reserved
[3:0]	RO	4'b0001	IID	This is used to indicates the highest priority pending interrupt which can be one of the following types 4'b0000: modem status 4'b0001: no interrupt pending 4'b0010: THR empty 4'b0100: received data available 4'b0110: receiver line status 4'b0111: busy detect 4'b1100: character timeout
0x08			**FCR(FIFO Control Register)**	**FIFO_MODE != NONE**
[31:8]	RO	24'b0	Reserved	Reserved
[7:6]	WO	2'b0	RT	This is used to select the trigger level in the receiver FIFO at which

				the Received Data Available Interrupt is generated,The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO ¼ full 2'b10: FIFO ½ full 2'b11: FIFO 2 less than full
[5:4]	WO	2'b0	TET	This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active,The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO ¼ full 2'b11: FIFO ½ full
[3]	WO	1'b0	DMAM	This determines the DMA signalling mode 1'b0: mode 0 1'b1: mode 1
[2]	WO	1'b0	XFIFOR	This resets the control portion of the transmit FIFO and treats the FIFO as empty
[1]	WO	1'b0	RFIFOR	This resets the control portion of the receive FIFO and treats the FIFO as empty
[0]	WO	1'b0	FIFOE	This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs 1'b0: disable 1'b1: enable
0x0C			**LCR(Line Control Register)**	
[31:8]	RO	24'b0	Reserved	Reserved
[7]	RW	1'b0	DLAB	USR[0]=0,the bit is writeable;This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART 1'b0: disable 1'b1: enable
[6]	RW	1'b0	Break	This is used to cause a break condition to be transmitted to the receiving device
[5]	RO	1'b0	Reserved	Reserved
[4]	RW	1'b0	EPS	USR[0]=0,the bit is writeable;This is used to select between even and odd parity,when parity is enabled (PEN set to one) 1'b0: an odd number of logic 1s is

				transmitted or checked 1'b1: an even number of logic 1s is transmitted or checked
[3]	R W	1'b0	PEN	USR[0]=0,the bit is writeable;enable and disable parity generation and detection in transmitted and received serial character respectively 1'b0: disable 1'b1: enable
[2]	R W	1'b0	STOP	USR[0]=0,the bit is writeable;select the number of stop bits per character that the peripheral transmits and receives 1'b0: 1 stop bit 1'b1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
[1:0]	R W	2'b0	DLS	USR[0]=0,the bit is writeable;This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 2'b00: 5 bits 2'b01: 6 bits 2'b10: 7 bits 2'b11: 8 bits
0x10			**MCR(Modem Control Register)**	
[31:7]	RO	25'b0	Reserved	Reserved
[6]	R W	1'b0	SIRE	SIR_MODE == Enabled,the bit is writeable;enable/disable the IrDA SIR Mode 1'b0: disable 1'b1: enable
[5]	R W	1'b0	Reserved	Reserved
[4]	R W	1'b0	LoopBack	This is used to put the UART into a diagnostic mode for test purposes
[3]	R W	1'b0	OUT2	This is used to directly control the user-designated Output2 (out2_n) output 1'b0: de-asserted (logic 1) 1'b1: asserted (logic 0)
[2]	R W	1'b0	OUT1	This is used to directly control the user-designated Output1 (out1_n) output 1'b0: de-asserted (logic 1)

				1'b1: asserted (logic 0)
[1]	R W	1'b0	Reserved	Reserved
[0]	R W	1'b0	DTR	This is used to directly control the Data Terminal Ready (dtr_n) output 1'b0: de-asserted (logic 1) 1'b1: asserted (logic 0)
0x14			**LSR(Line Status Register)**	
[31:8]	RO	24'b0	Reserved	Reserved
[7]	RO	1'b0	RFE	FIFO_MODE != NONE and FCR[0] = 1,the bit is relevant;This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO 1'b0: no error 1'b1: error
[6]	RO	1'b1	TEMT	Transmitter Empty bit; FIFO_MODE != NONE and FCR[0] = 1,this bit is set whenever the Transmitter Shift Register and the FIFO are both empty FIFO_MODE == NONE and FCR[0] = 0,this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty
[5]	RO	1'b1	THRE	Transmit Holding Register Empty bit
[4]	RO	1'b0	BI	This is used to indicate the detection of a break sequence on the serial input data.
[3]	RO	1'b0	FE	This is used to indicate the occurrence of a framing error in the receiver 1'b0: no framing error 1'b1: framing error
[2]	RO	1'b0	PE	This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set 1'b0: no parity error 1'b1: parity error
[1]	RO	1'b0	OE	This is used to indicate the occurrence of an overrun error 1'b0: no overrun error 1'b1: overrun error
[0]	RO	1'b0	DR	This is used to indicate that the receiver contains at least one

				character in the RBR or the receiver FIFO 1'b0: no data ready 1'b1: data ready
0x18			**MSR(Modem Status Register)**	
[31:8]	RO	24'b0	Reserved	Reserved
[7]	RO	1'b0	DCD	This is used to indicate the current state of the modem control line dcd_n 1'b0: de-asserted (logic 1) 1'b1: asserted (logic 0)
[6]	RO	1'b0	RI	This is used to indicate the current state of the modem control line ri_n 1'b0: de-asserted (logic 1) 1'b1: asserted (logic 0)
[5]	RO	1'b0	DSR	This is used to indicate the current state of the modem control line dsr_n 1'b0: de-asserted (logic 1) 1'b1: asserted (logic 0)
[4]	RO	1'b0	Reserved	Reserved
[3]	RO	1'b0	DDCD	This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read 1'b0: no change on dcd_n since last read of MSR 1'b1: change on dcd_n since last read of MSR
[2]	RO	1'b0	TERI	This is used to indicate that a change on the input ri_n has occurred since the last time the MSR was read 1'b0: no change on ri_n since last read of MSR 1'b1: change on ri_n since last read of MSR
[1]	RO	1'b0	DDSR	This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read 1'b0: no change on dsr_n since last read of MSR 1'b1: change on dsr_n since last read of MSR
[0]	RO	1'b0	Reserved	Reserved

0x1C			**SCR(Scratchpad Register)**	
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0	Scratchpad Register	This register is for programmers to use as a temporary storage space
0x20			**LPDLL(Low Power Divisor Latch Low Register)**	**SIR_LP_RX == Yes**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0	LPDLL	This register makes up the lower 8-bits of a 16-bit,this register that contains the baud rate divisor for the UART
0x24			**LPDLH(Low Power Divisor Latch High Register)**	**SIR_LP_RX == Yes**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RW	8'b0	LPDLH	This register makes up the upper 8-bits of a 16-bit,this register that contains the baud rate divisor for the UART

0x30~0x6c			**SRBR(Shadow Receive Buffer Register)**	**SHADOW == YES and LCR[7] bit = 0**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RO	8'b0	Shadow Receive Buffer Register	This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master
0x30~0x6c			**STHR(Shadow Transmit Holding Register)**	**SHADOW == YES and LCR[7] bit = 0**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	WO	8'b0	Shadow Transmit Holding Register	This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master
0x70			**FAR(FIFO Access Register)**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	FIFO Access Register	Writes have no effect when FIFO_ACCESS == No, always readable,This register is use to enable a FIFO access mode for testing 1'b0: disable 1'b1: enable
0x74			**TFR(Transmit FIFO Read)**	**FIFO_ACCESS == YES**
[31:8]	RO	24'b0	Reserved	Reserved
[7:0]	RO	8'b0	Transmit FIFO Read	FAR[0] = 1,the bit is valid;Reading this register gives the data at the

				top of the transmit FIFO or the data in the THR
0x78			**RFW(Receive FIFO Write)**	**FIFO_ACCESS == YES**
[31:10]	RO	22'b0	Reserved	Reserved
[9]	WO	1'b0	RFFE	FAR[0] = 1,the bit is valid;This bit is used to write framing error detection information to the receive FIFO or the RBR
[8]	WO	1'b0	RFPE	FAR[0] = 1,the bit is valid;This bit is used to write parity error detection information to the receive FIFO or the RBR
[7:0]	WO	8'b0	RFWD	FAR[0] = 1,the bit is valid;This bit of the data that is written to the RFWD is pushed into the receive FIFO or the RBR
0x7C			**USR(UART Status Register)**	
[31:5]	RO	27'b0	Reserved	Reserved
[4]	RO	1'b0	RFF	FIFO_STAT == YES,the bit is vlid;This is used to indicate that the receive FIFO is completely full 1'b0: not full 1'b1: full
[3]	RO	1'b0	RFNE	FIFO_STAT == YES,the bit is vlid;This is used to indicate that the receive FIFO contains one or more entries 1'b0: empty 1'b1: not empty
[2]	RO	1'b1	TFE	FIFO_STAT == YES,the bit is vlid;This is used to indicate that the transmit FIFO is completely empty 1'b0: not empty 1'b1: empty
[1]	RO	1'b1	TFNF	FIFO_STAT == YES,the bit is vlid;This is used to indicate that the transmit FIFO in not full 1'b0: full 1'b1: not full
[0]	RO	1'b0	BUSY	This is indicates that a serial transfer is in progress, when cleared indicates that the DW_apb_uart is idle or inactive 1'b0: idle or inactive 1'b1: busy (actively transferring data)
0x80			**TFL(Transmit FIFO Level)**	**FIFO_STAT == YES;FIFO_ADDR_WIDTH=4**
[31:5]	RO	27'b0	Reserved	Reserved

[4:0]	RO	5'b0	Transmit FIFO Level	This is indicates the number of data entries in the transmit FIFO
0x84			**RFL(Receive FIFO Level)**	**FIFO_STAT == YES;FIFO_ADDR_WIDTH=4**
[31:5]	RO	27'b0	Reserved	Reserved
[4:0]	RO	5'b0	Receive FIFO Level	This is indicates the number of data entries in the receive FIFO
0x88			**SRR(Software Reset Register)**	**SHADOW == YES**
[31:3]	RO	29'b0	Reserved	Reserved
[2]	WO	1'b0	XFR	FIFO_MODE == None,the written have no effect;XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit(FCR[2])
[1]	WO	1'b0	RFR	FIFO_MODE == None,the written have no effect;RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit(FCR[1])
[0]	WO	1'b0	UR	This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion
0x8C			**SRTS(Shadow Request to Send)**	**SHADOW == YES**
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Shadow Request to Send	This is a shadow register for the RTS bit(MCR[1])
0x90			**SBCR(Shadow Break Control Register)**	**SHADOW == YES**
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Shadow Break Control Register	This is a shadow register for the Break bit(LCR[6])
0x94			**SDMAM(Shadow DMA Mode)**	**FIFO_MODE != None and SHADOW == YES**
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Shadow DMA Mode	This is a shadow register for the DMA mode bit(FCR[3]) 1'b0: mode 0 1'b1: mode 1
0x98			**SFE(Shadow FIFO Enable)**	**FIFO_MODE != None and SHADOW == YES**
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Shadow FIFO Enable	This is a shadow register for the FIFO enable bit(FCR[0]) 1'b0: disable 1'b1: enable
0x9C			**SRT(Shadow RCVR Trigger)**	**FIFO_MODE != None and SHADOW == YES**
[31:2]	RO	30'b0	Reserved	Reserved
[1:0]	R	2'b0	Shadow RCVR Trigger	This is a shadow register for the

	W			RCVR trigger bits(FCR[7:6]) 2'b00: 1 character in the FIFO 2'b01: FIFO ¼ full 2'b10: FIFO ½ full 2'b11: FIFO 2 less than full
0xA0			**STET(Shadow TX Empty Trigger)**	**FIFO_MODE != None and THRE_MODE_USER == Enabled and SHADOW == YES**
[31:2]	RO	30'b0	Reserved	Reserved
[1:0]	RW	2'b0	Shadow TX Empty Trigger	THRE_MODE_USER == Disabled,the written have no effect;This is a shadow register for the TX empty trigger bits (FCR[5:4]) 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO ¼ full 2'b11: FIFO ½ full
0xA4			**HTX(Halt TX)**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	RW	1'b0	Halt TX	FIFO_MODE == None,the written have no effect;This register is use to halt transmissions for testing 1'b0: disable 1'b1: enable
0xA8			**DMASA(DMA Software Acknowledge)**	
[31:1]	RO	31'b0	Reserved	Reserved
[0]	WO	1'b0	DMA Software Acknowledge	DMA_EXTRA == No,the written have no effect;This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition
0xF4			**CPR(Component Parameter Register)**	**UART_ADD_ENCODED_PARAMS == YES**
[31:24]	RO	8'b0	Reserved	Reserved
[23:16]	RO	8'b0	FIFO_MODE	8'b0x00: 0 8'b0x01: 16 8'b0x02: 32 …… 8'b0x80: 2048 8'b0x81- 0xff: reserved
[15:14]	RO	2'b0	Reserved	Reserved
[13]	RO	1'b0	DMA_EXTRA	1'b0: FALSE 1'b1: TRUE
[12]	RO	1'b0	UART_ADD_ENCODED_PARAMS	1'b0: FALSE 1'b1: TRUE

[11]	RO	1'b0	SHADOW	1'b0: FALSE 1'b1: TRUE
[10]	RO	1'b0	FIFO_STAT	1'b0: FALSE 1'b1: TRUE
[9]	RO	1'b0	FIFO_ACCESS	1'b0: FALSE 1'b1: TRUE
[8]	RO	1'b0	ADDITIONAL_FEAT	1'b0: FALSE 1'b1: TRUE
[7]	RO	1'b0	SIR_LP_MODE	1'b0: FALSE 1'b1: TRUE
[6]	RO	1'b0	SIR_MODE	1'b0: FALSE 1'b1: TRUE
[5]	RO	1'b0	THRE_MODE	1'b0: FALSE 1'b1: TRUE
[4]	RO	1'b0	AFCE_MODE	1'b0: FALSE 1'b1: TRUE
[3:2]	RO	2'b0	Reserved	Reserved
[1:0]	RO	2'b0	APB_DATA_WIDTH	2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits 2'b11: reserved
0xF8			**UCV(UART Component Version)**	**ADDITIONAL_FEATURES == YES**
[31:0]	RO	32'b0	UART Component Version	ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*
0xFC			**CTR(Component Type Register)**	**ADDITIONAL_FEATURES == YES**
[31:0]	RO	32'b0x4457 0110	Peripheral ID	This register contains the peripherals identification code

表 200: UART 注册表

4.10 DMIC/AMIC 数据通道

语音输入接口支持一个模拟信号 MIC(SAR-ADC）和两个数字信号 MIC(L+R)，支持不同的输出采样率（64KHz、32KHz、16KHz、8KHz）以及不同的语音压缩算法。数字信号麦克风的 PDM 信号采样频率为 1.28MHz(4x320KHz)，L 通道在上升沿采样，R 通道在下降沿采样。PCM-LOG 和 CVDS 的输出数据速率为 64Kbps(8KHz x 8bit)。

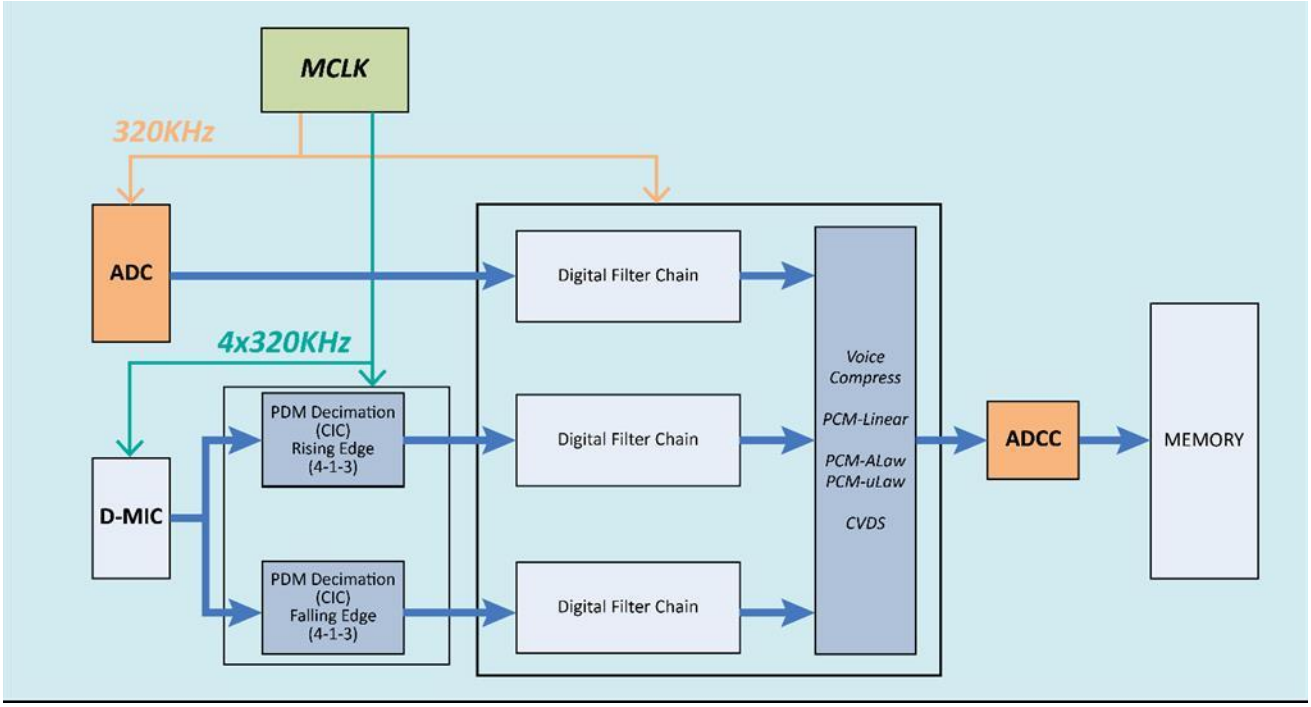


图 11: 语音输入框图

4.11 脉宽调制 (PWM)

CMT4502 系列芯片均支持 6 路脉宽调制(PWM)输出。PWM 的输出将生成可变占空比波形或由寄存器演算得来的脉冲宽度波形。每个 PWM 都可以单独编辑。他们的占空比将由与每个通道相关联的各个计数器控制。

主时钟是 16MHz 的。对于每个 PWM 输出而言，会有一个标度比数值为 2-128（仅支持数值为 2 的正整数幂次的标度比）的预分频器，和一个可编辑的、最大计数表示为 top_count 的 16 位计数器。当 16 位计数器从 0 计数到最大数值时，计数将重置为 0。由此可知，PWM 的频率如下所示：

Freq_PWM = 16MHz / (N_prescaler * N_top_count);

计数器的阈值是可编辑的，当 16 位计数器的计数到达阈值时，PWM 的输出将被切换。由此可知，其占空比如下所示：

Duty_cycle_PWM = N_threshold/N_top_count;

PWM 的极性同样是可编辑的，这意味着当计数低于或高于阈值时，输出将显示为 1 或 0。

PWM 波形与计数器值的关系如图 12 所示，此处极性为正。在这种情况下，数值将迅速上升，然后被重置，称之为“上升模式”。

同时还存在着一种“波动模式”，在这种情况下，数值将迅速上升，随即快速下降，这意味着数值并不会被重置。

综上所述，PWM 通道的关键寄存器位是：16bit top_count、16bit threshold count、3bit precaler

count、PWM 极性、PWM 模式（上升模式或波动模式）、PWM enable、PWM load enable (load new settings)。各个通道均可经由从 0x4000_E004 到 0x4000_E044 的寄存器进行单独编辑。此外，还应该启用寄存器 0x4000_E000<0><4>，以使所有 PWM 通道均可进行编辑。详见 CMT45 系列芯片寄存器注册表文件。

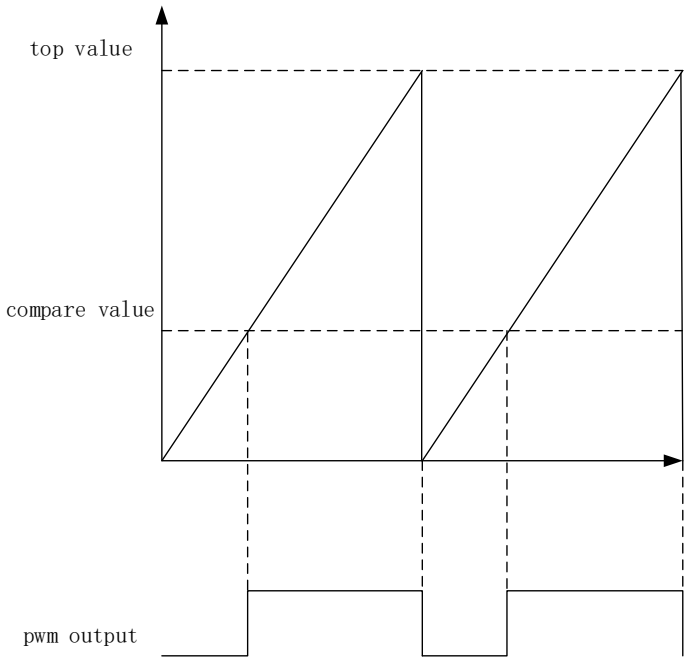


图 12: PWM 图示

4.11.1 寄存器注册表

PWM 的相关信息如下所示。

Base address: 4000_E000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			PWMEN	pwm enable
[31 : 18]	RO	14'b0	reserved	Reserved
[17]	RW	1'b0	pwm_load_45	load parameter of PWM channel 4, 5. need to be conjunction with setting bit16 of PWMxCTL0 registers. 1'b0: no load 1'b1: load
[16]	RW	1'b0	pwm_en_45	enable of PWM channel 4, 5. need to be conjunction with setting bit0 of PWMxCTL0 registers. 1'b0: disable 1'b1: enable
[15]	RW	1'b0	pwm_load_23	load parameter of PWM channel 2, 3. need to be conjunction with setting bit16 of PWMxCTL0 registers. 1'b0: no load 1'b1: load

[14]	RW	1'b0	pwm_en_23	enable of PWM channel 2, 3. need to be conjunction with setting bit0 of PWMxCTL0 registers. 1'b0: disable 1'b1: enable
[13]	RW	1'b0	pwm_load_01	load parameter of PWM channel 0, 1. need to be conjunction with setting bit16 of PWMxCTL0 registers. 1'b0: no load 1'b1: load
[12]	RW	1'b0	pwm_en_01	enable of PWM channel 0, 1. need to be conjunction with setting bit0 of PWMxCTL0 registers. 1'b0: disable 1'b1: enable
[11]	RW	1'b0	pwm_load_345	load parameter of PWM channel 3, 4, 5. need to be conjunction with setting bit16 of PWMxCTL0 registers. 1'b0: no load 1'b1: load
[10]	RW	1'b0	pwm_en_345	enable of PWM channel 3, 4, 5. need to be conjunction with setting bit0 of PWMxCTL0 registers. 1'b0: disable 1'b1: enable
[9]	RW	1'b0	pwm_load_012	load parameter of PWM channel 0, 1, 2. need to be conjunction with setting bit16 of PWMxCTL0 registers. 1'b0: no load 1'b1: load
[8]	RW	1'b0	pwm_en_012	enable of PWM channel 0, 1, 2. need to be conjunction with setting bit0 of PWMxCTL0 registers. 1'b0: disable 1'b1: enable
[7 : 5]	RO	3'b0	reserved	Reserved
[4]	RW	1'b0	pwm_load_all	load parameter of all six PWM channels. need to be conjunction with setting bit16 of PWMxCTL0 registers. 1'b0: no load 1'b1: load
[3 : 1]	RO	3'b0	reserved	Reserved
[0]	RW	1'b0	pwm_en_all	enable of all six PWM channels. need to be conjunction with setting bit0 of PWMxCTL0 registers. 1'b0: disable 1'b1: enable
0x04			**PWM0CTL0**	**pwm channel 0 contrl reigister**
[31]	RW	1'b0	pwm0_load_instant	instant load parameter of PWM channel 0. 1'b0: no load 1'b1: instant load
[30 : 17]	RO	14'b0	reserved	Reserved
[16]	RW	1'b0	pwm0_load	load parameter of PWM channel 0. 1'b0: no load 1'b1: load

[15]	RO	1'b0	reserved	Reserved
[14 : 12]	RW	3'b0	pwm0_clk_div	clock prescaler of PWM channel 0. 3'b000: pwm_clk is divided by 1 for count clock 3'b001: pwm_clk is divided by 2 for count clock 3'b010: pwm_clk is divided by 4 for count clock 3'b011: pwm_clk is divided by 8 for count clock 3'b100: pwm_clk is divided by 16 for count clock 3'b101: pwm_clk is divided by 32 for count clock 3'b110: pwm_clk is divided by 64 for count clock 3'b111: pwm_clk is divided by 128 for count clock
[11 : 9]	RO	3'b0	reserved	Reserved
[8]	RW	1'b0	pwm0_cnt_mode	count mode of PWM channel 0. 1'b0: up mode 1'b1: up and down mode
[7 : 5]	RO	3'b0	reserved	Reserved
[4]	RW	1'b0	pwm0_polarity	output polarity setting of PWM channel 0. 1'b0: rising edge. Second edge within the PWM period is rising 1'b1: falling edge. Second edge within the PWM period is falling
[3 : 1]	RO	3'b0	reserved	Reserved
[0]	RW	1'b0	pwm0_en	enable of PWM channel 0. 1'b0: disable 1'b1: enable
0x08			**PWM0CTL1**	**pwm channel 0 conter value setting**
[31 : 16]	RW	16'b0	pwm0_cmp_val	the compare value of PWM channel 0
[15 : 0]	RW	16'b0	pwm0_cnt_top	the counter top value of PWM channel 0
0x10			**PWM1CTL0**	**pwm channel 1 contrl reigister**
[31]	RW	1'b0	pwm1_load_instant	instant load parameter of PWM channel 1. 1'b0: no load 1'b1: instant load
[30 : 17]	RO	14'b0	reserved	Reserved
[16]	RW	1'b0	pwm1_load	load parameter of PWM channel 1. 1'b0: no load 1'b1: load
[15]	RO	1'b0	reserved	Reserved
[14 : 12]	RW	3'b0	pwm1_clk_div	clock prescaler of PWM channel 1. 3'b000: pwm_clk is divided by 1 for count clock 3'b001: pwm_clk is divided by 2 for count clock 3'b010: pwm_clk is divided by 4 for count clock 3'b011: pwm_clk is divided by 8 for count clock 3'b100: pwm_clk is divided by 16 for count clock 3'b101: pwm_clk is divided by 32 for count clock 3'b110: pwm_clk is divided by 64 for count clock

				3'b111: pwm_clk is divided by 128 for count clock
[11 : 9]	RO	3'b0	reserved	Reserved
[8]	RW	1'b0	pwm1_cnt_mode	count mode of PWM channel 1. 1'b0: up mode 1'b1: up and down mode
[7 : 5]	RO	3'b0	reserved	Reserved
[4]	RW	1'b0	pwm1_polarity	output polarity setting of PWM channel 1. 1'b0: rising edge. Second edge within the PWM period is rising 1'b1: falling edge. Second edge within the PWM period is falling
[3 : 1]	RO	3'b0	reserved	Reserved
[0]	RW	1'b0	pwm1_en	enable of PWM channel 1. 1'b0: disable 1'b1: enable
0x14			**PWM1CTL1**	**pwm channel 1 conter value setting**
[31 : 16]	RW	16'b0	pwm1_cmp_val	the compare value of PWM channel 1
[15 : 0]	RW	16'b0	pwm1_cnt_top	the counter top value of PWM channel 1
0x1C			**PWM2CTL0**	**pwm channel 2 contrl reigister**
[31]	RW	1'b0	pwm2_load_instant	instant load parameter of PWM channel 2. 1'b0: no load 1'b1: instant load
[30 : 17]	RO	14'b0	reserved	Reserved
[16]	RW	1'b0	pwm2_load	load parameter of PWM channel 2. 1'b0: no load 1'b1: load
[15]	RO	1'b0	reserved	Reserved
[14 : 12]	RW	3'b0	pwm2_clk_div	clock prescaler of PWM channel 2. 3'b000: pwm_clk is divided by 1 for count clock 3'b001: pwm_clk is divided by 2 for count clock 3'b010: pwm_clk is divided by 4 for count clock 3'b011: pwm_clk is divided by 8 for count clock 3'b100: pwm_clk is divided by 16 for count clock 3'b101: pwm_clk is divided by 32 for count clock 3'b110: pwm_clk is divided by 64 for count clock 3'b111: pwm_clk is divided by 128 for count clock
[11 : 9]	RO	3'b0	reserved	Reserved
[8]	RW	1'b0	pwm2_cnt_mode	count mode of PWM channel 2. 1'b0: up mode 1'b1: up and down mode
[7 : 5]	RO	3'b0	reserved	Reserved
[4]	RW	1'b0	pwm2_polarity	output polarity setting of PWM channel 2. 1'b0: rising edge. Second edge within the PWM period is rising 1'b1: falling edge. Second edge within the PWM period is falling

[3 : 1]	RO	3'b0	reserved	Reserved
[0]	RW	1'b0	pwm2_en	enable of PWM channel 2. 1'b0: disable 1'b1: enable

0x20		PWM2CTL1	pwm channel 2 conter value setting
[31 : 16]	RW	16'b0	pwm2_cmp_val	the compare value of PWM channel 2
[15 : 0]	RW	16'b0	pwm2_cnt_top	the counter top value of PWM channel 2
0x28		**PWM3CTL0**	**pwm channel 3 contrl reigister**
[31]	RW	1'b0	pwm3_load_instant	instant load parameter of PWM channel 3. 1'b0: no load 1'b1: instant load
[30 : 17]	RO	14'b0	reserved	Reserved
[16]	RW	1'b0	pwm3_load	load parameter of PWM channel 3. 1'b0: no load 1'b1: load
[15]	RO	1'b0	reserved	Reserved
[14 : 12]	RW	3'b0	pwm3_clk_div	clock prescaler of PWM channel 3. 3'b000: pwm_clk is divided by 1 for count clock 3'b001: pwm_clk is divided by 2 for count clock 3'b010: pwm_clk is divided by 4 for count clock 3'b011: pwm_clk is divided by 8 for count clock 3'b100: pwm_clk is divided by 16 for count clock 3'b101: pwm_clk is divided by 32 for count clock 3'b110: pwm_clk is divided by 64 for count clock 3'b111: pwm_clk is divided by 128 for count clock
[11 : 9]	RO	3'b0	reserved	Reserved
[8]	RW	1'b0	pwm3_cnt_mode	count mode of PWM channel 3. 1'b0: up mode 1'b1: up and down mode
[7 : 5]	RO	3'b0	reserved	Reserved
[4]	RW	1'b0	pwm3_polarity	output polarity setting of PWM channel 3. 1'b0: rising edge. Second edge within the PWM period is rising 1'b1: falling edge. Second edge within the PWM period is falling
[3 : 1]	RO	3'b0	reserved	Reserved
[0]	RW	1'b0	pwm3_en	enable of PWM channel 3. 1'b0: disable 1'b1: enable
0x2C		**PWM3CTL1**	**pwm channel 0 conter value setting**
[31 : 16]	RW	16'b0	pwm3_cmp_val	the compare value of PWM channel 3
[15 : 0]	RW	16'b0	pwm3_cnt_top	the counter top value of PWM channel 3
0x34		**PWM4CTL0**	**pwm channel 4 contrl reigister**
[31]	RW	1'b0	pwm4_load_instant	instant load parameter of PWM channel 4. 1'b0: no load

				1'b1: instant load
[30 : 17]	RO	14'b0	reserved	Reserved
[16]	RW	1'b0	pwm4_load	load parameter of PWM channel 4. 1'b0: no load 1'b1: load
[15]	RO	1'b0	reserved	Reserved
[14 : 12]	RW	3'b0	pwm4_clk_div	clock prescaler of PWM channel 4. 3'b000: pwm_clk is divided by 1 for count clock 3'b001: pwm_clk is divided by 2 for count clock 3'b010: pwm_clk is divided by 4 for count clock 3'b011: pwm_clk is divided by 8 for count clock 3'b100: pwm_clk is divided by 16 for count clock 3'b101: pwm_clk is divided by 32 for count clock 3'b110: pwm_clk is divided by 64 for count clock 3'b111: pwm_clk is divided by 128 for count clock
[11 : 9]	RO	3'b0	reserved	Reserved
[8]	RW	1'b0	pwm4_cnt_mode	count mode of PWM channel 4. 1'b0: up mode 1'b1: up and down mode
[7 : 5]	RO	3'b0	reserved	Reserved
[4]	RW	1'b0	pwm4_polarity	output polarity setting of PWM channel 4. 1'b0: rising edge. Second edge within the PWM period is rising 1'b1: falling edge. Second edge within the PWM period is falling
[3 : 1]	RO	3'b0	reserved	Reserved
[0]	RW	1'b0	pwm4_en	enable of PWM channel 4. 1'b0: disable 1'b1: enable
0x38			**PWM4CTL1**	**pwm channel 4 conter value setting**
[31 : 16]	RW	16'b0	pwm4_cmp_val	the compare value of PWM channel 4
[15 : 0]	RW	16'b0	pwm4_cnt_top	the counter top value of PWM channel 4
0x40			**PWM5CTL0**	**pwm channel 5 contrl reigister**
[31]	RW	1'b0	pwm5_load_instant	instant load parameter of PWM channel 5. 1'b0: no load 1'b1: instant load
[30 : 17]	RO	14'b0	reserved	Reserved
[16]	RW	1'b0	pwm5_load	load parameter of PWM channel 5. 1'b0: no load 1'b1: load
[15]	RO	1'b0	reserved	Reserved
[14 : 12]	RW	3'b0	pwm5_clk_div	clock prescaler of PWM channel 5. 3'b000: pwm_clk is divided by 1 for count clock 3'b001: pwm_clk is divided by 2 for count clock 3'b010: pwm_clk is divided by 4 for count clock 3'b011: pwm_clk is divided by 8 for count clock

				3'b100: pwm_clk is divided by 16 for count clock 3'b101: pwm_clk is divided by 32 for count clock 3'b110: pwm_clk is divided by 64 for count clock 3'b111: pwm_clk is divided by 128 for count clock
[11 : 9]	RO	3'b0	reserved	Reserved
[8]	RW	1'b0	pwm5_cnt_mode	count mode of PWM channel 5. 1'b0: up mode 1'b1: up and down mode
[7 : 5]	RO	3'b0	reserved	Reserved
[4]	RW	1'b0	pwm5_polarity	output polarity setting of PWM channel 5. 1'b0: rising edge. Second edge within the PWM period is rising 1'b1: falling edge. Second edge within the PWM period is falling
[3 : 1]	RO	3'b0	reserved	Reserved
[0]	RW	1'b0	pwm5_en	enable of PWM channel 5. 1'b0: disable 1'b1: enable
0x44			**PWM5CTL1**	**pwm channel 5 conter value setting**
[31 : 16]	RW	16'b0	pwm5_cmp_val	the compare value of PWM channel 5
[15 : 0]	RW	16'b0	pwm5_cnt_top	the counter top value of PWM channel 5

表 211: PWM 注册表

4.12 正交解码器 (QDEC)

正交解码器可进行带输入脱扣滤波器的四倍频编码传感信号缓冲解码，适用于机械和光学传感器。可配置示例周期和累积，以匹配应用程序需求。正交解码器支持三轴功能和索引通道，可编程为 4x/2x/1x 计数模式。

4.12.1 寄存器注册表

正交解码器的相关信息如下所示。

Base address: 4000_B000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00				
[31:9]	—	23'b0	reserved	
[8]	RW	1'b0	chnz_en	enable channel z
[7:5]	—	3'b0	reserved	
[4]	RW	1'b0	chny_en	enable channel y
[3:1]	—	3'b0	reserved	
[0]	RW	1'b0	chnx_en	enable channel x
0x04			**int_enable**	
[31:30]	—	2'b0	reserved	
[29]	RW	1'b0	int_quaz_02f_en	enable interupt, counter addition overflow (from 0 to F)

[28]	RW	1'b0	int_quaz_f20_en	enable interupt, counter subtraction overflow (from F to 0)
[27]	RW	1'b0	int_quay_02f_en	
[26]	RW	1'b0	int_quay_f20_en	
[25]	RW	1'b0	int_quax_02f_en	
[24]	RW	1'b0	int_quax_f20_en	
[23]	—	1'b0	reserved	
[22]	RW	1'b0	incz_int_mode	index counter interupt mode 0 index changes, 1 index equals hit
[21]	—	1'b0	reserved	
[20]	RW	1'b0	int_incz_en	enable index counter interupt
[19]	—	1'b0	reserved	
[18]	RW	1'b0	quaz_int_mode	quadrature counter interupt mode 0 index changes, 1 index equals hit
[17]	—	1'b0	reserved	
[16]	RW	1'b0	int_quaz_en	enable quadrature counter interupt
[15]	—	1'b0	reserved	
[14]	RW	1'b0	incy_int_mode	
[13]	—	1'b0	reserved	
[12]	RW	1'b0	int_incy_en	
[11]	—	1'b0	reserved	
[10]	RW	1'b0	quay_int_mode	
[9]	—	1'b0	reserved	
[8]	RW	1'b0	int_quay_en	
[7]	—	1'b0	reserved	
[6]	RW	1'b0	incx_int_mode	
[5]	—	1'b0	reserved	
[4]	RW	1'b0	int_incx_mode	
[3]	—	1'b0	reserved	
[2]	RW	1'b0	quax_int_mode	
[1]	—	1'b0	reserved	
[0]	RW	1'b0	int_quax_en	
0x08			**int_clear**	
[31:30]	—	2'b0	reserved	
[29]	WC	1'b0	quaz_02f_clr	clear 0 to F interupt
[28]	WC	1'b0	quaz_f20_clr	clear F to 0 interupt
[27]	WC	1'b0	quay_02f_clr	
[26]	WC	1'b0	quay_f20_clr	
[25]	WC	1'b0	quax_02f_clr	
[24]	WC	1'b0	quax_f20_clr	
[23:21]	—	3'b0	reserved	
[20]	WC	1'b0	incz_clr	clear index counter interupt
[19:17]	—	3'b0	reserved	
[16]	WC	1'b0	quaz_clr	clear quadrature counter interupt
[15:13]	—	3'b0	reserved	
[12]	WC	1'b0	incy_clr	
[11:9]	—	3'b0	reserved	
[8]	WC	1'b0	quay_clr	

[7:5]	—	3'b0	reserved	
[4]	WC	1'b0	incx_clr	
[3:1]	—	3'b0	reserved	
[0]	WC	1'b0	quax_clr	
0x0C			**int_status**	
[31:30]	—	2'b0	reserved	
[29]	RO	1'b0	int_quaz_02f	0 to F interupt status
[28]	RO	1'b0	int_quaz_f20	F to 0 interupt status
[27]	RO	1'b0	int_quay_02f	
[26]	RO	1'b0	int_quay_f20	
[25]	RO	1'b0	int_quax_02f	
[24]	RO	1'b0	int_quax_f20	
[23:21]	—	3'b0	reserved	
[20]	RO	1'b0	int_inc_z	index counter interupt status
[19:17]	—	3'b0	reserved	
[16]	RO	1'b0	int_qua_z	quadrature counter interupt status
[15:13]	—	3'b0	reserved	
[12]	RO	1'b0	int_inc_y	
[11:9]	—	3'b0	reserved	
[8]	RO	1'b0	int_qua_y	
[7:5]	—	3'b0	reserved	
[4]	RO	1'b0	int_inc_x	
[3:1]	—	3'b0	reserved	
[0]	RO	1'b0	int_qua_x	
0x10				
[31:18]	—	14'b0	reserved	
[17:16]	RW	2'b0	incx_mode	index counter mode 00 high level 01 positive edge 10 negtive edge 11 pos and neg edge
[15:2]	—	14'b0	reserved	
[1:0]	RW	2'b0	quax_mode	quadrature counter mode 01 mode 1x , 10 mode 2x, 11 mode 3x
0x14				
[31:0]	RW	32'b0	quax_hit	to compare with qua_cnt, trigger interupt
0x18				
[31:0]	RW	32'b0	incx_hit	to compare with inc_cnt, trigger interupt
0x1C				
[31:0]	RO	32'b0	quax_cnt	quadrature counter
0x20				
[31:0]	RO	32'b0	incx_cnt	index counter
0x24				
[31:18]	—	14'b0	reserved	
[17:16]	RW	2'b0	incy_mode	
[15:2]	—	14'b0	reserved	
[1:0]	RW	2'b0	quay_mode	
0x28				
[31:0]	RW	32'b0	quay_hit	

0x2C				
[31:0]	RW	32'b0	incy_hit	
0x30				
[31:0]	RO	32'b0	quay_cnt	
0x34				
[31:0]	RO	32'b0	incy_cnt	

0x38				
[31:18]	—	14'b0	reserved	
[17:16]	RW	2'b0	incz_mode	
[15:2]	—	14'b0	reserved	
[1:0]	RW	2'b0	quaz_mode	
0x3C				
[31:0]	RW	32'b0	quaz_hit	
0x40				
[31:0]	RW	32'b0	incz_hit	
0x44				
[31:0]	RO	32'b0	quaz_cnt	
0x48				
[31:0]	RO	32'b0	incz_cnt	
0x3FC				
[31:0]	RW	32'b0	dummy	
[15]	RO	1'b0	reserved	Reserved

表 22：正交解码器注册表

4.13 键扫描(KSCAN)

键扫描最高支持 16 行 18 列的键矩阵，每个行或列均可通过寄存器单独设置启用或禁用，也可以配置 GPIO 引脚用于键扫描。某些键扫描的参数可以通过寄存器设置，包括极性（按键力度）、单按键或多按键、255us 步进的从 0ms 到 128ms 抖动滤波时间（有效按键时间内）。

当键扫描可以执行中断时，有效的按键操作即可触发中断。中断完成后，在中断状态寄存器位中输入“1”即可退出中断状态。

键扫描支持手动模式和自动模式。手动模式下，键扫描收到中断信号，单片机/软件将检查输入引脚并扫描输出引脚，以确定哪些键被按下。手动模式相对较慢，且需要进行 CPU 处理。与之相对，自动模式下，键扫描将自动检查输入和输出引脚，同时将与按下的键对应的行/列信息存储到只读寄存器中，随即触发软件中断并检索按键信息。

4.13.1 寄存器注册表

键扫描的相关信息如下所示。

Base address: 4002_4000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0xC0				

[31:24]	RW	8'h00	mkdi	key scan debounce interval, 0-255, unit: 512uS
[23]	RW	1'b0	mk_pol	key mattrix polarity, 0: active scan high, active sense high; 1: active scan low, active sense low;
[22]	RO	1'b0	reserved	no use/as
[21]	RW	1'b0	asact	auto scan on activity: 0, no auto scan, 1, auto scan on activity
[20]	RW	1'b0	imkp	ignore multi key press
[19:2]	RW	18'h0	ms	mattrix scan outputs enable: 1: enable, 0: disable
[1]	RW	1'b0	ks_ie	key scan interupt enable
[0]	RW	1'b0	ks_en	key scan enable
0xC4				
[31:18]	RO	14'b0	reserved	
[17]	WC	1'b0	mkp	key pressed indicator, 0: no key press, 1: key pressed, write 1 to clear
[16:1]	RO	16'h0FFF	mr	key scan inputs states
[0]	WC	1'b0	mi	interupt state, write 1 to clear interupt, 0: no interupt, 1: interupt issued,
0xC8				
[31:13]	RO	19'b0	reserved	
[12]	RO	1'b0	so	scan on: 1: auto scan is on going, 0: scan off
[11:10]	RO	2'b0	mukp	multi key pressed, 00, no key press, 01: 1 key press, 10, more than 1 key pressed
[9:5]	RO	5'h1F	rp	row of key pressed, only for 1 key pressed case
[4:0]	RO	5'h1F	cp	column of key pressed, only for 1 key pressed case
0xCC				
[31:16]	RO	16'h0	mkc1	column 1 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc0	column 0 key pressed, for multi key pressed case
0xD0				
[31:16]	RO	16'h0	mkc3	column 3 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc2	column 2 key pressed, for multi key pressed case
0xD4				
[31:16]	RO	16'h0	mkc5	column 5 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc4	column 4 key pressed, for multi key pressed case
0xD8				
[31:16]	RO	16'h0	mkc7	column 7 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc6	column 6 key pressed, for multi key pressed case
0xDC				
[31:16]	RO	16'h0	mkc9	column 9 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc8	column 8 key pressed, for multi key pressed case
0xE0				
[31:16]	RO	16'h0	mkc11	column 11 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc10	column 10 key pressed, for multi key pressed case
0xE4				
[31:16]	RO	16'h0	mkc13	column 13 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc12	column 12 key pressed, for multi key pressed case
0xE8				
[31:16]	RO	16'h0	mkc15	column 15 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc14	column 14 key pressed, for multi key pressed case
0xEC				

[31:16]	RO	16'h0	mkc17	column 17 key pressed, for multi key pressed case
[15:0]	RO	16'h0	mkc16	column 16 key pressed, for multi key pressed case
0xF0				
[31:16]	RW	16'h0	reserved	
[15:0]	RW	16'h0FFF	mk_in_en	enable/disable key scan inputs: 0: disable, 1: enable
0xF4				
[31:2]	RW	30'h0	reserved	
[1:0]	RW	2'b0	ks_pena_i	
0xF8				
[31:0]	RW	32'h0	ks_iosel	

表 23: 键扫描注册表

4.14 带可编程增益装置(PGA)的模数转换器(ADC)

12 位的 SAR ADC 共有 10 个输入端口。其中，PGA 输入端口有 2 个，芯片温度传感器差分端口也有 2 个，其余 6 个输入端口可以被编辑为 3 对差分输入端口或 6 个单端输入端口。手动模式下，可设置 ADC，使其能够将某种特殊的输入方式转化为单端或差分输入，且具有特定的 ADC 时钟速率。在自动扫描模式下，ADC 可以自动扫描所有已启用的输入通道，并将转换后的数据存储在相应的内存位置。

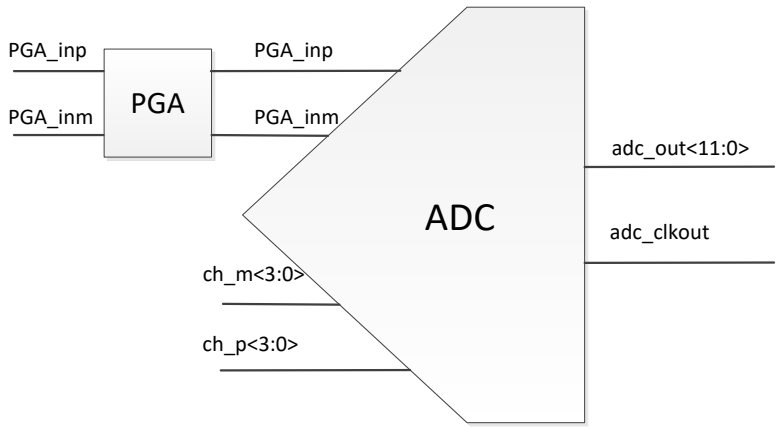


图 13：ADC 示意图

4.14.1 PGA 路径

该 PGA 支持 3 步进下从 0dB 到 42dB 的增益范围。

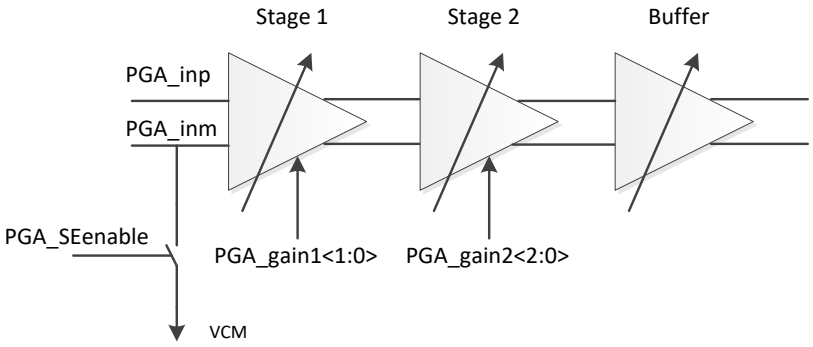


图 14：PGA 路径示意图

pga_gain1<1>	pga_gain1<0>	Stage1 gain (dB)	pga_gain2 <2>	pga_gain2<1>	pga_gain2<0>	Stage2 gain(dB)
0	0	0	0	0	0	0
0	1	12	0	0	1	3
1	0	24	0	1	0	6
			0	1	1	9
			1	0	0	12
			1	0	1	15
			1	1	0	18

表 24：PGA 增益表

通过将 PGA_SEenable 设置为“1”， 可以使 PGA 进入共模电压状态，此时 PGA 将被设置为单端模式。

4.14.2 ADC 路径

默认情况下，ADC 处于手动模式。在此模式下，ADC 采样的时钟速率可被设置为每秒 80k/160k/320k。输入端口可以设置为差分或单端(正或负)输入，默认情况下，它处于差分输入状态。设置完成后启动，ADC 将采用设置的时钟速率进行采样，并将数据储存在与通道相应的内存位置中。所有通道的内存大小均为 128Byte，数据存满即标记一个中断点位。每个 12 位的示例将占用 2Byte 的空间。

0x4000_F07C		Register Description
[4]	adc_ctrl_override	Set manual mode: 1: manual, 0: auto. Default 1
[3]	adc_tconv_sel	For auto mode only, adc conversion time sel: 0: 1.56us, 1: 2.34us
[2:1]	adc_clk_sel	For manual mode only, clksel: 00: 80k, 01: 160k, 10: 320k
[0]	max_rate_256k_320k	For auto mode only, max rate base: 0, 256k, 1, 320k
0x4000_F048		**Register Description**
[11]	adc12b_semode_enm	For manual mode only: 12 bit ADC signle-ended mode negative side enable. Bit<11> Bit<8> cannot both be 1; 1: Enable single-ended mode 0: Differential mode

[8]	Adc12b_semode_epm	For manual mode only: 12 bit ADC signle-ended mode positive side enable. Bit<8> Bit<11> cannot both be 1; 1: Enable single-ended mode 0: Differentail mode
[7:5]	Channel configure	For manual mode only: 12 bit ADC input channel select control bits. adc12_ctrl<3:1> Selected channel 000 PGA inputs, differential 001 Temperature sensing inputs, differential 010 input A, positive and negative 011 input B, positive and negative 100 input C, positive and negative
[3]	ADC enable	12b ADC power up control. 1: Power up ADC 0: Power down ADC

Memory start/end addresses	ADC channels
4005_0400 – 4005_047F	PAG inputs, differential
4005_0480 – 4005_04FF	Temperature sensing, differential
4005_0500 – 4005_057F	Input A, positive or differential
4005_0580 – 4005_05FF	Input A, negative
4005_0600 – 4005_067F	Input B, positive or differential
4005_0680 – 4005_06FF	Input B, negative
4005_0700 – 4005_077F	Input C, positive or differential
4005_0780 – 4005_07FF	Input C, negative

0x4005_003C	ADC interrupt status	Register Description
[7]		input C, negative
[6]		Input C, positive or differential
[5]		Input B, negative
[4]		Input B, positive or differential
[3]		Input A, negative
[2]		Input A, positive or differential
[1]		Temperature sensing, differential
[0]		PGA inputs, differential

0x4005_0038	ADC interrupt write clear	Register Description
[7]		input C, negative, write 1 to clear
[6]		Input C, positive or differential, write 1 to clear
[5]		Input B, negative, write 1 to clear
[4]		Input B, positive or differential, write 1 to clear
[3]		Input A, negative, write 1 to clear
[2]		Input A, positive or differential, write 1 to clear
[1]		Temperature sensing, differential, write 1 to clear
[0]		PGA inputs, differential, write 1 to clear

表 22：ADC 的手动模式

若将“adc_ctrl_override”设置为 0，ADC 即进入自动通道扫描模式，启用的通道将按照配置好的顺序进行自动采样。所有 ADC 输入通道均可通过相应的寄存器编程进行配置，可编辑的配置包括采样时间、启用/禁用、差分/单端和连续采样/单次采样，详见下表。和手动模式一样，采样数据将被储存在与通道相应的内存位置中。

0x4000_F06C	ADC_CTL0	Register Description
[31:16]	Temperature sensing, auto mode, differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	PGA inputs, differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

0x4000_F070	ADC_CTL1	Register Description
[31:16]	Inputs A, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	Input A, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

0x4000_F074	ADC_CTL2	Register Description
[31:16]	Input B, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	Input B, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

0x4000_F078	ADC_CTL3	Register Description
[31:16]	Input C, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	Input C, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

表 23：ADC 通道配置

4.14.3 ADC 通道<3:0>的连通性

PGA inputs	hardwired
temp sensing	hardwired
aio<0>	Input A negative
aio<1>	Input A positive
aio<2>	Input B negative
aio<3>	Input B positive
aio<4>	Input C negative
aio<9>	Input C positive

表 247：ADC 通道连通性

可以通过编辑 aio_pass<7:0>或 aio_attn<7:0>，从模拟 MUX 中选择 Aio<9, 4:0> and PGA inputs(Aio<7:8>)。例如，将寄存器 0x4000_F020<8><0>设置为 01，可将 Aio<0>连接至输入端口 A 的正节点。

0x4000_F020		Register Description
[13:8]	Attenuation ctrl	attn[5:0]. analogIO control for {aio<9>, aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass 10 attenuate to 1/4 11 NC
[5:0]	pass ctrl	pass[5:0]. analogIO control for {aio<9>, aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass 10 attenuate to 1/4 11 NC note: analog IO sharing gpio<11>/aio<0> gpio<12>/aio<1> gpio<13>/aio<2> gpio<14>/aio<3> gpio<15>/aio<4> gpio<16>/aio<5>/32K XTAL input gpio<17>/aio<6>/32K XTAL output gpio<18>/aio<7>/pga in+ gpio<19>/aio<8>/pga in- gpio<20>/aio<9>/mic bias

表 28：Mux 模拟 ADC 通道选择

5 绝对最大额定参数

最大额定参数是指在不会造成永久性损害的情况下，CMT4502 可以运行的极限环境。长时间在最大额定参数环境下运行有可能会影响芯片的可靠性。绝对最大额定参数值详见**表 29**。

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
DEC			1.32	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model Class 2		4	kV
ESD CDMQF	Charged Device Model(QFN48, 7x7 mm package)		750	V
Flash memory				
Endurance			20 000	write/erase cycles
Retention			10 years at 40 °C	
Number of times an address can be written between erase cycles			2	times

表 29：绝对最大额定参数

6 操作环境

操作环境指的是 CMT4502 能够在其中运行的物理参数。详见**表 30。**

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA	Operating temperature	-40	27	85	°C

表 250：CMT4502 操作环境

7 无线收发器

7.1 无线电电流消耗

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	with internal DC-DC @3V		8		mA
Rx Only	with internal DC-DC @3V		8		mA

表 26：无线电电流消耗

7.2 发射器规格

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
Error Vector Measure	Offset EVM for OQPSK modulation		0.02		
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

表 272：发射器规格

7.3 接收器规格

7.3.1 RX BLE 1Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-97		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB

Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3	50	I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3	55	I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3	22	I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3	-20	dBm
Carrier Frequency Offset Tolerance		+-350	KHz
Sample Clock Offset Tolerance		+-120	ppm

表 283：RX BLE 1Mbps GFSK 规格

7.3.2 RX BLE 2Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 2Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-94		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

表 294：RX BLE 2Mbps GFSK 规格

7.4 RSSI 规格

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

表 305：RSSI 规格

8 术语表

Term	Description
AHB	Advanced High-performance Bus (ARM bus standard)
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus (ARM bus standard)
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port (ARM bus standard)
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SWD	Serial Wire DAP (ARM bus standard)
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

表 36：术语表

9 订购资讯

Part No.	Package	Packing	MOQ(PCS)
CMT4502-EQR	QFN32	Tape&Reel	5000
CMT4502-EQR2	QFN48	Tape&Reel	3000

表 37：订购资讯

10 芯片打标

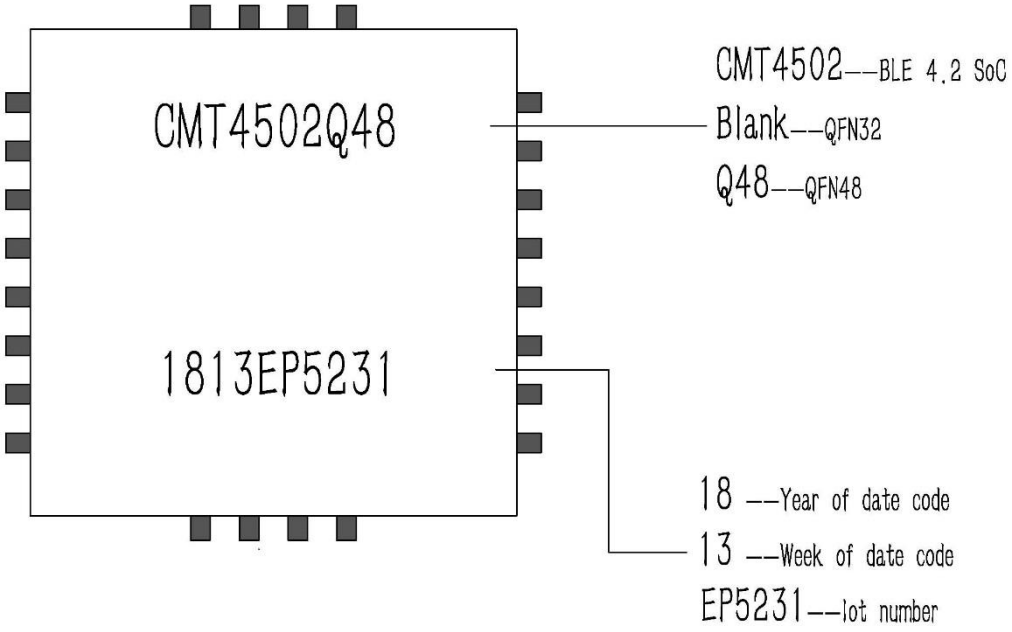
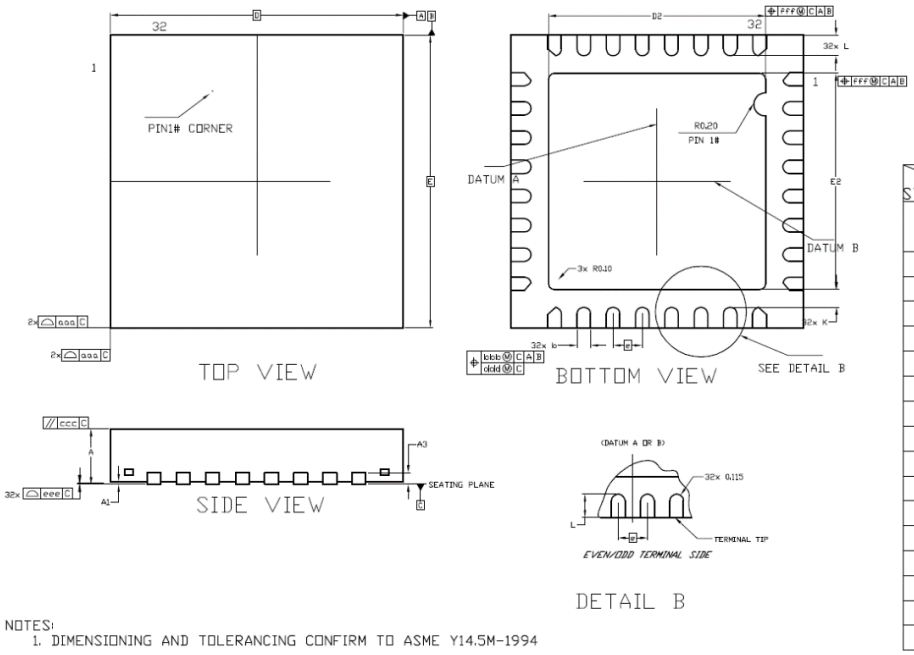


图 15：芯片打标

11 封装尺寸

11.1 QFN32 封装尺寸

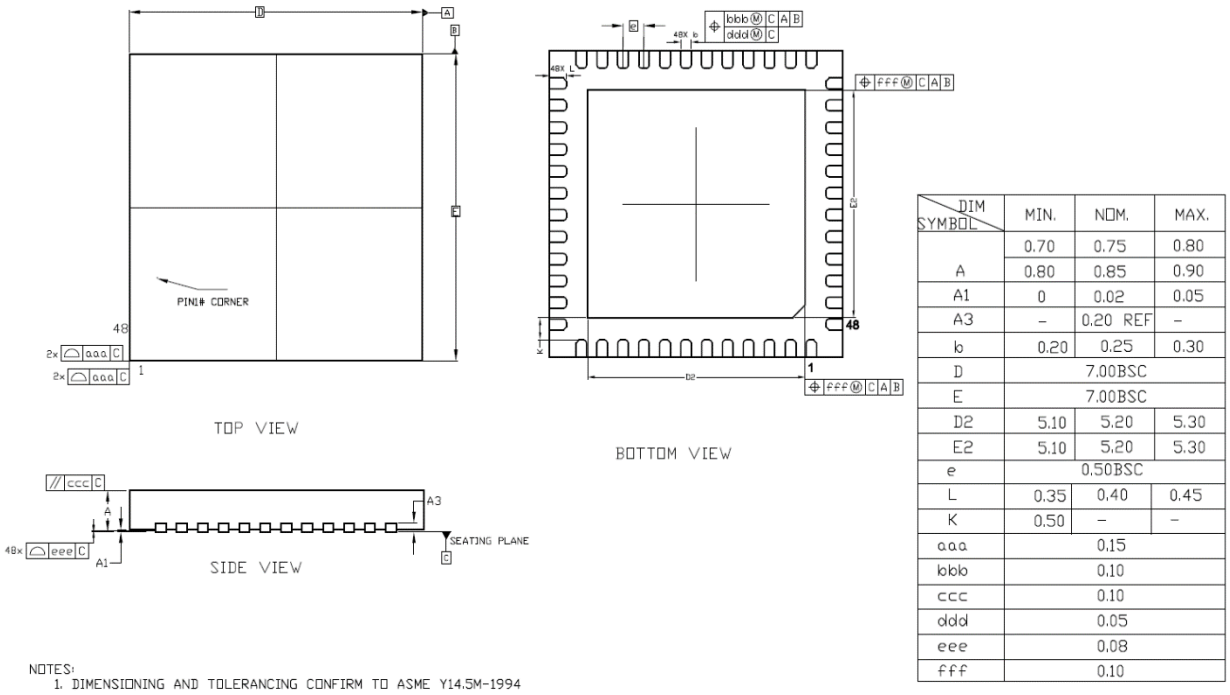


DIM / SYMBOL	MIN.	NOM.	MAX.
	0.70	0.75	0.80
A	0.85	0.90	0.95
A1	0	0.02	0.05
A3	–	0.20 REF	–
b	0.18	0.23	0.28
D		5.00BSC	
E		5.00BSC	
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
e		0.50BSC	
L	0.30	0.35	0.40
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

图 16：QFN32 封装尺寸

注：尺寸单位均为“毫米”，角度单位均为“度”

11.2 QFN48 封装尺寸



DIM / SYMBOL	MIN.	NOM.	MAX.
	0.70	0.75	0.80
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3	–	0.20 REF	–
b	0.20	0.25	0.30
D	7.00BSC		
E	7.00BSC		
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
e	0.50BSC		
L	0.35	0.40	0.45
K	0.50	–	–
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

图 17：QFN48 封装尺寸

注：尺寸单位均为“毫米”，角度单位均为“度”

12 应用程序范例和布局指南

12.1 应用程序范例

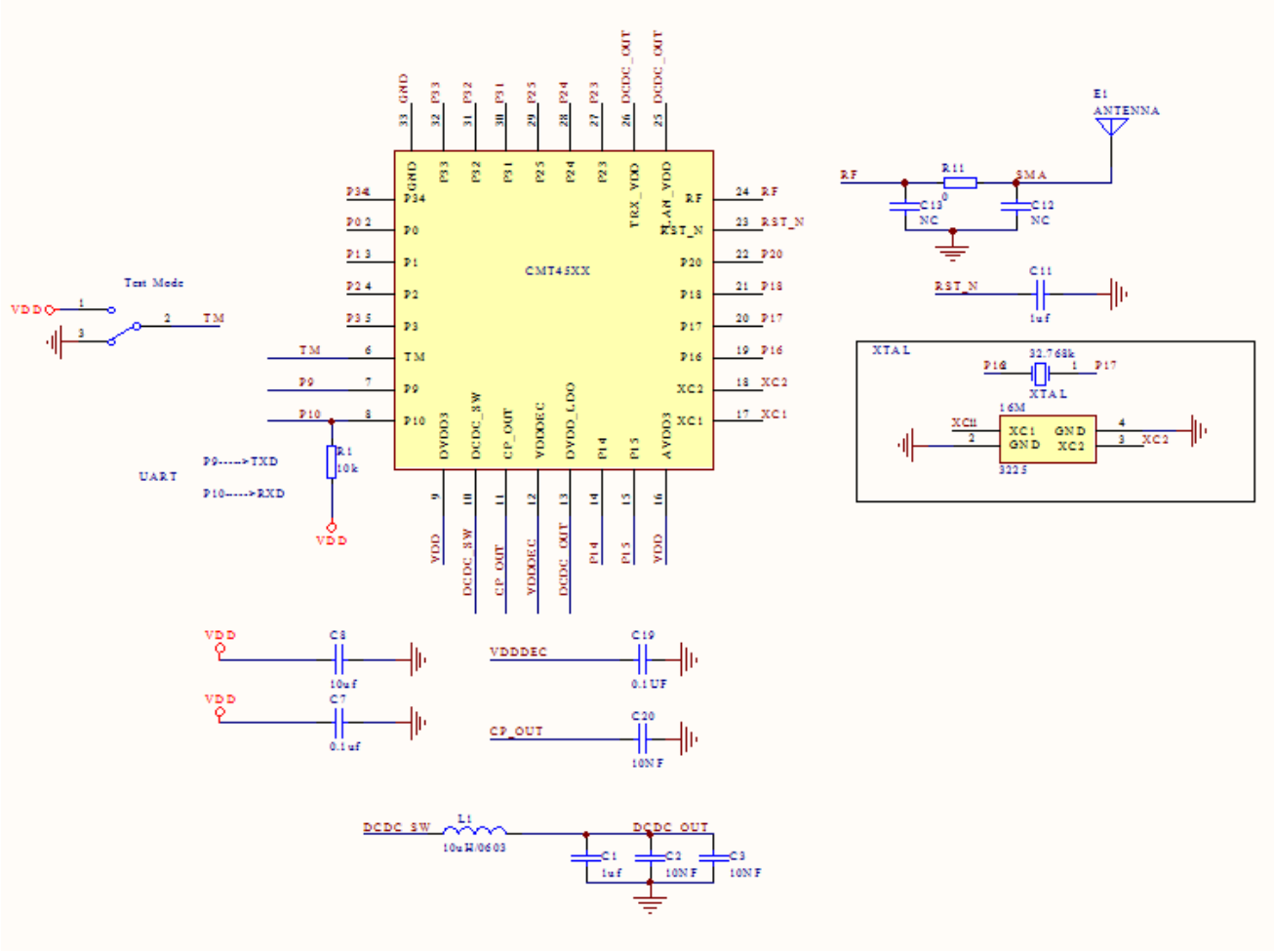


图 18：应用程序范例

12.2 布局指南

12.2.1 放置

1. 天线的射频匹配/环路滤波器应尽可能远离其他交流/直流信号；
2. Xtal/OSC 时钟是其他电路的噪声源，应尽可能缩短其电线长度，并远离重要区域；
3. LDO 是易受污染和易损的设备，应注意选择使用/存放环境；
4. 天线是主要的射频辐射点，其他重要的区块应尽可能与之隔离或保持较远距离。
5. 射频痕迹
6. 根据给定的介质厚度(PCB 介质层到地面平面的厚度)定义 RF 线宽，以达到 50ohm 阻抗;这主要用于匹配/环路滤波器和天线的射频线路的连接；
7. 差分布线应保持长度一致，元件应保持对称放置；

8. 一定长度的射频轨迹也应算作射频匹配的一部分。

12.2.2 旁路电容器

1. 每个 VDD 引脚都需要一个旁路电容来释放芯片内部的噪声并隔离来自电源的噪声；
2. 若需外接电线，旁路电容应尽可能靠近 VDD 引脚；
3. 当引脚需要两个电容器时，可使用一大一小两个电容器。一般情况下，大电容器的电容值是小电容器的 100 倍左右，但较小的电容器通常比较大的电容器具有更好的品质因数。较大的电容器需更靠近引脚；
4. 回路滤波器的电容器之间需要保留较大间隙，以防止出现电磁兼容和 EMI 问题；
5. 接地通径应靠近电容器接地侧，并远离强信号。

12.2.3 PCB 的层规格

1. 推荐使用 4 层 PCB；
2. 射频电线必须在表面层——即顶层或底层出现；
3. 射频 PCB 的第 2 层必须是“接地”层，对于信号接地和射频基准接地而言均是如此。第 2 层不能出现任何其他电线或平面，否则“层天线效应”会使调试过程复杂化；
4. 第 3 层通常为电源层；
5. 底层为信号层；
6. 请注意，使用 2 层的 PCB 一般情况下会影响到芯片的表现。若坚持如此，应尽可能保证底层拥有最大的尺寸，以避免信号电线与其它噪声线或 VDD 交叉影响，同时使用底层屏蔽临界信号线，并最大限度地增加旁路电容和地通数。

12.2.4 基准时钟与轨迹

1. 建议在第一层布置振荡器信号电源线；
2. 不要让基准时钟（振荡器）附近或之上出现任何电线；
3. 使用在参考时钟和振荡器周围添加接地线路的方法将其隔离；
4. 不要让振荡器下方出现任何电线。

12.2.5 外接电路

1. 是否使用外接电路取决于所需的电流量、噪声和布局。对射频芯片而言，建议使用电源线将电源导入 IC 引脚，线路具有寄生电感，可以形成低通滤波器，降低 PCB 周围噪声；
2. 在电流源上增加导电性通道口，可提高通道口的最大电流极限，降低通道口电感；
3. 若电源线过长，可在电源线附近增加一些电容器；
4. 请勿将电源线或任何平面置于射频线或振荡器及其时钟线之下，因为强时钟或射频的信

号会随电源线移动。

12.2.6 接地线路

1. 接地线路必须尽可能靠近旁路电容的接地端口，因为线路与接地端子之间的距离过大会降低旁路电容的作用；
2. 尽可能多放置接地线路；
3. 将接地线路放置在射频线路附近，因为射频线路可以通过此线路达到屏蔽效果。