HOPERF

E541580 **CMT8602X**

Reinforced Isolation Dual-Channel Gate Driver

Features

- General: dual channel low side, dual channel high side or half-bridge driver
- Junction temperature range: –40°C to 125°C
- Up to 4-A peak source and 6-A peak sink output
- 3V to 5.5V VCCI working range, can be connected digital and analog controller
- CMTI greater than 150 kV/us
- Isolated layer life ＞ 40 years
- TLL and CMOS compatible
- Up to 30V VDD output drive voltage
  - 9V and 13V VDD UVLO option
- Switching parameters:
  - 40 ns typical propagation delay
  - 50 ns minimum pulse width
  - 5 ns maximum delay matching
  - 9 ns maximum pulse-width distortion
- Programmable overlap and dead time
- Suppress input pulses and noise transients ＜ 25ns
- Fast disable the power sequence
- Safety-related certifications:
  - 8000-V_{PK} reinforced isolation per DIN V VDE V 0884-11:2017-01
  - 5700-V_{RMS} isolation for 1 minute per UL 1577
  - CSA certified in accordance with IEC 60950-1 and IEC 62368-1, IEC 61010-1 and IEC 60601-1 terminal equipment standards
  - CQC certification per GB4943.1-2011 (Planned)
- Applied in SOW14 / SOW16 / SOP16 packages

Application

- HEV and EV battery chargers
- Isolated converters in AC-to-DC and DC-to-DC power supplies
- Motor drives and inverters
- LED lighting
- Sensor heating
- Uninterruptible power supply (UPS)

Description

The CMT8602X device is an isolated dual channel gate driver with programmable dead time and wide temperature range. This device exhibits consistent performance and robustness under extreme temperature conditions. It is designed with 4-A peak- source and 6-A peak-sink current to drive 2MHz power MOSFET, IGBT, and SIC MOSEFT, which owns character of first-class propagation delay and pulse width distortion.

The input side is isolated from the two output drivers by a 5.7 kV_{RMS} isolation barrier, with 150 kV/us common-mode transient immunity (CMTI). Internal functional isolation between the two side drives, supports operating voltages up to 1500V_{DC}.

The CMT8602X can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. The disabled pins close the 2 outputs simultaneously when it is set to high level, while operates the device at open or grounded state. As a fail-safe mechanism, the primary side logic failure forces both outputs to be low.

Ordering Information

Part No.	Package	Minimum Order Quantity
CMT8602X-K	SOW14	1000
CMT8602X-W	SOW16	1000
CMT8602X-N	SOP16	3000

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1 Pin Description

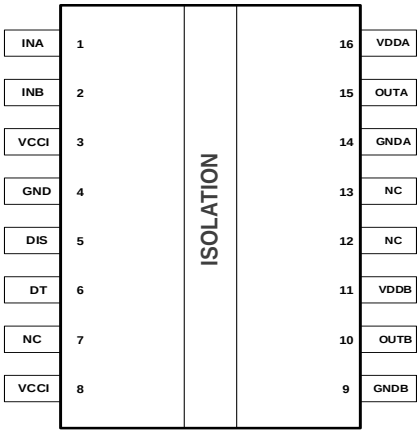


Figure 1-1. CMT8602X SOW16 Pin Arrangement

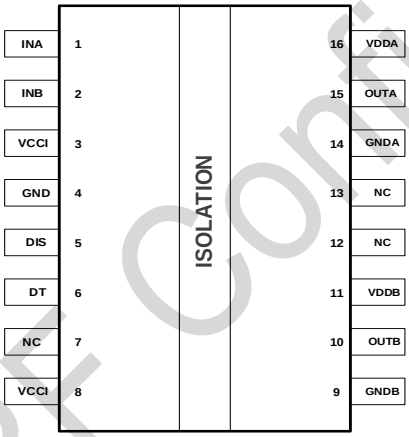


Figure 1-2. CMT8602X SOP16 Pin Arrangement

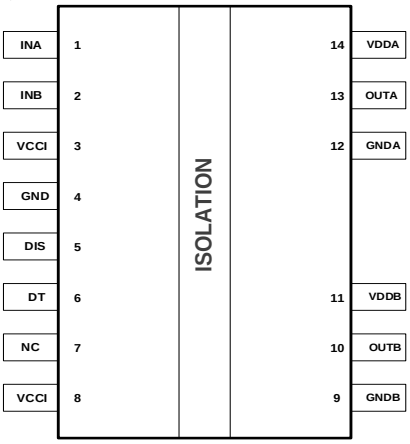


Figure 1-3. CMT8602X SOW14 Pin Arrangement

Table 1-1. CMT8602X Pin Description

Pin #			Pin Name	I/O[1]	Description
SOW16	SOW14	SOP16			
5	5	5	DIS	I	Disables both driver outputs if asserted high, enables if set low. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈ 1-nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.
6	6	6	DT	I	DT pin configuration: • Tying DT to V_{CCI} disables the DT feature and allows the outputs to overlap. • Placing a resistor (R_{DT}) between DT and GND adjusts dead time according to the equation: DT (in ns) = 10 × R_{DT} (in kΩ). HOPE recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, close to DT pin to achieve better noise immunity.
4	4	4	GND	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
14	12	14	GNDA		Side A ground terminal.
9	9	9	GNDB		Side B ground terminal.
1	1	1	INA	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
2	2	2	INB	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
7		7	NC	-	No internal connection. This pin can be left floating, tied to V_{CCI}, or tied to GND.
12		12	NC	-	No internal connection.
13		13	NC	-	No internal connection.
15	13	15	OUTA	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
10	10	10	OUTB	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
3	3	3	VCCI	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
8	8	8	VCCI	P	This pin is internally shorted to pin 3. Preference should be given to bypassing pin 3-4 instead of pins 8-4.
16	14	16	VDDA	P	Secondary-side power for driver A. Locally decoupled to V_{SSA} using a low ESR/ESL capacitor located as close to the device as possible.
11	11	11	VDDB	P	Secondary-side power for driver B. Locally decoupled to GNDB using a low ESR/ESL capacitor located as close to the device as possible.

Notes:

[1] P = power, I = input, O = output

2 Specifications

2.1 Recommended Operating Ratings

Over operating free-air temperature range (unless otherwise noted).

Table 2-1. Recommended Operating Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VCCI Input supply voltage	V_{CCI}		3		5.5	V
Driver output bias supply	V_{DDA}, V_{DDB}	CMT8602X	9		25	V
Junction Temperature	T_J		–40		150	°C

Ambient Temperature	T_A		–40		125	°C

2.2 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).

Table 2-2. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input bias pin supply voltage	V_{CCI} to GND		–0.3		5.5	V
Driver bias supply	V_{DDA}-GNDA, V_{DDB}-GNDB		–0.3		30	V
Output signal voltage	OUTA to GNDA, OUTB to GNDB		–0.3		V_{VDDA} + 0.3, V_{VDDB} + 0.3	V
	OUTA to GNDA, OUTB to GNDB, Transient for 200 ns		–2		V_{VDDA}+0.3, V_{VDDB}+0.3	V
Input signal voltage	INA, INB, DIS and DT to GND		–0.3		V_{VCCI} + 0.3	V
	INA, INB Transient for 50ns		–5		V_{VCCI} + 0.3	V
Channel to channel isolation voltage	|GNDA-GNDB|	SOW14			1500	V
Junction temperature	T_J		–40		150	°C
Storage temperature	T_{stg}		–65		150	°C

Notes:

[1]. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

2.3 ESD Ratings

Table 2-3. ESD Ratings

Parameter	Symbol	Condition	Max.	Unit
Electrostatic Discharge	V_{ESD}	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22- V C101[2]	±1500	

Notes:
[1]. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
[2]. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

2.4 Thermal Information

Table 2-4. Thermal Information

Parameter	Symbol	CMT8602X	Unit
		SOW16/SOW14	
Junction-to-ambient thermal resistance	$R_{\theta JA}$	97.3	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	23.3	°C/W
Junction-to-top characterization parameter	ψ_{JT}	35	°C/W
Junction-to-board characterization parameter	ψ_{JB}	34	°C/W

2.5 Power Ratings

Table 2-5. Power Information

Parameter	Symbol	Condition	CMT8602X	Unit
Power dissipation	P_D	V_{CCI} =5.5 V, $V_{DDA/B}$ = 13 V, INA/B = 3.3 V, 2 MHz 50% duty cycle square wave 1.0 nF load.	1.33	W
Power dissipation by transmitter side	P_{DI}		0.01	W
Power dissipation by each driver side	P_{DA}, P_{DB}		0.66	W

2.6 Insulation Specifications

Table 2-6. Thermal Information

Parameter	Symbol	Condition	Value	Unit
External clearance [1]	CLR	Shortest pin-to-pin distance through air	> 8	mm
External creepage[1]	CRP	Shortest pin-to-pin distance across the package surface	> 8	mm
Distance through insulation	DTI	Minimum internal gap (internal clearance) of the double insulation (2 × 8.5 µm)	>30	µm
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
Material group		According to IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01[2]				
Maximum repetitive peak isolation voltage	V_{IORM}	AC voltage (bipolar)	2121	V_{PK}
Maximum working isolation voltage	V_{IOWM}	AC voltage (sine wave); time dependent dielectric breakdown (TDDB), test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
Maximum transient isolation voltage	V_{IOTM}	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	8000	V_{PK}
Maximum surge isolation voltage[3]	V_{IOSM}	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
Apparent charge[4]	q_{pd}	Method a, After I/O safety test subgroup 2/3. $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, t_m = 10 s	<5	pC
		Method a, After environmental tests subgroup 1. $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, t_m = 10 s	<5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; t_{ini} = 1 s; $V_{pd(m)} = 1.875 * V_{IORM} = 3977\ V_{PK}$, t_m = 1 s	<5	
Barrier capacitance, input to output[5]	C_{IO}	V_{IO} = 0.4 sin (2πft), f =1 MHz	1.2	pF

Parameter	Symbol	Condition	Value	Unit
Isolation resistance, input to output[5]	R_{IO}	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S =150°C	> 10^{9}	
Pollution degree			2	
Climatic category			40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 sec. (qualification), V_{TEST} = 1.2 × V_{ISO} = 6840V_{RMS}, t = 1 sec (100% production)	5700	V_{RMS}

Notes:

[1]. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications..

[2]. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

[3]. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

[4]. Apparent charge is electrical discharge caused by a partial discharge (pd).

[5]. All pins on each side of the barrier tied together creating a two-pin device.

2.7 Safety-Related Certifications

Table 2-7. Safety-Related Certifications

VDE	UL		CQC	TUV
DIN VDE V0884-11:2017-01 (Patents pending)	UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	GB 4943.1-2011	EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013 (Patents pending)
Certificate number: pending	Certificate number: E541580		Certificate number: CQC11-471543-2022	Client ID number: pending

2.8 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

Table 2-8. Safety-Limiting Values

Parameter	Symbol	TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
Safety output supply current	I_S	θ_{JA} = 97.3 °C/W, $V_{VDDA/B}$ = 15 V, T_J = 150°C, T_A = 25°C	DRIVER A, DRIVER B			TBD	mA
		θ_{JA} = 97.3°C/W, $V_{DDA/B}$ = 30 V, T_J = 150°C, T_A = 25°C	DRIVER A,			TBD	mA

			DRIVER B				
Safety supply power	P_S	$R_{\theta JA}$ = 97.3°C/W, T_A = 25°C, T_J = 150°C	INPUT			TBD	mW
			DRIVER A			TBD	
			DRIVER B			TBD	
			TOTAL			TBD	
Safety temperature[1]	T_S					TBD	°C

Notes:

[1]. The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The IS and PS parameters represent the safety current and safety power respectively. The maximum limits of I_S and PS should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the Section 1.4 table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where V_I is the maximum input voltage.

2.9 Electrical Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 15 V, 1-µF capacitor from V_{DDA} and V_{DDB} to GNDA and GNDB, T_A = –40°C to +125°C unless otherwise noted[1].

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENTS						
V_{CCI} quiescent current	I_{VCCI}	V_{INA} = 0 V, V_{INB} = 0 V		1.4	2.0	mA
V_{DDA} and V_{DDB} quiescent current	I_{VDDA}, I_{VDDB}	V_{INA} = 0 V, V_{INB} = 0 V		1.1	1.8	mA
V_{CCI} operating current	I_{VCCI}	current per channel C_{OUT} = 100 pF (f = 500 kHz)		2.0		mA
V_{DDA} and V_{DDB} operating current	I_{VDDA}, I_{VDDB}	current per channel C_{OUT} = 100 pF (f = 500 kHz)		3		mA
VCCI SUPPLY VOLTAGE UNDER VOLTAGE THRESHOLDS						
Rising threshold	V_{VCCI_ON}		2.55	2.7	2.85	V
Falling threshold	V_{VCCI_OFF}		2.35	2.5	2.65	V
Threshold hysteresis	V_{VCCI_HYS}			0.2		V
VDD UVLO THRESHOLDS						
Rising threshold V_{DDA_ON}, V_{DDB_ON}	V_{VDDA_ON} V_{VDDB_ON}		8.1	8.6	9.1	V
Falling threshold V_{DDA_OFF}, V_{DDB_OFF}	V_{VDDA_OFF} V_{VDDB_OFF}		7.45	7.95	8.55	V

Threshold hysteresis	V_{VDDA_HYS} V_{VDDB_HYS}			0.65		V
INA, INB AND DISABLE						
Input high threshold voltage	V_{INAH} V_{INBH} V_{DISH}		1.6	1.8	2	V
Input low threshold voltage	V_{INAL}, V_{INBL}, V_{DISL}		0.8	1	1.2	V
Input threshold hysteresis	V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}			0.8		V
Negative transient, ref to GND, 50 ns pulse	V_{INA}, V_{INB}	Not production tested, bench test only	-5			V
OUTPUT						
Peak output source current	I_{OA+}, I_{OB+}	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		4		A
Peak output sink current	I_{OA-}, I_{OB-}	I_{OUT} = –10 mA, R_{OHA}, R_{OHB} do not represent drive pull-up performance		6		A
Output resistance at high state	R_{OHA}, R_{OHB}	I_{OUT} = 10 mA, TA = 25°C, R_{OHA}, R_{OHB} do not represent drive pull-up performance.		5		Ω
Output resistance at low state	R_{OLA}, R_{OLB}	I_{OUT} = 10 mA, TA = 25°C		0.55		Ω
Output voltage at high state	V_{OHA}, V_{OHB}	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = - 10 mA, TA = 25°C		11.95		V
Output voltage at low state	V_{OLA}, V_{OLB}	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = 10 mA, TA = 25°C		5.5		mV
DEAD TIME AND OVERLAP PROGRAMMING						
Dead time	DT	DT pin tied to V_{CCI}	Overlap determined by INA, INB			-
		DT pin is left open, min spec characterized only, tested for outliers	0	12	20	ns
		R_{DT} = 20 kΩ	160	200	240	

Notes:

[1]. Current direction in the testing conditions is defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted)

2.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5.5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 15 V, 1-µF capacitor from V_{DDA} and V_{DDB} to GNDA and GNDB, T_J = –40°C to +125°C unless otherwise noted.

PARAMETER	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output rise time, 20% to 80% measured points	t_{RISE}	C_{OUT} = 1.8 nF		6	16	ns
Output fall time, 90% to 10% measured points	t_{FALL}	C_{OUT} = 1.8 nF		7	12	ns
Minimum input pulse width	t_{PWmin}	Output does not change the state if input signal less than t_{PWmin}		30	50	ns
Propagation delay at falling edge	t_{PDHL}	INx high threshold, V_{INH}, to 90% of the output	30	40	50	ns
Propagation delay at rising edge	t_{PDLH}	INx low threshold, V_{INL}, to 10% of the output	25	35	45	ns
Pulse width distortion	t_{PWD}	$\lvert t_{PDLHA} - t_{PDHLA} \rvert$, $\lvert t_{PDLHB} - t_{PDHLB} \rvert$			9	ns
Propagation delays matching between V_{OUTA}, V_{OUTB}	t_{DM}	f = 100 kHz			5	ns
V_{DDA}, V_{DDB} Power-up Delay Time; UVLO Rise to OUTA, OUTB.	$t_{VDD+ to OUT}$	INA or INB tied to V_{CCI}		50		µs
High-level common-mode transient immunity	$\lvert CM_H \rvert$	INA and INB both are tied to V_{CCI}; V_{CM}=1500 V;		150		V/ns
Low-level common-mode transient immunity	$\lvert CM_L \rvert$	INA and INB both are tied to GND; V_{CM}=1500 V;		150		V/ns

2.11 Typical Characteristics

VDDA = VDDB = 15 V, VCCI = 3.3 V, T_A = 25° C, C_L = 0 pF unless otherwise noted.

Figure 2-11-1. Per Channel Current Consumption vs Frequency (No Load, V_{DD} = 15 V/25V)

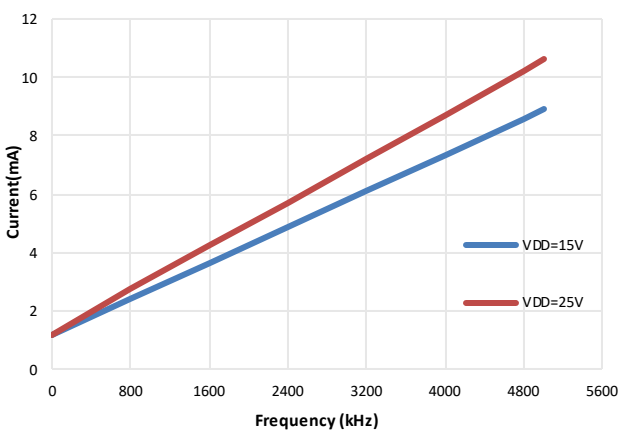


Figure 2-11-2. Per Channel Current Consumption (IVDDA/B) vs Frequency (1-nF Load, V_{DD} = 15 V/25V)

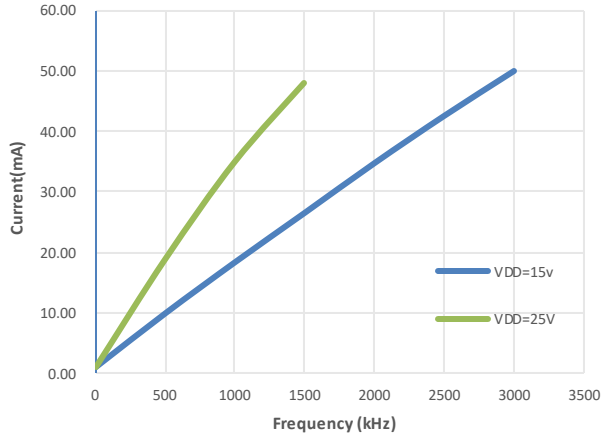


Figure 2-11-3. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (10-nF Load, V_{DD} = 15 V/25V)

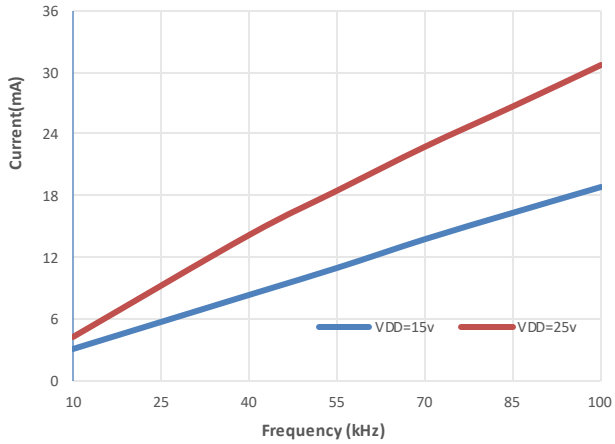


Figure 2-11-4. Per Channel ($I_{VDDA/B}$) Supply Current Vs. Temperature (No Load, Different Switching Frequencies)

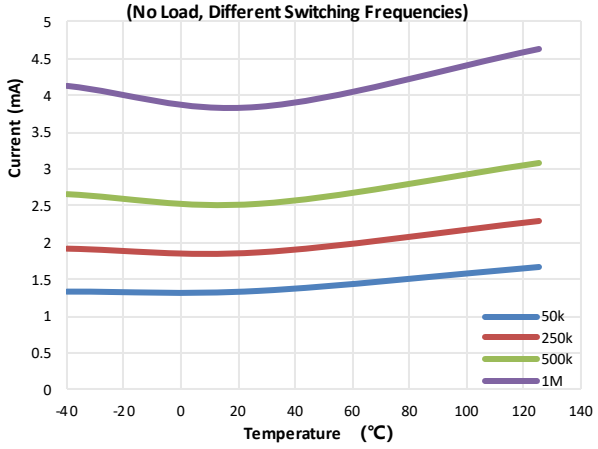


Figure 2-11-5. Per Channel ($I_{VDDA/B}$)Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

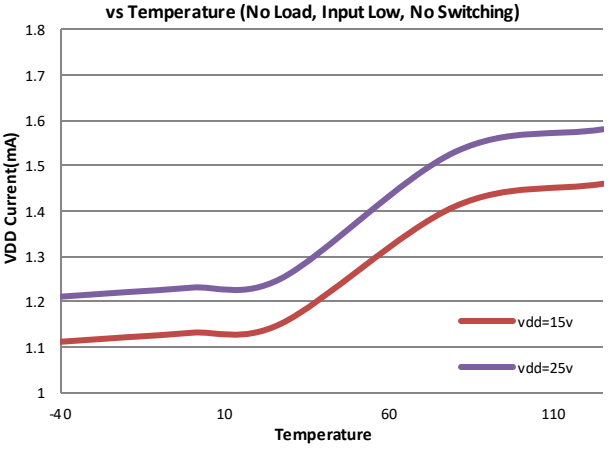


Figure 2-11-6. Per channel ($I_{VDDA/B}$) Quiescent supply current vs temperature (no load, input HIG, no switching)

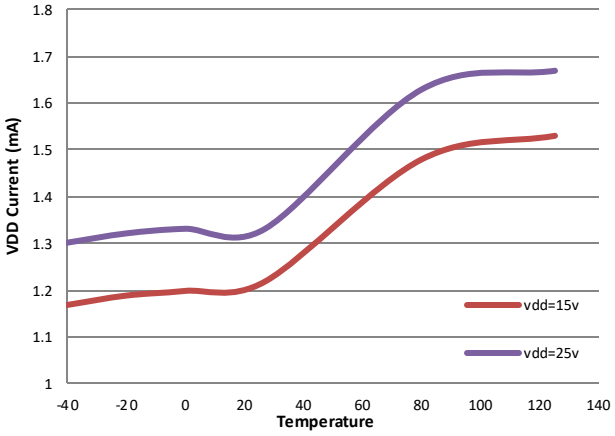


Figure 2-11-7. Rising and Falling Times vs Load (VDD = 15 V)

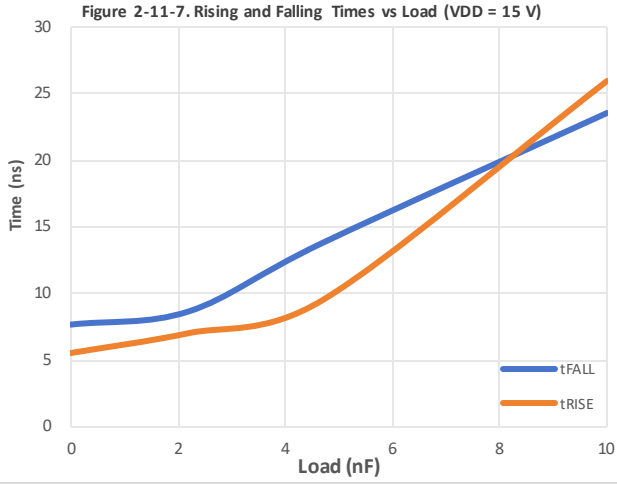


Figure 2-11-8. Output Resistance vs Temperature

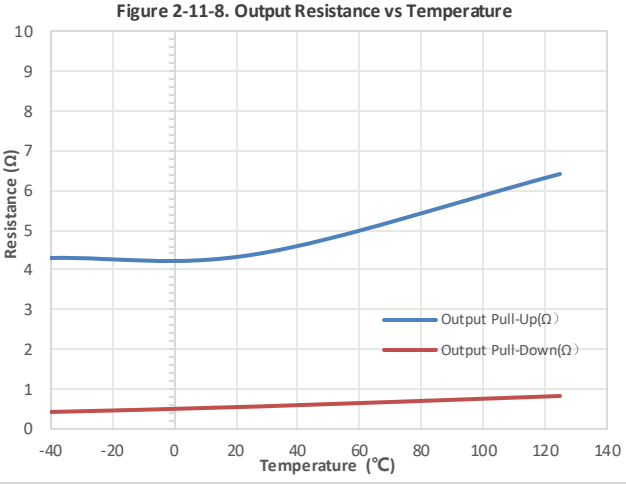


Figure 2-11-9. Propagation Delay vs Temperature

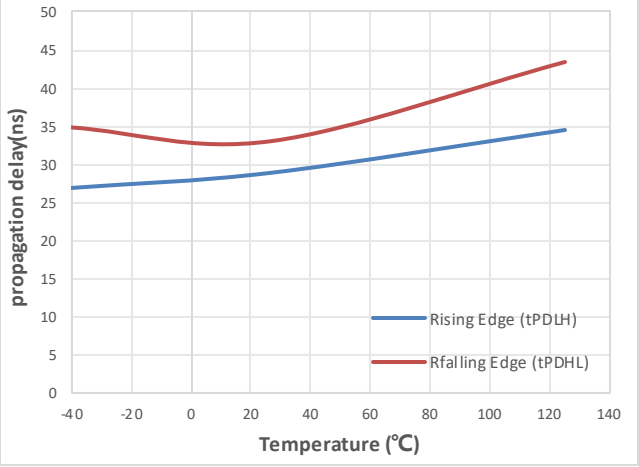


Figure 2-11-10. Pulse Width Distortion vs Temperature

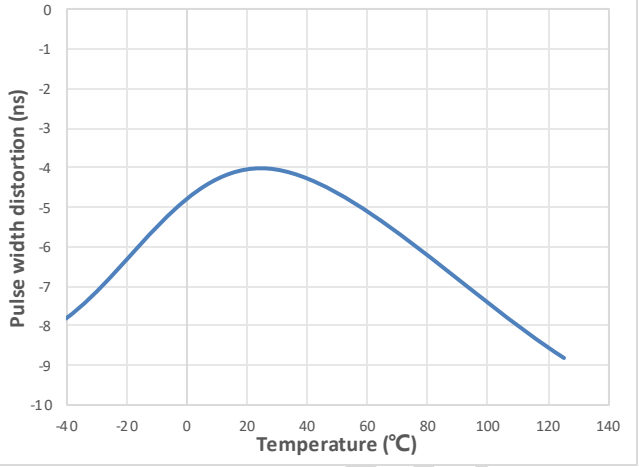


Figure 2-11-11. Propagation Delay vs V_{CCI}

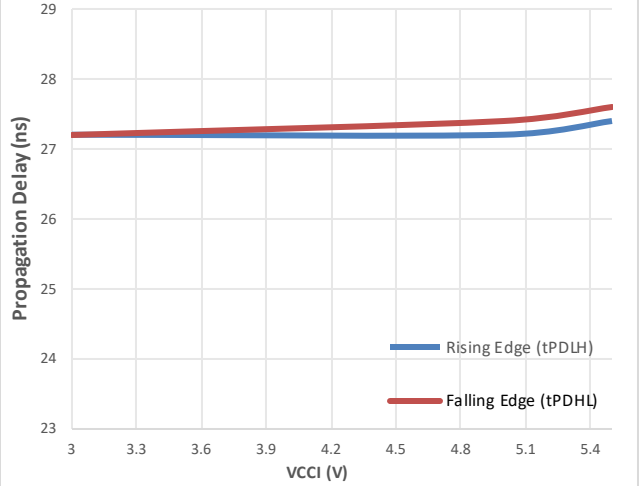


Figure 2-11-12. Propagation Delay Matching (t_{DM}) vs V_{DD}

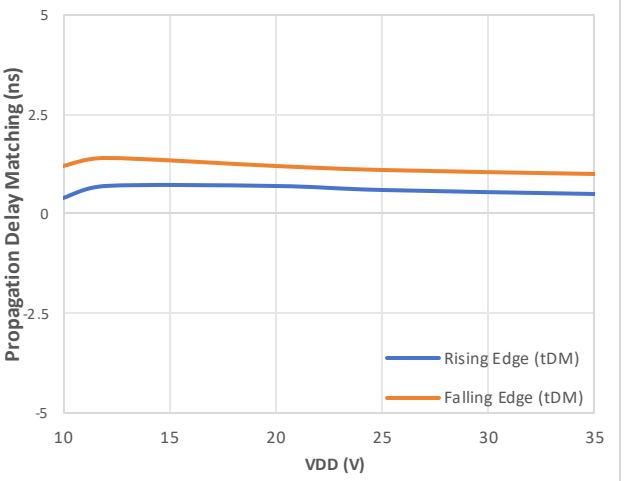


Figure 2-11-13. Propagation Delay Matching (t_{DM}) vs Temperature

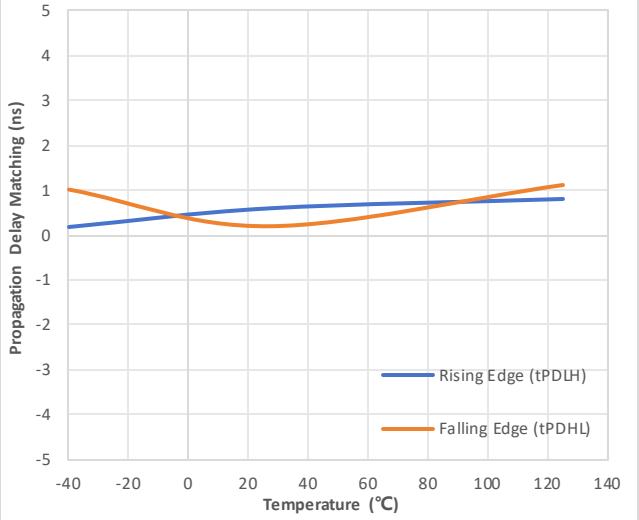


Figure 2-11-14. VDD 9-V UVLO Threshold vs Temperature

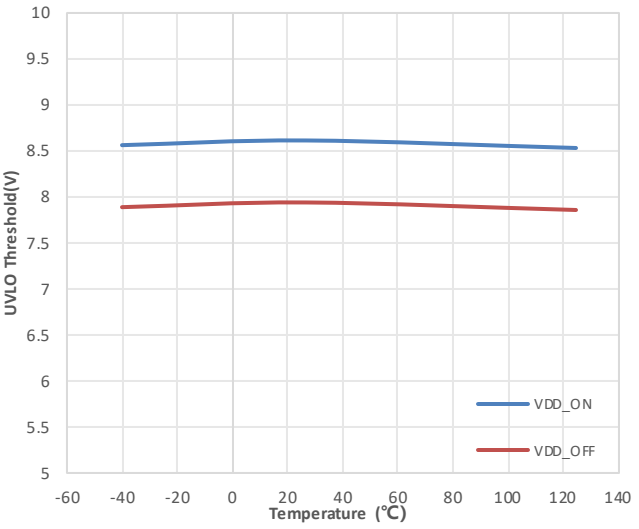


Figure 2-11-15. UVLO Hysteresis Temperature

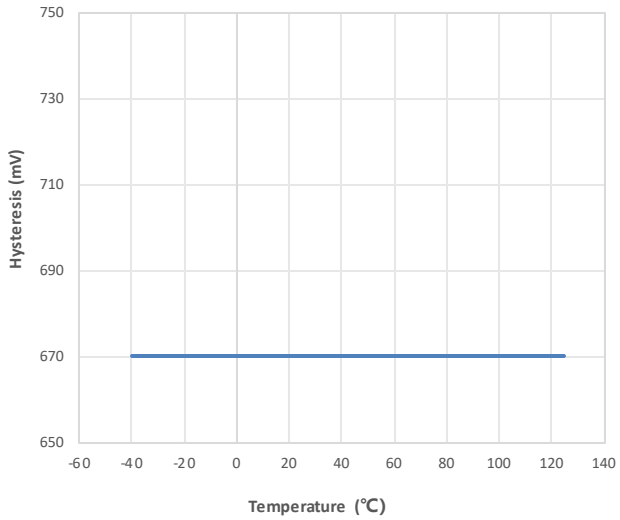


Figure 2-11-16. IN/DIS High Threshold

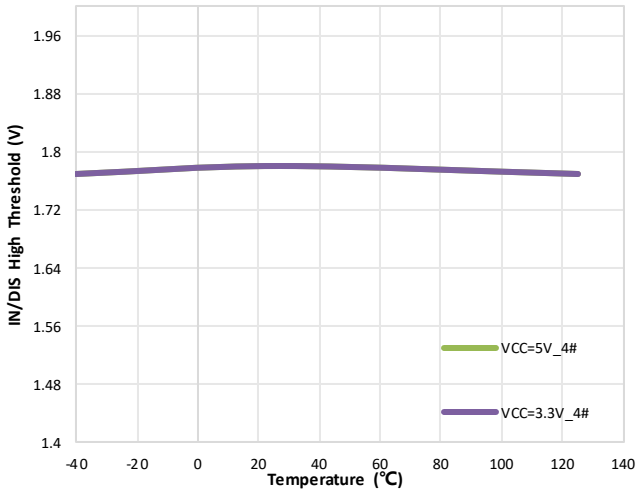


Figure 2-11-17. IN/DIS LOW Threshold

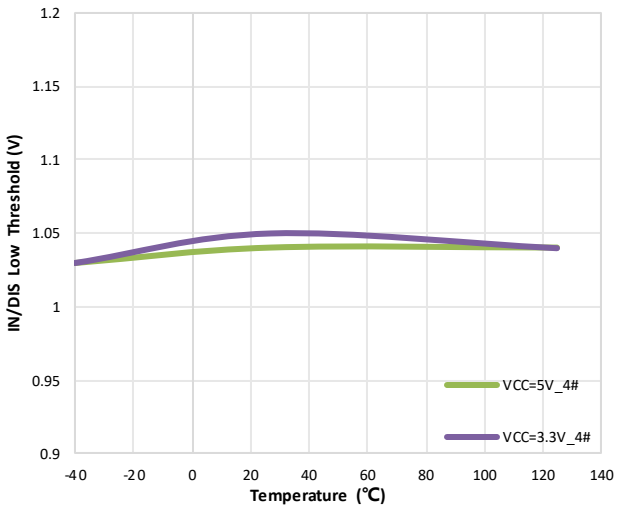


Figure 2-11-18. IN/DIS Hysteresis vs Temperature

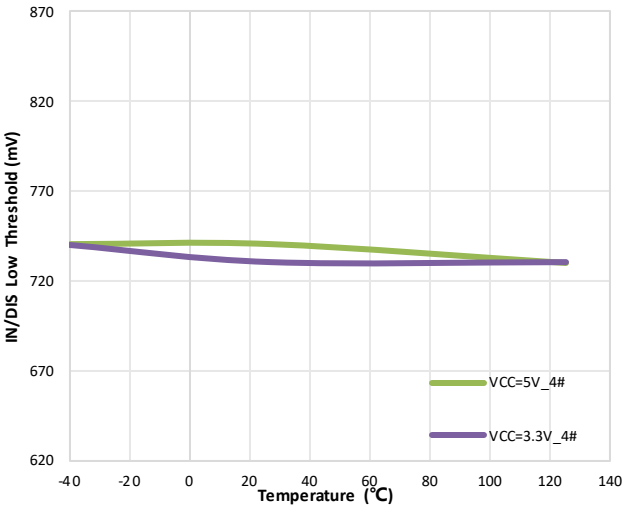


Figure 2-11-19. Dead Time vs Temperature
(with RDT = 20 kΩ and 100 kΩ)

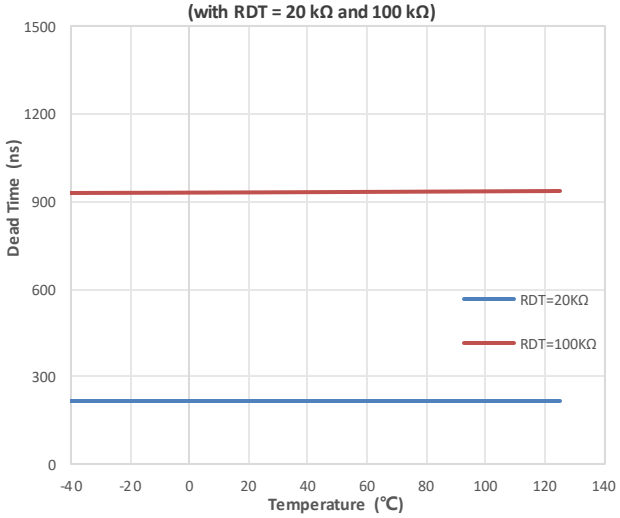


Figure 2-11-20. Dead Time Matching vs Temperature
(with RDT = 20 kΩ and 100 kΩ)

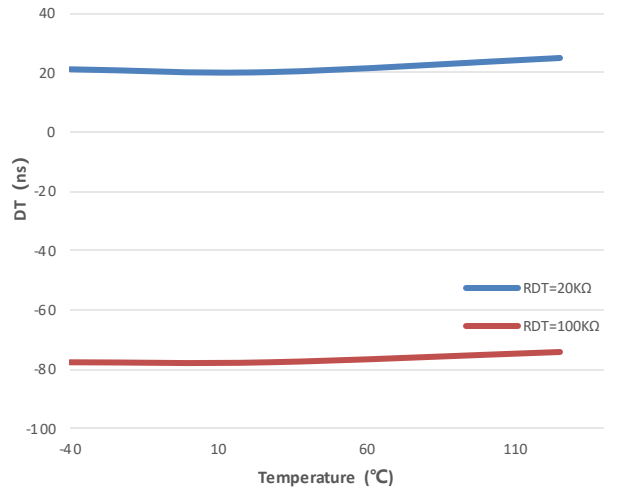


Figure 2-11-21. Typical Output Waveforms

3 Parameter Measurement Information

3.1 Minimum Pulses

A typical 30 ns deglitch filter removes small input pulses introduced by ground bounce or switching transients. An input pulse with duration longer than t_{PWmin}, typically 30 ns, must be asserted on INA or INB to guarantee an output state change at OUTA or OUTB. See the 2 figures below for detailed information of the operation of deglitch filter.

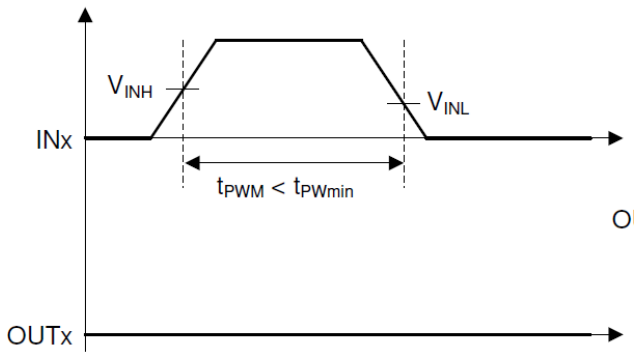


Figure 3-1. Deglitch Filter – Turn ON

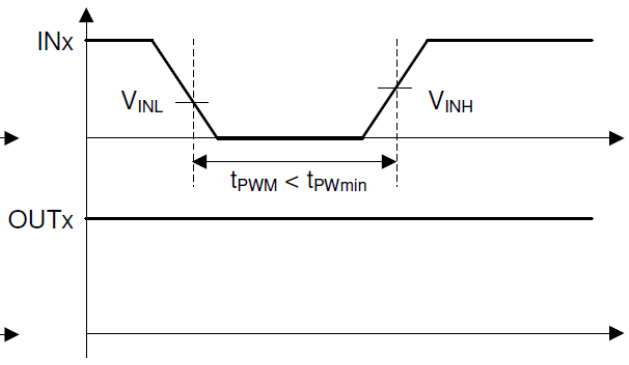


Figure 3-2. Deglitch Filter – Turn OFF

3.2 Propagation Delay and Pulse Width Distortion

The figure below shows calculation of pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. To measure delay matching, both inputs must be in phase, and the DT pin must be shorted to V_{CCI} to enable output overlap.

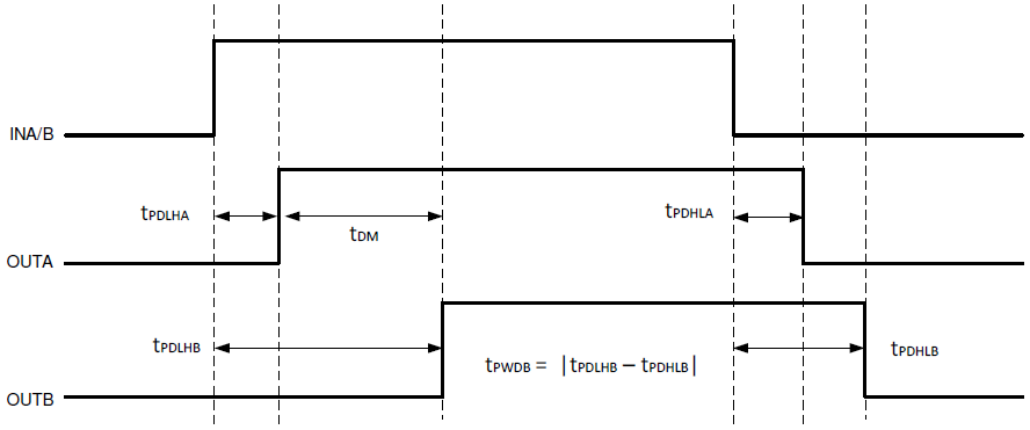


Figure 3-3. Delay Matching and Pulse Width Distortion

3.3 Rising and Falling Time

The figure below shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) time.

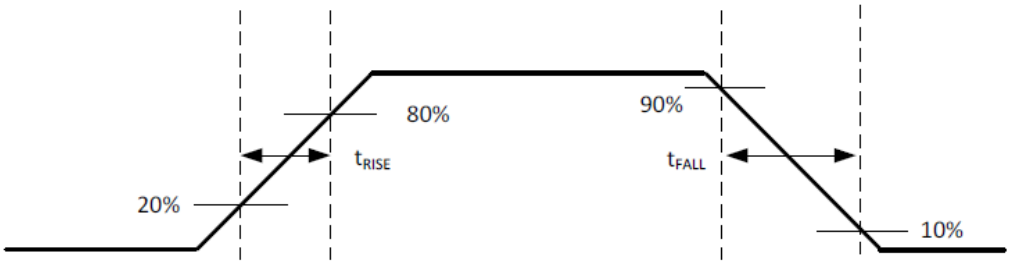


Figure 3-4. Rising and Falling Time Criteria

3.4 Input and Disable Response Time

The figure below shows the response time of the disable function.

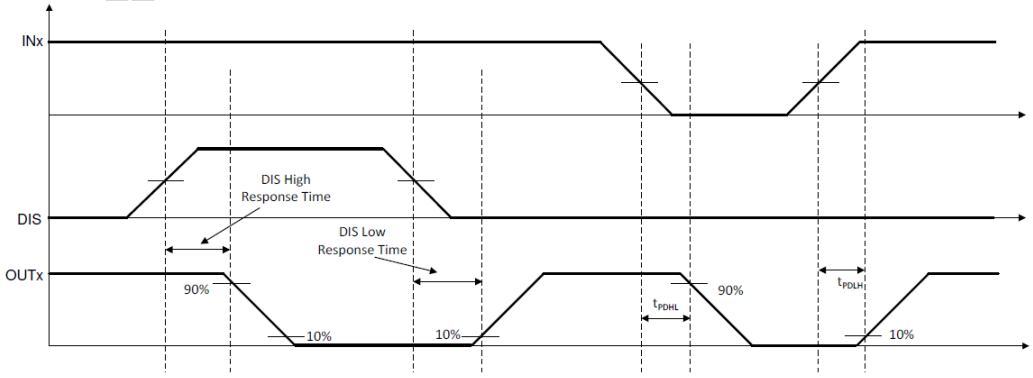


Figure 3-5. Disable Pin Timing

3.5 Programmable Dead Time

Tying DT to VCCI disables DT feature and allows the outputs to overlap. Placing a resistor (R_{DT}) between DT and GND adjusts dead time according to the equation: DT (in ns) = 10 × R_{DT} (in kΩ). HOPE recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, close to DT pin to achieve better noise immunity.

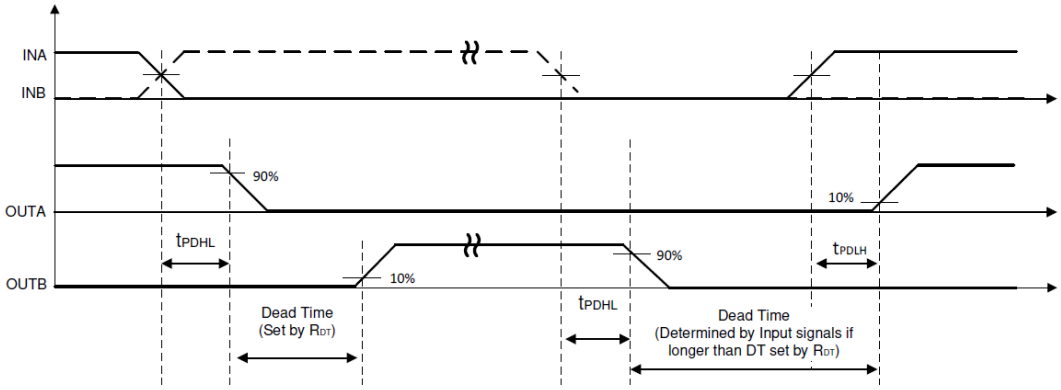


Figure 3-6. Dead Time Switching Parameters

3.6 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for V_{CCI} UVLO (typically 40 us) and $t_{VDD+\ to\ OUT}$ for V_{DD} UVLO (typically 50 us). It is recommended to consider proper margin before launching PWM signal after the driver's V_{CCI} and V_{DD} bias supply is ready. Figure 3-7 and Figure 3-8 show the power-up UVLO delay timing diagram for V_{CCI} and V_{DD}. If INA or INB are active before V_{CCI} or V_{DD} have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ after V_{CCI} or V_{DD} crossing its UVLO rising threshold. However, when either V_{CCI} or V_{DD} receive a voltage less than their respective off thresholds, there is <1μs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during V_{CCI} or V_{DD} brownouts.

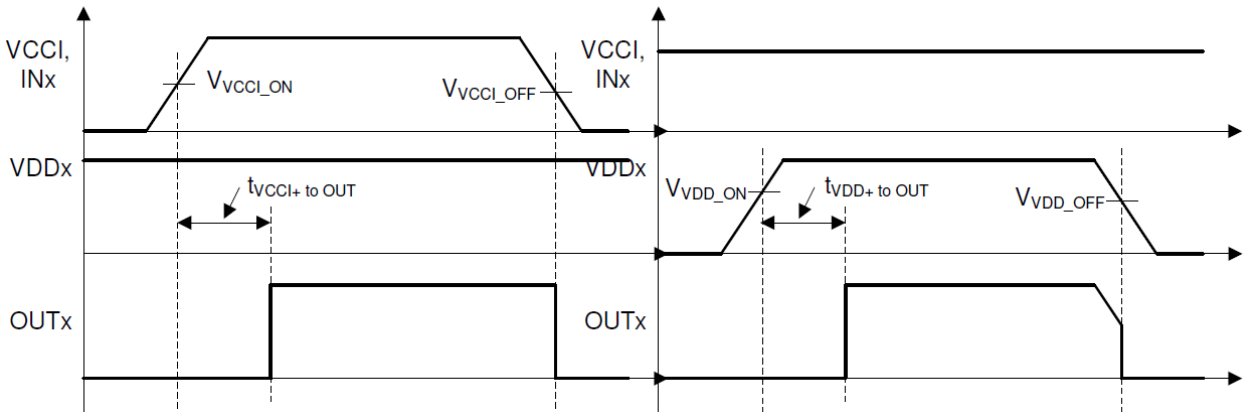


Figure 3-7. V_{CCI} Power-up UVLO Delay

Figure 3-8. $V_{DDA/B}$ Power-up UVLO Delay

3.7 CMTI Testing

The figure below is a simplified diagram of the CMTI testing configuration.

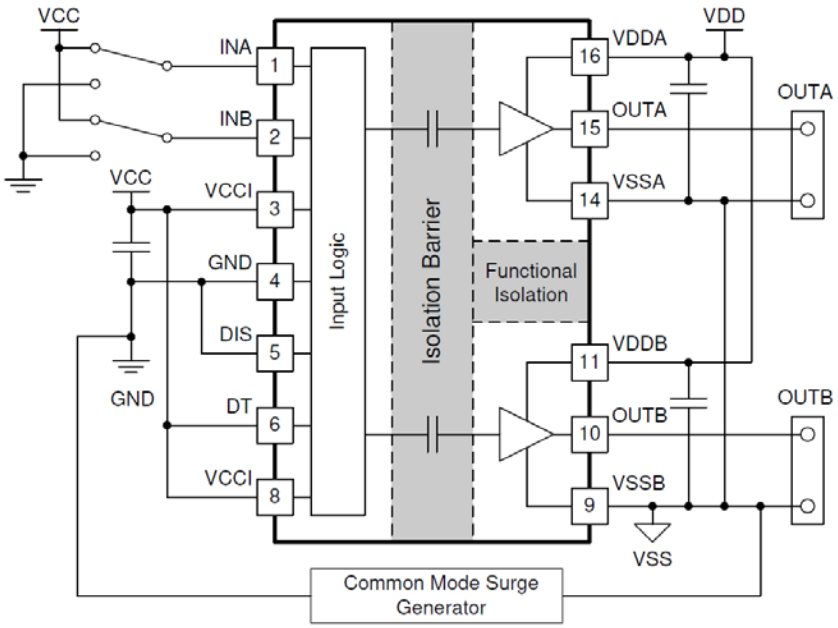


Figure 3-9. Simplified CMTI Testing Setup

4 Function Description

4.1 Function Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3V logic signal capable of only delivering a few mA.

The CMT8602X is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors. The CMT8602X has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, disable pin, and under voltage lock out (UVLO) for both input and output supplies. The CMT8602X also holds its outputs low when the inputs are left open or when the input pulse duration is too short. The driver inputs are CMOS and TTL compatible for interfacing with digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each one of the outputs.

4.2 Functional Block Diagram

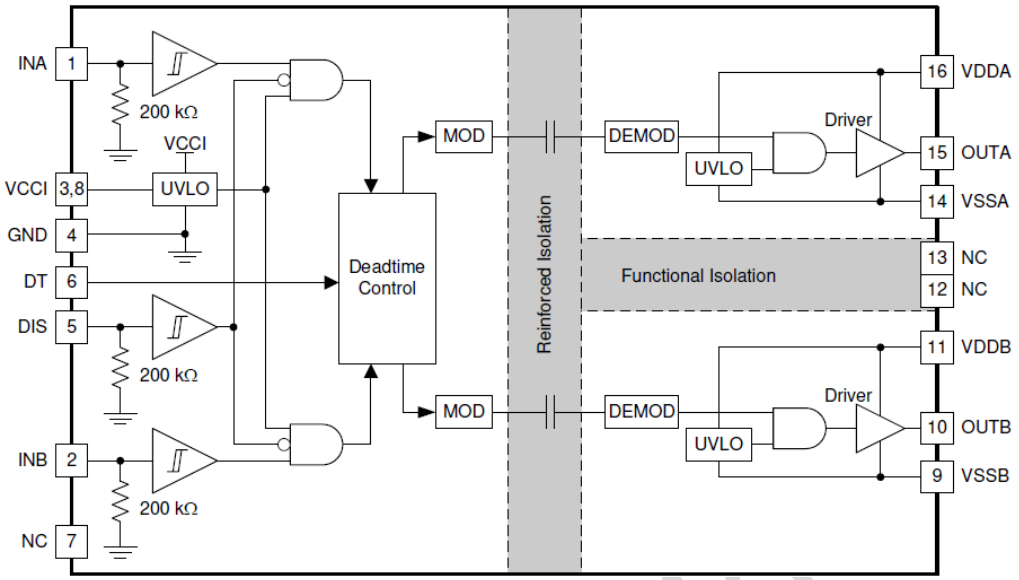


Figure 4-1. Simplified Representation of Active Pull Down Feature

4.3 Feature Description

4.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The CMT8602X has an internal under voltage lock out (UVLO) protection feature on each supply voltage between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the channel output low, regardless of the status of the input pins.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (illustrated in the figure below). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.75 V, regardless of whether bias power is available.

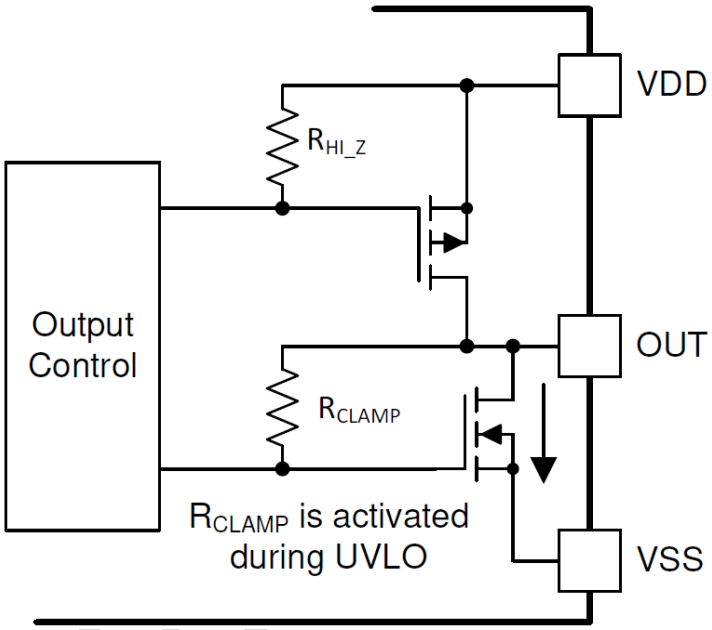


Figure 4-2. Simplified Representation of Active PullDown Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. This also allows the device to accept small drops in bias voltage, which commonly occurs when the device starts switching and operating current consumption increases suddenly.

The inputs of the CMT8602X also have internal under voltage lock out (UVLO) protection feature. The inputs cannot affect the outputs unless the supply voltage VCCI exceeds V_{VCCI_ON} on start-up. The outputs are held low and cannot respond to inputs when the supply voltage VCCI drops below V_{VCCI_OFF} after start-up. Like the UVLO for VDD, there is hysteresis (V_{VCCI_HYS}) to ensure stable operation.

Table 4-1. VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L

VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

Table 4-2.VDD UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_ONF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_ONF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_ONF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_ONF} after device start up	L	L	L	L

4.3.2 Input and Output Logic Table

Assume VCCI, VDDA, VDDB are powered up. The following table shows the operation with INA, INB and DIS and the corresponding output state.

Table 4-3. INPUT/OUTPUT Logic Table [1][2]

INPUTS		DIS	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L	L	L	If the dead time function is used, output transitions occur after the dead time expires.
L	H	L	L	H	
H	L	L	H	L	
H	H	L	L	L	DT is programmed with R_{DT}.
H	H	L	H	H	DT pin pulled high to V_{CCI}.
Left Open	Left Open	L	L	L	
X	X	H	L	L	

Notes:

[1]. "X" means L, H or left open.

[2]. For improved noise immunity, recommend connecting INA, INB, and DIS to GND, and DT to VCCI, when these pins are not used.

4.3.3 Input Stage

The input pins (INA, INB, and DIS) of the CMT8602X is based on a TTL and CMOS compatible input- threshold logic that is totally isolated from the VDD supply voltage of the output channels. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), since the CMT8602X has a typical high threshold (V_{INAH}) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature. A wide hysteresis (V_{INA_HYS}) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ. HOPE recommends grounding any unused inputs.

The amplitude of any signal applied to the inputs should not exceed the voltage at the V_{CCI} pin. The CMT8602X cannot be driven from an analog controller with an output voltage greater than the V_{CCI} voltage.

4.3.4 Output Stage

The CMT8602X output stage features a pull-up structure which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the pull-up N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the CMT8602X pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter.

The pull-down structure of the CMT8602X is composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. The output voltage swings between VDD and VSS for rail-to-rail operation.

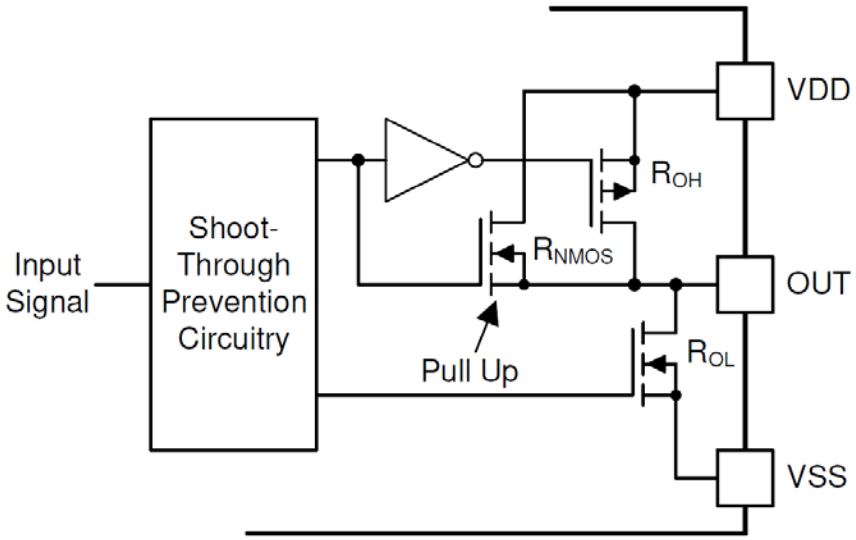


Figure 4-3. Output Stage

4.4 Device Functional Modes

4.4.1 Disable Pin

Setting the DISABLE pin high shuts down both outputs simultaneously. Grounding (or left open) the DISABLE pin allows the device to operate normally. The DISABLE response time is in the range of 40 ns and quite responsive, which is as fast as propagation delay. The DISABLE pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DISABLE pin is not used to achieve better noise immunity, and it is recommended to bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

4.4.2 Programmable Dead Time (DT) Pin

The CMT8602X allows the user to adjust dead time (DT) in the following ways:

4.4.2.1 Connecting a Programming Resistor between DT and GND Pins

One can program t_{DT} by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined from foemula (1), where R_{DT} is in kΩ and t_{DT} is in ns

$t_{DT} \approx 10 * R_{DT}$ (1)

The steady state voltage at DT pin is around 0.8 V, and the DT pin current will be less than 10uA when R_{DT}=100kΩ. When using R_{DT}> 5kΩ, it is recommended to parallel a ceramic capacitor, 2.2nF or above, close to the chip with R_{DT} to achieve better noise immunity and better dead time matching between two channels. It is not recommended to leave the DT pin floating.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through, and it doesn't affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in the following figure:

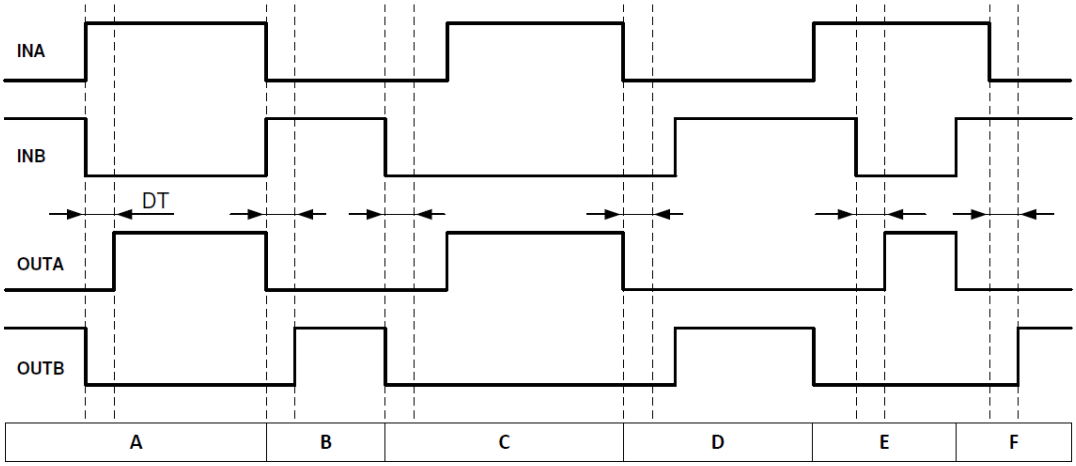


Figure 4-4. Input and Output Logic Relationship with Input Signals

Condition A: INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

Condition B: INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

Condition C: INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal dead time is longer than the programmed dead time. When INA goes high after the duration of the input signal dead time, it immediately sets OUTA high.

Condition D: INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. In this case, the input signal dead time is longer than the programmed dead time. When INB goes high after the duration of the input signal dead time, it immediately sets OUTB high.

Condition E: INA goes high, while INB and OUTB are still high. To avoid overshoot, OUTB is immediately pulled low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

Condition F: INB goes high, while INA and OUTA are still high. To avoid overshoot, OUTA is immediately pulled low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

5 Application and Implementation

5.1 Application Information

The CMT8602X effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the CMT8602X (with up to 5.5-V VCCI and 30-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or GaN transistor. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance, the CMT8602X enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

5.2 Typical Application

The circuit in the figure below shows a reference design with the CMT8602X driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

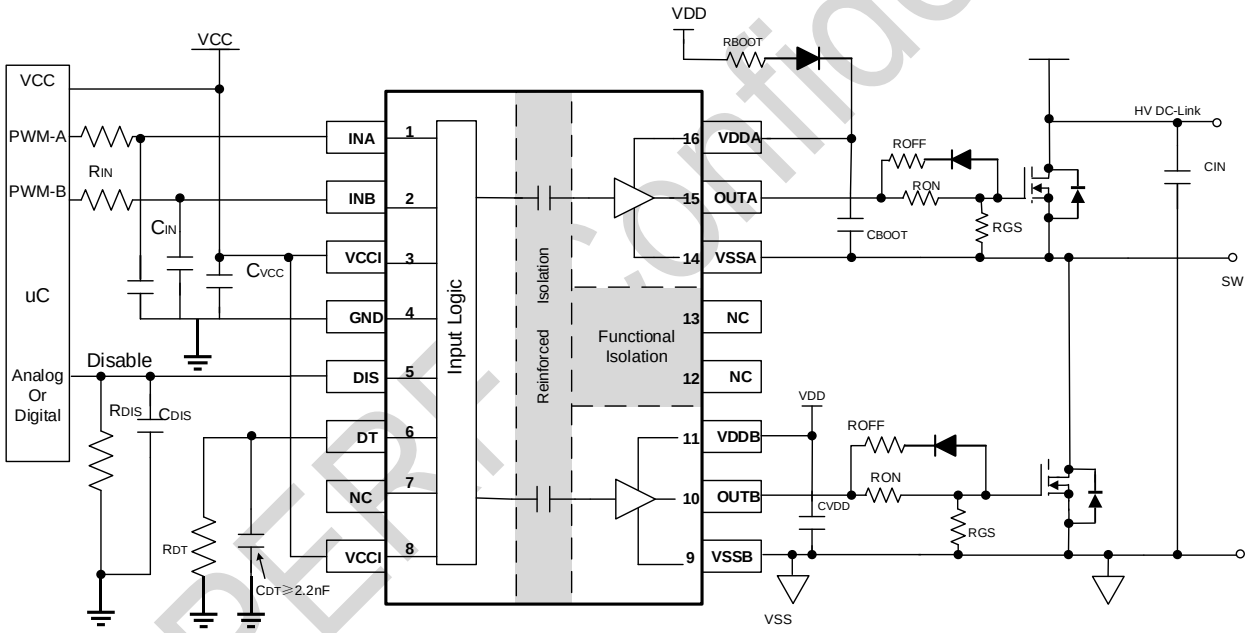


Figure 5-1. Typical Application Schematic

6 Power Supply Recommendations

The recommended input supply voltage (V_{CCI}) for the CMT8602X is between 3 V and 5.5 V. The output bias supply voltage (V_{DDA}/V_{DDB}) ranges from 9 V to 30 V. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of the device. V_{DD} and V_{CCI} must not fall below their respective UVLO thresholds during normal operation. The upper end of the V_{DDA}/V_{DDB} range depends on the maximum gate voltage of the power device being driven by the CMT8602X. The recommended maximum V_{DDA}/V_{DDB} is 30 V.

A local bypass capacitor should be placed between the V_{DD} and V_{SS} pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of ≈10 μF for device biasing, and an additional ≤100 nF capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the V_{CCI} and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the CMT8602X, this bypass capacitor has a minimum recommended value of 100 nF.

7 PCB Layout

7.1 Layout Guidelines

Consider these PCB layout guidelines in order to achieve optimum performance for the CMT8602X.

7.1.1 Component Placement Considerations

- Low-ESR and low-ESL capacitors must be connected close to the device between the V_{CCI} and GND pins and between the V_{DD} and V_{SS} pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node GNDA (HS) pin in bridge configurations, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to place the dead-time setting resistor, R_{DT}, and its bypassing capacitor close to DT pin of the device.
- It is recommended to bypass using a ≈ 1nF low ESR/ESL capacitor, C_{DIS}, close to DIS pin when connecting to a µC with distance.

7.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical loop area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local GNDB referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the V_{DD} bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

7.1.3 High Voltage Considerations

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the isolation performance.
- For half-bridge or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to 1500 V_{DC}, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

7.1.4 Thermal Considerations

- A large amount of power may be dissipated by the CMT8602X if the driving voltage is high, the load is heavy, or the switching frequency is high. Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to V_{DDA}, V_{DDB}, GNDA and V_{SSB} pins is recommended, with priority on maximizing the connection to GNDA and GNDB. However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the V_{DDA}, V_{DDB}, GNDA and GNDB pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or copper from different high-voltage planes overlap.

7.2 Layout Example

The figure below shows a 2-layer PCB layout example with the signals and key components labeled for the SOIC-16 wide body package.

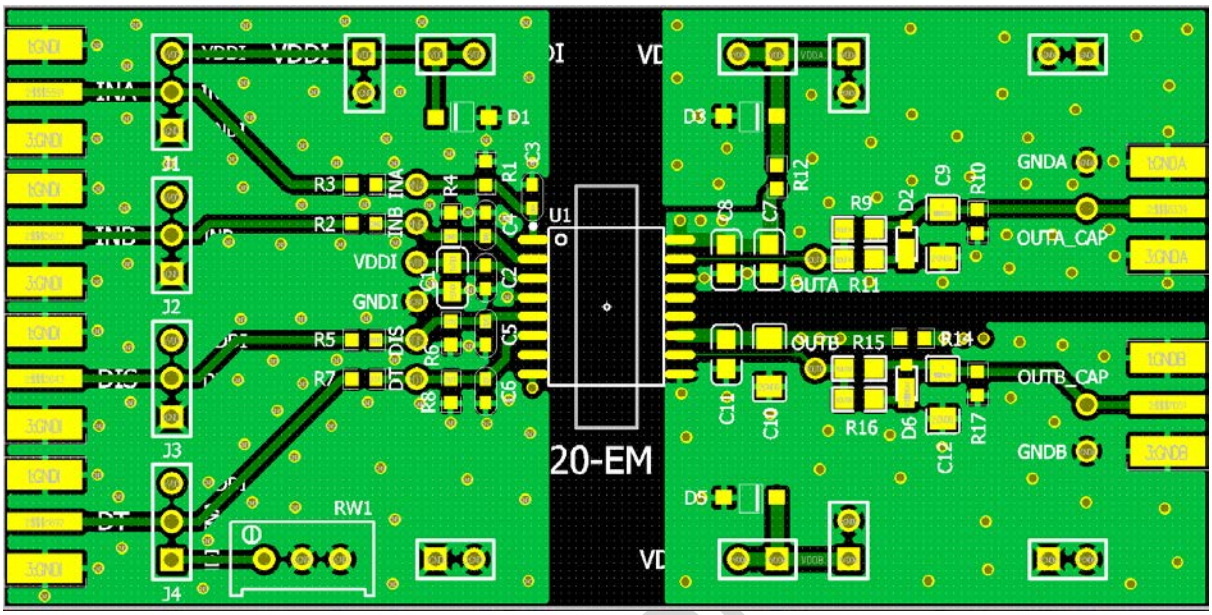


Figure 7-1. Layout Example

Notes:

1. There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

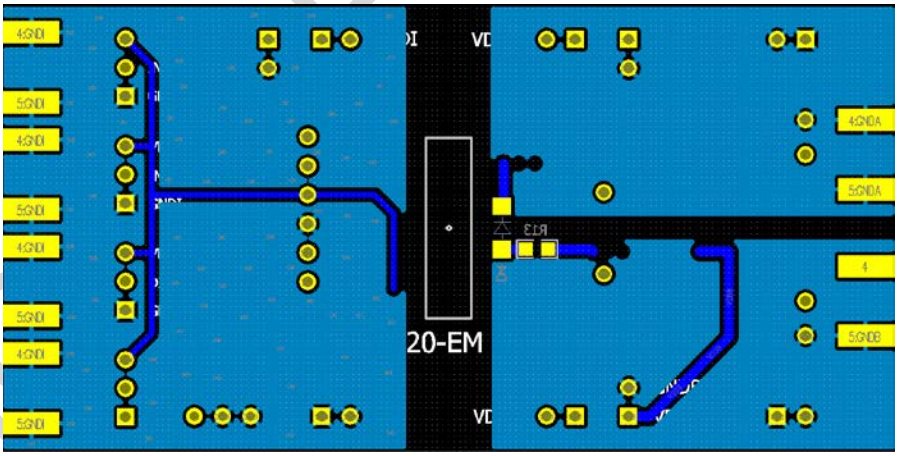


Figure 7-2. Bottom Layer Traces and Copper (Flipped)

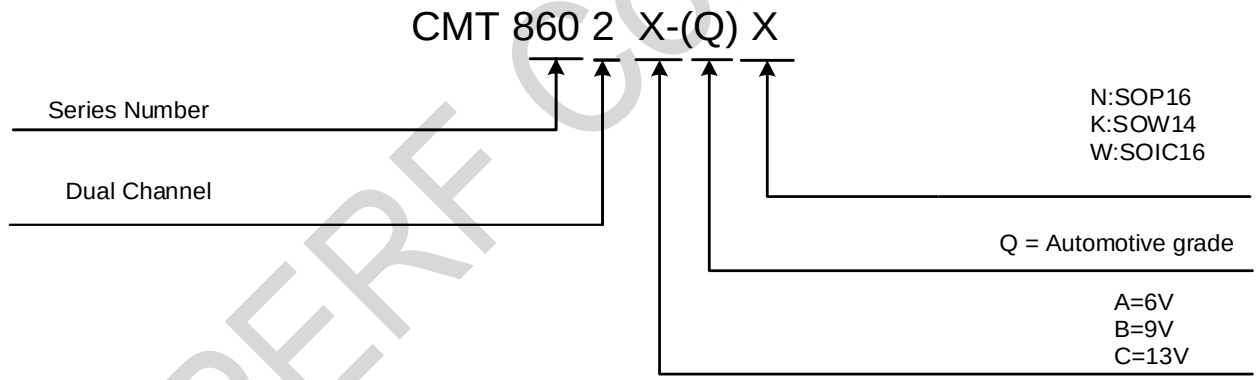
8 Ordering Information

Table 8-1. CMT8602X Ordering Information

Part Number	Isolation Rating (V_{RMS})	Driver side UVLO TYP.	Operating Condition	Auto-motive	Pakcage	Minimum Order Quantity	MSL
CMT8602A-W	5700	6V	-40 to 125℃	/	SOW16	1000	3
CMT8602A-K	5700	6V	-40 to 125℃	/	SOW14	1000	3
CMT8602A-N	3750	6V	-40 to 125℃	/	SOP16	3000	3
CMT8602B-W	5700	9V	-40 to 125℃	/	SOW16	1000	3
CMT8602B-K	5700	9V	-40 to 125℃	/	SOW14	1000	3
CMT8602B-N	3750	9V	-40 to 125℃	/	SOP16	3000	3
CMT8602C-W	5700	13V	-40 to 125℃	/	SOW16	1000	3
CMT8602C-K	5700	13V	-40 to 125℃	/	SOW14	1000	3
CMT8602C-N	3750	13V	-40 to 125℃	/	SOP16	3000	3

Please visit www.hoperf.com for more product/product line information.
Please contact sales@hoperf.com or your local sales representative for sales or pricing requirements.

Part Number Naming Rule:



9 Packaging Information

The packaging information of the CMT8602X is shown in the figure below.

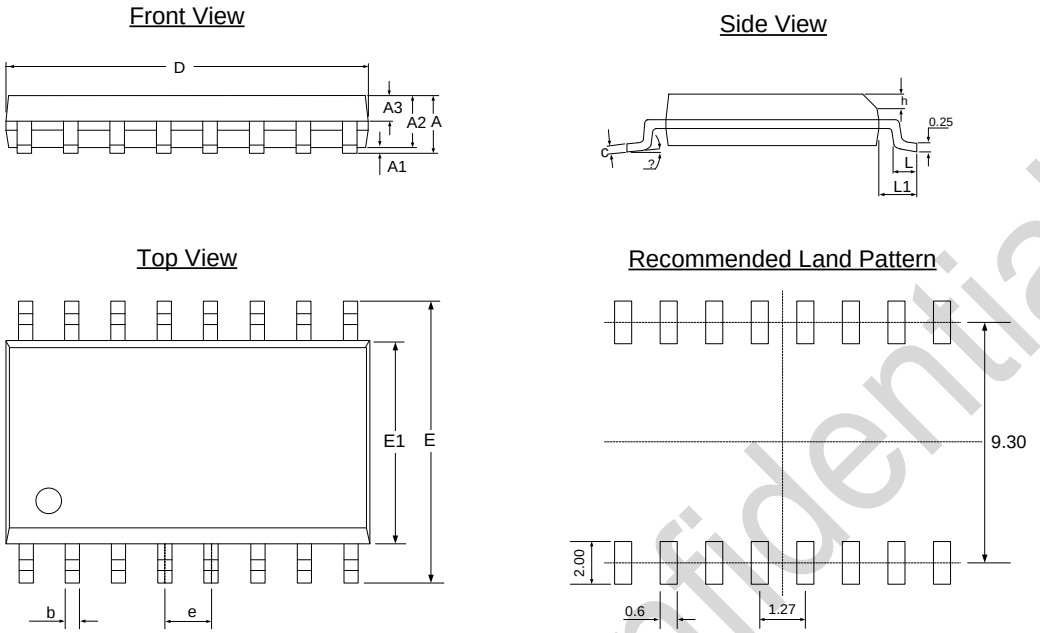


Figure 9-1. SOW 16 Packaging

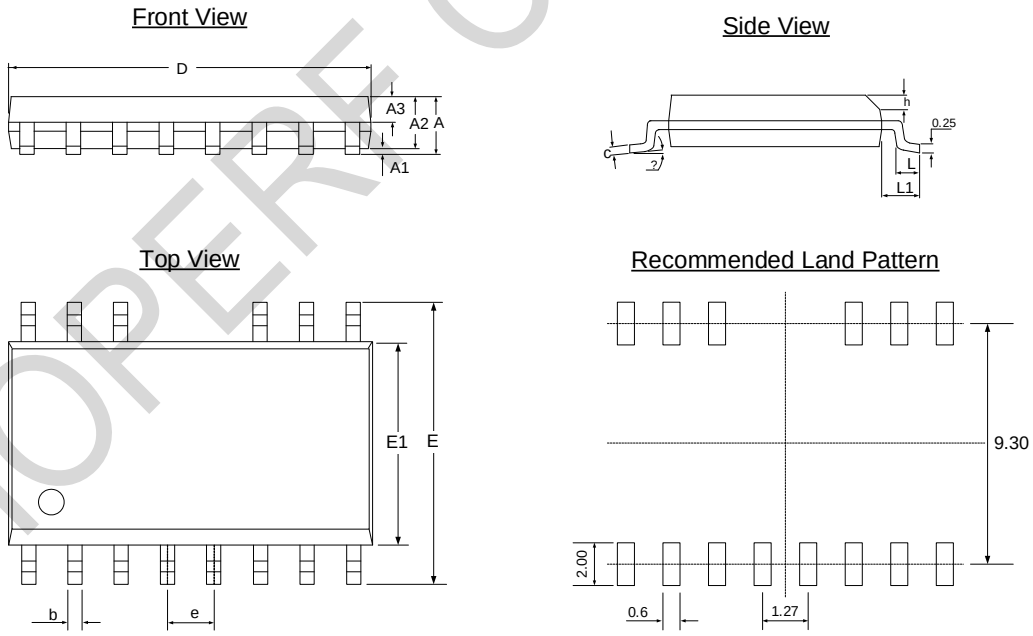


Figure 9-2. SOW 14 Packaging

Table 9-1. SOW16/SOW14 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	-	0.10	-
b	0.31	-	0.51
c	0.10	-	0.33
D	10.1	-	10.50
E	9.97	-	10.63
E1	7.40	-	7.60
e	1.27		
L	0.40	-	1.27
L1	1.40		
θ	0	-	8°

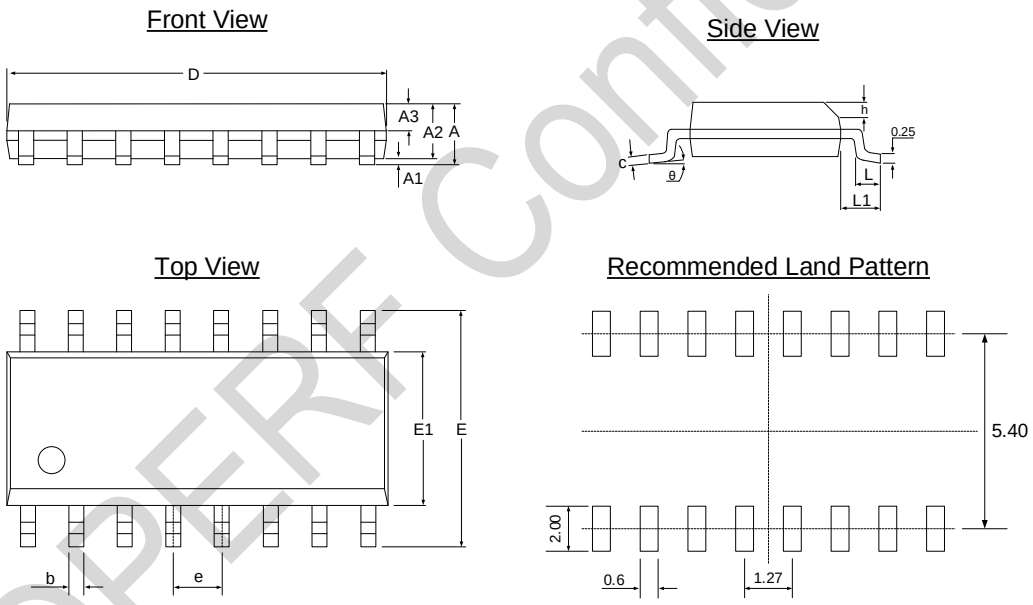


Figure 9-3. SOP 16 Packaging

Table 9-2. SOP16 Packaging Scale

符号	尺寸 (毫米 mm)		
	最小值	典型值	最大值
A	-	-	1.75
A1	0.10	-	0.25
b	0.36	-	0.49
c	0.19	-	0.25
D	9.80	9.90	10.0
E	5.80	-	6.20
E1	3.80	3.90	4.00
e	1.27		
L	0.40	-	1.00
L1	1.05		
θ	0	-	8°

10 Revise History

Table 10-1. Revise History Records

Version No.	Chapter	Description	Date
0.1	All	Initial version	2023-03-27
0.2	All	Update the driver side supply voltage to 30V, while the recommended driver side supply voltage is 25V.	2023/7/22
	1.11	Update the typical chracteristic diagram	
	8	Add MSL in order information	2024/12/3

11 Contacts

Shenzhen Hope Microelectronics Co., Ltd.

Address: 30th floor of 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China

Tel: +86-755-82973805 / 4001-189-180
Fax: +86-755-82973550
Post Code: 518052
Sales: sales@hoperf.com
Website: www.hoperf.com