210-960 MHz OOK/(G)FSK Transmitter SoC

MCU Feature

- CPU kernal
  - High performance single instruction period 1T-8051 kernal
  - Support operating frequency up to 26MHz（XOSC）or 24Mhz（HFOSC）with address efficiency of 20MIPS
  - Operating power consumption is 78 uA/MHz
- Storage
  - 4-KB MTP program storage, support 10 K erasing time
  - 512-Byte XRAM and 256-Byte IRAM
  - 512-Bit EEPROM，support 100,000 erasing time
- Power
  - Power on reset and low voltage detection
  - Embedded LDO provide power for CPU and digital circuit
  - Embedded ultra-low power ULPLDO, the chip achieves Retention function of some peripherals of CPU/RAM/SFR in STOP mode
- I/O
  - 6 multi-functional IO pins (SOP14)
  - Supports highly flexible peripheral function mapping
  - Support level change interrupt/wake up
- Clock source
  - Support up to 26MHz XOSC (high speed frequency crystal oscillator)
  - Embedded high speed 24MHz HFOSC（±1% RC oscillator）
  - Embedded low power 32kHz LFOSC（±1% RC oscillator）
- On-chip debug
  - 1-Wire debugger hardware circuit embedded in CPU
  - Support Keil C51 for program online debugging CMT2187A
  - Support 3 hardware breakpoints, single step debugging
- Peripheral
  - 1 x UART
  - 1 x SPI
  - 1 x CDR (Single-wire RX input clock recovery)
  - 1 x WDT（Independent hardware）
  - 1 x sleep timer（32KHz LFOSC）
  - 2 x 16bit simple timer
  - 2 x 16bit multifunctional timer (3-channel PWM/CCP)
- Code security
  - Burning serial port and single-line debugging interface with lockup function

Sub-1G Transmitter Module Characteristic

- Working frequency：210 – 960MHz
- Modulation Mode: OOK/FSK/GFSK
- Data rate: 0.5– 40 kbps（OOK）
  0.5 - 200kbps（GFSK/FSK）
- Output power：+13dBm（Max.）
- Working current：24mA @+13dBm，433.92MHz CW
- Single-ended high efficiency Class E high frequency transmitting PA
- PA Ramping varies according to the data rate

Working Condition

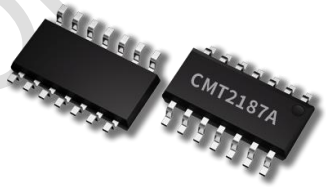
- Temperature range: -40℃ - 85℃
- Working voltage range: 1.8 V - 3.6 V

Application

- Garage door remote control
- Remote control access system
- Consumer wireless remote control
- Smart home
- Home security
- RFID source tag
- Wireless sensor network
- WM-Bus T1 mode

Ordering Information

Part Number	Package	MOQ
CMT2187A-ESR14	SOP14, T&R	3,000 pcs

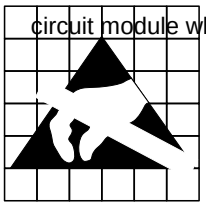


SOP-14

8.65 x 6 x 1.75 mm

Introduction

CMT2187A is a low-power Sub-1G wireless transmitter SoC embedded with an enhanced 1T-8051 core, supporting 210 ~ 960 MHz, OOK/FSK/GFSK modulated wireless transmitter function. The chip is embedded with efficient single-ended PA with output power range which is adjustable from 0 to +13dBm, +13dBm only required 24mA while transmission. MCU programs are stored and run in 4KB MTP storage. The ultra-low-power ULPLDO can save CPU status, RAM data, and configuration register data in STOP mode. Users can use the dedicated 1-WIRE debugger and KEIL51 software to download and run the target debugging code directly into MTP for online simulation. The MTP has a dedicated area for burning 64-bit serial numbers (ids), making it ideal for remote control or active RFID applications while transmitting encrypted information. The chip supports main frequency clock source switching. The system starts with the built-in 24MHz HFOSC by default and optionally switch to the more accurate external 26MHz XOSC as the main frequency clock source of the system according to the MTP burning configuration. The built-in low-power RC oscillator 32kHz LFOSC allows the MCU to perform low-power timed wake-up. HFOSC and LFOSC are calibrated to ±1% accuracy at the factory, and can also be calibrated by calling API functions to access the correction circuit module while using.



Caution! ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.

Table of Contents

1 Electrical Feature

Unless otherwise noted, all electrical performance parameters were measured through the evaluation board CMT2187A-EM Rev 001 under the following conditions: VDD= 3.3V，T_{OP}= 25°C，F_{RF} = 433.92MHz, matching to a 50Ω impedance antenna with an output power of +10dBm.

1.1 Recommended Operation Condition

Table 1- 1. Recommended Operation Condition

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operation digital supply voltage	$V_{AVDDMAX}$	Temperature range is from -40℃ to +85℃	1.8		3.6	V
Operation RF supply voltage	$V_{AVDDMAX}$	Temperature range is from -40℃ to +85℃	1.8		3.6	V
System clock frequency	f_{SYSCLK}			24	26	MHz
Operation temperature	T_{OP}		-40		+85	℃
Supply power slope			1			mV/us

1.2 Absolute Maximum Rating

Table 1-2. Absolute Maximum Rating [1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD supply power	$V_{DVDDMAX}$		-0.3		3.6	V
AVDD supply power	$V_{AVDDMAX}$		-0.3		3.6	V
Interface voltage	V_{PIN}		-0.3		V_{DD}+0.3	V
Junction temperature	T_{JMAX}		-40		125	℃
Storage temperature	T_{STG}		-50		150	℃
Soldering	T_{SDR}	Last at least 30 seconds			255	℃
ESD rating [2]	V_{ESD}	Human Body Model (HBM)	-2		2	kV
Latch current	I_{LATCH}	@ 85℃	-100		100	mA
Input current of I/O port	I_{IOMAX}	Source		3.0		mA
		Sink		3.7		mA

Notes:

1. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Caution! ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.

1.3 Power on reset and low voltage detection

Table 1-3. Supply Voltage Detection Characteristic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
POR power on release lag	t_{RST}	$V_{VDD} > V_{POR}$, Supply voltage <100 us rising to V_{POR}		10		us
POR power on to release voltage threshold	V_{POR}	VDD voltage rising		1.8		V
Reset voltage threshold	V_{RST}		1.64			V
Setup time of the battery sensing device circuit	t_{STAB}			5		us
RSTn pin reset lag	t_{RSTn}			5		ns
Notes: 1. Indicators are based on the average of two measurements.						

1.4 Wakeup Time

Table 1-4. Wakeup Time

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IDLE Mode Wakeup Time	t_{IDLEWK}	Main frequency is 24MHz HFOSC	2		3	SYSCLKs
STOP Mode Wakeup Time	t_{STOPWK}	Main frequency is 24MHz HFOSC		180		us
Notes: 1. STOP mode equals to sleep mode, and the wakeup time is mainly consumed in the internal power start and clock.						

1.5 Transmitter Module Specification

Table 1-5. Transmitter Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency range	F_{RF}	The HXOSC connects to a 26 MHz crystal oscillator	210		480	MHz
			630		960	MHz
Data rate	DR	OOK	0.5		40	kbps
		(G)FSK	0.5		200	
Output power range	P_{OUT}	Single end PA mode	0		+13	dBm
FSK frequency offset range	F_{DEV}	630 ~ 960 MHz	1		300	kHz
		320 ~ 480 MHz	0.5		150	kHz
		210 ~ 320 MHz	0.33		100	kHz
Output power by step	P_{STEP}			1		dB
Transmitting locking time [1] （Startup time）	T_{PLL}	Execute time of API function tx_sym_prepare_for_transmission		620		uS
FSK Transmitting current	$I_{DD-315F}$	0dBm		8.1		mA
		+5dBm		11.5		mA
		+7dBm		13.6		mA
		+10dBm		17.9		mA
		+13dBm		22.2		mA
	$I_{DD-434F}$	0dBm		7.3		mA
		+5dBm		9.7		mA
		+7dBm		11.4		mA
		+10dBm		14.7		mA
		+13dBm		23.5		mA
	$I_{DD-868F}$	0dBm		9.7		mA
		+5dBm		12.6		mA
		+7dBm		14.7		mA
		+10dBm		18.9		mA
		+13dBm		28.8		mA
	$I_{DD-915F}$	0dBm		8.7		mA
		+5dBm		11.4		mA
		+7dBm		13.3		mA
		+10dBm		17.8		mA
		+13dBm		28.6		mA
OOK Transmitting current [3]	$I_{DD-434O}$	0 dBm		5.5		mA
		+5 dBm		6.7		mA
		+7 dBm		7.6		mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		+10 dBm		9.2		mA
		+13 dBm		13.8		mA
	$I_{DD-868O}$	0 dBm		6.6		mA
		+5 dBm		8.1		mA
		+7 dBm		11.0		mA
		+10 dBm		11.3		mA
		+13 dBm		16.5		mA
Phase noise	PN_{434}	100kHz Frequency Offset		82		dBc/Hz
		200kHz Frequency Offset		84		dBc/Hz
		500kHz Frequency Offset		98		dBc/Hz
		1MHz Frequency Offset		105		dBc/Hz
		10MHz Frequency Offset		123		dBc/Hz
	PN_{868}	100kHz Frequency Offset		74		dBc/Hz
		200kHz Frequency Offset		77		dBc/Hz
		500kHz Frequency Offset		89		dBc/Hz
		1MHz Frequency Offset		100		dBc/Hz
		10MHz Frequency Offset		119		dBc/Hz
Harmonic Output	$H2_{315}$	2 times Harmonic @630 MHz，+13 dBm		< -45		dBm
	$H3_{315}$	3 times Harmonic @945 MHz，+13 dBm		< -45		dBm
	$H2_{434}$	2 times Harmonic @868 MHz，+13 dBm		< -45		dBm
	$H3_{434}$	3 times Harmonic @1302MHz，+13 dBm		< -45		dBm
	$H2_{868}$	2 times Harmonic @1736MHz，+13 dBm		< -36		dBm
	$H3_{868}$	3 times Harmonic @2604MHz，+13 dBm		< -36		dBm
	$H2_{915}$	2 times Harmonic @1830MHz，+13 dBm		< -36		dBm
	$H3_{915}$	3 times Harmonic @2745MHz，+13 dBm		< -36		dBm
OOK modulate the flattering ratio				60		dB
Occupied bandwidth	OBW_{315}	-20 dBc bandwidth，RBW = 1kHz，SR = 1.2 kbps		6		kHz
	OBW_{434}	-20 dBc bandwidth. RBW = 1kHz，SR = 1.2 kbps		7		kHz

Notes:

[1]. The term has included the crystal start-up time.

[2] With the 8051 core current, HFOSC uses an internal 24MHz high-speed RC as the clock source.

[3] Baseband data is 50% high-low duty cycle.

1.6 Oscillator

Table 1-6. Oscillator Specification

Type	Parameter	Symbol	Test Condition	Min	Typ	Max	Parameter
High frequency crystal oscillator XOSC	Crystal frequency [1]	F_{HXOSC}			26		MHz
	Frequency accuracy [2]				±20		ppm
	Load capacitance	$C_{HX-LOAD}$			15		pF
	Equivalent resistance	R_{HX-ESR}				60	Ω
	Startup time [3]	t_{HXOSC}			400		us
High frequency RC oscillator HFOSC	RC oscillation frequency	F_{HF_RC}		3	24	24	MHz
	Frequency accuracy [4]				1		%
Embedded 32KHz RC oscillator LFOSC	Oscillator frequency	F_{LP_RC}			32		kHz
	Frequency accuracy [4]				1		%

Notes:

[1]. CMT2187A can drive the XTAL pin directly from external reference clock via coupling capacitor. The peak value of external clock signal is required to be between 0.3 and 0.7 V.

[2]. Which include: initial error, crystal load, aging and change with temperature. The acceptable crystal frequency error is limited by the RF frequency deviation between the receiver bandwidth and the corresponding transmitter.

[3]. This parameter is largely related to the crystal.

[4]. Frequency accuracy is the corrected index, and related to environmental factors, users can actively call the relevant correction API function for correction.

1.7 MTP Feature

Table 1-7. MTP Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Parameter
Burning voltage	V_{PROG}		3.0		3.6	V
Burning time	T_{PROG}	1 Word（4 bytes），clock is 24MHz	20.8		37.5	us
Erasing time	T_{ERASE}	1 page，clock is 24MHz	10.4		18.8	ms
Read time	T_{READ}	1 Word（4 bytes），clock is 24MHz		41.7		ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Parameter
		2.0 V ≤ DVDD < 2.4 V				
		1 Word（4 bytes），clock is 24MHz 2.4 V ≤ DVDD < 3.6 V		125		ns
Maximum erasing time	EC_{MTP}		10K			cycles
Data saving time	RET_{MTP}	@+85℃		10		years

Notes:
1. The MTP program space capacity is 1K x 32, and the limiting throughput at 24 MHz clock is 96 M Byte/S. The instruction cache circuit is integrated on the chip, which converts the 32-bit content of the current address into four 8-bit instructions gradually to the 8051 kernal after each reading, and the actual address rate is about 20MIPS, depending on the cache hit rate and the program code.
2. The chip will detect the DVDD voltage in real time. If the current MCU clock (used for MTP access) is greater than or equal to 8 MHz, the MTP read time will be automatically reduced when the voltage is lower than 2.4V. This function can be accomplished without user manual operation, because when the voltage is lower than 2.4 V, the MCU working efficiency will be reduced.

1.8 EEPROM Feature

Table 1-8. EEPROM Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Parameter
Erasing time	t_{EE-WR}	EEPROM operation process		14		ms/unit
		EEPROM operation process		42		ms
Burning times	t_{EE-CNT}	EEPROM operation process	10,000	100,000		cycles

Notes: [1]. The operation address refers to 2 Bytes storage units, that is, each unit is 2 Bytes.

1.9 Direct Current Feature

Table 1-9. Direct Current Feature @3.3V，25℃

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Normal mode	I_{NORMAL}	Main frequency = 26 MHz，XOSC		78		uA/MHz
		Main frequency = 24 MHz，HFOSC		70		uA/MHz
		Main frequency = 3.25 MHz，XOSC		372		uA/MHz
		Main frequency = 3 MHz，HFOSC		301		uA/MHz
IDLE mode	I_{IDLE}	Main frequency = 26 MHz，XOSC		54		uA/MHz
		Main frequency = 24 MHz，HFOSC		45		uA/MHz
		Main frequency = 3.25 MHz，XOSC		336		uA/MHz
		Main frequency = 3 MHz，HFOSC		266		uA/MHz
STOP mode	I_{STOP_LFOSC}	Open the sleep timer and LFOSC		2.6		uA
	I_{STOP}	Turn off the sleep timer and LFOSC		1.6		
Notes: [1]. Test program operates with While（1）in loop and the GPIO with no load.						

1.10 AC Characteristic

Table 1-10. AC characteristic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level output	V_{OH}	Load in 1KΩ，VDD = 3.3 V	VDD-0.4			V
Low level output	V_{OL}	Load in 1KΩ，VDD = 3.3 V			0.4	V
High level input	V_{IH}	VDD = 3.3 V		0.7*VDD		V
		VDD = 2.0 V		0.7*VDD		V
Low level input	V_{IL}	VDD = 3.3 V		0.2*VDD		V
		VDD = 2.0 V		0.2*VDD		V
Port leakage current	I_{LKG}	VDD = 2.0 V – 3.6 V		TBD		nA

1.11 High Frequency Transmitting Typical Performance

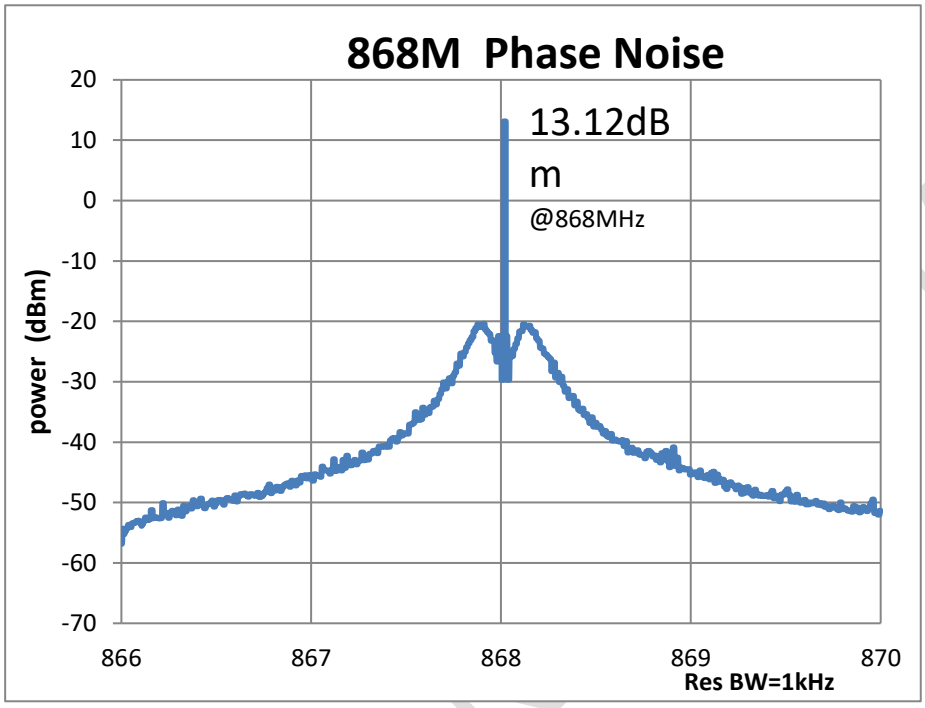


Figure 1-1. Phase Noise F_{RF} = 868MHz, P_{OUT} = +13dBm, without modulated

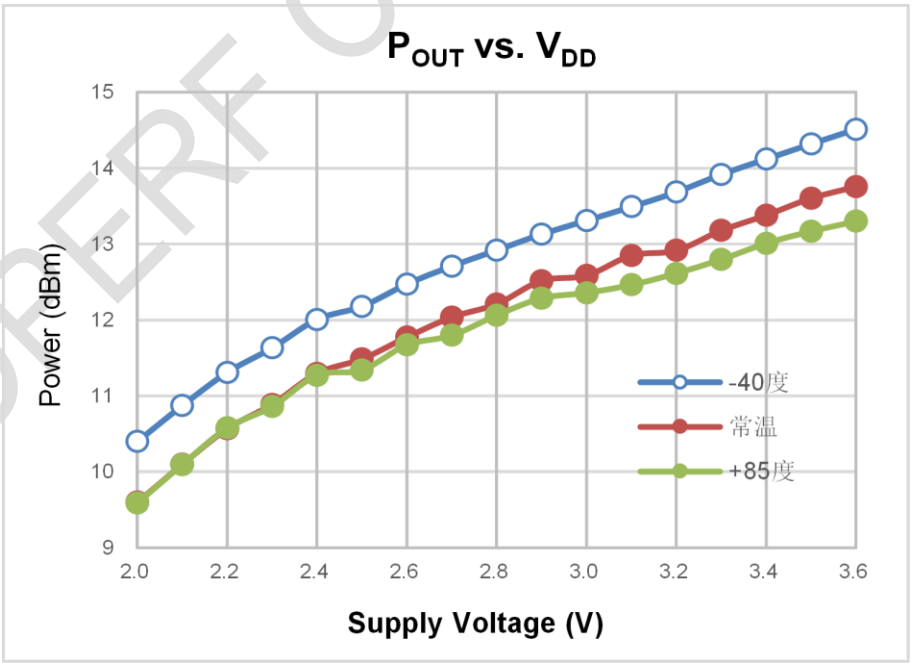


Figure 1-2. Output Power Changes Along with the Supply Voltage

F_{RF} = 433.92MHz, P_{OUT} = +13dBm

2 Pin Description

2.1 CMT2187A-ESR16 Pin Definition

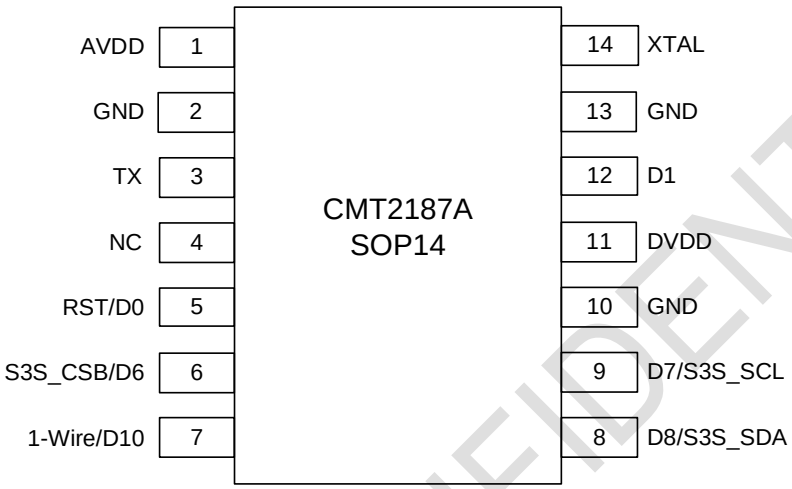


Figure 2-1. CMT2187A-ESR SOP14 Pin Arrangement

Table 2-1. CMT2187A-ESR Pin Description

Pin	Name	Pin Character		Function Description
1	AVDD	A		Analog RF power source input
2	GND	A		Ground
3	TX	A		Single end PA transmitting output
4	NC	--		Float
5	RSTn/D0	IO	D0	GPIO0，belongs to general GPIO
		IO	RSTn	Whole reset input, low effective
6	S3S_CSB/D6	IO	D6	GPIO6，belongs to general GPIO
		IO	S3S_CSB	CSB selected input of the S3S burning interface
7	1-WIRE/D10	IO	D10	GPIO10，belongs to general GPIO
		IO	1-WIRE	Single wire debug line
8	D8/S3S_SDA	IO	D8	GPIO8，belongs to general GPIO
		IO	S3S_SDA	SDA data input /output of the S3S burning interface
9	D7/S3S_SCL	IO	D7	GPIO7，belongs to general GPIO
		IO	S3S_SCL	SCL clock input of the S3S burning interface
10	GND	A		Ground
11	DVDD	A		Power supply of the digital circuit

Pin	Name	Pin Character	Function Description
12	D1	IO	GPIO1，belongs to general GPIO
13	GND	A	Ground
14	XTAL	A	Crystal input pin, connecting the 26MHz crystal to GND
Notes: S3S is the burning interface and the burner needs to be connected to the chip through this interface.			

3 Typical Reference Design

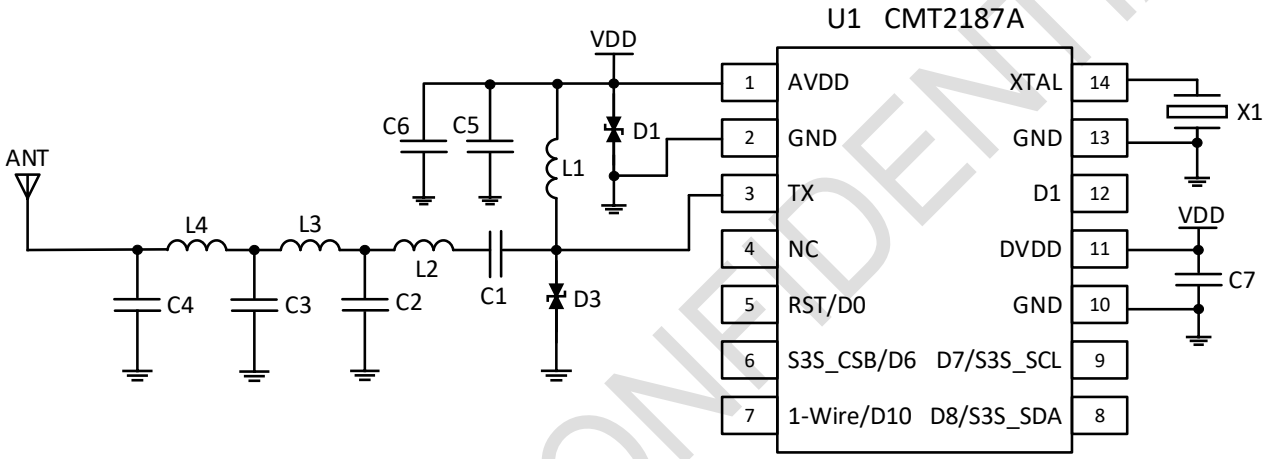


Figure 3-1. CMT2187A Single End PA Output Reference Schematic Diagram

Table 3-1. CMT2187A Single End PA Output Matching Reference BOM

Sign	Description	315 MHz	434 MHz	868 MHz	915 MHz	Unit	Vendor
U1	CMT2187A	--				-	CMOSTEK
X1	±20 ppm, SMD3225 mm, crystal	26				MHz	EPSON
L1	±10%, 0603 layer inductance	220	180	100	100	nH	Sunlord LQG18
L2	±10%, 0603 layer inductance	75	39	12	10	nH	Sunlord LQG18
L3	±10%, 0603 layer inductance	75	39	10	5.6	nH	Sunlord LQG18
L4	±10%, 0603 layer inductance	56	47	8.2	8.2	nH	Sunlord LQG18
C1	±0.25 pF, 0402 NP0, 50 V	33	15	4.7	4.7	pF	-
C2	±0.25 pF, 0402 NP0, 50 V	3.6	5.6	5.6	4.3	pF	-
C3	±0.25 pF, 0402 NP0, 50 V	5.6	4.7	2.2	2.2	pF	-
C4	±20%, 0402, NP0, 50 V	NC	3.3	NC	NC	pF	-
C5	±20%, 0402 X7R, 25 V	100				nF	
C6	±20%, 0402 X7R, 25 V	470				pF	
C7	±20%, 0402 X7R, 25 V	100				nF	
D1	XE5D5VB，ESD protective diode						

Sign	Description	315 MHz	434 MHz	868 MHz	915 MHz	Unit	Vendor
D3	XE5D5VB，ESD protective diode						

4 Feature Description

The CMT2187A is a high-performance 8051 SoC with embedded Sub-1GHz OOK/(G)FSK transmitters and user programs are burned in 4K Bytes of MTP and run at clock frequencies up to 26MHz. The chip is applied in low-power wireless transmission among frequency band from 210 to 960MHz, where integrates the following core modules:

- High performance 8051 based on MTP with 1-Wire on-line debugging circuit;
- abundant digital and analog peripheral resources;
- Sub-1G OOK / G(F)SK modulated transmitting module；

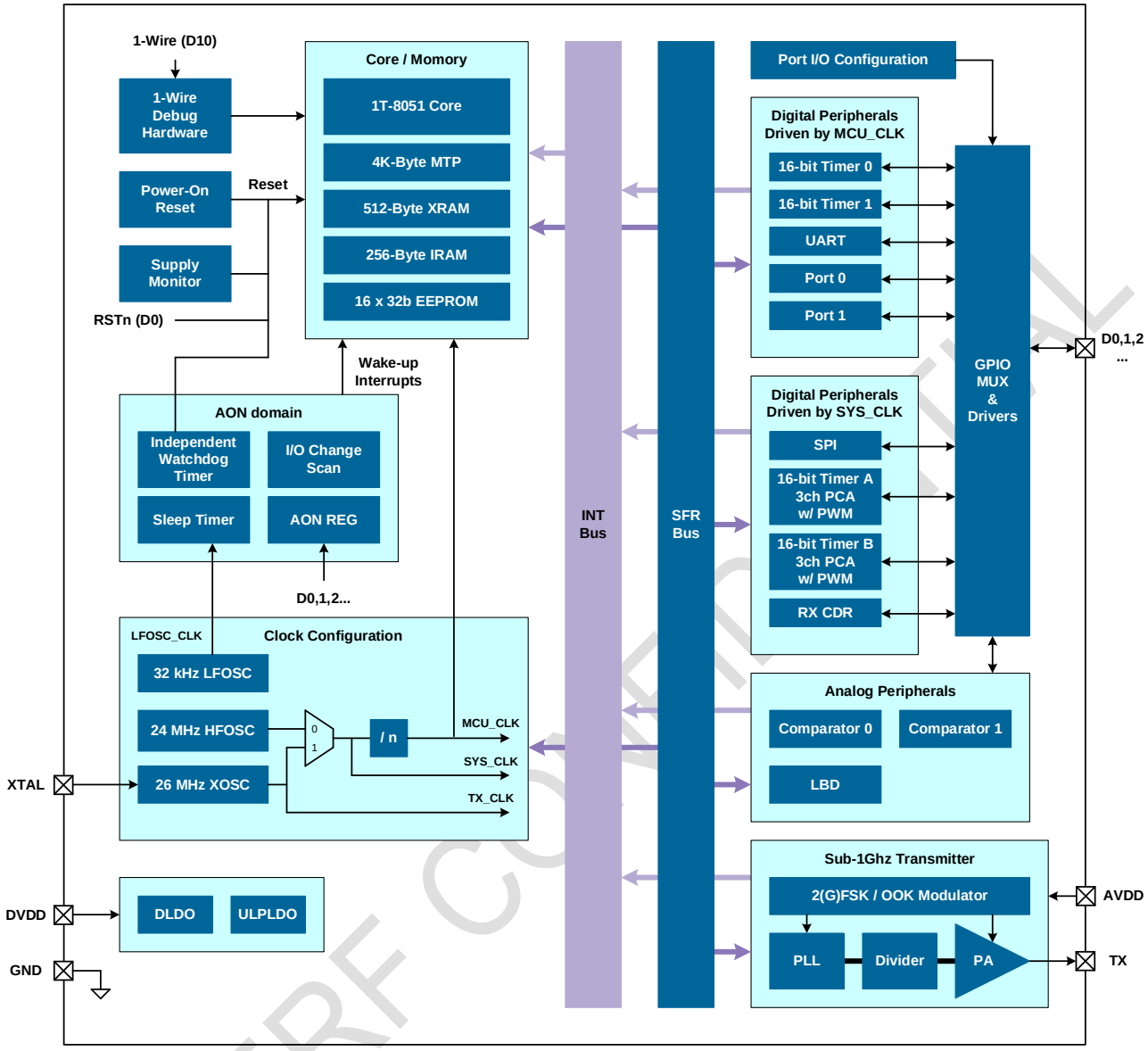


Figure 4-1. System Diagram

（Note：D 0，1，2 are literally refers to GPIO，the numbers of GPIO are vary according to different package .）

4.1 High Performance 1T-8051

CMT2187A is embedded with enhanced 1T-8051, single period run instructions, which is fully compatible with MCS-51 instructions, and the access efficiency is up to 20 MIPS. The CPU comes with a 1-Wire interface for online debugging hardware module, which can be connected to Keil C51 software on the PC through the debugger.

4.2 CMT2187A Storage

Embedded with MTP (non-volatile storage) on chip for storing user code, which runs directly on MTP, supporting 10K times of repeated erasing and burning. The user code space is 4K Byte and the address range

is 0x0000 – 0x0FFF. There is a separate 512 Byte space in the MTP dedicated to the chip configuration and ID, which can only be accessed by the chip burner and not by the user program. The burning 64 Byte ID is copied to the SFR register in the Always-ON area when powered on.

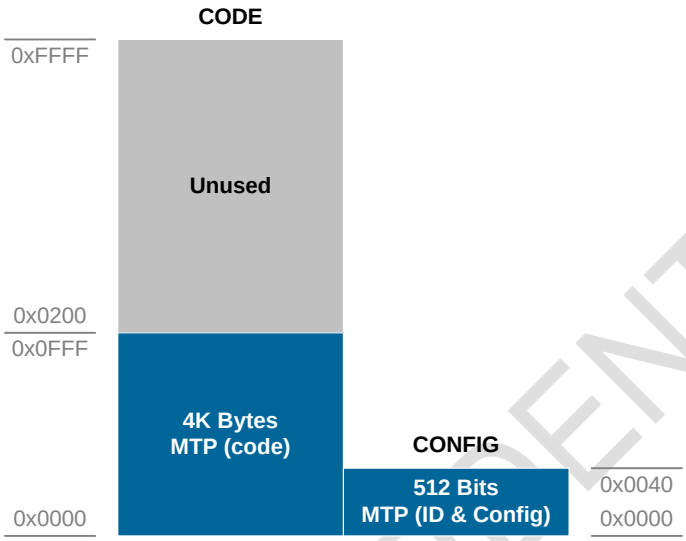


Figure 4-2. MTP Address Mapping

There are 256 Bytes of IRAM on chip as internal data storage, and two pages of SFR as registers to configure and control chip operation. SFR page switching is done by accessing Bit 0 at SFR address 0xFF. There are 512 Bytes of XRAM on chip as data storage, and the address range is 0x0000 – 0x01FF.

AON SFR does not map directly to the following address range. Users can access the AON SFR indirectly by enabling the AON_ADDR, AON_WDATA, and AON_RDATA register port in SFR Page 0 or Page 1.

The chip also provides 512 bits EEPROM as important data for power down storage. Users can access through the SFR register with erasing time of 100,000. If the erasing time was required to 1 million or more, the regular increase/decrease data for the feature can be supported by a specific algorithm (such as balanced gray code). More information please consult to the sale representative of HOPERF.

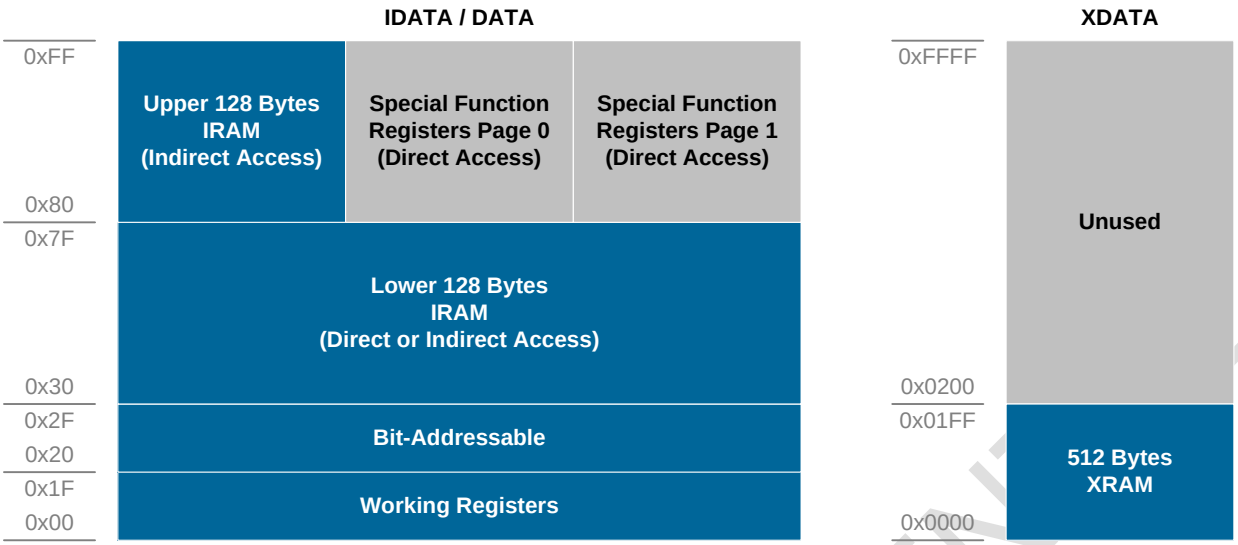


Figure 4-3. IRAM，SFR and XRAM Address Mapping

4.3 Work Mode

CMT2187A has two power pins, AVDD is responsible for powering the internal RF circuit, and the DVDD is responsible for powering the Always-On digital module and the analog module except RF. Most of the digital modules work under the built-in DLDO and can be switched to ULPLDO power supply at STOP mode to achieve low leakage Retention mode. For digital and analog peripherals, user can turn them off when not in use, while the clock gating of the peripherals can be turned off independently to save more power.

Table 4-1. CMT2187A work mode

Work mode	Description	Entry mode	Wakeup source
Normal	Normal operating condition	The user program is automatically entered after being burned and powered on	None
IDLE	● DLDO enabled ● System clock（HFOSC or XOSC）open ● CPU kernal suspend ● Peripheral operation	Set the IDLE bit in the PCON register	I/O level variation Comparator output

Work mode	Description	Entry mode	Wakeup source
STOP (Retention)	● ULPLDO enabled ● System clock（HFOSC or XOSC）Close ● CPU core，all memory, peripheral configuration as well as status reservation ● LFOSC enabled，Always-On module and comparator work ● GPIO state remained unchanged	1. Set the STOP bit in the PCON register 2. Set the SLEEP bit in the AON_SFR_03 register	I/O level variation Comparator output twirling Sleep timer timed out

4.4 Retention under STOP Mode

The ultra-low power ULPLDO is integrated on chip to provide stable voltage to save the working state of the chip when the CPU enters the STOP mode, which is called Retention function. The Retention mode allows the chip to recover from its previous state from a STOP wake-up immediately and continue working without restarting the program. In Retention mode, all RAM data is stored; MTP and EEPROM data can be stored at power off.

Table 4-2. CMT2187A Stores Content in STOP Mode

Storage Name	Reserve Data	Power Supply Method
MTP	√	Power off Saving
EEPROM	√	Power off Saving
IRAM	√	ULPLDO
XRAM	√	ULPLDO

In Retention mode, both power-on reset (POR) and real-time voltage Monitor (Power Monitor) remain in working state. The following lists whether all functional modules have saved the SFR configuration and working status as well as their corresponding power supply mode. Users can disable the modules that can work under STOP mode. For a module that only saves its configuration and working state loss, there's no need for users to reconfigure the SFR and the module will restart working. Which means that the module will be automatically reset.

Table 4-3. CMT2187A Stores Content of the Function Modules in STOP Mode

Module Name	Reserve configuration	Reserve working state	Whether to work	Power Supply Method
Watch Dog Timer	√	√	√	DVDD
Sleep Timer	√	√	√	DVDD
Key Scan	√	√	√	DVDD
Comparator 0	√	√	√	DVDD
Comparator 1	√	√	√	DVDD
UID & CFG register	√	√	×	DVDD
IO configuration and state	√	√	×	DVDD
1T-8051 kernel	√	√	×	ULPLDO
Timer 0	√	√	×	ULPLDO
Timer 1	√	√	×	ULPLDO
UART	√	√	×	ULPLDO
Port 0	√	√	×	ULPLDO
Port 1	√	√	×	ULPLDO
SPI	√	×	×	ULPLDO
Timer A	√	×	×	ULPLDO
Timer B	√	×	×	ULPLDO
CDR	√	×	×	ULPLDO
Sub-1G Transmitter	√	×	×	ULPLDO
LBD	√	×	×	Power off
1-Wire Debug	×	×	×	Power off

4.5 I/O

Functional mapping of all I/O of CMT2187A is listed in Table 2-1 and Table 2-2. External reset pin RSTn and D0 are multiplexed, user can set the RST_IN_EN bit of the AON_SFR_07 register to 0 to mask the external reset. All GPIOs can be configured uniformly with 2 drive capabilities, and each GPIO can be mapped to Port 0, Port 1, or multiple digital peripherals, more information please refer to the user manual.

The S3S interface for burning MTP and the 1-Wire interface for online debugging are only effective within 6 ms after the chip is powered on and reset. If the S3S command is detected within 6 ms, it will enter MTP burn mode; If the 1-Wire debugging start command is detected, the chip will enter to online debugging mode. If no commands are detected, the chip goes into normal operating mode. After entering to the STOP mode, all I/ O remain in the status before the STOP mode.

4.6 Clock

The system supports the main frequency clock source switching. The embedded 24MHz HFOSC is used to start the system by default, and optionally switch to the more accurate external 26MHz XOSC as the main frequency clock source of the system according to the MTP burning configuration. The built-in low-power RC oscillator 32kHz LFOSC allows the MCU to perform low-power timed wake-up.

HFOSC and LFOSC are calibrated to ±1% accuracy at the factory, and can also be calibrated by calling API functions to access the correction circuit module while using. Each peripheral has an independent clock gating, and users can further save power by configuring SFR to turn off clock gating when the related peripherals are not in use.

4.7 Reset Source

The chip reset enables the entire system to its initial state, restarts and corrects the internal modules, and the program will restart from PC address 0 x 0000. CMT2187A support the following 4 reset source:

- Power on reset（POR）
- External pin reset RSTn
- VDD power detect reset
- Watch dog reset

4.8 Digital and Analog Peripheral

In terms of digital peripherals, CMT2186 on-chip offers one UART, one SPI, independent watchdog, one sleep timer, two 16-bit simple timers, two 16-bit multifunction timers (which supports 3 capture/comparators and PWM output). There is also an RX CDR for clock recovery on single-bit I/O inputs, which are typically demodulated signals for wireless receivers. The analog peripherals include 2 independent comparators, as well as a low voltage detection (LBD) module which is used for compensating the power of wireless transmission.

4.9 Sub-1G Single Transmitter

CMT2187A integrates a high-performance Sub-1G single transmitter and adopts an efficient single-ended Class E PA structure, with transmitting power up to +13dBm and consuming only 24mA current on this occasion. The transmitter supports OOK/GFSK/FSK modulation mode, and adopts fractional frequency division phase-locked loop technology, which only needs an external 26MHz crystal oscillator to cover most of the commonly used frequency bands of 210 - 960MHz.

5 Ordering Information

Table 5-1. CMT2187A Ordering Information

Part Number	Description	Package	Pack	Operational Condition	Minimum Order Quantity（Integral multiple）
CMT2187A-ESR	210-960Mhz transmitting SoC	SOP14	T&R	1.8 to 3.6V -40 to 85℃	3,000
Notes: “E” refers to extended industrial grade. The temperature range is from -40 to +85. “S” refers to SOP package. “R” refers to tape & reel packing. MOQ is 3000 pcs.					

For more information about product, please visit www.hoperf.com.

For purchasing or price requirements, please contact sales@hoperf.com or local sales representative

6 Package Outline

Package information of CMT2187A-ESR are shown as followed:

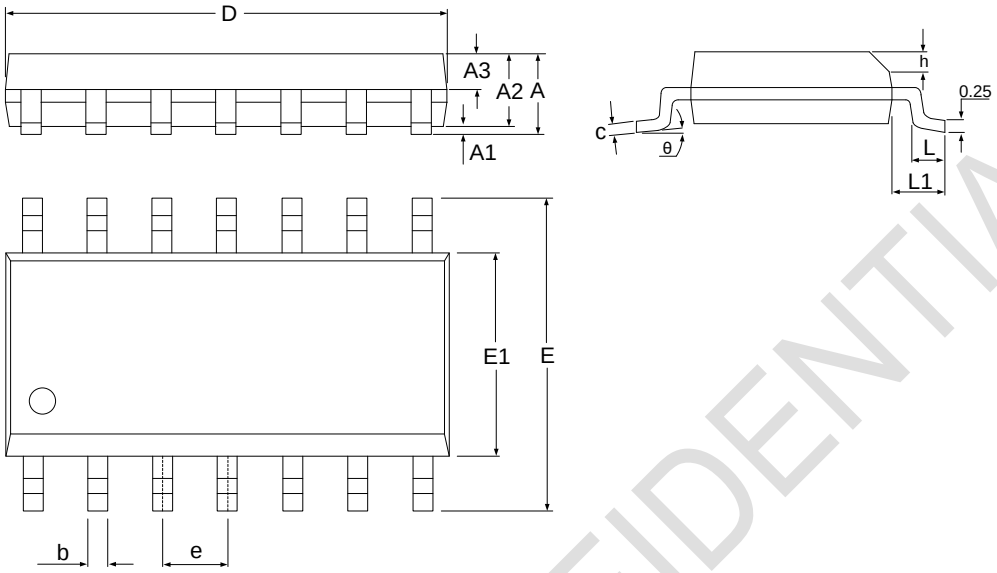


Figure 6-1. SOP14 Package Outline

Table 6-1. SOP14 Package Scale

Symbol	Scale (mm)		
	Min	Typ	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.30	-	0.60
L1	1.05 BSC		
θ	0	-	8°

7 Top Silk Printing

Figure 7-1. CMT2187A Top Silk

Table 7-1. CMT2187A Top Silk Description

Silk printing	Laser
Pin 1 label	Circle diameter = 1 mm
Font size	High 0.6 mm, right-aligned； Wide 0.4 mm
First line silk print	CMT2187A, represents part number CMT2187A
Second line silk print	YYWW represents the date number of factory manufacture. YY represents the last 2 digit of the year, WW represents the working week of the year. ①②③④⑤⑥ is the internal trace code.

8 Related Documentation

Table 8-1. CMT2187A Related Documentation

Document No.	Document Name	Description
	CMT2187A User Manual	CMT2187A user instruction manual
	SFR Register Table	
	GPIO Function Mapping Information Quick Search	

9 Revise History

Table 9-1. CMT2187A Revise Record

Rev No.	Update	Revise Record	Release Date
0.1	All	Initial version	2024/11/12
0.2	1	Update some electrical characteristic parameters	2024/11/18
0.3	All	Review	2024/11/21

10 Contacts

Shenzhen Hope Microelectronics Co., Ltd.

Address: 30th floor of 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China

Tel: +86-755-82973805 / 4001-189-180

Fax: +86-755-82973550

Post Code: 518052

Sales: sales@hoperf.com

Website: www.hoperf.com