CMOSTEK

CMT2189A

240 – 960 MHz SoC (G)FSK/OOK Transmitter

Features

- High-Performance RISC Microcontroller Core
  - All Single-Cycle Instructions Except Branches
  - Up to 8 MHz Clock
  - Multiple Interruption Supported
  - 32 Bytes EEPROM / 64 Bytes SRAM / 1024 Words Flash
- High-Performance OOK Transmitter
  - All Features Programmable on the RFPDK
  - Frequency Range: 240 to 960 MHz
  - FSK, GFSK and OOK Modulation
  - Symbol Rate up to 100 ksps
  - Configurable Single-Ended or Differential PA Output
  - Output Power: -10 to +13 dBm
- Supply Voltage: 2.3 to 3.6 V
- 1-pin Crystal
- FCC / ETSI Compliant
- RoHS Compliant
- 14-pin SOP Package

Applications

- Remote Keyless Entry (RKE)
- Garage and gate door openers
- Home/Building Automation and Security
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Consumer Electronics Applications

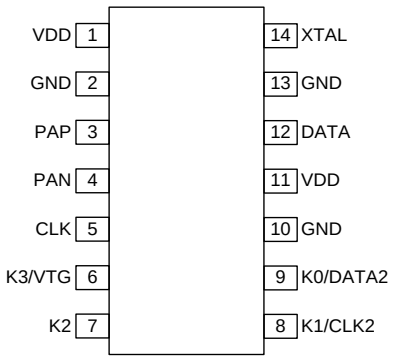
Ordering Information

Part Number	Frequency	Package Option	MOQ
CMT2189A-ESR	868.35 MHz	T&R	2,500 pcs
CMT2189A-ESB	868.35 MHz	Tube	1,000 pcs
More Ordering Info: See Page 62			

Descriptions

The CMT2189A devices are fully integrated, highly flexible, high performance, SoC (G)FSK/OOK transmitters with embedded RISC microcontroller core for various 240 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The CMT2189A includes a 1024 words flash for programming the user's application, supports up to 4 push buttons to implement the user defined functions. All the device features (such as frequency, output power, WDT, Security and etc.) and programs can be burned into the device using the CMOSTEK USB Programmer and RFPDK. Alternatively, in stock product of 868.35 MHz is available for immediate demands. The CMT2189A uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the BOM counts. The device can deliver up to +13 dBm output power and the PA output can be either single-ended or differential. The device operates from 2.3 V to 3.6 V. Its low power design enables superior operation life for battery powered application. The CMT2189A transmitter together with CMOSTEK NextGenRF™ receiver enables a highly flexible, low cost RF link..

SOP14



CMT2189A

Typical Application

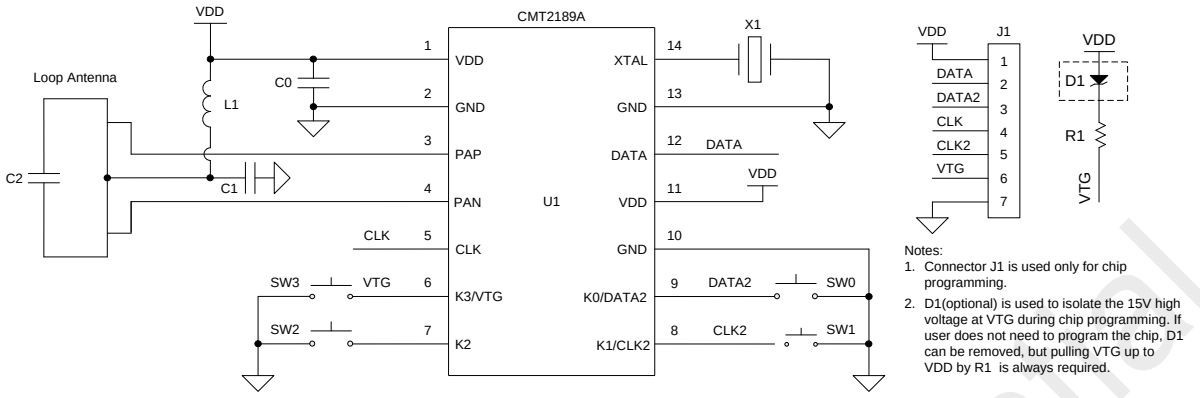


Figure 1. CMT2189A Typical Application with Differential PA Output

Table 1. BOM of 868.35 MHz Application with Differential PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189A, 240 – 960 MHz SoC (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
C2	±0.25 pF, 0402 NP0, 50 V	1.5	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	100	nH	Murata LQG18

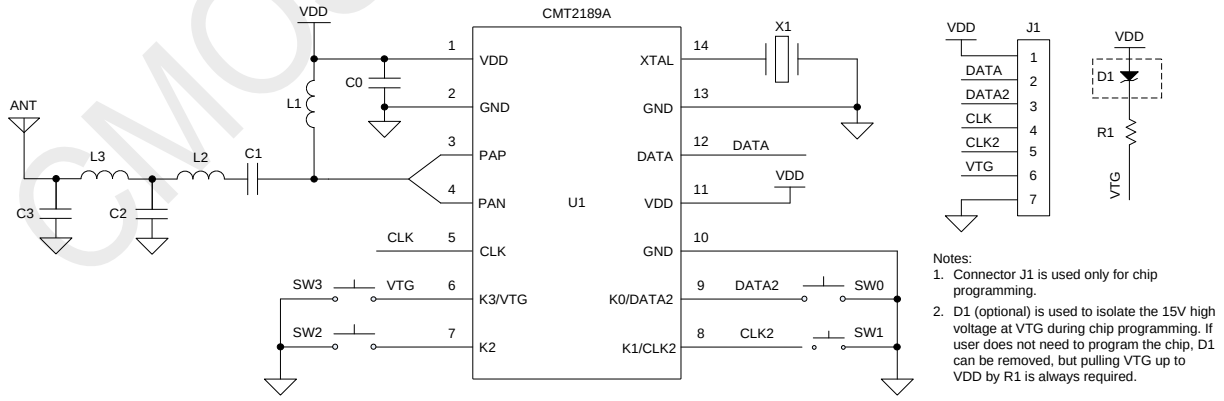


Figure 2. CMT2189A Typical Application with Single-ended PA Output

Table 2. BOM of 433.92 MHz Application with Single-ended PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189A, 240 – 960 MHz SoC (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	9.1	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	8.2	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	100	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	8.2	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	8.2	nH	Murata LQG18

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
BW	Bandwidth
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
GFSK	Gauss Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
LDO	Low Drop-Out
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PN	Phase Noise
RBW	Resolution Bandwidth
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
TBD	To Be Determined
Tx	Transmission, Transmitter
Typ	Typical
XO/XOSC	Crystal Oscillator
XTAL	Crystal

Table of Contents

1. Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 868.35 MHz, FSK modulation, output power is +10 dBm terminated in a matched 50 Ω impedance with single-ended PA output, unless otherwise noted.

1.1 Recommended Operating Conditions

Table 3. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		2.3		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

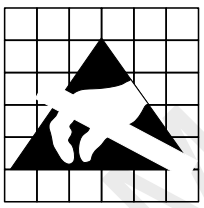
1.2 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Transmitter Specifications

Table 5. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}		240		480	MHz
Synthesizer Frequency Resolution	F_{RES}			198		Hz
Symbol Rate	SR		0.5		30	ksps
Maximum Output Power[2]	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
PA Ramping Time[3]	t_{RAMP}		0		1024	us
Current Consumption, Single-ended	$I_{DD-S-433.92}$	0 dBm, 433.92 MHz, FSK		9.1		mA
		+10 dBm, 433.92 MHz, FSK		20.5		mA
		+13 dBm, 433.92 MHz, FSK		27.4		mA
	$I_{DD-S-868.35}$	0 dBm, 868.35 MHz, FSK		10		mA
		+10 dBm, 868.35 MHz, FSK		21.3		mA
		+13 dBm, 868.35 MHz, FSK		28		mA
Current Consumption, Differential	$I_{DD-D-433.92}$	0 dBm, 433.92 MHz, FSK		5.8		mA
		+10 dBm, 433.92 MHz, FSK		13.1		mA
		+13 dBm, 433.92 MHz, FSK		15.3		mA
	$I_{DD-D-868.35}$	0 dBm, 868.35 MHz, FSK		6.5		mA
		+10 dBm, 868.35 MHz, FSK		14.3		mA
		+13 dBm, 868.35 MHz, FSK		16.7		mA
Sleep Current	I_{SLEEP}			2.5		uA
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise @433.92 MHz	$PN_{433.92}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Phase Noise @868.35 MHz	$PN_{868.35}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RFI}		-107		dBc/Hz
Harmonics Output for 315 MHz[4]	$H2_{315}$	2^{nd} harm @ 630 MHz, +13 dBm P_{OUT}		-60		dBm
	$H3_{315}$	3^{rd} harm @ 945 MHz, +13 dBm P_{OUT}		-65		dBm
Harmonics Output for 433.92 MHz[4]	$H2_{433.92}$	2^{nd} harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	$H3_{433.92}$	3^{rd} harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
OOK Extinction Ration				60		dB

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. Measured with single-ended PA output, and it is not applicable for when the device is configured as differential PA output.

[3]. 0 and 2^n us, n = 0 to 10, when set to "0", the PA output power will ramp to its configured value in the shortest possible time.

[4]. The harmonics output is measured with the application shown as Figure 11.

1.4 Crystal Oscillator

Table 6. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency[1]	F_{XTAL}		26	26	26	MHz
Crystal Tolerance[2]				±20		ppm
Load Capacitance[3]	C_{LOAD}		12		20	pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[4]	t_{XTAL}			400		us

Notes:

[1]. The CMT2189A can directly work with external 26 MHz reference clock input to XTAL pin (a coupling capacitor is required) with amplitude 0.3 to 0.7 Vpp.

[2]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[3]. The required crystal load capacitance is integrated on-chip to minimize the number of external components.

[4]. This parameter is to a large degree crystal dependent.

2. Pin Descriptions

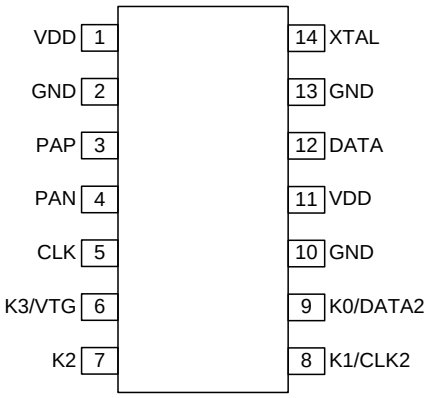


Figure 3. CMT2189A Pin Assignments

Table 7. CMT2189A Pin Descriptions

Pin Number	Name	I/O	Descriptions
1	VDD	I	Power supply input
2	GND	I	Ground
3	PAP	O	The differential power amplifier output, when using as singled-ended output, PAN/PAP should be connected together before connecting to the matching network
4	PAN	O	
5	CLK	I	Clock1 for the chip programming, internally pulled up to VDD
6	K3/VTG	I	Push button key 3 or voltage for the chip programming
7	K2	I	Push button key 2
8	K1/CLK2	I	Push button key 1 or clock2 for the chip programming
9	K0/DATA2	IO	Push button key 0 or data2 for the chip programming
10	GND	I	Ground
11	VDD	I	Power supply input
12	DATA	IO	Data1 for the chip programming, internally pulled up to GND
13	GND	I	Ground
14	XTAL	I	26 MHz single-ended crystal oscillator input or external 26 MHz reference clock input

3. Typical Performance Characteristics

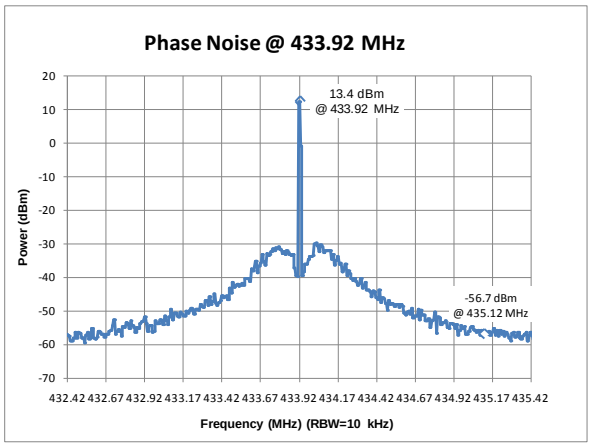


Figure 4. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Unmodulated

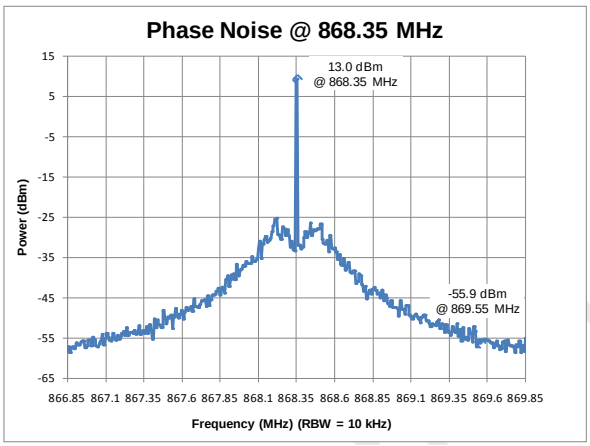


Figure 5. Phase Noise, F_{RF} = 868.35 MHz, P_{OUT} = +13 dBm, Unmodulated

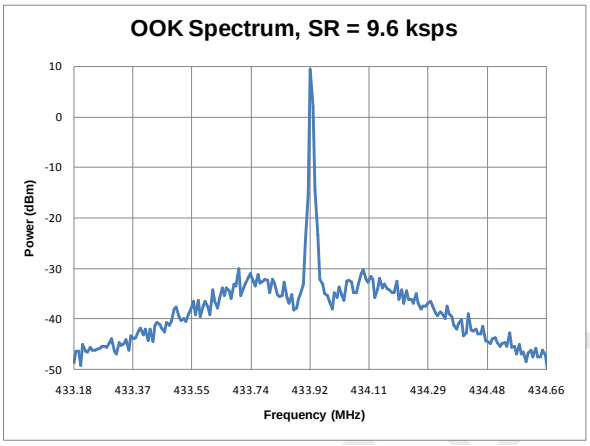


Figure 6. OOK Spectrum, SR = 9.6 ksps, P_{OUT} = +10 dBm, t_{RAMP} = 32 us

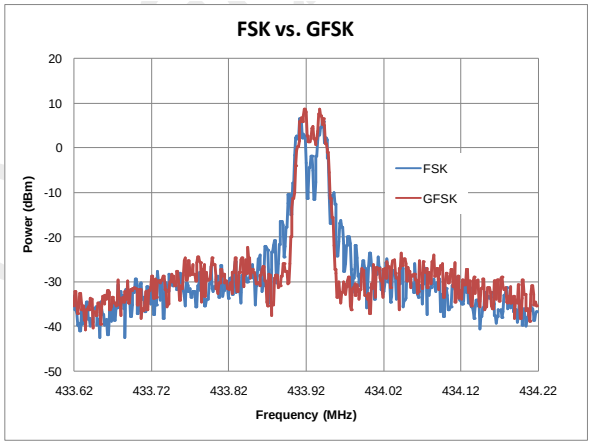


Figure 7. FSK/GFSK Spectrum, SR = 9.6 ksps, F_{DEV} = 15 kHz

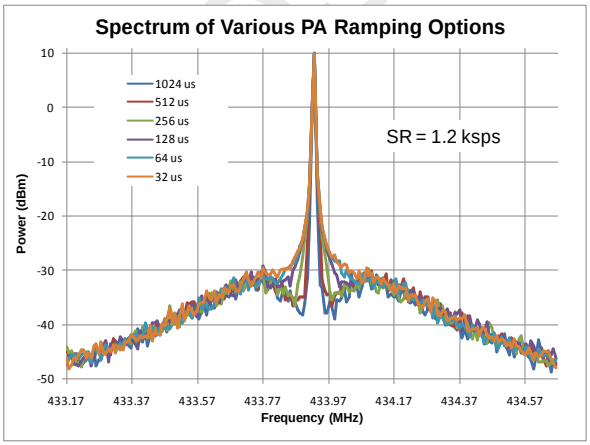


Figure 8. Spectrum of PA Ramping, SR = 1.2 ksps, P_{OUT} = +10 dBm

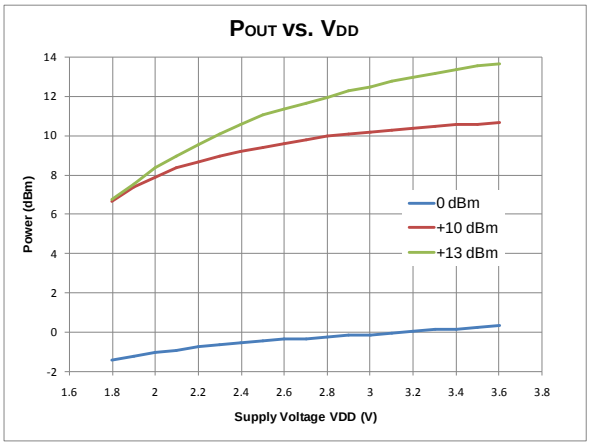


Figure 9. Output Power vs. Supply Voltages, F_{RF} = 433.92 MHz

4. Typical Application Schematics

4.1 Typical Application with Differential PA Output

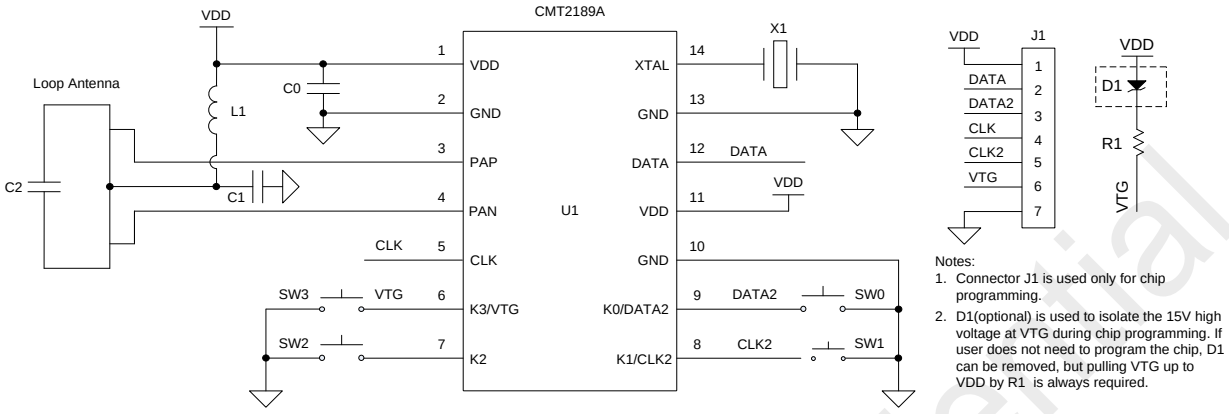


Figure 10. CMT2189A Typical Application with Differential PA Output

Notes:

1. Connector J1 is a must for the CMT2189A chip programming during development or manufacture.
2. D1 is an optional protection device for the chip programming. It is not needed during the normal operation.
3. The general layout guidelines are listed below. For more design details, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2189A as possible for better filtering.
4. The table below shows the BOM of 868.35 Application with Differential PA Output. For the BOM of other applications, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.

Table 8. BOM of 868.35 MHz Application with Differential PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189A, 240 – 960 MHz SoC (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
C2	±0.25 pF, 0402 NP0, 50 V	1.5	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	100	nH	Murata LQG18

4.2 Typical Application with Single-ended PA Output

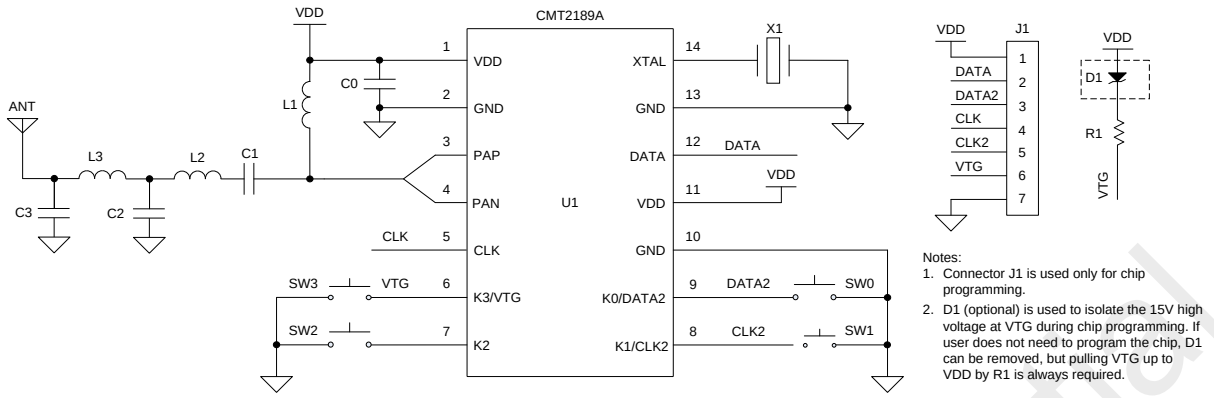


Figure 11. CMT2189A Typical Application with Single-ended PA Output

Notes:

1. Connector J1 is a must for the CMT2189A EEPROM access during development or manufacture.
2. D1 is an optional protection device for the chip programming. It is not needed during the normal operation.
3. The general layout guidelines are listed below. For more design details, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2189A as possible for better filtering.
4. The table below shows the BOM of 868.35 Application with single-ended PA output. For the BOM of other applications, please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.

Table 9. BOM of 868.35 MHz FCC/ETSI Compliant Application

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189A, 240 – 960 MHz SoC (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	9.1	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	8.2	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	100	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	8.2	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	8.2	nH	Murata LQG18

5. Functional Descriptions

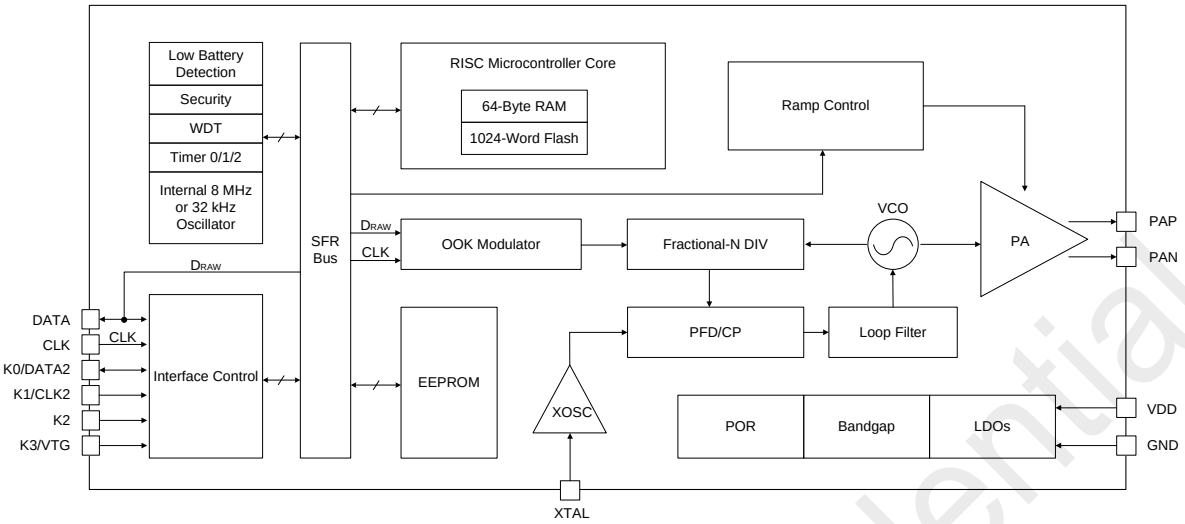


Figure 12. CMT2189A Functional Block Diagram

5.1 Overview

The CMT2189A devices are fully integrated, highly flexible, high performance, SoC (G)FSK/OOK transmitters with embedded RISC microcontroller core for various 240 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF^{TM} family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the CMT2189A is shown in the figure above. The CMT2189A is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the reference voltage generated by Bandgap. The calibration can help the chip to finely work under different temperatures and supply voltages. The CMT2189A has a highly efficient PA built in, the PA can be configured as single-ended or differential outputs, and the output power can be configured from -10 to +13 dBm in 1 dB step size. The RISC microcontroller core provides the core functionality of the CMT2189A. A 1024-word of flash area is available to store the user program of the applications. Up to 4 push buttons are supported with their function customized by the user program. RF Frequency, PA output power, other product features and unique transmit IDs can be programmed into the embedded EEPROM by the RFPDK and USB Programmer. This saves the cost and simplifies the product development and manufacturing effort. Alternatively, in stock products of 868.35 MHz is available for immediate demands. The CMT2189A operates from 2.3 to 3.6 V, only consumes 21.3 mA when transmitting +10 dBm power under 3.3 V supply voltage(868.35 MHz, FSK, single-ended PA output). The device together with CMOSTEK NextGenRF^{TM} receiver enables a highly flexible, low cost RF link.

5.2 Modulation, Frequency, Deviation and Symbol Rate

The CMT2189A supports OOK modulation with the symbol rate up to 30 ksps, as well as the (G)FSK modulation with the symbol rate up to 100 ksps. The supported deviation frequency is from 1 kHz to 200 kHz. The CMT2189A continuously covers the frequency range from 240 to 960 MHz, including the license free ISM frequency band around 315 MHz 433.92 MHz, 868.35 MHz and 915 MHz. The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz when the RF frequency is lower than 480 MHz, and is 397 Hz when the RF frequency is higher than 480 MHz. See the table below for the modulation, frequency, Deviation and symbol rate specifications.

Table 10. Modulation, Frequency, Deviation and Symbol Rate

Parameter	Value	Unit
Modulation	(G)FSK/OOK	-
Frequency	240 to 960	MHz
Deviation	1 to 200	kHz
Frequency Resolution (F_{RF} ≤ 480 MHz)	<198	Hz
Frequency Resolution (F_{RF} > 480 MHz)	397	Hz
(G)FSK Symbol Rate	0.5 to 100	ksps
OOK Symbol Rate	0.5 to 30	ksps

5.3 Embedded EEPROM and RFPDK

The RFPDK (RF Products Development Kit) is a very user-friendly software tool delivered for the user configuring the CMT2189A in the most intuitional way. The user only needs to fill in/select the proper value of each parameter and click the "Burn" button to complete the chip configuration. No register access and control is required in the application program. See the figure below for the accessing of the EEPROM and Table 11 for the summary of all the configurable parameters of the CMT2189A in the RFPDK.

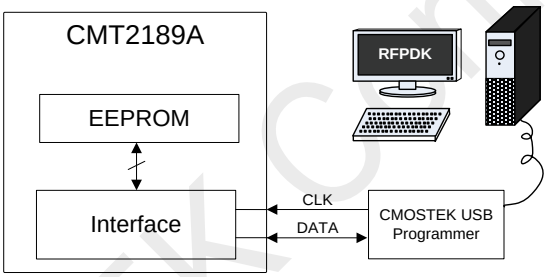


Figure 13. Accessing Embedded EEPROM

For the detail of CMT2189A configurations with the RFPDK, please refer to "AN132 CMT2180/89A Configuration Guideline".

Table 11. Configurable Parameters in RFPDK

Category	Parameters	Descriptions	Default	Mode
RF Settings	Frequency	To input a desired transmitting radio frequency in the range from 240 to 480 MHz. The step size is 0.001 MHz.	868.35 MHz	Basic Advanced
	Modulation	The option is FSK or GFSK and OOK.	FSK	Basic Advanced
	Deviation	The FSK frequency deviation. The range is from 1 to 100 kHz.	35 kHz	Basic Advanced
	Symbol Rate	The GFSK symbol rate. The user does not need to specify symbol rate for FSK and OOK modulation.	2.4 ksps	Basic Advanced
	Tx Power	To select a proper transmitting output power from -10 dBm to +14 dBm, 1 dB margin is given above +13 dBm.	+13 dBm	Basic Advanced

Category	Parameters	Descriptions	Default	Mode
	Xtal Load	On-chip XOSC load capacitance options: from 10 to 22 pF. The step size is 0.33 pF.	15.00 pF	Basic Advanced
	Data Representation	To select whether the frequency “Fo + Fdev” represent data 0 or 1. The options are: 0: F-high 1: F-low, or 0: F-low 1: F-high.	0: F-low 1: F-high	Advanced
	PA Ramping	To control PA output power ramp up/down time, options are 0 and 2^n us (n from 0 to 10).	0 us	Advanced
	PA Output	To select the PA output mode, the option is Single-ended or Differential.	Differential	Basic Advanced
Transmitting Settings	Start by	Start condition of a transmitting cycle, by Data Pin Rising/Falling Edge.	Data Pin Rising Edge	Advanced
	Stop by	Stop condition of a transmitting cycle, by Data Pin Holding Low for 2 to 90 ms.	Data Pin Holding Low for 20 ms	Advanced
Flash SN Settings	Start Addr (Hex)	Defines the starting address of a consecutive address space in the Flash to store the series number.	0008	Basic Advanced
	End Addr (Hex)	Defines the ending address to store the series number to the Flash.	000A	Basic Advanced
	Init SN	Defines the initial SN value (in Dec), this value will be stored in the Flash with address defined from Start Addr (Hex) to End Addr (Hex).	1193046	Basic Advanced
	Step Size	Defines the incremental step size of the SN value, it can be a positive integer or zero.	1	Basic Advanced
	Current SN	Displays the next SN value to be burned into the device in the next burning operation.	1193046	Basic Advanced
Feature Bits	Clock Source	To select the internal clock source for the microcontroller, the options are: Blank, 8 MHz and 32 kHz.	8 MHz	Basic Advanced
	WDT	To enable or disable the watchdog timer, the options are Blank, Enable or Disable.	Disable	Basic Advanced
	K3/MCLR	To configure the K3 pin as Master Clear (MCLR) or push button key.	K3	Basic Advanced
	LBD	Defines the battery low threshold, the options are: Blank, Disable and Typ 2.3V.	Typ 2.3V	Basic Advanced
	Security	To enable or disable the code protection. When it is enabled, the readouts of bit11-7, bit4-0 in each word are fixed at 1. The options are Disable or Enable.	Enable	Basic Advanced
ID Memory Settings	-	This is a 12 x 7-bit ID area in the microcontroller section that allows the user to store any data.	-	Basic Advanced

5.4 Power Amplifier

A highly efficient Power Amplifier (PA) is integrated in the CMT2189A to transmit the modulated signal out. Depending on the application, the PA can be configured as single-ended or differential output on the RFPDK, and the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or

monopole antenna. Typical application schematics and the required BOM are shown in “Chapter 4 Typical Application Schematic”. For the schematic, layout guideline and the other detailed information please refer to “AN131 CMT218xA Schematic and PCB Layout Design Guideline”.

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the CMOSTEK USB Programmer and the RFPDK.

5.5 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The CMT2189A has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 14. When the option is set to “0”, the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

CMOSTEK recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping “rate”, as shown in the formula below.

$$SR_{Max} \le 0.5 * (\frac{1}{t_{RAMP}})$$

In which the PA ramping “rate” is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by formula below.

$$t_{RAMP} \le 0.5 * (\frac{1}{SR_{MAX}})$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than “0.5 * ($1/SR_{Max}$)”, it will possibly bring additional challenges to the OOK demodulation of the Rx device. For more detail of calculating t_{RAMP}, please refer to “AN132 CMT2180/89A Configuration Guideline”.

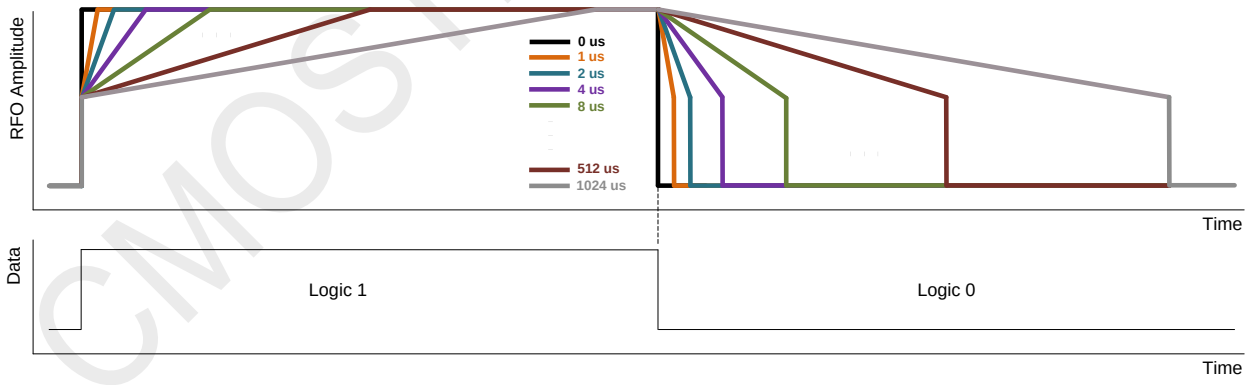


Figure 14. PA Ramping Time

5.6 Crystal Oscillator and RCLK

The CMT2189A uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 16 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is 26 MHz with ±20 ppm, ESR (Rm) < 60 Ω, load capacitance C_{LOAD} ranging from 12 to 20 pF. To save the external load capacitors, a set

of variable load capacitors C_L is built inside the CMT2189A to support the oscillation of the crystal.

The value of load capacitors is configurable with the CMOSTEK USB Programmer and RFPDK. To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO frequency.

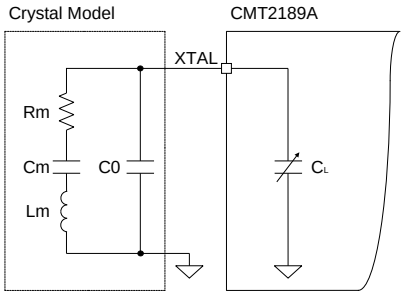


Figure 16. XTAL Circuitry and Crystal Model

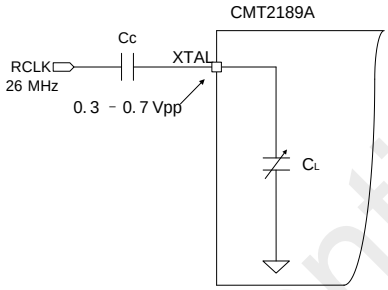


Figure 15. RCLK Circuitry

If a 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2189A by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 15 for the RCLK circuitry.

6. Working States and Control Interface

6.1 Working States

The CMT2189A has following 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the CMT2189A is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized. The 4 push buttons keys are ready to sense valid pressing actions to start a transmitting cycle.

XO-STARTUP

Once the modulator of the CMT2189A detect valid signal on the D_{RAW} wire (see Figure 12), the RF section will go into the XO-STARTUP state, and the internal XO starts to work. The user has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in the Table 12.

TUNE

The frequency synthesizer will tune the CMT2189A to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the data only after the TUNE state is done, before that the data will not be transmitted. See Figure 17 for the details.

TRANSMIT

The CMT2189A starts to modulate and transmit the data (D_{RAW}) generated by the microcontroller core responding to the push buttons. The transmission can be ended in 2 methods: firstly, driving the DATA pin low for t_{STOP} time, where the t_{STOP} can be configured from 20 to 90 ms on the RFPDK; secondly, issuing SOFT_RST command over the two-wire interface, this will stop the transmission in 1 ms. See section 6.2.3 for details of the two-wire interface.

Table 12.Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop The Transmission[2]	t_{STOP}	2		90	ms

Notes:

[1]. This parameter is to a large degree crystal dependent.

[2]. Configurable from 2 to 9 in 1 ms step size and 20 to 90 ms in 10 ms step size.

6.2 Transmission Control Interface

The CMT2189A uses the D_{RAW} wire for the microcontroller core to send in data for modulation and transmission. The D_{RAW} wire, which also connects to the DATA pin, can be used as pin for EEPROM programming, data transmission, as well as controlling the transmission. The transmission can be started by detecting rising or falling edge on the D_{RAW} wire (DATA Pin), and stopped by driving the D_{RAW} wire low for t_{STOP} as shown in the table above. Besides communicating over the D_{RAW} wire, the microcontroller core can also communicate with the RF section over the two-wire interface, so that the transmission is more robust, and consumes less current.

6.2.1 Tx Enabled by DATA Pin Rising Edge

As shown in the figure below, once the CMT2189A detects a rising edge on the D_{RAW} wire (DATA pin), it goes into the XO-STARTUP state. The user has to pull the D_{RAW} wire high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as

wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the D_{RAW} wire. The logic state of the D_{RAW} wire is “Don't Care” from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the D_{RAW} wire low for t_{STOP} in order to end the transmission.

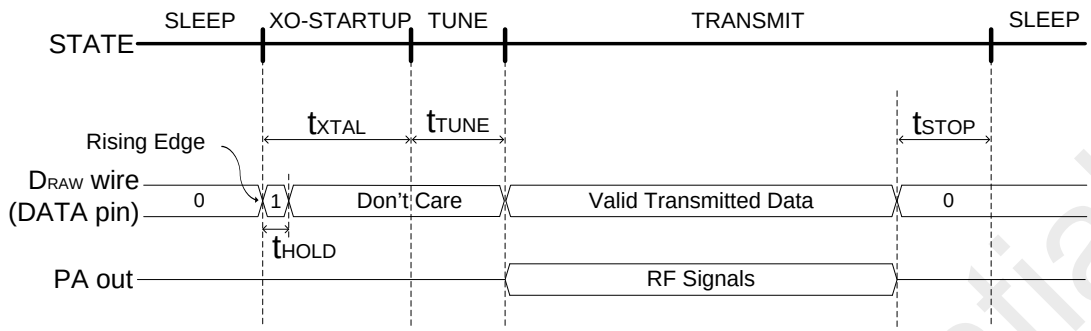


Figure 17. Transmission Enabled by DATA Pin Rising Edge

6.2.2 Two-wire Interface

For power-saving and reliable transmission purposes, the CMT21810A is recommended to communicate with the microcontroller core over a two-wire interface (TWI): D_{RAW} (DATA) and CLK. The TWI is designed to operate at a maximum of 1 MHz. The timing requirement and data transmission control through the TWI are shown in this section.

Table 13. TWI Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	V_{IH}		0.8			V_{DD}
Digital Input Level Low	V_{IL}				0.2	V_{DD}
CLK Frequency	F_{CLK}		10		1,000	kHz
CLK High Time	t_{CH}		500			ns
CLK Low Time	t_{CL}		500			ns
CLK Delay Time	t_{CD}	CLK delay time for the first falling edge of the TWI_RST command, see Figure 21	20		15,000	ns
DATA Delay Time	t_{DD}	The data delay time from the last CLK rising edge of the TWI command to the time DATA return to default state			15,000	ns
DATA Setup Time	t_{DS}	From DATA change to CLK falling edge	20			ns
DATA Hold Time	t_{DH}	From CLK falling edge to DATA change	200			ns

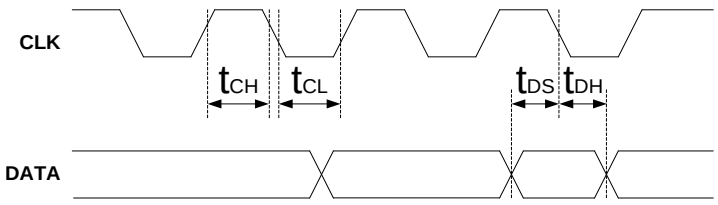


Figure 18. Two-wire Interface Timing Diagram

Once the device is powered up, TWI_RST and SOFT_RST should be issued to make sure the device works in SLEEP state robustly. On every transmission, TWI_RST and TWI_OFF should be issued before the transmission to make sure the TWI

circuit functions correctly. TWI_RST and SOFT_RST should be issued again after the transmission for the device going back to SLEEP state reliably till the next transmission. The operation flow with TWI is shown as the figure below.

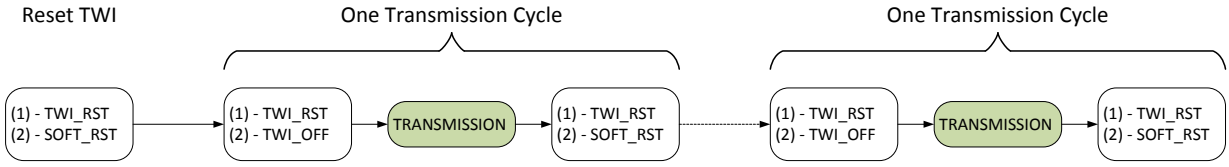


Figure 19. CMT21819A Operation Flow with TWI

Table 14. TWI Commands Descriptions

Command	Descriptions
TWI_RST	Implemented by pulling the DATA pin low for 32 clock cycles and clocking in 0x8D00, 48 clock cycles in total. It only resets the TWI circuit to make sure it functions correctly. The DATA pin cannot detect the Rising/Falling edge to trigger transmission after this command, until the TWI_OFF command is issued. **Note:** a) Please ensure the DATA pin is firmly pulled low during the first 32 clock cycles.
TWI_OFF	Implemented by clocking in 0x8D02, 16 clock cycles in total. It turns off the TWI circuit, and the DATA pin is able to detect the Rising/Falling edge to trigger transmission after this command, till the TWI_RST command is issued. The command is shown as Figure 23.
SOFT_RST	Implemented by clocking in 0xBD01, 16 clock cycles in total. It resets all the other circuits of the chip except the TWI circuit. This command will trigger internal calibration for getting the optimal device performance. After issuing the SOFT_RST command, the host MCU should wait 1 ms before sending in any new command. After that, the device goes to SLEEP state. The command is shown as Figure 24.

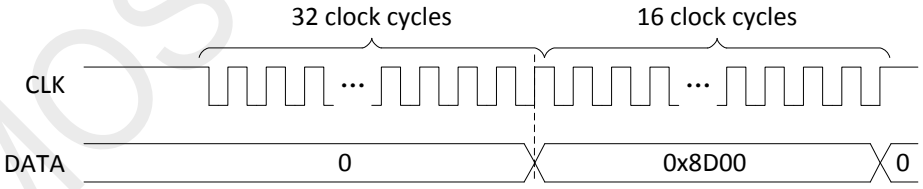


Figure 20. TWI_RST Command

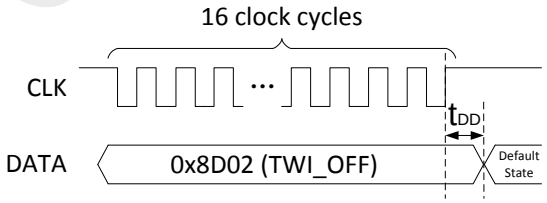


Figure 21. TWI_OFF Command

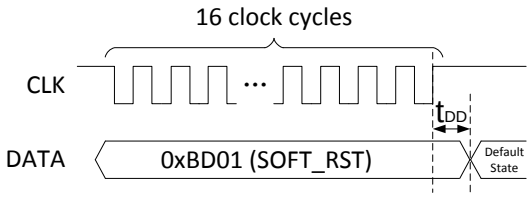


Figure 22. SOFT_RST Command

The DATA is generated by the host MCU on the rising edge of CLK, and is sampled by the device on the falling edge. The CLK should be pulled up by the host MCU during the TRANSMISSION shown in Figure 20. The TRANSMISSION process should refer to Figure 17 or Figure 18 for its timing requirement, depending on the “Start By” setting configured on the RFPDK.

The device will go to SLEEP state by driving the DATA low for t_{STOP}, or issuing SOFT_RST command. A helpful practice for the device to go to SLEEP is to issue TWI_RST and SOFT_RST commands right after the useful data is transmitted, instead of waiting the t_{STOP}, this can save power significantly.

7. RISC Microcontroller Core

The embedded MCU core is a high performance RISC Microcontroller. It includes the following features.

High-Performance RISC CPU:

- 1024 words Flash, 64 bytes SRAM
- Only 37 Instructions to Learn
- All single-cycle instructions except branches
- Operating Speed:
  - DC - 8MHz oscillator
  - DC - 250 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Direct, Indirect, and Relative Addressing modes

Special Microcontroller Features:

- Internal 8 MHz oscillator
- Power-Saving Sleep mode
- Industrial and Extended Temperature Range
- Watchdog timer with on-chip RC oscillator
- Power-on Reset (POR)
- Multiplexed MCLR/Input Pin
- Interrupt-on-Pin Change
- Individual Programmable Weak Pull-ups

Peripheral Features:

- 4 I/O Pins with Individual Direction Control
- Timer0 : 8-bit timer with 3-bit prescaler
- Timer1 : 16-bit timer with 2-bit prescaler
- Timer2 : 8-bit timer with 3-bit prescaler and
- K0~3 port with pull-up resister
- K0~3 port with open drain function
- K0~2 port with pull-down resister
- Internal RC clock select at 8 MHz to 32 kHz
- Five interrupt sources:
  - Three internal interrupts: TM0, TM1, TM2
  - Two external interrupts K1 or K0~3 pin change
- One level buffer PUSH status (without /TF, /PF), and
- W data if interrupt executes, then POP data after RTFI instruction

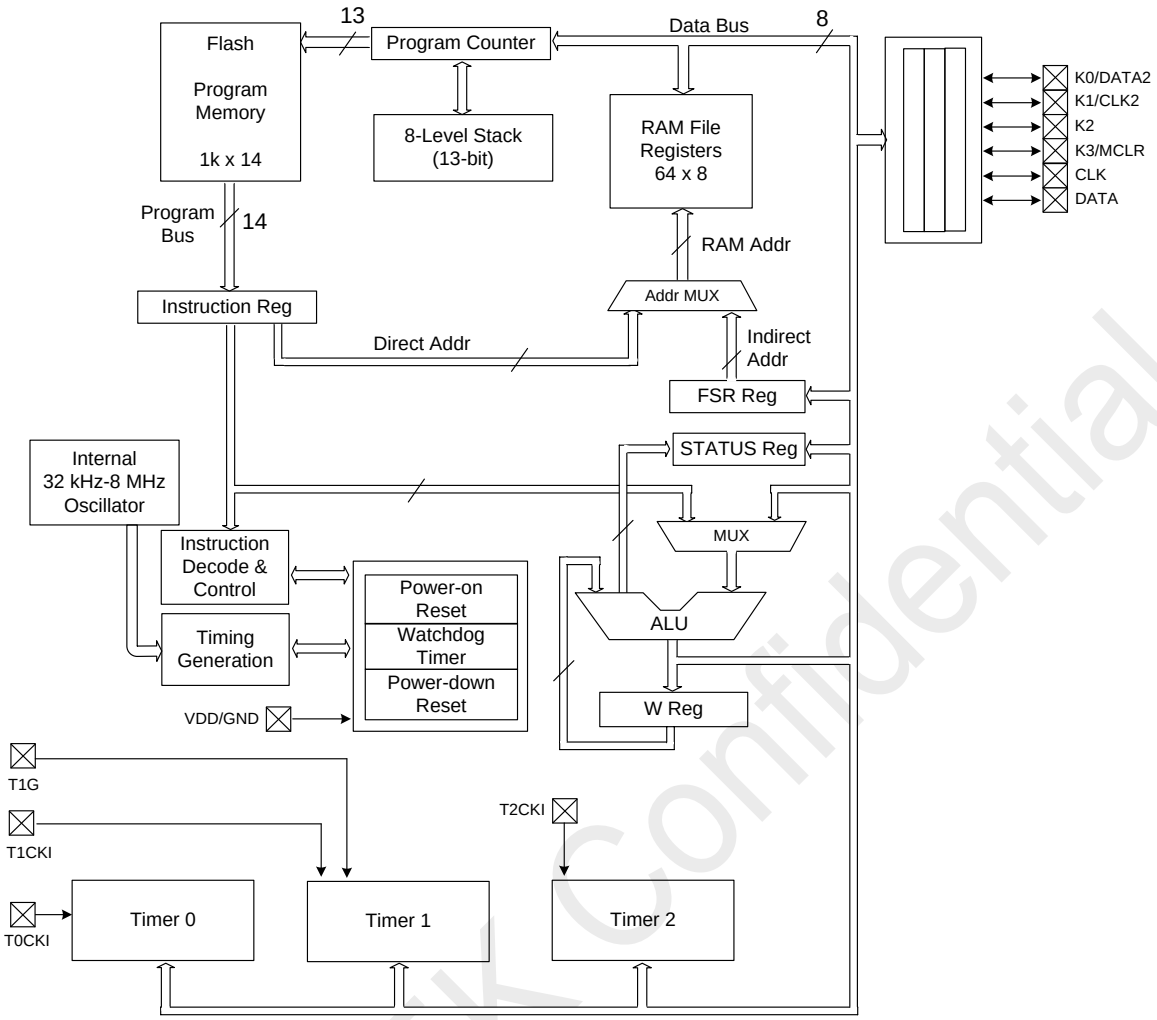


Figure 23. Microcontroller Core Block Diagram

7.1 Memory Organization

7.1.1 Program Memory Organization

The CMT2189A device has 1k x 14 (0000h-03FFh) for program memory. Accessing a location above these boundaries will cause a wrap-around within the first 1k x 14 space. The Reset Vector is at 0000h and the Interrupt Vector is at 0004h (see figure below).

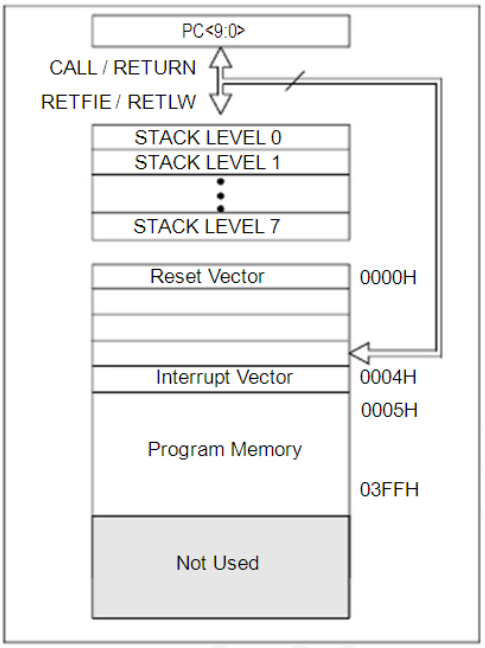


Figure 24. Program Memory Map and Stack

7.1.2 Data Memory Organization

The data memory (see Figure 27) is partitioned into two banks: the General Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when being read. PAGE0 (STATUS<5>) is the bank select bit.

•PAGE0 = 0 Bank 0 is selected.
•PAGE0 = 1 Bank 1 is selected.

7.1.2.1 General Purpose Register File

The register file is organized as 64 x 8 in the CMT2189A. Each register is accessed, either directly or indirectly, through the Memory Select Register (MSR see Section 7.1.4 "Indirect Addressing, IAR and MSR Registers").

7.1.2.2 Special Function Register File

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 15). These registers are static RAM. The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

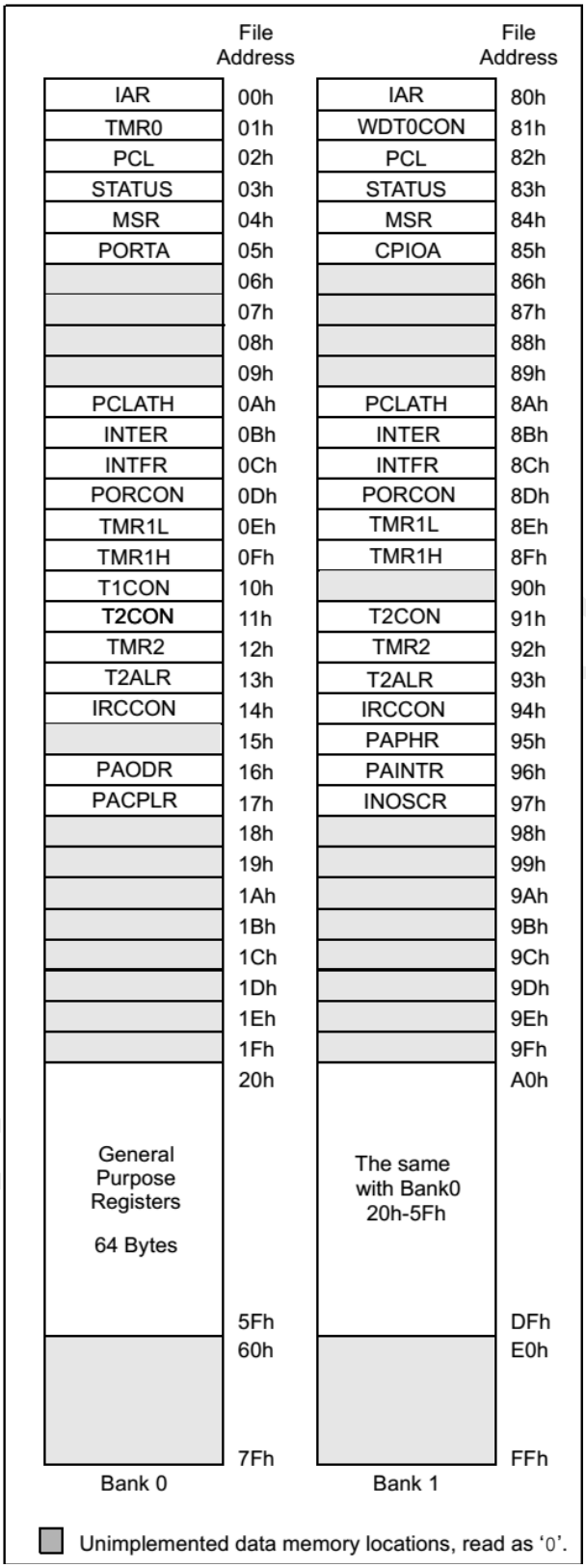


Figure 25. Data Memory Map of the CMT2189A

Table 15. CMT2189A Special Registers Summary Bank0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, PDR
Bank0										
00h	IAR	Addressing this location uses contents of MSR to address data memory (not a physical register)								xxxx xxxx
01h	TMR0	Timer0 Module's Register								xxxx xxxx
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
03h	STATUS	--	--	PAGE0	/TF	/PF	Z	DC	C	0001 1xxx
04h	MSR	Indirect data memory Address Pointer								xxxx xxxx
05h	PORT A	--	--	I/O Control Registers						----xx xxxx
06h	--	Unimplemented								
07h	--	Unimplemented								
08h	--	Unimplemented								
09h	--	Unimplemented								
0Ah	PCLATH	--	--	--	Write buffer for upper 5 bits of program counter					------0 0000
0Bh	INTER	GIE	--	--	INTE	PAIE	T2IE	T1IE	T0IE	0000 0000
0Ch	INTFR	--	--	--	INTF	PAIF	T2IF	T1IF	T0IF	0000 0000
0Dh	PORCON	3Fx2F	SWDTEN	--	ENPOP	3Fx2EN	LOST	PORB	PEDHB	0001 00qq
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON	0000 0000
11h	T2CON	T2ON	T2RATE2	T2RATE1	T2RATE0	T2ECKS	ALOAD	T2OUT	PWMOUT	0000 0000
12h	TMR2	Timer2 Module's Register								0000 0000
13h	T2ALR	Timer2 auto-load register								0000 0000
14h	IRCCON	IFDIV3	IFDIV2	IFDIV1	IFDIV0	T2OCK	/GMF	CHWCK	GREMD	1110 0100
15h	--	Unimplemented								
16h	PAODR	--	--	APOD5	APOD4	--	APOD2	APOD1	APOD0	0000 0000
17h	PACPLR	--	--	--	--	--	APLB2	APLB1	APLB0	0000 0000
18h	--	Unimplemented								
19h	--	Unimplemented								
1Ah	--	Unimplemented								
1Bh	--	Unimplemented								
1Ch	--	Unimplemented								
1Dh	--	Unimplemented								
1Eh	--	Unimplemented								
1Fh	--	Unimplemented								

Note:

[1]. Legend: – = Unimplemented locations, u= unchanged, x= unknown, q= value depends on condition

Table 16. CMT2189A Special Function Registers Summary Bank1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, PDR
Bank1										
80h	IAR	Addressing this location uses contents of MSR to address data memory (not a physical register)								xxxx xxxx
81h	WDT0CON	--	IES	TCS	TCE	PSC	PS2	PS1	PS0	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000
83h	STATUS	--	--	PAGE0	/TF	/PF	Z	DC	C	0001 1xxx
84h	MSR	Indirect data memory Address Pointer								xxxx xxxx
85h	CPIO A	--	--	CPIO PA5	CPIO PA4	CPIO PA3	CPIO PA2	CPIO PA1	CPIO PA0	---11 1111
86h	--	Unimplemented								
87h	--	Unimplemented								
88h	--	Unimplemented								
89h	--	Unimplemented								
8Ah	PCLATH	--	--	--	Write buffer for upper 5 bits of program counter					----0 0000
8Bh	INTER	GIE	--	--	INTE	PAIE	T2IE	T1IE	T0IE	0000 0000
8Ch	INTFR	--	--	--	INTF	PAIF	T2IF	T1IF	T0IF	0000 0000
8Dh	PORCON	3Fx2F	SWDTEN	--	ENPOP	3Fx2EN	LOST	PORB	PEDHB	0001 00qq
8Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx
8Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx
90h	--	Unimplemented								0000 0000
91h	T2CON	T2ON	T2RATE2	T2RATE1	T2RATE0	T2ECKS	ALOAD	T2OUT	PWMOUT	0000 0000
92h	TMR2	Timer2 Module's Register								0000 0000
93h	T2ALR	Timer2 auto-load register								0000 0000
94h	IRCCON	IFDIV3	IFDIV2	IFDIV1	IFDIV0	T2OCK	/GMF	CHWCK	GREMD	1110 0100
95h	PAPHR	--	--	APHB 5	APHB 4	APHB 3	APHB 2	APHB 1	APHB 0	0000 0000
96h	PAINTR	--	--	PINT A5	PINT A4	PINT A3	PINT A2	PINT A1	PINT A0	0000 0000
97h	INOSCR	SYCKF	--	IRCLVC	MK0	ECKIN	OSO2E	OSO2O	/OSCIN	1010 0000
98h	--	Unimplemented								
99h	--	Unimplemented								
9Ah	--	Unimplemented								
9Bh	--	Unimplemented								
9Ch	--	Unimplemented								
9Dh	--	Unimplemented								
9Eh	--	Unimplemented								
9Fh	--	Unimplemented								

Note:

[1]. Legend: – = Unimplemented locations, u= unchanged, x= unknown, q= value depends on condition.

7.1.2.2.1 W Register

When any interrupt occurs, system will jump to Interrupt Vector (Address: 0x0004) and execute interrupt service routine. It is necessary to save **W, STATUS** data. If PORCON (0DH bit 4) ENPOP = "1" is enable chip can save **W, STATUS** data into buffers, after "RTFI " instructions pop buffer data to **W, STATUS** register data.

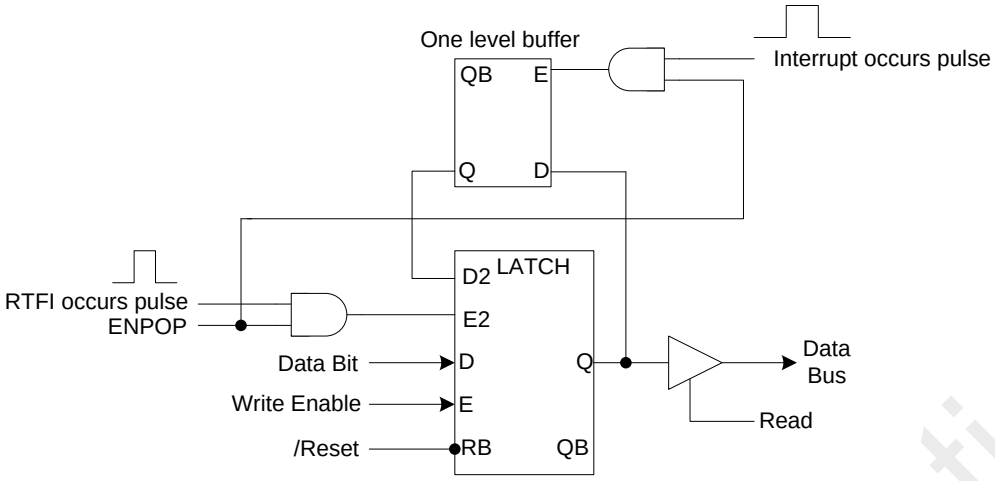


Figure 26. W Register

7.1.2.2.2 STATUS Register

The STATUS register, shown in Register 1, contains the below sections.

- The arithmetic status of the ALU
- The Reset status
- The bank selects bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended. For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u= unchanged).

Register 1. STATUS – STATUS Register (Address: 03h or 83h)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
		PAGE0	/TF	/PF	Z	DC	C
bit7							bit0

bit 5	**PAGE0**: Register Bank Select bit (used for direct addressing). 1 = Bank 1 (80h-FFh). 0 = Bank 0 (00h-7Fh).
bit 4	**/TF:** WDT time-out flag bit. 1 = After power-up, CLRWT instruction, or SLEEP instruction. 0 = A WDT time-out occurred.
bit 3	**/PF:** Power-Down flag bit. 1 = After power-up or by the CLRWT instruction. 0 = By execution of the SLEEP instruction.
bit 2	**Z:** Zero bit. 1 = The result of an arithmetic or logic operation is zero. 0 = The result of an arithmetic or logic operation is not zero.

bit 1	**DC:** Digit carry/borrow bit (ADDWR, ADDWI, SUBWI, SUBWR instructions) For borrow, the polarity is reversed. 1 = A carry-out from the 4th low order bit of the result occurred. 0 = No carry-out from the 4th low order bit of the result.
bit 0	**C:** Carry/borrow bit (ADDWR, ADDWI, SUBWI, SUBWR instructions). 1 = A carry-out from the Most Significant bit of the result occurred. 0 = No carry-out from the Most Significant bit of the result occurred.
Notes: [1]. For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register. [2]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.1.2.2.3 WDT0CON Register

The WDT0CON register is a readable and writable register, which contains various control bits to configure:

• TMR0/WDT prescaler
• External RA2/INT interrupts
•TMR0

Register 2. WDT0CON Register (Address: 81h)

Reserved	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	IES	TCS	TCE	PSC	PS2	PS1	PS0
bit7							bit0

bit 6	**IES:** Interrupt Edge Select bit. 1 = Interrupt on rising edge of PA0/INT pin. 0 = Interrupt on falling edge of PA0/INT pin.
bit 5	**TCS:** TMR0 Clock Source Select bit. 1 = Transition on PA1/T0CKI pin. 0 = Internal instruction cycle clock.
bit 4	**TCE:** TMR0 Source Edge Select bit. 1 = Increment on high-to-low transition on RA1/T0CKI pin. 0 = Increment on low-to-high transition on RA1/T0CKI pin.
bit 3	**PSC:** Prescaler Assignment bit. 1 = Prescaler is assigned to the WDT. 0 = Prescaler is assigned to the Timer0 module.
bit 2 - 0	**PS2-PS0:** Prescaler Rate Select bits.

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8

	100 1:32 1:16 101 1:64 1:32 110 1:128 1:64 111 1:256 1:128
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.1.2.2.4 INTER Register

The INTER register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA0/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTER <7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

Register 3. INTER – Interrupt Control Register (Address: 0Bh or 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE			INTE	PAIE	T2IE	T1IE	T0IE
bit7							bit0

bit 7	**GIE:** Global Interrupt Enable bit. 1 = Enables all unmasked interrupts. 0 = Disables all interrupts.
bit 5	**T0IE:** TMR0 Overflow Interrupt Enable bit. 1 = Enables the TMR0 interrupt. 0 = Disables the TMR0 interrupt.
bit 4	**INTE:** RA0/INT External Interrupt Enable bit. 1 = Enables the RA0/INT external interrupt. 0 = Disables the RA0/INT external interrupt.
bit 3	**PAIE:** Port Change Interrupt Enable bit 1. 1 = Enables the PORTA change interrupt. 0 = Disables the PORTA change interrupt.
bit 2	**T2IE:** TMR2 Overflow Interrupt Enable bit. 1 = Enables the TMR2 interrupt. 0 = Disables the TMR2 interrupt.
bit 1	**T1IE:** TMR1 Overflow Interrupt Enable bit. 1 = Enables the TMR1 interrupt. 0 = Disables the TMR1 interrupt.
bit 0	**T0IE:** TMR0 Overflow Interrupt Enable bit. 1 = Enables the TMR0 interrupt. 0 = Disables the TMR0 interrupt.
Notes: [1]. IOCA register must also be enabled. [2]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.1.2.2.5 INTFR Register

The INTFR register contains the interrupt flag bits, as shown in Register 4.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTER <7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

Register 4. INTFR – Peripheral Interrupt Flags (Address: 0Ch or 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INTF	PAIF	T2IF	T1IF	T0IF
bit7							bit0

bit 4	**INTF:** PA0/INT External Interrupt Flag bit. 1 = The PA0/INT external interrupt occurred (must be cleared in software). 0 = The PA0/INT external interrupt did not occur.
bit 3	**PAIF:** Port Change Interrupt Flag bit. 1 = When at least one of the PORTA <5:0> pins changed state (must be cleared in software). 0 = None of the PORTA <5:0> pins have changed state.
bit 2	**T2IF:** TMR2 Overflow Interrupt Flag bit. 1 = TMR2 register overflowed (must be cleared in software). 0 = TMR2 register did not overflow.
bit 1	**T1IF:** TMR1 Overflow Interrupt Flag bit. 1 = TMR1 register overflowed (must be cleared in software). 0 = TMR1 register did not overflow.
bit 0	**T0IF:** TMR0 Overflow Interrupt Flag bit. 1 = TMR0 register overflowed (must be cleared in software). 0 = TMR0 register did not overflow.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.1.2.2.6 PORCON Register

The Power Control (PORCON) Register bits are shown in Register 5.

Register 5. PORCON – Power Control Register (Address: 0Eh or 8Eh)

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-x	R/W-x
3Fx2F	SWDTEN	—	ENPOP	3Fx2EN	LOST	PORB	LBDHB
bit7							bit0

bit 7	**3Fx2F:** ROM code run 3FFF instruction twice reset flag bit. 0 = None 3FFF x 2 reset occurred. 1 = The 3FFF x 2 reset occurred.
bit 6	**SWDTEN:** Software WDT enable bit. (When device option WDT select disable). 0 = Disable software WDT.

	1 = Enable software WDT. (If device option WDT select enable, irrespective of the SWDTEN bit).
bit 4	**ENPOP:** Interrupt PUSH and POP (W, STATUS) register enable bit. 0 = Disable interrupt PUSH and POP function. 1 = Enable interrupt PUSH and POP function.
bit 3	**3Fx2EN:** ROM code run 3FFF instruction twice reset enable bit. 0 = Disable 3FFF x 2 reset function. 1 = Enable 3FFF x 2 reset function.
bit 2	**LOST:** Long external oscillator start time control bit. 0 = 20ms Internal RC change to external oscillator start time. 1 = 40ms Internal RC change to external oscillator start time.
bit 1	**PORB:** Power On Reset Status Bit. 0 = A power on reset occurred (must be set in software after a power on reset occurs). 1 = No power on reset occurred.
bit 0	**LBDHB:** Power Detect High Level Status Bit. 0 = An LBD high level reset occurred (must be set in software after a power on reset occurs). 1 = No LBD high level reset occurred.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.1.2.2.7 IRCCON Register

The Internal RC Control register (IRCCON) is used to configure system frequency. The IRCCON register bits are shown in Register 6.

Register 6. IRCCON – Internal-RC Control (Address: 14h or 94h)

R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
IFDIV3	IFDIV2	IFDIV1	IFDIV0	T2OCK	/GMF	CHWCK	GREMD
bit7							bit0

bit 7-4	**FDIV[3:0]:** System clock select Bit. **Bit Value** / **F_{osc}** 11xx – 8 MHz (default) 10xx – 32 kHz (WDT) 0111 – 4 MHz 0110 – 2 MHz 0101 – 1 MHz 0100 – 500 kHz 0011 – 250 kHz 0010 – 125 kHz 0001 – 62.5 kHz 0000 – 15.625 kHz
bit 3	**T2OCK:** Timer2 clock source select bit. 0 = From Fcpu. 1 = From Fosc.

bit 2	**/GMF:** Green mode flag bit. 0 = Green mode occurred. 1 = None Green mode occurred.
bit 1	**CHWCK:** Change WDT Input Clock Bit. 0 = WDT Input Clock from WDT. 1 = WDT Input Clock from System clock.
bit 0	**GREMD:** Green Mode Enable Bit. 0 = Disable green mode. 1 = Enable green mode.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.1.2.2.8 INOSCR Register

The INOSCR register bits are shown in Register 7.

Register 7. INOSCR – MCU Oscillator Control (Address: 97h)

R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYCKF	—	IRCLVC	MK0	ECKIN	OSO2E	OSC2O	/OSCIN
bit7							bit0

bit 7	**SYCKF:** System clock operation flag bit. 0 = System clock by external oscillator. 1 = System clock by internal oscillator
bit 5	**IRCLVC:** Internal RC low-voltage compensate bits. 0 = Disable IRC low voltage compensate. 1 = Enable IRC low voltage compensate.
bit 4	**MK0:** Must keep "0" bit.
bit 3	**ECKIN:** External Clock Input Enable bit. 0 = Disable oscillator external clock input. 1 = Enable oscillator external clock input (must be set in external oscillator of RC mode).
bit 2	**OSO2E:** Both of Internal and external oscillator Enable bit. 0 = Only use internal oscillator or external oscillator. 1 = Internal and external (LF mode only) oscillator enable both.
bit 1	**OSC2O:** OSC2/PA4 Oscillator Clock Output Enable bit. 0 = Disable OSC2/PA4 oscillator clock output in internal or external of RC mode oscillator. 1 = Enable OSC2/PA4 oscillator clock output in internal or external of RC mode oscillator.
bit 0	**/OSCIN:** MCU Internal Or external oscillator Select bit. 0 = Default the MCU clock based on internal 8MHz oscillator. 1 = The MCU clock based on external oscillator (type from option select). When internal 8MHz oscillator change to external oscillator must wait OST time 20ms.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.1.3 PCL and PCHLAT

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCHLAT. On any Reset, the PC is cleared. Figure 29 shows the two situations for the loading of the PC. The upper example in Figure 29 shows how the PC is loaded on a write to PCL (PCHLAT<4:0> → PCH). The lower example in Figure 29 shows how the PC is loaded during a LCALL or LJUMP instruction (PCLATH<4:3> →PCH).

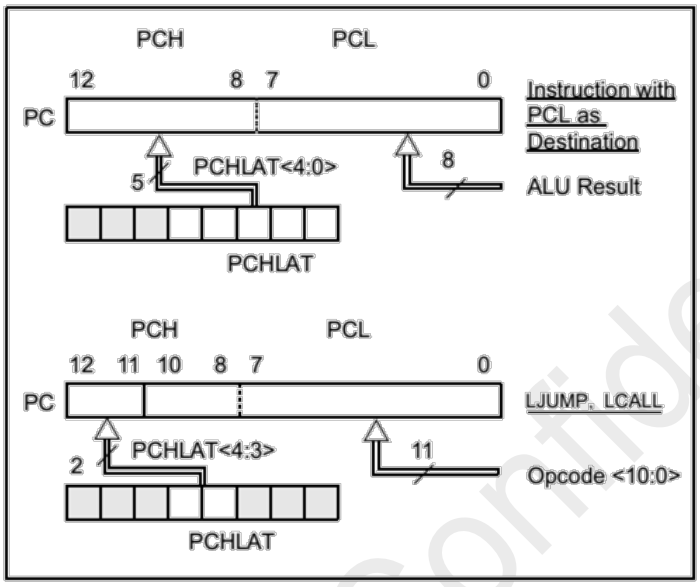


Figure 27. Loading of PC in Different Situations

7.1.3.1 Computed LJUMP

A computed LJUMP is accomplished by adding an offset to the program counter (ADDWR PCL). When performing a table read using a computed LJUMP method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

7.1.3.2 Stack

The CMT2189A has an 8-level x 13-bit wide hardware stack (see Figure 26). The stack space is not part of either program or data space and the Stack Pointer are not readable or writable. The PC is PUSHed onto the stack when a LCALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RET, RTIW or a RTFI instruction execution. PCHLAT is not affected by a PUSH or POP operation. The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and etc.).

Notes

1. There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.
2. There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the LCALL, RET, RTIW and RTFI instructions or the vectoring to an interrupt address.

7.1.4 Indirect Addressing Register (IAR) and MSR Registers

The IAR is not a physical register. Addressing the IAR will cause indirect addressing. Indirect addressing is possible by using the IAR. Any instruction using the IAR actually accesses data pointed to by the Memory Select Register (MSR). Reading IAR itself indirectly will produce 00h. Writing to the IAR indirectly results in a no operation (although Status bits may be affected).

An effective 8-bit address is obtained by concatenating the 8-bit MSR, as shown in Figure 30. A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 1.

Example 1. Indirect Addressing

```
        LDWI    0x20    ; initialize pointer
        STWR    MSR     ; to RAM
NEXT    CLRR    IAR     ; clear IAR register
        INCR    MSR, f  ; inc pointer
        BTSS    MSR, 4  ; all done?
        LJUMP   NEXT    ; no clear next
CONTINUE                ; yes continue
```

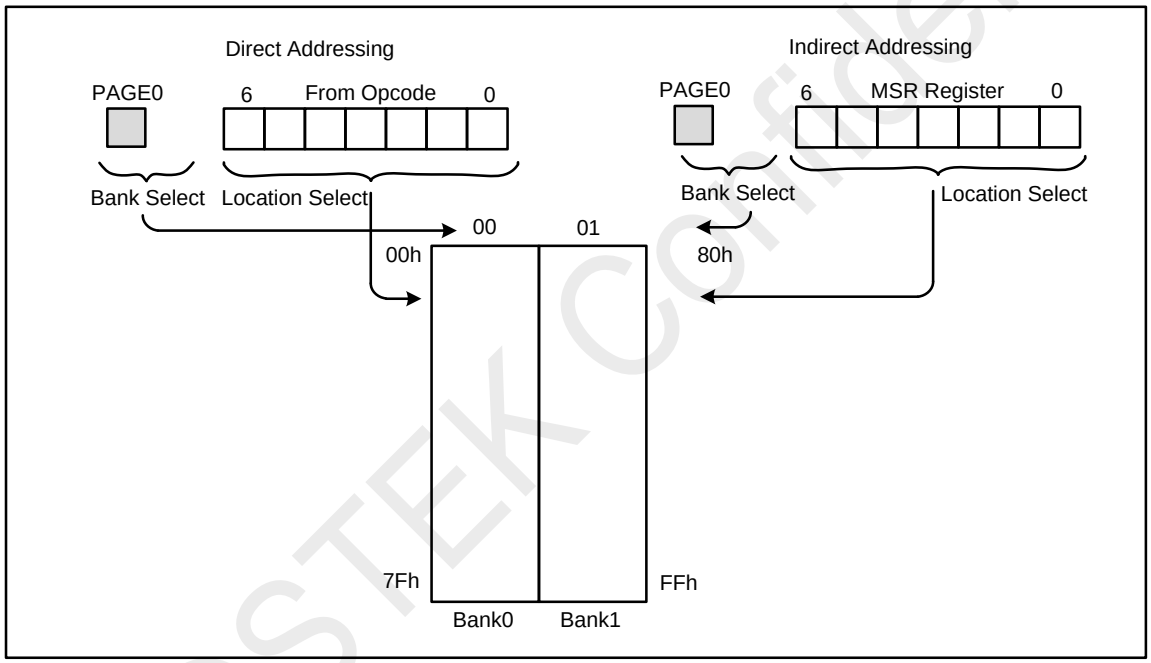


Figure 28. Direct/Indirect Addressing CMT2189A

7.2 Port A

There have four general purpose I/O pins available, PA0 ~ PA3, which map to the K0 ~ K3 pins in the manner as shown in the figure below. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Table 17. Mapping from the GPIOs to the Pinouts

GPOI	Pinout
PA0	K1/CLK2
PA1	K0/DATA2
PA2	K2
PA3	K3/MCLR

7.2.1 PORTA and the CPIOA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is CPIOA. Setting a CPIOA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a CPIOA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The exception is PA3, which is input only and its CPIO bit will always read as '1'. Example 2 shows how to initialize PORTA.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; this value is modified and then written to the PORT data latch. PA3 reads '0' when MCLR = 1.

Example 2. Initializing PORTA

```
BCR     STATUS, PAGE0   ;Bank0
CLRR    PORTA           ;Init PORTA
LDWI    05h             ;Set PA<2:0> to DIO
BSR     STATUS, PAGE0   ;Bank 1
LDWI    0Ch             ;Set PA<3:2> as inputs
STWR    CPIOA           ;and set PA<5:4, 1:0> as
                        ;outputs
BCR     STATUS, PAGE0   ;Bank 0
```

Register 8. PORTA – PORTA Register (Address: 05h)

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
		DATA	CLK	PA3	PA2	PA1	PA0
bit7							bit0

bit 5	**PORTA<5>:** DATA I/O pin bit. 1 = Port pin is >VIH. 0 = Port pin is <VIL.
bit 4	**PORTA<4>:** CLK Input pin bit. 1 = Port pin is >VIH. 0 = Port pin is <VIL.
bit 3-0	**PORTA<3:0>:** PORTA I/O pin bits. 1 = Port pin is >VIH. 0 = Port pin is <VIL.

Register 9. CPIOA – PORTA Input / Output Control Register (Address: 85h)

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	CPIOA5	CPIOA4	CPIOA3	CPIOA2	CPIOA1	CPIOA0
bit7							bit0

bit 5	**CPIOA<5>:** DATA Input / Output Control bits. 1 = PORTA pin configured as an input. 0 = PORTA pin configured as an output.

bit 4	**CPIOA<4>:** CLK Input Control bits, when used as CLK it need to configured as input pin. 1 = PORTA pin configured as an input. 0 = PORTA pin configured as an output.
bit 3-0	**CPIOA<3:0>:** PORTA Input / Output Control bits. 1 = PORTA pin configured as an input. 0 = PORTA pin configured as an output.
Notes: [1]. CPIOA<3> always reads 1. [2]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.2.2 Additional Pin Functions

Every PORTA pin on the CMT2189A has an interrupt-on-change option and every PORTA pin has a pull-up option. Every PORTA pin, except PA3, can be configured to open-drain output mode. But only PORTA<2:0> has a pull-down option. The next sections describe these functions.

7.2.2.1 Pull-up

Each of the PORTA pins has an individually configurable internal pull-up. Control bits APHBx enable or disable each pull-up. Refer to Register 10. The pull-ups are disabled on a POR.

Register 10. PAPHR – Pull-up Control Register (Address: 95h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	APHB5	APHB4	APHB3	APHB2	APHB1	APHB0
bit7							bit0

bit 5-0	**WPUA<5:0>:** Pull-up Register bits. 1 = Pull-up enabled. 0 = Pull-up disabled.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.2.2.2 Interrupt-On-Change

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits PAINTx enable or disable the interrupt function for each pin. Refer to Register 11. The interrupt-on-change is disabled on a Power-on Reset. For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set, the PORTA Change Interrupt Flag bit (PAIF) in the INTFR register. This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner.

a) Any read or write of PORTA. This will end the mismatch condition.
b) Clear the flag bit PAIF.

A mismatch condition will continue to set flag bit PAIF. Reading PORTA will end the mismatch condition and allow flag bit PAIF to be cleared.

Register 11. PAINTR– Interrupt-On-Change PORTA Register (Address: 96h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PAINT5	PAINT4	PAINT3	PAINT2	PAINT1	PAINT0
bit7							bit0

bit 5-4	**IOCA<5:4>: I**nterrupt-on-Change PORTA Control bits. When PA5 is used as DATA pin or PA4 is used as CLK pin, the corresponding bit need to be set to 0 to disable the Interrupt-on-change. 1 = Interrupt-on-change enabled. 0 = Interrupt-on-change disabled.
bit 3-0	**IOCA<3:0>: I**nterrupt-on-Change PORTA Control bits. 1 = Interrupt-on-change enabled. 0 = Interrupt-on-change disabled.
Notes: [1]. Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized. [2]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.2.2.3 Open-Drain

Each of the PORTA pins, except PA3, has an individually configurable open-drain output. Control bits PAODx enable or disable each open-drain. Refer to Register 12. The open-drain is disabled on a POR.

Register 12. PAODR – Open-Drain Output Control Register (Address: 16h)

U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	PAOD5	PAOD4		PAOD2	PAOD1	PAOD0
bit7							bit0

bit 5-0	**PAOD<5:0>:** Open-drain Output Control bits. 1 = open-drain output enabled. 0 = open-drain output disabled.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.2.2.4 Pull-Down

Only PORTA<2:0> pins have individually configurable internal pull-down. Control bits APLBx enable or disable each pull-down. Refer to Register 13. The pull-down are disabled on a POR.

Register 13. PACPLR – Pull-Down Control Register (Address: 17h)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	APLB2	APLB1	APLB0
bit7							bit0

bit 2-0	**APLB<2:0>:** Pull-down Control bits. 1 = Pull-down enabled. 0 = Pull-down disabled.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.3 Timer0 Module

The Timer0 module timer/counter has the following features.

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 31 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

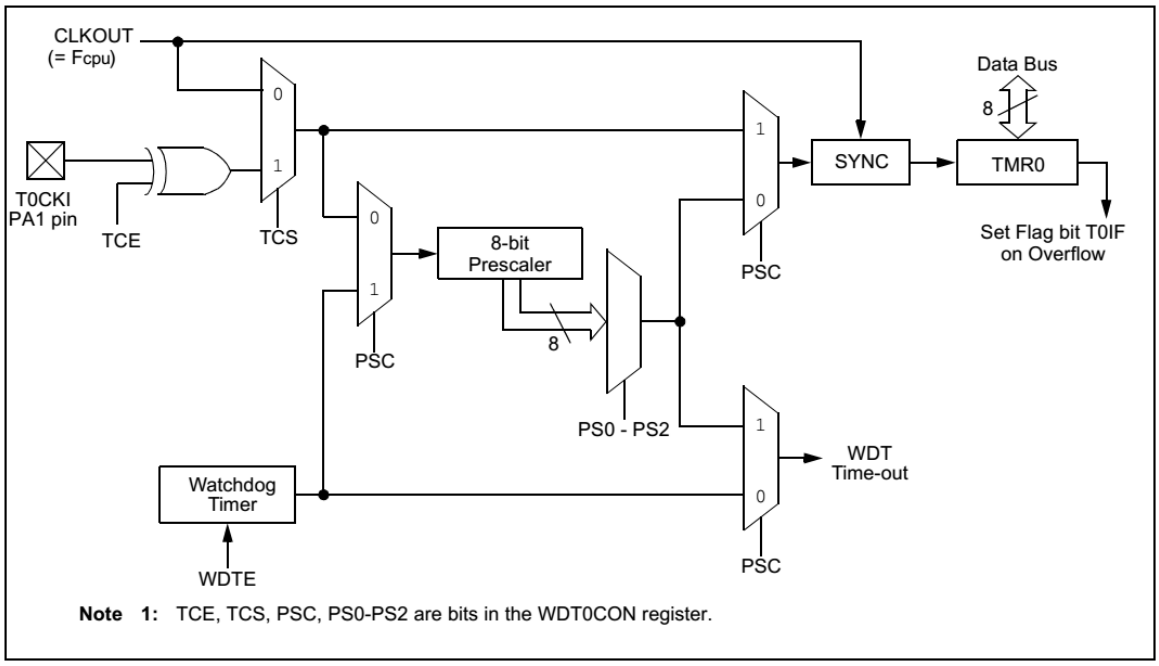


Figure 29. Block Diagram of the Timer0/WDT Prescaler

7.3.1 Timer0 Operation

Timer mode is selected by clearing the TCS bit (WDT0CON <5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the TCS bit (WDT0CON <5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin PA1/T0CKI. The incrementing edge is determined by the source edge (TCE) control bit (WDT0CON <4>). Clearing the TCE bit selects the rising edge.

7.3.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTER<0>). The T0IF bit (INTFR<0>) must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from Sleep, since the timer is shutoff during Sleep.

7.3.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 T_{OSC} (and a small RC delay of 20 ns) and low for at least 2 T_{OSC} (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

7.3.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this Datasheet. The prescaler assignment is controlled in software by the control bit PSC (WDT0CON<3>). Clearing the PSC bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (WDT0CON _REG<2:0>). The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRR 1, STWR 1, BSR 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWT instruction will clear the prescaler along with the Watchdog Timer.

7.3.4.1 Switching Prescaler Assignment

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 3) must be executed when changing the prescaler assignment from Timer0 to WDT.

Example 3. Changing Prescaler (Timer0 → WDT)

```
BCR     STATUS, PAGE0   ; Bank0
CLRWT                   ; Clear WDT
CLRR    TMR0            ; Clear TMR0 and prescaler
BSR     STATUS, PAGE0   ; Bank 1

LDWI    b’00101111’     ; Required if desired
STWR    WDT0CON         ; PS2:PS0 is 000 or 001
CLRWT                   ;

LDWI    b’00101xxx’     ; Set postscaler to desired
STWR    WDT0CON         ; WDT rate
BCR     STATUS, PAGE0   ; Bank 0
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 4. This precaution must be taken even if the WDT is disabled.

Example 4. Changing Prescaler (WDT → Timer0)

```
CLRWT                          ; Clear WDT and postscalter
BSR       STATUS, PAGE0        ; Bank 1

LDWI      b'xxxx0xxx'          ; Select TMR0, prescale, and
                               ; clock source
STWR      WDT0CON              ;
BCR       STATUS, PAGE0        ; Bank 0
```

Table 18. Registers Association with Timer0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, PDR
01h	TMR0	Timer0 Module's Register								xxxx xxxx
0Bh/8Bh	INTER	GIE	--	--	INTE	PAIE	T2IE	T1IE	T0IE	0000 0000
0Ch/8Ch	INTFR	--	--	--	INTF	PAIF	T2IF	T1IF	T0IF	0000 0000
81h	WDT0CON	--	IES	TCS	TCE	PSC	PS2	PS1	PS0	1111 1111
85h	CPIO A	--	--	CPIO PA5	CPIO PA4	CPIO PA3	CPIO PA2	CPIO PA1	CPIO PA0	---11 1111

Notes:

[1]. Legend: – = Unimplemented locations, read as '0', u= unchanged, x= unknown.

[2]. Shaded cell are not used by Timer0 module.

7.4 Timer1 Module with Gate Control

The CMT2189A devices have a 16-bit timer. Figure 26 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input (T1G)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 14, is used to enable/disable Timer1 and select the various features of the Timer1 module.

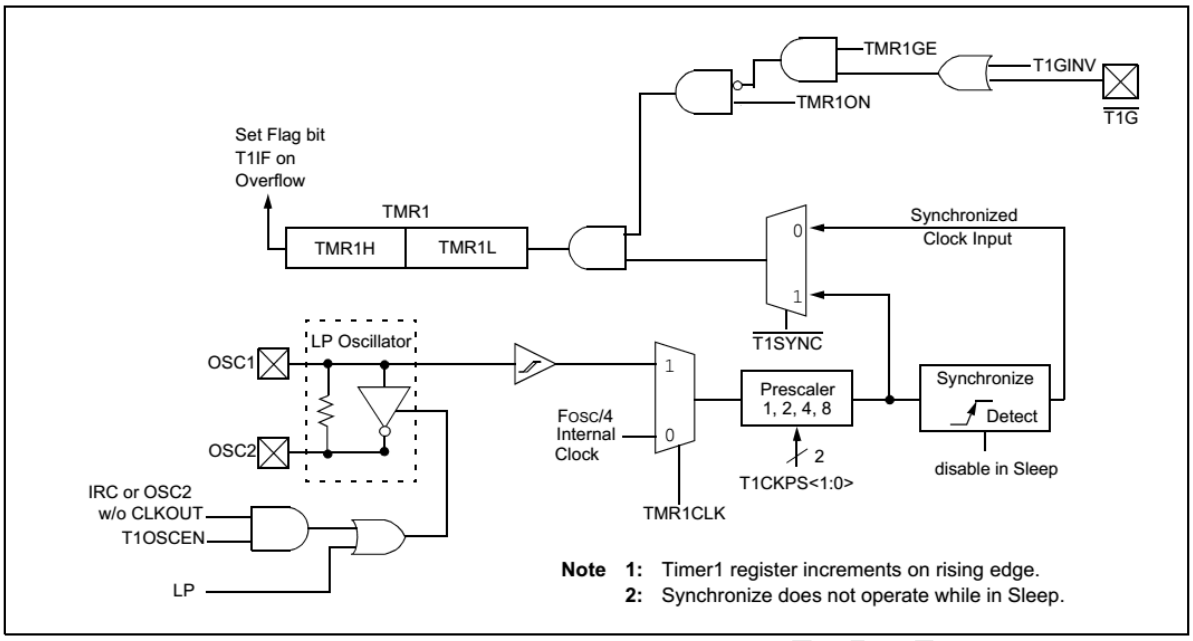


Figure 30. Timer 1 Block Diagram

Register 14. T1CON – Timer1 Control Register (Address: 10h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON
bit7							bit0

bit 7	**T1GINV:** Timer1 gate invert bit. 0 = Timer1 gate (PA4) is low active. 1 = Timer1 gate (PA4) is high active.
bit 6	**TMR1GE:** Timer1 Gate Enable Bit. If TMR1ON = 0 this bit is ignored. If TMR1ON = 1. 0 = Timer1 is on. 1 = Timer1 is on when T1GINVand /T1G(PA4) pin is both low, or T1GINV and /T1G(PA4) pin is both high.
bit 5-4	**T1CKPS1& T1CKPS0:** Timer1 Input Clock Prescale Select bits. 00 = 1 : 1 Prescale value. 01 = 1 : 2 Prescale value . 10 = 1 : 4 Prescale value. 11 = 1 : 8 Prescale value.
bit 3	**T1OSCEN:** LF Oscillator Enable Bit. If INTOSC without CLKOUT oscillator is active : 0 = LP oscillator is off. 1 = LP oscillator is enabled for Timer1 clock.
bit 2	**/T1SYNC:** Timer1 External Clock Input Synchronization Control Bit. If TMR1CLK = 0 this bit is ignored, Timer1 use internal clock If TMR1CLK = 1. 0 = Synchronize external clock input. 1 = Do not synchronize external clock input.

bit 1	**TMR1CLK:** Timer1 Clock Source Select Bit. 0 = Select internal clock Fcpu. 1 = Select External clock from T1CKI pin (on rising edge).
bit 0	**TMR1ON:** TMR1 On Bit. 0 = Stop Timer1. 1 = Enable Timer1.
Note: [1]. Legend: R = Readable bit, W = Writable bit, U = Unimplemented bit, -n = Value at POR, '1' = Bit is set, '0' = Bit is cleared, x = Bit is unknown.	

7.4.1 Timer1 Mode Operation

Timer1 can operate in one of three modes.

- 16-bit timer with prescaler
- 16-bit synchronous counter
- 16-bit asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI (PA5). In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously. In counter and timer modules, the counter/timer clock can be gated by the T1G (PA4) input. If an external clock oscillator is needed (and the microcontroller is using the INTOSC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

Please note that the PA4 and PA5 are also used as CLK and DATA pins in the chip pinouts, if the user want to use them as T1CKI or T1G, please make sure the Timer1 functions does not conflict with the CLK/DATA functions.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

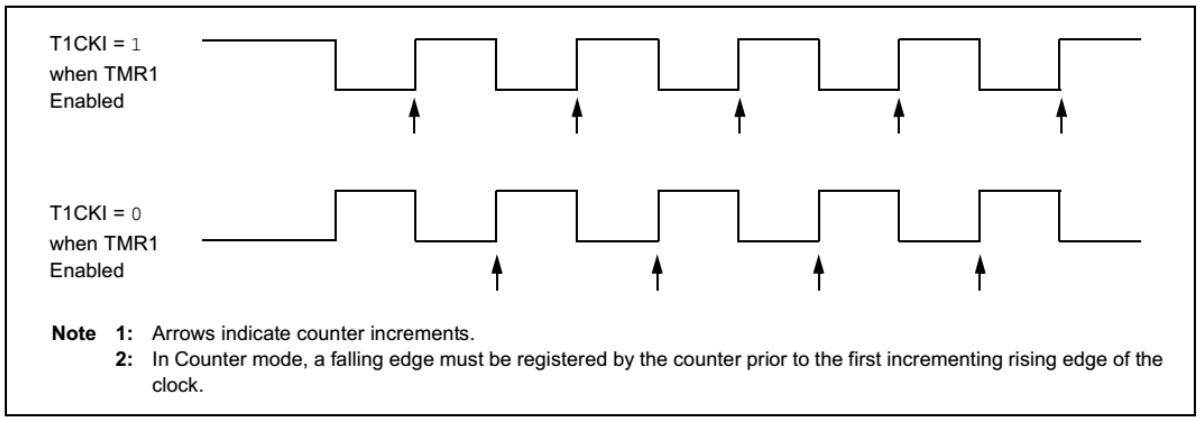


Table 19. Timer1 Incrementing Edge

7.4.2 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit (INTFR<1>) is set. To enable the interrupt on rollover, you must set these bits.

- Timer1 interrupt Enable bit (INTER<1>)
- GIE bit (INTER<7>)

The interrupt is cleared by clearing the T1IF in the Interrupt Service Routine.

Note: The TMR1H:TTMR1L register pair and the T1IF bit should be cleared before enabling interrupts.

7.4.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4, or 8 divisions of the clock input. The T1CKPS bits (T1CON<5:4>) control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

7.4.4 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 5.12.4.1).

7.4.4.1 Reading and Writing Timer1 in Asynchronous Counter Mode

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

7.4.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 32 kHz. It will continue to run during Sleep. It is primarily intended for a 32 kHz crystal.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the system clock is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

CPIOA5 and CPIOA4 bits are set when the Timer1 oscillator is enabled. PA5 and PA4 read as ‘0’ and CPIOA5 and CPIOA4 bits read as ‘1’.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

7.4.6 Timer1 Operation during Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external clock source can be used to increment the counter. To setup the timer to wake the device,

- Timer1 must be on (T1CON<0>);
- T1IE bit (INTER<1>) must be set.

The device will wake-up on an overflow. If the GIE bit (INTER<7>) is set, the device will wake-up and jump to the

Interrupt Service Routine on an overflow.

Table 20. Registers Association with Timer1 as a Timer/Counter

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, PDR
0Bh/8Bh	INTER	GIE	--	--	INTE	PAIE	T2IE	T1IE	T0IE	0000 0000
0Ch/8Ch	INTFR	--	--	--	INTF	PAIF	T2IF	T1IF	T0IF	0000 0000
0Eh/8Ch	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx
0Fh/8Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON	0000 0000

Notes:

[1]. Legend: – = Unimplemented locations, u= unchanged, x= unknown.

[2]. Shaded cell are not used by Timer1 module.

7.5 Timer2 Module with PWM/Buzzer Output Control

Timer2 can operate for PWM or Buzzer output mode. Figure 27 shows the basic block diagram of the Timer2 module.

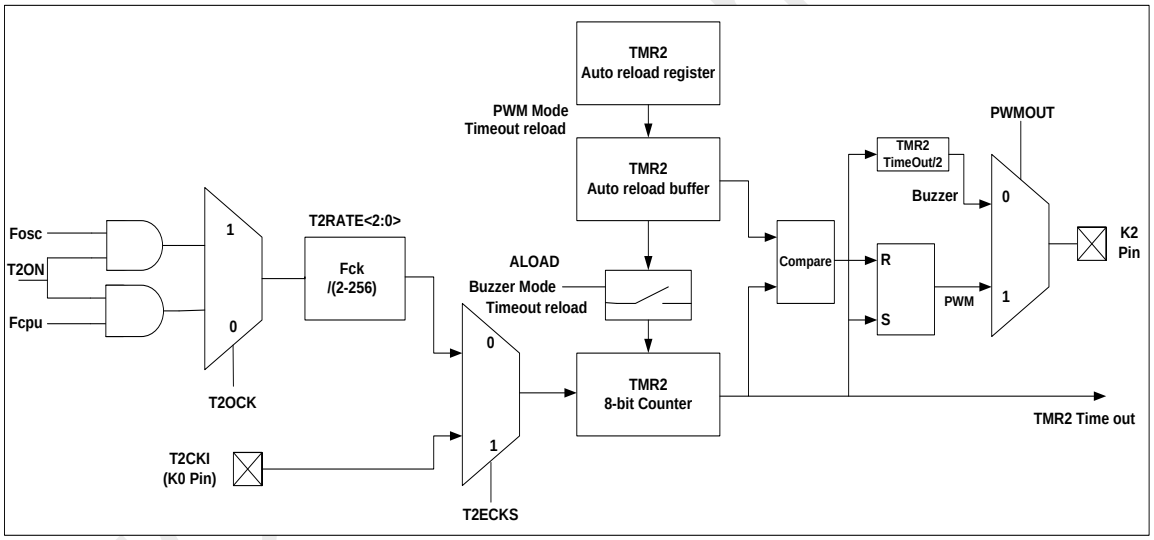


Figure 31. Timer2 Block Diagram

7.5.1 Timer2 Operation in Clock Frequency Output (Buzzer)

Buzzer output (T2OUT) is from TMR2 timer/counter frequency output function. By setting the TMR2 clock frequency, the clock signal is output to K2 and the K2 general purpose I/O function is auto-disable. The T2OUT frequency is divided by 2 from TMR2 interval time. T20OUT frequency is 1/2 TMR2 frequency. The TMR2 clock has many combinations and easily to make difference frequency. The T2OUT frequency waveform is as following figure.

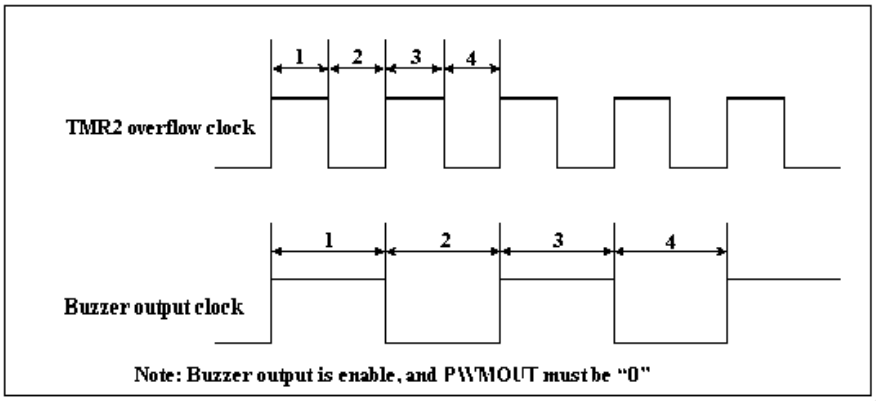


Figure 32. Timer2 Clock Frequency Output

Example 5. Setup T2OUT output from TMR2 to T2OUT (PA2)

The internal high-speed clock is 8 MHz. The T2OUT frequency is 2 kHz. Because the T2OUT signal is divided by 2, set the TMR2 clock to 4 kHz. (Interval time for TMR2 interrupt is 1/8 kHz = 0.125ms). The TMR2 clock source is from internal oscillator clock. TMR2 rate is Fcpu/4. The T2rate2~0 = 110. TMR2 = T2ALR2 = 131.

```
LDWI    60h             ;
STWR    T2CON           ; Set the T2rate to Fcpu/4
LDWI    83h             ;
STWR    TMR2            ;
STWR    T2ALR           ; Set the auto-reload reference
                        ; value 131D=83h
BSR     T2CON, T2OUT    ; Enable TMR2 output to PA2
                        ; and disable PA2 I/O function
BSR     T2CON, ALOAD    ; Enable TMR2 auto-reload
                        ; function
BSR     T2CON, T2ON     ; Enable TMR2 Timer
```

7.5.2 Timer2 Operation in PWM Output

7.5.2.1 Timer2 PWM Output Mode

PWM function is generated by TMR2 timer counter and output the PWM signal to PWMOUT pin (K2). The 8-bit counter counts modulus 256, 64, 32, 16 controlled by ALOAD2, T2OUT bits. The value of the 8-bit counter (TMR2) is compared to the contents of the reference register (T2ALR). When the reference register value (T2ALR) is equal to the counter value (TMR2), the PWM output goes low. When the counter reaches zero, the PWM output is forced high. The low-to-high ratio (duty) of the PWM0 output is T2ALR/256, 64, 32, 16. PWM output can be held at low level by continuously loading the reference register with 00H. Under PWM operating, to change the PWM's duty cycle is to modify the T2ALR.

The equation of TMR2 initial value is as following.

TMR2 initial value = N_Period - (TMR2interrupt interval time * input clock)

N_Periodis TMR2 overflow boundary number. TMR2 timer overflow time has six types (TMR2 timer, TMR2 event counter, TMR2 Fcpu clock source, TMR2 Fosc clock source, PWM mode and no PWM mode). These parameters decide TMR2 overflow time and valid value as Table 19.

Example 6. Setup Periodic 8 us, Duty Cycle 50% PWM Output

At internal osc = 8MHz. Fcpu=Fosc/2. Select T2rate2~0 = 000 (Fcpu/2), bit2~0 = 111 the TMR2 valid value = 00~0FH.

```
CLRR    T2CON       ; Clear TMR2 control register
CLRR    TMR2        ; Clear TMR2 counter register
LDWI    08h         ;
STWR    T2ALR       ; Set PWM data 08H,
                    ; duty=50%; if data 04h
                    ; duty=25%
LDWI    077h        ;
STWR    T2CON       ; Set PWM output and
                    ; TMR2valid value00~0Fh
BSR     T2CON, 7    ; Enable TMR2 timer
```

Table 21. The Basic Timer Table Internal Time of TMR2

T2RATE[2:0]	TMR2 Input Clock	Fcpu = 8 MHz / 2		Fcpu = 32768 Hz / 2	
		Max overflow interval (ms)	One step=max/256 (us)	Max overflow interval (ms)	One step = max/256 (us)
111	Fcpu/2	0.128	0.5	31.25	122.070
110	Fcpu/4	0.256	1	62.5	244.141
101	Fcpu/8	0.512	2	125	488.281
100	Fcpu/16	1.024	4	250	976.563
011	Fcpu/32	2.048	8	500	1953.125
010	Fcpu/64	4.096	16	1000	3906.25
001	Fcpu/128	8.192	32	2000	7812.5
000	Fcpu/256	16.384	64	4000	15625

Example 7. To set 2.5ms interval time for TMR2 interrupt

TMR2 clock source is Fcpu (T2ECKS=0) and no PWM output (PWMOUT=0).
High clock is internal 8MHz. Fcpu=Fosc/2. Select T2rate = 010 (Fcpu/64).
TMR2 initial value = N_Period- (TMR2 interrupt interval time * input clock)
= 256 – (2.5ms * 8MHz /2 / 64)
= 256 – ((0.005 * 4 * 1000000) / 2 / 64)
= 256 – 156 (Real value =156.25)
= 100
= 64h

Table 22. TMR2 Overflow Time and Valid Value

PWMOUT	T2OUT	ALOAD	N_Period	TM2 valid value	Remark
0	X	X	256	000~0FF	Per 256 count overflow
1	0	0	256	000~0FF	Per 256 count overflow
1	1	0	64	000~03F	Per 64 count overflow
1	0	1	32	000~01F	Per 32 count overflow
1	1	1	16	000~00F	Per 16 count overflow
X	X	X	256	000~0FF	Per 256 count overflow

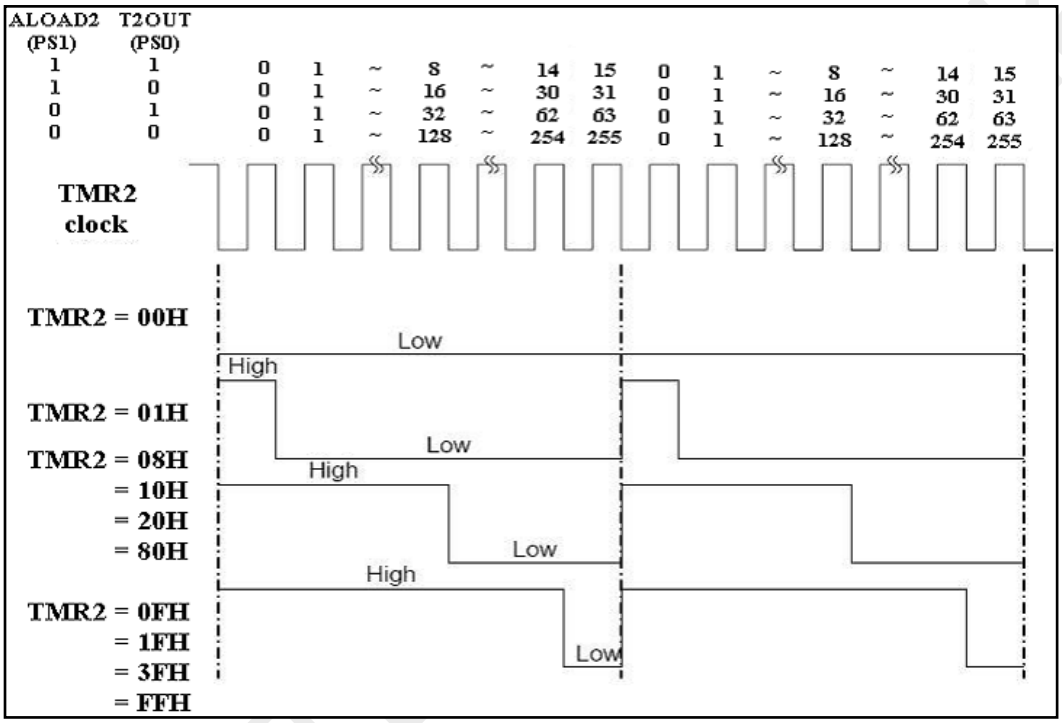


Figure 33. Timing of the PWM Output

7.5.2.2 T2IF and PWM Duty

In PWM mode, the frequency of T2IF is depended on PWM duty range. See the figure below, the T2IF frequency is related with PWM duty.

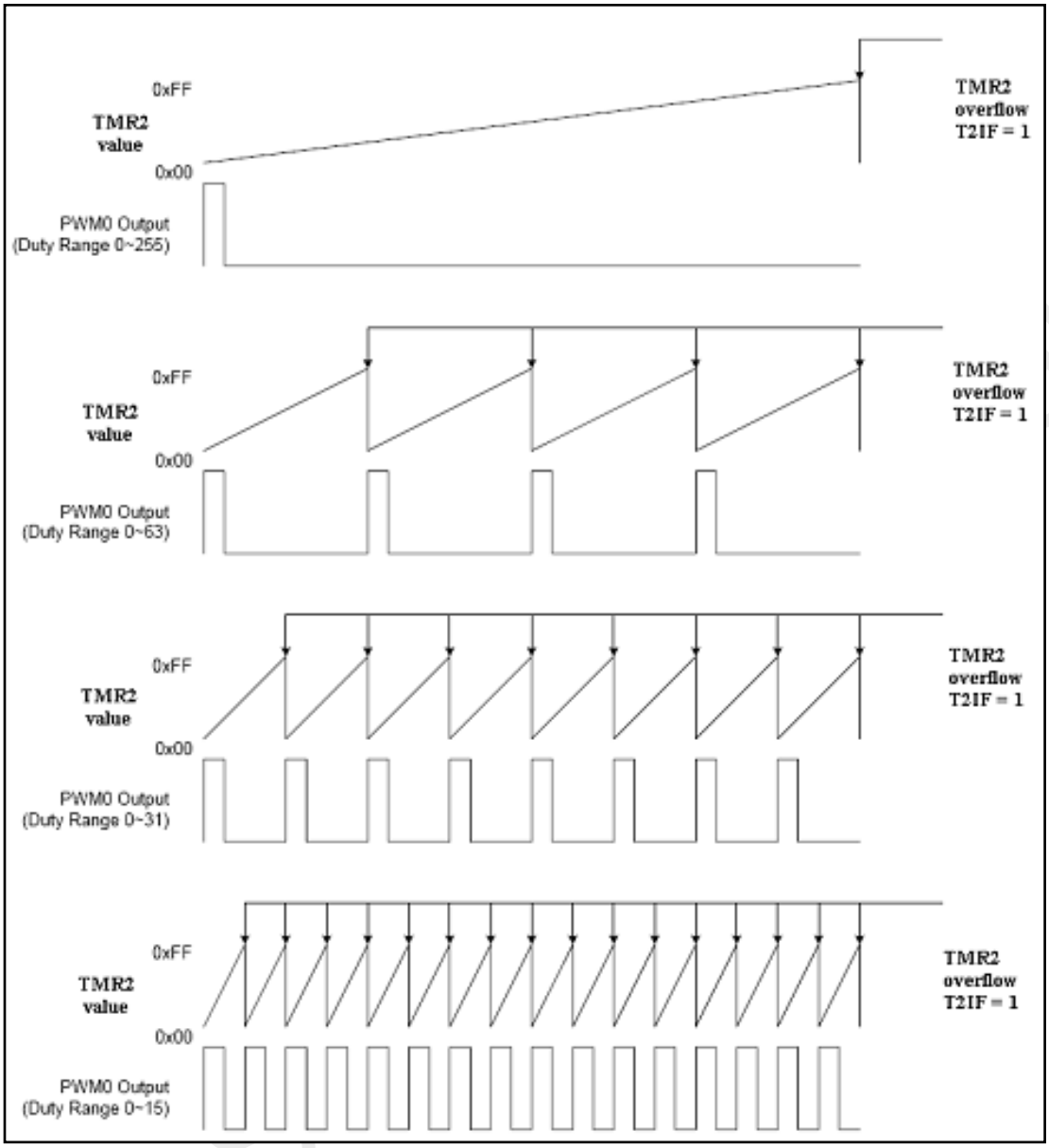


Figure 34. T2IF Frequency Relate with PWM Duty

7.5.2.3 PWM Duty with T2ALR Changing

In PWM mode, the system will compare TMR2 and T2ALR all the time. When TMR2 <T2ALR, the PWM will output logic “High”, when TMR2 ≥ T2ALR, the PWM will output logic “Low”. If TMR2is changed in certain period, the PWM duty will change in next PWM period. If T2ALR is fixed all the time, the PWM waveform is also the same.

Figure 31 is shown the waveform with fixed T2ALR. In every TMR2overflow PWM output “High, when TMR2 ≥ T2ALR PWM outputs “Low”. If T2ALR is changing in the program processing, the PWM waveform will became as Figure 38. In period 2 and period 4, new Duty (T2ALR) is set. T2ALRis double buffer design. The PWM still keeps the same duty in period 2 and period 4, and the new duty is changed in next period. By the way, system can avoid the PWM not changing or H/L changing twice in the same cycle and will prevent the unexpected or error operation.

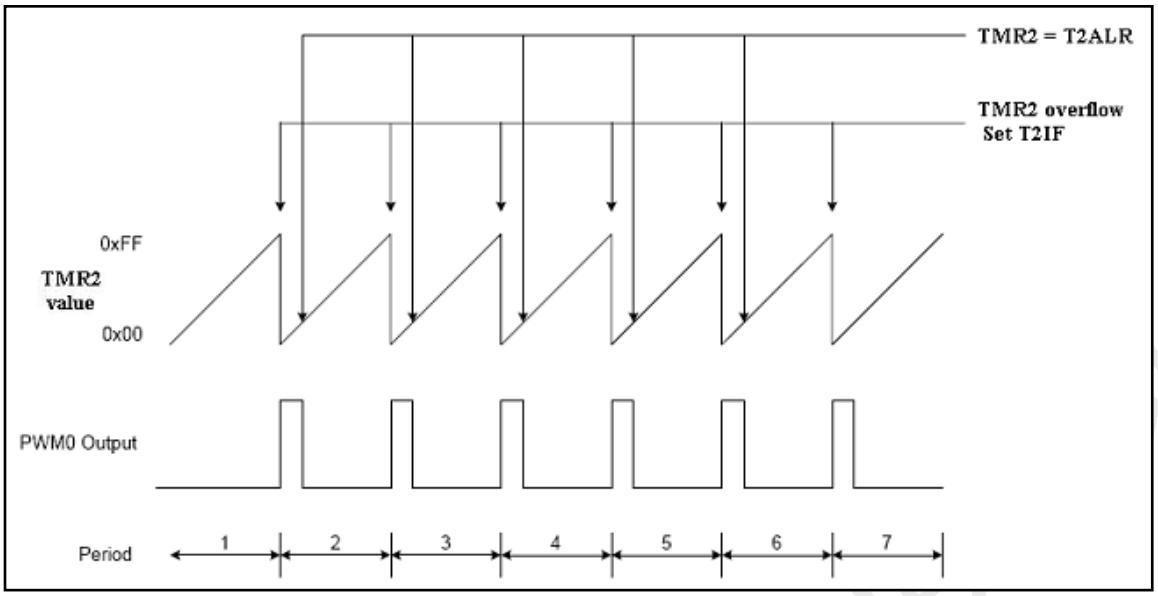


Figure 35. The Waveform with Fixed T2ALR

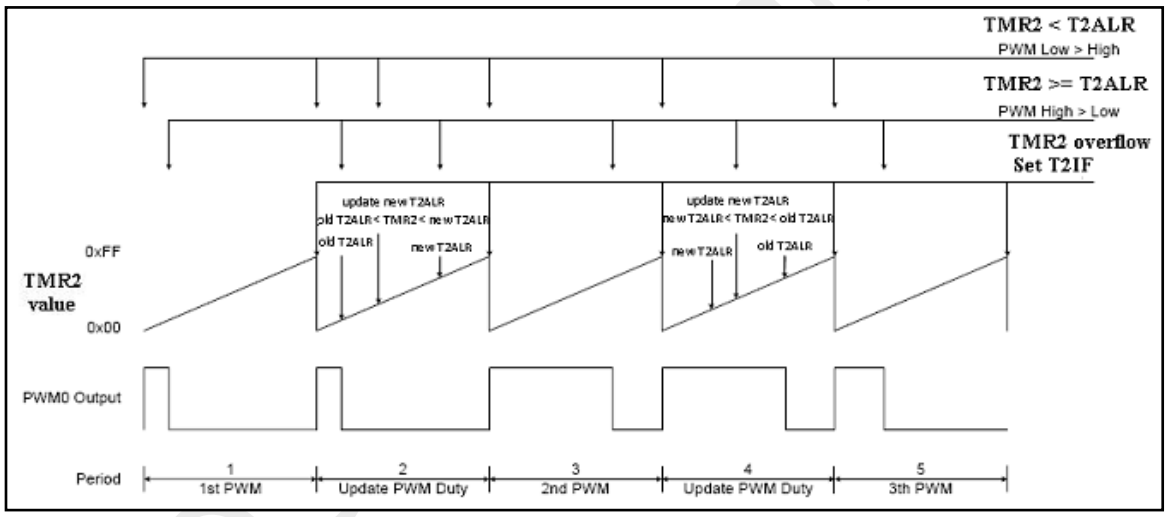


Figure 36. The Waveform when Changing the Program Processing

7.5.3 Timer2 Registers

Register 15. T2CON – Timer2 Control Register (Address: 11h and 91h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2ON	T2RATE2	T2RATE1	T2RATE0	T2ECKS	ALOAD	T2OUT	PWMOUT
bit 7							bit 0

bit 7	**T2ON:** Timer2 enable bit. 0 = Stop Timer2. 1 = Enable Timer2.
bit 6-4	**T2RATE<2:0>:** Timer2 Input Clock Prescale Select bits. 0 0 0 = Fck/256

	0 0 1 = Fck/128 0 1 0 = Fck/64 0 1 1 = Fck/32 1 0 0 = Fck/16 1 0 1 = Fck/8 1 1 0 = Fck/4 1 1 1 = Fck/2
bit 3	**T2ECKS:** Timer2 clock source select bit. 0 = Internal clock (Fcpu or Fosc). 1 = External clock from PA0 pin.
bit 2	**ALOAD:** Auto-reload control bit. Only valid when PWMOUT = 0. 0 = Disable Timer2auto-reload function. 1 = Enable Timer2auto-reload function.
bit 1	**T2OUT:** Timer2time out toggle signal output control bit. Only valid when PWMOUT = 0. 0 = Disable, PA2 is I/O function. 1 = Enable, PA2 is output T2OUT signal.
bit 0	**PWMOUT:** PWM output control bit. 0 = Disable PWM output. 1 = Enable PWM output. PWM duty controlled by T2OUT, ALOAD 2 bits.

Table 23. Registers Association with Timer2 as a Timer/Counter

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, PDR
0Bh/8Bh	INTER	GIE	--	--	INTE	PAIE	T2IE	T1IE	T0IE	0000 0000
0Ch/8Ch	INTFR	--	--	--	INTF	PAIF	T2IF	T1IF	T0IF	0000 0000
12h/92h	TMR2	Timer2 Module's Register								0000 0000
13h/93h	T2ALR	Timer2 auto-load register								0000 0000
11h/91h	T2CON	T2ON	T2RATE2	T2RATE1	T2RATE0	T2ECKS	ALOAD	T2OUT	PWMOUT	0000 0000
14h/94h	IRCCON	IFDIV3	IFDIV2	IFDIV1	IFDIV0	T2OCK	/GMF	CHWCK	GREMD	1110 0100

Notes:

[3]. Legend: – = Unimplemented locations, u= unchanged, x= unknown.

[4]. Shaded cell are not used by Timer2 module.

7.6 Reset Condition for All Registers

Table 24. Reset Condition for All Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h(80h)	0000 0000	0000 0000	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h(82h)	0000 0000	0000 0000	0000 0100
STATUS	03h(83h)	0001 1xxx	000# #uuu	uuu# #uuu
MSR	04h(84h)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	----xx xxxx	--uu uuuu	----uu uuuu
PCHLAT	0Ah(8Ah)	------0 0000	---0 0000	------u uuuu
INTER	0Bh(8Bh)	0000 0000	0000 0000	uuuu uuuu
INTFR	0Ch(8Ch)	-----0 0000	-----0 0000	-----u uuuu
PORCON	0Dh(8Dh)	00--1 00##	00--1 00uu	uu--u uuuu
TMR1L	0Eh(8Eh)	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh(8Fh)	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	0000 0000	uuuu uuuu
T2CON	11h(91h)	0000 0000	0000 0000	uuuu uuuu
TMR2	12h(92h)	0000 0000	0000 0000	uuuu uuuu
T2ALR	13h(93h)	0000 0000	0000 0000	uuuu uuuu
IRCCON	14h(94h)	1110 0100	1110 0#00	uuuu u#uu
PCPHR	15h	0000 0000	0000 0000	uuuu uuuu
PAODR	16h	----00 0--00	----00 0--00	----uu u--uu
PACPLR	17h	0000 0000	0000 0000	uuuu uuuu
WDT0CON	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	----11 1111	----11 1111	----uu uuuu
CPIOC	87h	----11 1111	----11 1111	----uu uuuu
PAPHR	95h	----00 0000	----00 0000	----uu uuuu
PAINTR	96h	----00 0000	----00 0000	----uu uuuu
INOSCR	97h	1010 0000	uuuu uuuu	uuuu uuuu

Note:
[1]. x = unknown; u = unchanged; – = unimplemented, read as 0; # = value depends on condition.

7.7 Instruction Set Summary

The CMT2189A instruction set is highly orthogonal and is comprised of three basic categories listed as below.

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

Each instruction is a 14-bit word divided into an opcode, which specifies the instruction type, and one or more operands, which further specify the operation of the instruction. The formats for each of the categories are presented in Figure 39, while the various opcode fields are summarized in Table 25.

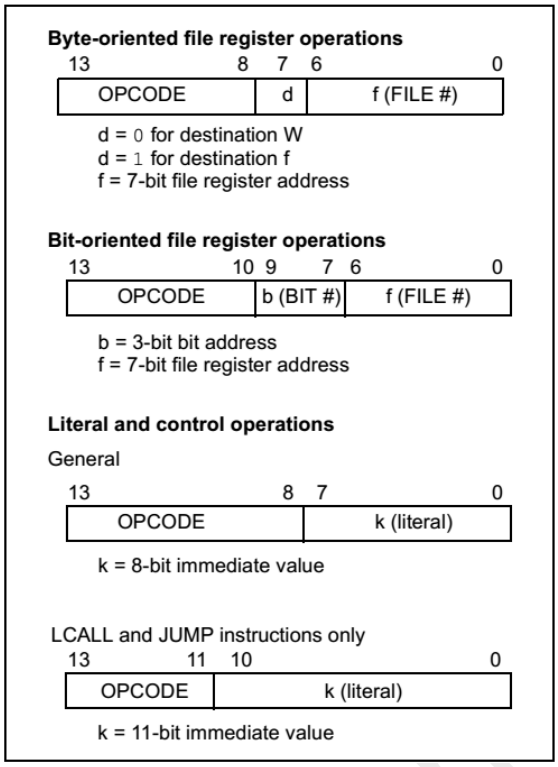


Figure 37. General Format for Instructions

Table 25. Opcode Field Decription

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

Table 26 lists the instructions recognized by assembler.

For byte-oriented instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction. For bit-oriented instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For literal and control operations, ‘k’ represents an 8-bit or 11-bit constant or literal value. One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1us. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP. All instruction examples use the format ‘0xhh’ to represent a hexadecimal number, where ‘h’ signifies a hexadecimal digit.

7.7.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register. For example, a CLRR PORTA instruction will read PORTA, clear all the data bits, and then write the result back to PORTA. This example would have the unintended result of clearing the condition that set the PAIF flag.

Table 26. CMT2189A Instruction Set

Mnemonic, Operands	Description	Cycles	14-Bit Opcode MSB LSB	Status Affected	Note
Byte-Oriented File Register Operations					
ADDWR f, d	Add W and f	1	0 1 1 0 1 1 d f f f f f f f	C, DC, Z	1, 2
ANDWR f, d	AND W with f	1	0 1 0 0 1 0 d f f f f f f f	Z	1, 2
CLRR f	Clear f	1	0 1 0 0 0 1 0 f f f f f f f	Z	1, 2
CLRW -	Clear W	1	0 1 0 0 0 0 1 x x x x x x x	Z	
COMR f, d	Complenment f	1	0 1 1 1 1 1 d f f f f f f f	Z	1, 2
CPIO f	Load W to Control I/O PORT Register	1	0 1 0 0 0 0 0 0 0 0 0 f f f		
DECR f, d	Decrement f	1	0 1 1 1 0 1 d f f f f f f f	Z	1, 2
DECRSZ f, d	Decrement f, Skip if 0	1(2)	0 1 1 1 1 0 d f f f f f f f		1, 2, 3
INCR f, d	Increment f	1	0 1 1 0 0 1 d f f f f f f f	Z	1, 2
INCRSZ f, d	Increment f, Skip if 0	1(2)	0 1 1 0 1 0 d f f f f f f f		1, 2, 3
IORWR f, d	Inclusive OR W with f	1	0 1 0 0 1 1 d f f f f f f f	Z	1, 2
LDR f, d	Move f	1	0 1 1 0 0 0 d f f f f f f f	Z	1, 2
NOP -	No Operation	1	0 1 0 0 0 0 0 0 0 0 0 0 0 0		
RLR f, d	Rotate Left f through Carry	1	0 1 0 1 0 1 d f f f f f f f	C	1, 2
RRR f, d	Rotate Right f through Carry	1	0 1 0 1 1 0 d f f f f f f f	C	1, 2
STWR f	Move W to f	1	0 1 0 0 0 1 1 f f f f f f f		
SUBWR f, d	Subtract W from f	1	0 1 1 1 0 0 d f f f f f f f	C, DC, Z	1, 2
SWAPR f, d	Swap nibbles in f	1	0 1 0 1 1 1 d f f f f f f f		1, 2
TMODE -	Load W to WDT0CON Register	1	0 1 0 0 0 0 0 0 0 0 0 0 1 1		
XORWR f, d	Exclusive OR W with f	1	0 1 0 1 0 0 d f f f f f f f	Z	1, 2
Bit-Oriented File Register Operations					
BCR f, b	Bit Clear f	1	0 0 0 0 b b b f f f f f f f		1, 2
BSR f, b	Bit Set f	1	0 0 1 0 b b b f f f f f f f		1, 2
BTSC f, b	Bit Test f, Skip if Clear	1(2)	0 0 0 1 b b b f f f f f f f		3
BTSS f, b	Bit Test f, Skip if Set	1(2)	0 0 1 1 b b b f f f f f f f		3
Literal and Control Operations					
ADDWI k	Add literal and W	1	1 1 0 1 1 1 k k k k k k k k	C, DC, Z	
ANDWI k	AND literal with W	1	1 1 0 1 0 0 k k k k k k k k	Z	
CLRWT -	Clear Watchdog Timer	1	0 1 0 0 0 0 0 0 0 0 0 0 0 1	/TF, /PF	
IORWI k	Inclusive OR literal with W	1	1 1 0 1 0 1 k k k k k k k k	Z	
LCALL k	Call subroutine	2	1 0 0 k k k k k k k k k k k		
LDWI k	Move literal to W	1	1 1 1 0 1 0 k k k k k k k k		
LJUMP k	Go to address	2	1 0 1 k k k k k k k k k k k		
RTFI -	Return from interrupt	2	0 1 0 0 0 0 0 0 0 0 1 0 0 1		
RTIW k	Return with literal in W	2	1 1 0 0 0 1 k k k k k k k k		
RET -	Return from Subroutine	2	0 1 0 0 0 0 0 0 0 0 0 1 0 0		
SLEEP -	Go into Standby mode	1	0 1 0 0 0 0 0 0 0 0 0 0 1 0	/TF, /PF	
SUBWI k	Subtract W from literal	1	1 1 1 0 0 0 k k k k k k k k	C, DC, Z	
XORWI k	Exclusive OR W literal with W	1	1 1 0 1 1 0 k k k k k k k k	Z	

Notes:

[1]. When an I/O register is modified as a function of itself (e.g., MOVF PORTA, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

[2]. If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

[3]. If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

7.7.2 Instruction Descriptions

ADDWI	Add Literal and W
Syntax:	[label] ADDWI k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWR	Add W and f
Syntax:	[label] ADDWR f, d
Operands:	0 ≤ f ≤ 127 d∈[0, 1]
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ANDWI	AND Literal with W
Syntax:	[label] ANDWI k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWR	AND W with f
Syntax:	[label] ANDWR f, d
Operands:	0 ≤ f ≤ 127 d∈[0, 1]
Operation:	(W) .AND. (f) →(destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCR	Bit Clear f
Syntax:	[label] BCR f, b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSR	Bit Set f
Syntax:	[label] BSR f, b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTSS	Bit Test f, Skip if Set
Syntax:	[label] BTSS f, b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

BTSC	Bit Test, Skip if Clear
Syntax:	[label] BTSC f, b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

LCALL	LCall Subroutine
Syntax:	[label] LCALL k
Operands:	0 ≤ k ≤ 2047
Operation:	(PC)+ 1→TOS, K → PC<10:0>, (PCHLAT<4:3>) →PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCHLAT. LCALL is a two-cycle instruction.

CLRR	Clear f
Syntax:	[label] CLRR f
Operands:	0 ≤ f ≤ 127
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register ‘f’ are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWT	Clear Watchdog Timer
Syntax:	[label] CLRWT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → /TF 1 → /PF
Status Affected:	/TF, /PF
Description:	CLRWT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.

COMR	Complement f
Syntax:	[label] COMR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(/f) → (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are complemented. If ‘d’ is 0, the result is stored in W. If ‘d’ is 1, the result is stored back in register ‘f’.

DECR	Decrement f
Syntax:	[label] DECR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register ‘f’. If ‘d’ is 0, the result is stored in the W register. If ‘d’ is 1, the result is stored back in register ‘f’.

DECRSZ	Decrement f, Skip if 0
Syntax:	[label] DECRSZ f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) -1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are decremented. If ‘d’ is 0, the result is placed in the W register. If ‘d’ is 1, the result is placed back in register ‘f’. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2-cycle instruction.

LJUMP	Unconditional Branch
Syntax:	[label] LJUMP k
Operands:	0 ≤ f ≤ 127
Operation:	k → PC<10:0> PCHLAT<4:3> → PC<12:11>
Status Affected:	None
Description:	LJUMP is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCHLAT<4:3>. GOTO is a two-cycle instruction.

INCR	Increment f
Syntax:	[label] INCR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are incremented. If ‘d’ is 0, the result is placed in the W register. If ‘d’ is 1, the result is placed back in register ‘f’.

INCRSZ	Increment f, Skip if 0
Syntax:	[label] INCRSZ f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are incremented. If ‘d’ is 0, the result is placed in the W register. If ‘d’ is 1, the result is placed back in register ‘f’. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2-cycle instruction.

IORWI	Inclusive OR Literal with W
Syntax:	[label] IORWI k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR’ed with the eight-bit literal ‘k’. The result is placed in the W register.

IORWR	Inclusive OR W with f
Syntax:	[label] IORWR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register ‘f’. If ‘d’ is 0, the result is placed in the W register. If ‘d’ is 1, the result is placed back in register ‘f’.

LDR	Move f
Syntax:	[label] LDR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) → (destination)
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1is useful to test a file register, since status flag Z is affected.

LDWI	Move Literal to W
Syntax:	[label] LDWI k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal ‘k’ is loaded into W register. They don’t cares will assemble as 0’s.

STWR	Move W to f
Syntax:	[label] STWR f
Operands:	0 ≤ f ≤ 127
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from W register to register ‘f’.

NOP	No Operation
Syntax:	[label] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RTFI	Return from Interrupt
Syntax:	[label] RTFI
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from interrupt.

RTIW	Return with Literal in W
Syntax:	[label] RTIW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RLR	Rotate Left f through Carry
Syntax:	[label] RLR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the left through the Carry Flag. If ‘d’ is 0, the result is placed in the W register. If ‘d’ is 1, the result is stored back in register ‘f’.

RET	Return from Subroutine
Syntax:	[label] RET
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RRR	Rotate Right f through Carry
Syntax:	[label] RRR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the right through the Carry Flag. If ‘d’ is 0, the result is placed in the W register. If ‘d’ is 1, the result is placed back in register ‘f’.

SLEEP	
Syntax:	[label] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → /TF 0 → /PF
Status Affected:	/TF, /PF
Description:	The power-down Status bit, /PF is cleared. Time-out Status bit, /TF is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBWI	Subtract W from Literal
Syntax:	[label] SUBWI k
Operands:	0 ≤ k ≤ 255
Operation:	k - (W) → (W)
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2’s complement method) from the eight-bit literal ‘k’. The result is placed in the W register.

SUBWR	Subtract W from f
Syntax:	[label] SUBWR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) - (W) → destination
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

SWAPR	Swap Nibbles in f
Syntax:	[label] SWAPR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	f<3:0>→destination<7:4> f<7:4>→ destination<3:0>
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.

XORWI	Exclusive OR Literal with W
Syntax:	[label] XORWI k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .XOR. k → W
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWR	Exclusive OR W with f
Syntax:	[label] XORWR f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W).XOR.(f) → destination
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

8. Ordering Information

Table 27. CMT2189A Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2189A-ESR[1]	240 – 960 MHz SoC (G)FSK/OOK Transmitter	SOP14	Tape & Reel	2.3 to 3.6 V, -40 to 85 ℃	2,500
CMT2189A-ESB[1]	240 – 960 MHz SoC (G)FSK/OOK Transmitter	SOP14	Tube	2.3 to 3.6 V, -40 to 85 ℃	1,000

Notes:

[1]. "E" stands for extended industrial product grade, which supports the temperature range from -40 to +85 ℃.
"S" stands for the package type of SOP14.
"R" stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 2,500 pcs. "B" stands for the tube package option, with the MOQ of 1,000 pcs.
The default frequency for CMT2189A is 868.35 MHz, for the other settings, please refer to the Table 11 of Page 15.

Visit www.cmostek.com/products to know more about the product and product line.
Contact sales@cmostek.com or your local sales representatives for more information.

9. Package Outline

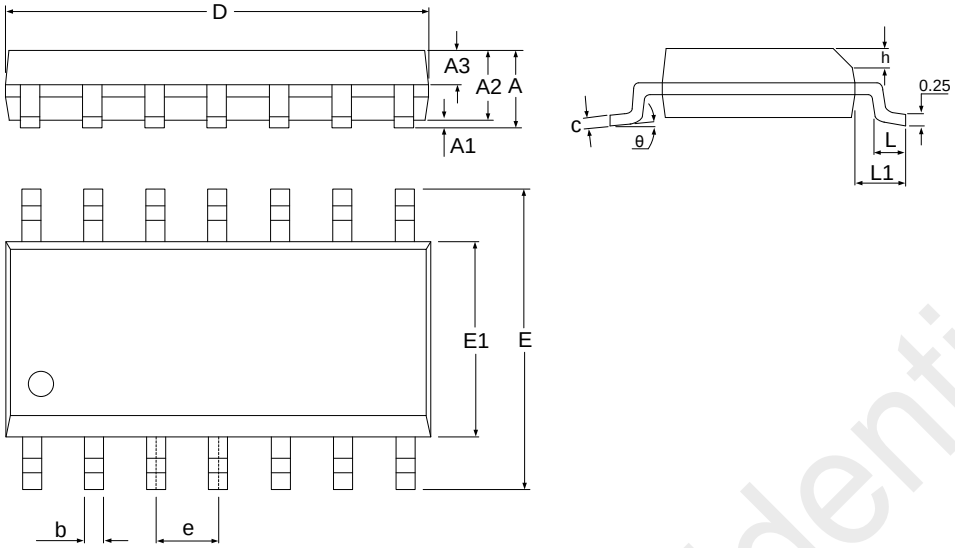


Figure 38. 14-Pin SOP Package

Table 28. 14-Pin SOP Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
C	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.30	-	0.60
L1	1.05 BSC		
θ	0	-	8°

10. Top Marking

10.1 CMT2189A Top Marking

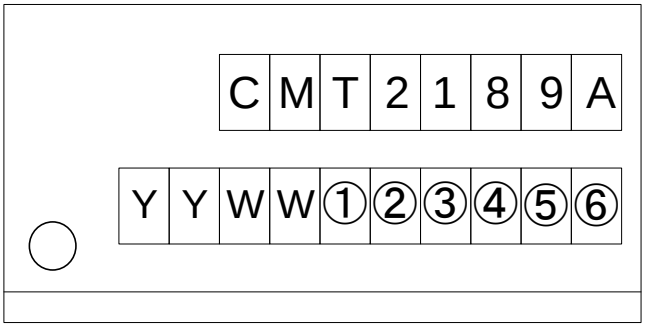


Figure 39. CMT2189A Top Marking

Table 29. CMT2189A Top Marking Explanation

Mark Method :	Laser
Pin 1 Mark :	Circle's diameter = 1 mm.
Font Size :	0.35 mm, right-justified.
Line 1 Marking :	CMT2189A represents part number CMT2189A
Line 2 Marking :	YYWW is the Date code assigned by the assembly house. YY represents the last two digits of the mold year and WW represents the workweek. ①②③④⑤⑥ is the internal tracking number.

11. Other Documentations

Table 30. Other Documentations for CMT2189A

Brief	Name	Descriptions
AN131	CMT218xA Schematic and PCB Layout Design Guideline	Details of CMT2180A, CMT2189A PCB schematic and layout design rules, RF matching network and other application layout design related issues.
AN132	CMT2180/89A Configuration Guideline	Details of configuring CMT2180/89A features on the RFPDK.

12. Document Change List

Table 31. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.6	All	Initial Released	

13. Contact Information

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