CMT2186A

210-960 MHz OOK/ASK Transmitter SoC

MCU characteristic

- CPU Kernel
  - High performance single instruction cycle 1T-8051 Kernel
  - Supports up to 26MHz (XOSC) or 24Mhz (HFOSC) operating frequency, with a maximum addressing efficiency of 20MIPS
  - Operating power consumption is 111uA/MHz
- Storage
  - 4-KB MTP Program storage, supports 10K Erase
  - 512-Byte XRAM and 256-Byte IRAM
  - 512-Bit EEPROM , supports 100 Thousands of times of erasure
- power supply
  - Power-on reset and low voltage detection
  - Built-in independent LDO Give CPU and digital circuit power supply
  - Built-in ultra-low power ULPLDO , in STOP Mode implementation Retention of CPU/RAM/SFR/ some peripherals Function
- I/O
  - 11 / 9 Multi-function IO Pinout (SOP16 / SOP14)
  - Supports highly flexible peripheral function mapping
  - Support level change interrupt / wake-up
- Clock Source
  - Support high speed 26MHz XOSC (Crystal Oscillator)
  - Built-in high speed 24MHz HFOSC (± 1% RC Oscillator)
  - Built-in low power 32kHz LFOSC (± 1% RC Oscillator)
- On-chip debugging
  - CPU Built-in 1-Wire Debugger Hardware Circuit
  - Support using Keil C51 Perform program online debugging
  - Support 3 Hardware breakpoints, single-step debugging
- Peripherals
  - 1x UART
  - 1x SPI
  - 1x CDR (Single Line RX Input clock recovery)
  - 1x WDT (independent hardware)
  - 1x Sleep Timer (32KHz LFOSC)
  - 2x 16 Simple timer
  - 2x 16 Bit Multi-Function Timer (3 Channel PWM/CCP)
  - 2x Analog Comparator
- Code Security
  - Burning serial port and single-line debugging interface

Sub-1G Transmitter module characteristics

- Operating frequency: 210 - 960MHz
- Debug mode: OOK / ASK
- Data Rate: 0.5–40kbps (OOK)
- Output power: +13dBm (Max.)
- Working current: 24mA @+13dBm , 433.92MHz CW
- Single-ended high efficiency Class E High frequency transmitting PA
- PA Ramping Slope is variable depending on rate

Working conditions

- -40 To85 ℃ temperature range
- 1.8 to3.6V Operating voltage range

application

- Garage door remote control
- Remote access control system
- Consumer wireless remote control
- Smart Home
- Home Security
- Active RFID Label
- Wireless Sensor Networks
- WM-Bus T1 model

Ordering Information

model	Encapsulation	MOQ
CMT2186A-ESR16	SOP16, T&R	3,000 pcs
CMT2186A-ESR14	SOP14, T&R	3,000 pcs

SOP- 14

8.65 x 6 x 1.75 mm

SOP- 16

9.9 x 6 x 1.75 mm

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Introduction

CMT2186A It is an embedded enhanced 1T-8051 Low power consumption of the core Sub-1G Wireless transmitter SoC , supports 210 ~ 960 MHz , OOK / ASK Modulation modulation wireless transmission function. The chip has a built-in efficient single-ended PA with an adjustable output power range of 0 ~ +13dBm , +13dBm Only 24mA is required when transmitting . MCU Program in 4 KB MTP The ultra-low power ULPLDO Support chip in STOP Mode Save CPU Status, RAM data, and configuration register data. Users can use the dedicated 1-WIRE Debugger and KEIL51 Software, download the target debugging code directly to MTP Run in MTP for online simulation. There is a dedicated area for burning 64 1-bit serial number (ID) , very suitable for remote control or active RFID where the transmitted information needs to be encrypted The chip supports switching of main frequency clock source, and the system uses the built-in 24MHz by default . HFOSC starts, and according to the MTP burning configuration, it is optional to switch to a more accurate external 26MHz XOSC As the system main frequency clock source. Built-in low power RC The 32kHz LFOSC oscillator allows the MCU Perform low power consumption timer wake-up. HFOSC andLFOSC Calibrated at the factory to achieve an accuracy of ± 1% , and can also be adjusted during user use by calling the API The function accesses the correction circuit module for correction.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

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1 Electrical Characteristics

Unless otherwise stated, all electrical performance parameters are obtained by using the evaluation board CMT2186A - EM Rev 00 1 and tested under the following conditions: VDD = 3.3V , TOP = 25° C , FRF = 433.92MHz , matched to 50Ω impedance antenna, output +10dBm power.

1.1 Recommended operating conditions

Table1-1 . Recommended operating conditions

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
Operating digital supply voltage	V DVDD	Temperature range -40 ° C to +85 ° C	1.8		3.6	V
Operating RF power supply voltage	V AVDD	Temperature range -40 ° C to +85 ° C	1.8		3.6	V
System main clock frequency	fSYSCLK			twenty four	26	MHz
Operating temperature	T OP		- 40		+ 85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Ratings

Table1-2 . Absolute Maximum Ratings [1]

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
DVDD Supply voltage	V DVDDMAX		- 0.3		3.6	V
AVDD Supply voltage	V AVDDMAX		- 0.3		3.6	V
Interface voltage	V PIN		- 0.3		VDD +0.3	V
Junction temperature	T JMAX		- 40		125	℃
Storage temperature	T S		- 50		150	℃
Soldering temperature	T SDR	Lasts at least 30 Second			255	℃
ESD Level [2]	V ESD	Human Body Model (HBM)	- 2		2	kV
Latch-up Current	I LATCH	@ 85 ℃	- 100		100	mA
Each I/O Input Current	I IOMAX	Source		3.0		mA
		Sink		3.7		mA

Remark:

1. Exceeding the " Absolute Maximum Ratings " may cause permanent damage to the device. This value is a stress rating and does not mean that the device functions are affected under this stress condition, but exposure to the absolute maximum rating conditions for a long time may affect the device reliability.
2. CMT2186A It is a high-performance RF integrated circuit. Please pay attention to ESD when operating and assembling this chip. protection.

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1.3 Reset and supply voltage detection

Table1-3 . Supply voltage detection characteristics

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
POR Power-on release delay	t RST	V VDD > V POR , Supply voltage <100 us Rising to V POR		10		us
POR power-on release voltage threshold	V POR	VDD Voltage rise		1.8		V
BOR Reset voltage threshold	V BOR		1.64			V
LBD voltage detection range	V LBD	The step is 200mV	1.45		4.45	V
Battery Sensor Circuit Settling Time	t STAB			5		us
RSTn Pin reset delay	RST			5		ns
Remark : 1. The indicator is based on the average of two measurements .						

1.4 Wake-up time

Table1-4 . Wake-up time

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
IDLE Mode wake-up time	t IDLEWK	The main frequency is 24MHz HFOSC	2		3	SYSCLKs
STOP Mode wake-up time	t STOPWK	The main frequency is 24MHz HFOSC		180		us
Remark : 1. STOP This mode is equivalent to sleep mode, and the wake-up time is mainly consumed in starting the internal power supply and clock.						

1.5 Transmitter module specifications

Table1-5 . Transmitter specifications

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
Frequency range	F RF	HkDJ Access to 26MHz crystal oscillator	210		480	MHz
			630		960	MHz
Data rate	DR	OOK	0.5		40	kbps
Output power range	P OUT	Single- ended PA model	0		+13	dBm
Output power step	P STEP			1		dB
Transmitter lock time [1] (Startup time)	T PLL	API Function tx_sym_prepare_for_transmission Execution time		620		uS
OOK Emission current [3]	IDD - 434O	0dBm		6.5		mA
		+5dBm		7.2		mA

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parameter	symbol	Test conditions	Minimum	typical	maximum	unit
		+7dBm		7.8		mA
		+10dBm		8.5		mA
		+13dBm		12.0		mA
	IDD - 868O	0dBm		8.1		mA
		+5dBm		12.1		mA
		+7dBm		12.5		mA
		+10dBm		15.8		mA
		+13dBm		23.6		mA
Phase Noise	PN 434	100kHz Frequency offset		80		dBc/Hz
		200kHz Frequency offset		82		dBc/Hz
		400kHz Frequency offset		97		dBc/Hz
		600kHz Frequency offset		100		dBc/Hz
		1.2MHz Frequency offset		105		dBc/Hz
	PN 868	100kHz Frequency offset		72		dBc/Hz
		200kHz Frequency offset		77		dBc/Hz
		400kHz Frequency offset		91		dBc/Hz
		600kHz Frequency offset		93		dBc/Hz
		1.2MHz Frequency offset		98		dBc/Hz
Harmonic output	H2 315	2 Subharmonic @630MHz , +13dBm		< - 45		dBm
	H3 315	3 Subharmonic @945MHz , +13dBm		< - 45		dBm
	H2 434	2 Subharmonic @868MHz , +13dBm		< - 45		dBm
	H3 434	3 Subharmonic @1302MHz , +13dBm		< - 45		dBm
	H2 868	2 Subharmonic @1736MHz , +13dBm		< - 36		dBm
	H3 868	3 Subharmonic @2604MHz , +13dBm		< - 36		dBm
	H2 915	2 Subharmonic @1830MHz , +13dBm		< - 36		dBm
	H3 915	3 Subharmonic @2745MHz , +13dBm		< - 36		dBm
OOK Adjusting the extinction ratio				60		dB
Bandwidth occupied	OBW 315	-20dBc Bandwidth, RBW = 1kHz , SR = 1.2kbps		6		kHz
	OBW 434	-20dBc Bandwidth. RBW = 1kHz , SR = 1.2kbps		7		kHz

Remark:

[1] This item already includes the crystal startup time.

[2] . Including 8051 Core Current, HFOSC Using internal 24MHz High-speed RC as a clock source.

[3] Baseband data 50% high and low duty cycle.

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1.6 Oscillator

Table1-6 . Oscillator specifications

type	parameter	symbol	Test conditions	Minimum	typical	maximum	parameter
High frequency crystal oscillator XOSC	Crystal frequency [1]	F			26		MHz
	Frequency accuracy [2]				±20		ppm
	Load Capacitance	C HX- LOAD			15		pF
	Equivalent resistance	R HX- ESR				60	Ω
	Startup time [3]	tHX			400		us
Internal high frequency RC oscillator HFOSC	RC Oscillation frequency	F HF_RC		3	twenty four	twenty four	MHz
	Frequency accuracy [4]				1		%
Internal 32KHz RC Oscillator LFOSC	Oscillator frequency	F LP_RC			32		kHz
	Frequency accuracy [4]				1		%

Remark :

[1] . CMT2186A The XTAL can be driven directly by an external reference clock through a coupling capacitor The pin works. The peak-to-peak value of the external clock signal is required to be between 0.3 and 0.7V .

[2] This value includes initial error, crystal loading, aging and changes with temperature. The acceptable crystal frequency error is limited by the bandwidth of the receiver and the RF frequency deviation between the transmitter and receiver.

[3] . This parameter is largely crystal dependent.

[4]. Frequency accuracy is a calibrated indicator and is related to environmental factors. Users can actively call relevant calibration API functions for active calibration.

1.7 MTP characteristic

Table1-7 . MTP Specification

parameter	symbol	Test conditions	Minimum	typical	maximum	parameter
Burning voltage	V PROG		3.0		3.6	V
Burning time	T PROG	1 Word(4 bytes) , the clock is 24MHz	20.8		37.5	us
Erase Time	T ERASE	1 Page, clock is 24MHz	10.4		18.8	ms
Reading time	T READ	1 Word (4 bytes) , the clock is 24MHz 2.0V ≤ DVDD < 2.4V		41.7		ns
		1 Word (4 bytes) , the clock is 24MHz 2.4V ≤ DVDD < 3.6V		125		ns
Maximum number of erase times	EC MTP		10K			cycles
Data retention period	RET MTP	@+ 85 ℃		10		years

Remark:

1. MTP The program space capacity is 1K x 32 , 24 MHz The maximum throughput under the clock is 96MByte/S . The chip integrates the instruction cache circuit, which stores 32 bits of the current address after each read. Convert the bit contents to 4 Article 8 The instructions are sent to 8051 step by step. Kernel, the actual addressing efficiency depends on the cache hit rate and the program code itself, which is about 20MIPS .

2. The chip will detect DVDD in real time Voltage, when lower than 2.4V When, as the current MCU Clock (for MTP addressing) is greater than or equal to 8MHz , it will automatically

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parameter	symbol	Test conditions	Minimum	typical	maximum	parameter
Automatically reduce MTP The reading time of this function does not require user intervention, and its effect is lower than 2.4V Post-MCU The execution efficiency will be reduced.						

1.8 EEPROM characteristic

Table1-8 . EEPROM Specification

parameter	symbol	Test conditions	Minimum	typical	maximum	parameter
Erase time	**tEE** - WR	Calling eeprom_write_words Operation [1]		14		ms/unit
		Call eeprom_set_dec_count Operation [2]		42		ms
Burn times		Calling eeprom_write_words Operation [1]	10,000	100,000		cycles
		Call eeprom_set_dec_count Operation [2]		1,000,000		cycles
Remark : [1] Internal EEPROM Through eeprom_write_words (API Function) performs erase operation in direct erase mode, and the operation address points to 2 Bytes Storage unit, that is, each unit For 2 Bytes ; [2] Internal EEPROM Through eeprom_set_dec_count (API To enhance the erase mode, the operation process adds a " balanced Gray code " algorithm to ensure that the storage field of the operation can support 1,000,000 The above erase and write operations. It should be noted that this function fixedly operates 3 units , that is, the field Occupancy 6 Bytes , and the write value and read value are only 22 lower bits The data is valid.						

1.9 Comparator Characteristics

Table1-9 . Comparator characteristics

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
Operating voltage	VDD		1.8	3.0	3.6	V
Working current	I COMP			75		μA
Input voltage range	V in_range		0		Vdd	
Input offset voltage	V OS			1.4	4.2	mV
Hysteresis	V HYST			0		mV
Response time	T Delay_RISE	Output low to high		<1		us
	T Delay_FALL	Output high to low		<1		us
Common Mode Rejection Ratio			55			dB
Remark:						

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1.10 DC Characteristics

Table1-10 . DC characteristics @3.3V , 25 ℃

parameter	symbol	Test conditions	Minimum	typical	maximum	unit
Normal model	I NORMAL	Main frequency = 26 MHz , XOSC		97		uA/MHz
		Main frequency = 24 MHz , HFOSC		111		uA/MHz
		Main frequency = 3.25 MHz , XOSC		460		uA/MHz
		Main frequency = 3 MHz , HFOSC		568		uA/MHz
IDLE model	I IDLE	Main frequency = 26 MHz , XOSC		75		uA/MHz
		Main frequency = 24 MHz , HFOSC		89		uA/MHz
		Main frequency = 3.25 MHz , XOSC		426		uA/MHz
		Main frequency = 3 MHz , HFOSC		534		uA/MHz
STOP model	I STOP	Turn on the sleep timer and LFOSC		2.2		uA
SDN model	I SDN			0.8		uA
Remark: [1] . The test program runs the While (1) loop, GPIO Without any load.						

1.11 AC Characteristics

Table1-12 . AC characteristics

parameter	symbol	Test conditions	Minimum	Typical Value	Maximum	unit
High level output	V	Load1KΩ , VDD = 3.3V	VDD -0.4			V
Low level output	V OL	Load1KΩ , VDD = 3.3V			0.4	V
High level input	V I	VDD = 3.3V		0.7*VDD		V
		VDD = 2.0V		0.7*VDD		V
Low level input	V I L	VDD = 3.3V		0.2*VDD		V
		VDD = 2.0V		0.2*VDD		V
Port leakage current	I LKG	VDD = 2.0V – 3.6V		TBD		nA
Remark:						

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1.12 Typical performance of high frequency transmission

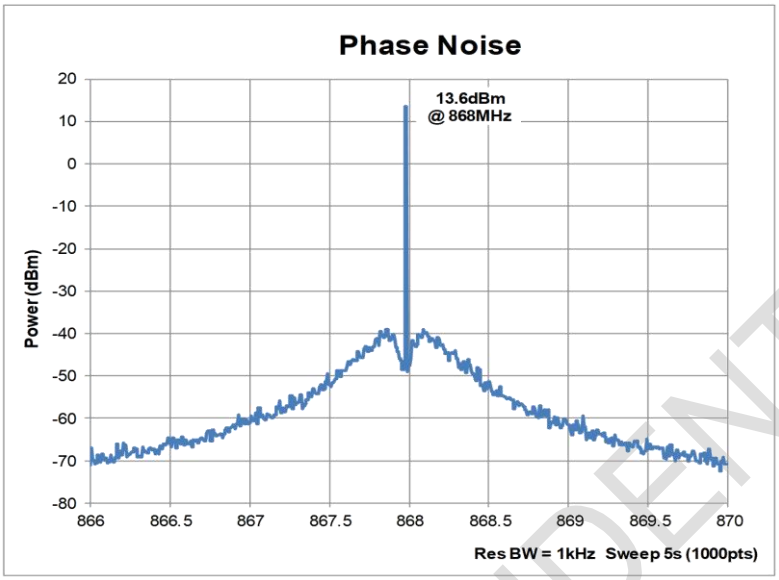

Figure1-1 . Phase noise F RF = 868MHz, P OUT = +13dBm, Unmodulated

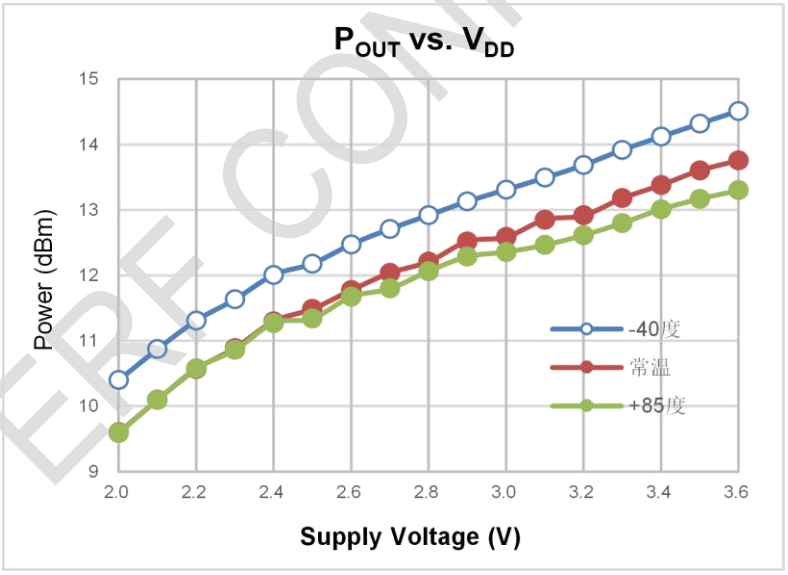

Figure1-2. Output power versus power supply voltage
F RF = 433.92MHz, POUT = +13dBm

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2 Pin Description

2.1 CMT2186A-ESR16 Pin Definition

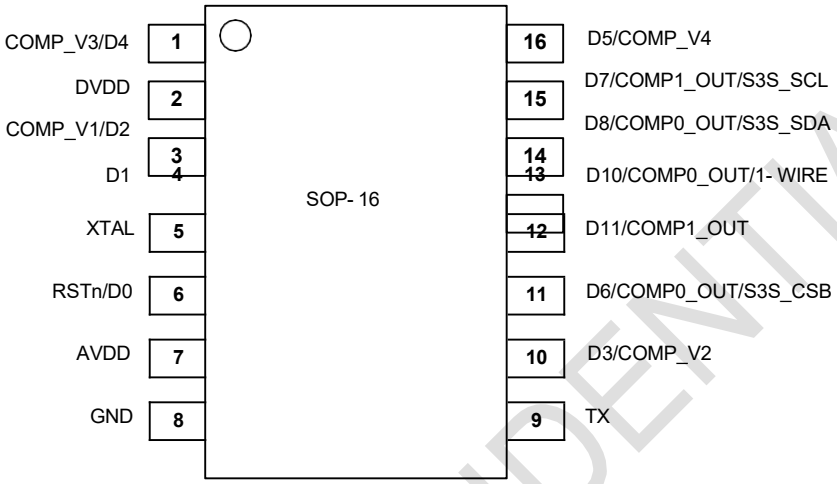

Figure 2-1. CMT2186A-ESR 16 Pin Assignment Table

2-1 . CMT2186-ESR16 Package Pin Description

管脚	名称	管脚属性		功能说明
1	COMP_V3 / D4	IO	D4	GPIO4，通用 GPIO 之一
		A	COMP_V3	模拟比较器输入源 V3
2	DVDD	A		数字和部分模拟电路电源供电输入
3	COMP_V1/ D2	IO	D2	GPIO2，通用 GPIO 之一
		A	COMP_V1	模拟比较器输入源 V1
4	D1	IO		GPIO1，通用 GPIO 之一
5	XTAL	A		晶体输入脚，连接 26MHz 晶体到 GND
6	RSTn/D0	IO	D0	GPIO0，通用 GPIO 之一
		IO	RSTn	全局复位输入，低有效
7	AVDD	A		模拟射频电源供电输入
8	GND	A		电源地
9	TX	A		单端 PA 射频输出
10	COMP_V2 / D3	IO	D3	GPIO3，通用 GPIO 之一
		A	COMP_V2	模拟比较器输入源 V2
11	D6/COMP0_OUT/S3S_CSB	IO	D6	GPIO6，通用 GPIO 之一
		A	COMP0_OUT	比较器 0 的输出
		IO	S3S_CSB	S3S 烧录接口的 CSB 片选输入
12	D11/COMP1_OUT	IO	D11	GPIO11，通用 GPIO 之一
		A	COMP1_OUT	比较器 1 的输出

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Pins	name	Pin properties		Functional Description
13	D10/COMP0_OUT/1- WIRE	IO	D10	GPIO10 , general purpose GPIO one
		A	COMP0_OUT	Comparator 0 Output
		IO	1- WIRE	Chip single-line debugging line
14	D8/COMP0_OUT/S3S_SDA	IO	D8	GPIO8 , one of the general GPIOs
		A	COMP0_OUT	Comparator 0 Output
		IO	S3S_SDA	S3S SDA data input / output of the burning interface
15	D7/COMP1_OUT/S3S_SCL	IO	D7	GPIO7 , one of the general GPIOs
		A	COMP1_OUT	Comparator 1 Output
		IO	S3S_SCL	SCL of S3S programming interface Clock Input
16	D5 / COMP_V4	IO	D5	GPIO5 , one of the general GPIOs
		A	COMP_V4	Analog comparator input source V4
Note: S3S This is a dedicated interface for burning. The burner needs to connect to the chip through this interface.				

2.2 SOP-14 Package pin definition

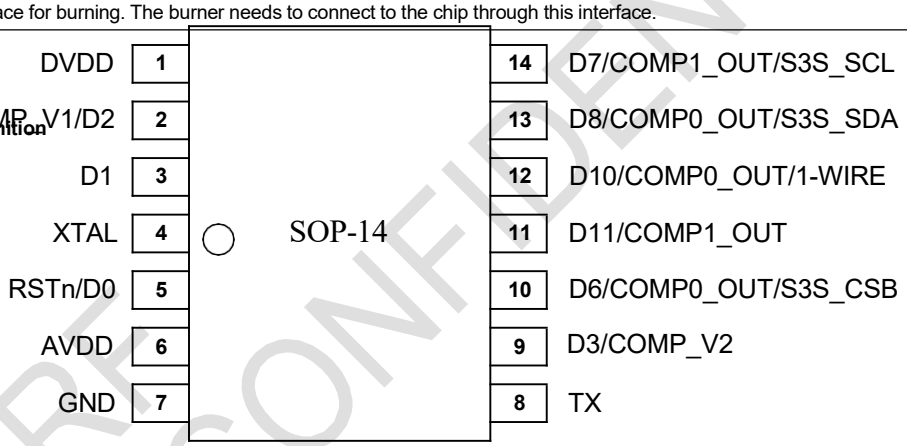

Figure 2-2. CMT2186A-ESR14 pin arrangement Table

2-2 . CMT2186A-ESR14 Package Pin Description

Pins	name	Pin properties		Functional Description
1	DVDD	A		Power supply input for digital and some analog circuits
2	COMP_V1/D2	IO	D2	GPIO2 , one of the general GPIOs
		A	COMP0_N	Comparator 0 Negative input
3	D1	IO		GPIO1 , one of the general GPIOs
4	XTAL	A		Crystal input pin, connect 26MHz Crystal to GND
5	RSTn/D0	IO	D0	GPIO0 , one of the general GPIOs
		IO	RSTn	Global reset input, active low

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Pins	name	Pin properties		Functional Description
6	AVDD	A		Analog RF power supply input
7	GND	A		Power Ground
8	TX	A		Single-ended PA RF Output
9	COMP_V2/D3	IO	D3	GPIO3 , one of the general GPIOs
		A	COMP0_P	Comparator 0 Positive input
10	D6/COMP0_OUT/S3S_CSB	IO	D6	GPIO6 , one of the general GPIOs
		A	COMP0_OUT	Comparator 0 Output
		IO	S3S_CSB	CSB chip select input of S3S programming interface
11	D11/COMP1_OUT	IO	D11	GPIO11 , general purpose GPIO one
		A	COMP1_OUT	Comparator 1 Output
12	D10/COMP0_OUT/1- WIRE	IO	D10	GPIO10 , general purpose GPIO one
		A	COMP0_OUT	Comparator 0 Output
		IO	1- WIRE	Chip single-line debugging line
13	D8/COMP0_OUT/S3S_SDA	IO	D8	GPIO8 , one of the general GPIOs
		A	COMP0_OUT	Comparator 0 Output
		IO	S3S_SDA	S3S SDA data input / output of the burning interface
14	D7/COMP1_OUT/S3S_SCL	IO	D7	GPIO7 , one of the general GPIOs
		A	COMP1_OUT	Comparator 1 Output
		IO	S3S_SCL	SCL of S3S programming interface Clock Input
Note: S3S This is a dedicated interface for burning. The burner needs to connect to the chip through this interface.				

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3 Typical reference design

3.1 Sub-1G Single-ended PA Output reference design

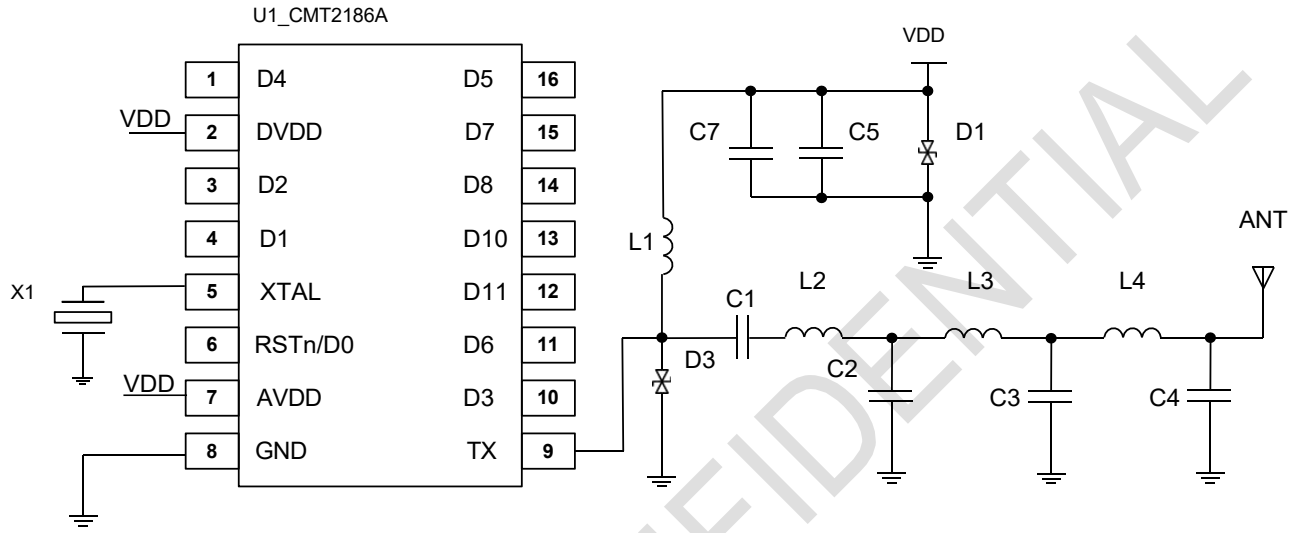

Figure 3-1. CMT2186A single-ended PA output reference

schematic Figure 3-1. CMT2186A Single-ended PA Output matches

reference BOM

Label	illustrate	315MHz	434MHz	868MHz	915MHz	unit	supplier
U1	CMT2186A	- -				-	CMOSTEK
X1	±20 ppm, SMD3225 mm, Crystal	26				MHz	EPSON
L1	±10 %, 0603 Multilayer Inductor	220	180	100	100	nH	Sunlord LQG18
L2	±10 %, 0603 Multilayer Inductor	75	39	12	10	nH	Sunlord LQG18
L3	±10 %, 0603 Multilayer Inductor	75	39	10	5.6	nH	Sunlord LQG18
L4	±10 %, 0603 Multilayer Inductor	56	47	8.2	8.2	nH	Sunlord LQG18
C1	±0.25 pF, 0402 NP0, 50 V	33	15	4.7	4.7	pF	-
C2	±0.25 pF, 0402 NP0, 50 V	3.6	5.6	5.6	4.3	pF	-
C3	±0.25 pF, 0402 NP0, 50 V	5.6	4.7	2.2	2.2	pF	-
C4	±20%, 0402, NP0, 50 V	NC	3.3	NC	NC	pF	-
C5	±20%, 0402 X7R, 25 V	100				nF	
C7	±20%, 0402 X7R, 25 V	470				pF	
D1	XE5D5VB , ESD Protection diode						
D3	XE5D5VB , ESD Protection diode						

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4 Function Introduction

CMT2186A Is a built-in Sub-1GHz OOK / ASK Transmitter high performance 8051 SoC , user program burned in 4K Bytes MTP and can run at up to 26MHz The chip is suitable for the frequency band 210 ~ 960MHz Low-power wireless transmission applications, which integrate the following core modules:

- MTP- based High-performance 8051 with 1-Wire Online debugging circuit;
- Rich digital and analog peripheral resources;
- Sub-1G OOK / ASK Modulation transmission module;

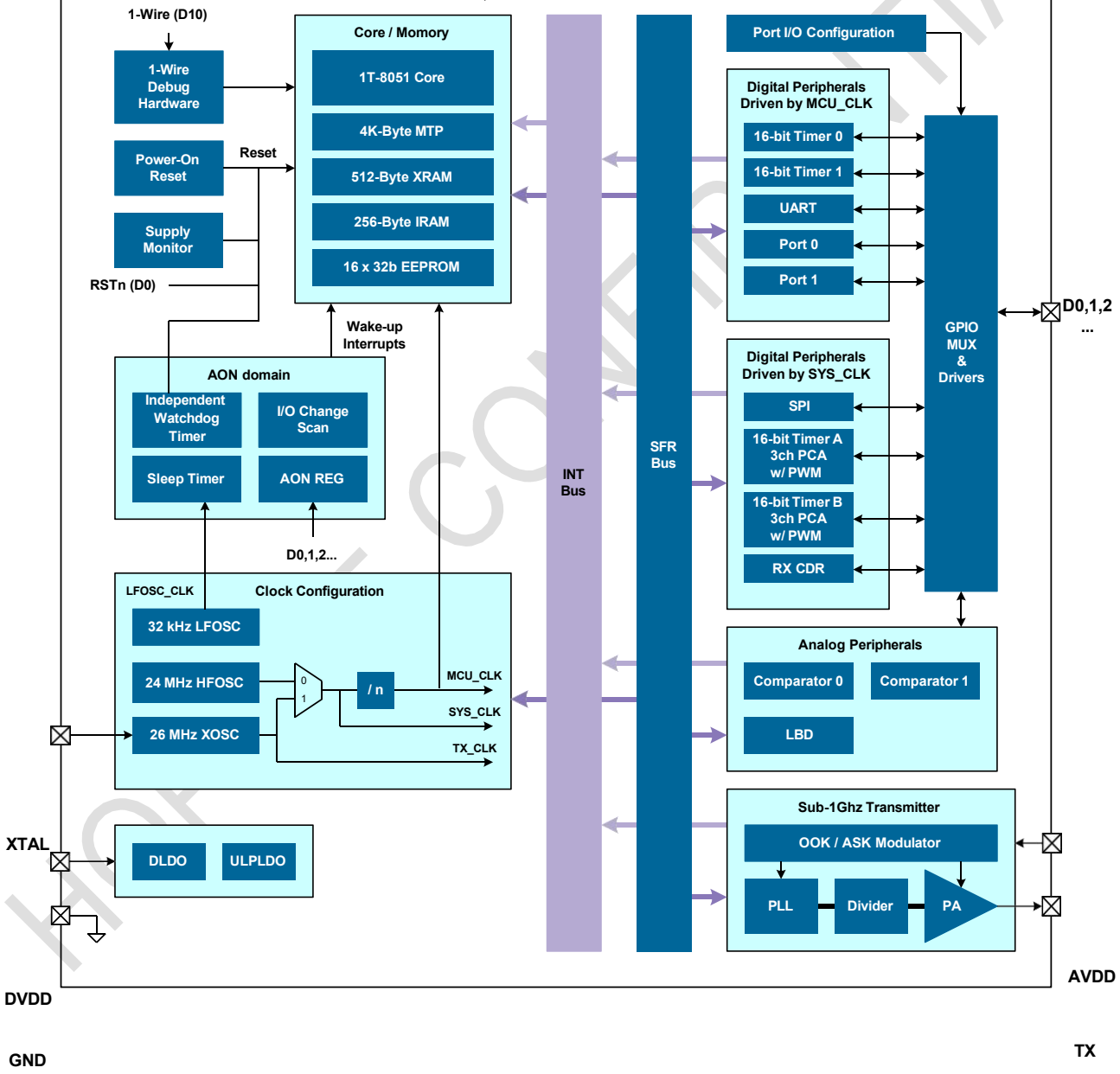

Figure4-1 . System Block Diagram

(Note: *D0* , *1* , *2* in this diagram generally refers to *GPIO* , *GPIO* The quantity varies according to the package.)

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4.1 High performance 1T- 8051

CMT2186A Embedded enhanced 1T-8051 , single cycle operation instruction, fully compatible with MCS-51 Instruction set, addressing efficiency can reach up to 20 MIPS

The CPU has a built-in 1 -Wire interface online debugging hardware module, which can be connected to the PCKeil debugger through the debugger C51 software for online debugging.

4.2 Storage

The chip has an MTP (non-volatile storage) for storing user code. The code is directly stored in the MTP MTP Support 10K Repeated erasing and burning. User code space is 4K Byte , address range is 0x0000 - 0x0FFF . MTP There is an independent block of size 512 Byte , specially used for burning chip configuration and ID The area is only accessible by the chip programmer and cannot be accessed by the user program. The programmed 64- Byte ID will be copied to the SFR register in the Always-ON area when the power is turned on .

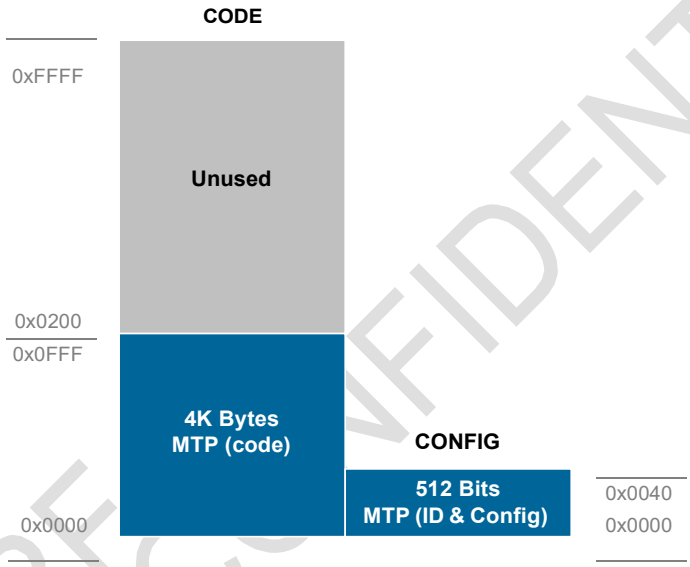

Figure4-2 . MTP Address Map

There are 256 Bytes IRAM As internal data storage, there are 2 Page of SFRs As registers for configuring and controlling chip operation . SFR The page switching is done by accessing SFR Address 0xFF Bit 0 There are 512 Bytes XRAM As data storage, the address range is 0x0000 - 0x01FF .

AON SFR is not directly mapped to the address range in the figure below. Users can access AON SFR indirectly by operating SFR Page 0 orPage 1 AON_ADDR, AON_WDATA , AON_RDATA This is done using three port registers.

The film also provides 512 bits EEPROM As important data power-off storage, users can use SFR Register access, erase and write times are 100

If the user wants to increase the erase and write times to 300 Ten thousand times, relevant APIs can be called For details , please refer to AN .

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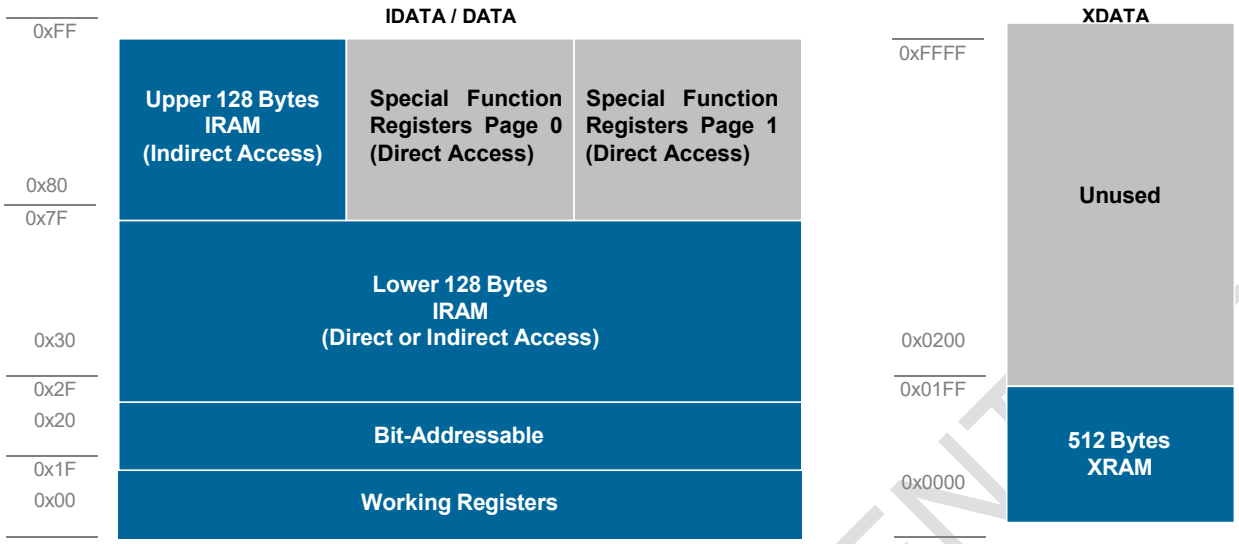

Figure4-3 . IRAM , SFR andXRAM Address map of

4.3 Working Mode

CMT 2 1 86 A have2 A power supply pin, AVD D Responsible for supplying power to the internal RF circuit, D V D D Responsible forA l w ays - On The digital modules and analog modules other than RF are powered. Most of the digital modules work on the built-inD L DO Next, inS T O P You can switch toU L P L DO The MCU can be powered up to achieve low leakage retention mode . For digital and analog peripherals, users can shut them down when not in use and independently shut down the clock gating of peripherals to save more power.

Table4-1 . CMT2186A Working Mode

Working Mode	Detailed Description	Entry method	Wake-up source
Normal	Normal working status	Automatically enter after power on after user program is burned	none
IDLE	● DLDO Open ● System clock (HFOSC orXOSC) to turn on ● CPU Nuclear Pause ● Peripheral work	Setting up PCON IDLE in the register Bit	I/O Level Change Comparator Output
STOP (Retention)	● ULPLDO Open ● System clock (HFOSC orXOSC) off ● CPU Core, all storage, and peripheral configuration and state preservation ● LFOSC Always- On Module and Comparator Operation ● GPIO Status remains unchanged	1. Setthe STOP bit in the PCON register 2. Setting AON_SFR_03 In the register SLEEP Bit	I/O Level Change Comparator output toggles when sleep timer times out

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Working Mode	Detailed Description	Entry method	Wake-up source
SDN	● ULPLDO closure ● System clock (HFOSC orXOSC) off ● CPU The core, all memory, and peripheral state and configuration are lost ● LFOSC Off, Always-On Module and comparator off ● GPIO Status remains unchanged	1. Setting AON_SFR_04 In the register PD_LFOSC bitturns offLFOSC 2. Setting HV_SFR_02 In the register TIMER_SLEEP_EN Turn off the sleep timer 3. SettingupPCON STOP Bit 4. SettingAON_SFR_03 SLEEP Bit	Power-On Reset RSTn Pin reset

4.4 STOP Retention inmodeFunction

ultra-low power ULPLDO is integrated in the chip . Enter STOP In the Retention mode, a stable voltage is provided to save the working state of the chip, which is called Retention Function. Retention Mode allows the chip to be in STOP After waking up, it can immediately resume work from the previous state without having to re-execute the program. mode, all RAM All data is saved; MTP andEEPROM The data can be saved when power is off.

Table4-2 . CMT2186A AtSTOP Storage content saved in mode

Storage Name	Save data	Power supply
MTP	√	Power off save
EEPROM	√	Power off save
IRAM	√	ULPLDO
XRAM	√	ULPLDO

In Retention In this mode, the power-on reset (POR) and real-time voltage monitoring (Power The following lists whether all functional modules save SFR Configuration and working status, whether it can work, and its corresponding power supply method. For modules that only save the configuration and lose the working status , the chip switches from STOP to After waking up, the user does not need to reconfigure the SFR of the module , the module will start working from the beginning, and the behavior is similar to the module being automatically reset.

Table4-3 . CMT2186A AtSTOP Save the content of each functional module

Module Name	Save Configuration	Save work status	Can I work?	Power supply
Watch Dog Timer	√	√	√	DVDD
Sleep Timer	√	√	√	DVDD
Key Scan	√	√	√	DVDD
Comparator 0	√	√	√	DVDD
Comparator 1	√	√	√	DVDD
UID & CFG register	√	√	×	DVDD
IO Configuration and Status	√	√	×	DVDD

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Module Name	Save Configuration	Save work status	Can I work?	Power supply
1T-8051 Kernel	√	√	×	ULPLDO
Timer 0	√	√	×	ULPLDO
Timer 1	√	√	×	ULPLDO
UART	√	√	×	ULPLDO
Port 0	√	√	×	ULPLDO
Port 1	√	√	×	ULPLDO
SPI	√	×	×	ULPLDO
Timer A	√	×	×	ULPLDO
Timer B	√	×	×	ULPLDO
CDR	√	×	×	ULPLDO
Sub-1G Transmitter	√	×	×	ULPLDO
LBD	√	×	×	Power outage
1-Wire Debug	×	×	×	Power outage

4.5 I/O

Table2-1 and Table 2-2 list the function mapping of all I/Os of CMT2186A . The external reset pin RSTn is multiplexed withD0 . Users can set AON_SFR_07 TheRST_IN_EN bit of the register is set to 0 to shield the external reset. All GPIOs have2 levels of drive capability that can be configured uniformly. Each GPIO can be mapped to Port0 , Port1 , or multiple digital peripherals. For details, please refer to the user manual.

For burning MTP S3S interface, and 1-Wire for in-circuit debugging interface, only on chip after power-on reset is released 6 ms effective within 6 ms If S3S is detected The command will enter MTP Burn mode; if 1-Wire is detected If the debug start command is received , the chip will enter the online debug mode; if no command is detected, the chip will enter the normal working mode. After the mode, all I/O The status before entering STOP mode will be maintained and remain unchanged.

4.6 clock

The system supports switching the main frequency clock source, and the built-in 24MHz is used by default. HFOSC Start, according to MTP The programming configuration can choose whether to switch to a more accurate external 26MHz XOSC As the system main frequency clock source. Built-in low power RC Oscillator 32kHz LFOSC Allows MCU Perform low power consumption timed wake-up.

HFOSC TheLFOSCand LFOSC are calibrated at the factory to achieve an accuracy of ± 1% . During use, users can also access the calibration circuit module by calling the API function . Each peripheral has an independent clock gating. When the relevant peripheral is not in use, the user can configure the SFR to turn off clock gating to further save power.

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4.7 Reset Source

Chip reset can restore the entire system to its initial state, restart and calibrate internal modules, and the program will be Address 0x0000 Restart execution. CMT2186A supports the following 4 reset sources:

- Power-On Reset (POR)
- External pin reset RSTn
- VDD power supply monitor reset
- Watchdog reset

4.8 Digital and analog peripherals

In terms of digital peripherals, the chip provides one UART , one SPI , an independent watchdog, a sleep timer, two 16 Bit simple timer, two 16 bit multi-function timer (supports 3 Capture / Comparator and PWM output)and one for single-bit I/O Input (usually the demodulated signal of a wireless receiver) for clock recovery CDR . Analog peripherals include 2 The MCU also includes an independent comparator and a low voltage detection (LBD) module , which is used to compensate the power of wireless transmission.

4.9 Sub-1G Single transmitter

CMT2186A Integrated high-performance Sub-1G Single transmitter, using high efficiency single-ended Class E- frame PA , the transmit power can reach +13dBm , and the current consumption is only 24mA . The transmitter supports OOK / ASK Modulation mode, and using fractional frequency phase-locked loop technology, only 1 external 26MHz Crystal oscillator can cover most of the commonly used frequency bands from 210 to 960MHz .

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5 Ordering Information

Table5-1 . CMT2186A Ordering Information

Product Model	describe	Encapsulation	Package	Operating conditions	Minimum Order Quantity (integer multiple)
CMT2186A-ESR16	210-960MHz Transmitter SoC	SOP16	T&R	1.8 to 3.6V -40 to 85 ℃	3,000
CMT2186A-ESR14	210-960MHz Transmitter SoC	SOP14	T&R	1.8 to 3.6V -40 to 85 ℃	3,000

Remark :

"E " stands for extended industrial product grade, which supports the temperature range from -40 to +85 ℃.

“S” stands for SOP Package type.

"R" stands for Tape and Reel type, the minimum order quantity (MOQ) is3,000 piece.

For more information on our products and product lines, please visit www.hoperf.cn .

For purchase or price inquiries, please contact sales@hoperf.com or your local sales representative.

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6 Package Outline

6.1 CMT2186A-ESR14 Encapsulation

CMT2186A-ESR14 The packaging information is shown in the figure and table below.

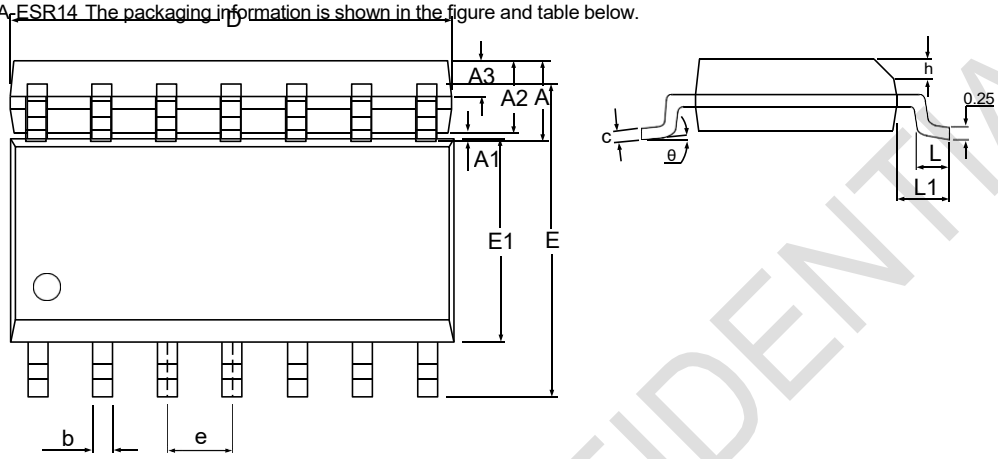

Figure6-1 . SOP14 Package size chart

6-1. SOP14 package size

symbol	Dimensions (mm)		
	Minimum	Typical Value	Maximum
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.30	-	0.60
L1	1.05 BSC		
θ	0	-	8°

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6.2 CMT2186A-ESR16 Encapsulation

CMT2186A-ESR16 The packaging information is shown in the figure and table below.

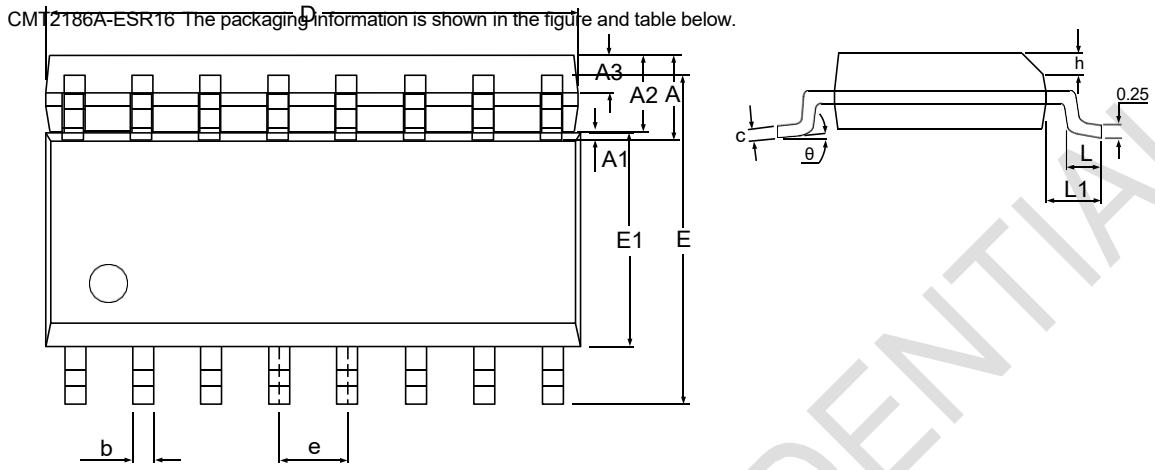

Figure6-2 . SOP16 Package size chart

6-2. SOP16 package size

conform to	Dimensions (mm)		
	Minimum	Typical Value	Maximum
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
C	0.21	-	0.26
d	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSc		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 BSC		
θ	0	-	8°

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7 Top screen printing

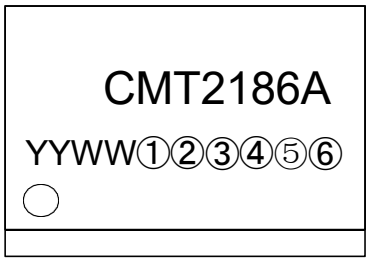

Figure7-1 . CMT2186A Top screen printing

Table7-1 . CMT2186A Top screen printing instructions

Silk screen printing method	laser
Pin1 mark	Circle diameter = 1 mm
Font size	Height0.6 mm，right aligned; width0.4mm
First line of silk screen	CMT2186A，representative model CMT2186A
Second line of silk screen	YYWW It is the date code set by the packaging factory . The last 2 digits of the year WW stands for work week ①②③④⑤⑥ are internal tracking numbers

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8 Related Documents

Table8-1 . CMT2186A Related Documents

Document Number	file name	describe
	CMT2186A User Manual	CMT2186A Chip user manual
	SFR Register Preview Table	
	GPIO Function Mapping Quick Lookup Table	

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9 Change Log

Table 9-1 . CMT2186A Specification Change Record

Version Number	Changed Sections	Change Log	release date
0.1	all	Initial release	2023/12/12

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