CMT216xA Register Introduction

Overview

This document discusses CMT216xA register details for users to query and view CMT216xA register details.

The product models covered in this document are shown in the table below.

Table 1. Product Models Covered in This Document

Product Model	Single-end PA	Differential PA	12-Bit ADC	Operational Amplifier	Low-frequency Wakeup	External 32.768 kHz	Packaging
CMT2160A		●	4-ch				SOP14
CMT2162A	●		8-ch		●		SSOP20
CMT2163A	●	●	9-ch		●	●	TSSOP28
CMT2165A	●		12-ch	●		●	TSSOP28
CMT2168A	●		12-ch	●	●	●	QFN32

Notes: The performance and parameter details as well as the package size, silk screen and ordering information of each chip model are NOT covered in this document, please refer to the datasheet document of each chip model for details. For specific function details of the CMT216xA series, please refer to CMT216xA User Guide.

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1 Register Introduction

The register sets of the CMT216xA series SoC chip are located in 2 areas, Block 0 and Block 1, which have different functions and operation methods.

- **Block 0:** the access address range of this area is 0x00 ~ 0x7F, partially inaccessible to users. The inaccessible part is used to store on-chip system key parameters. Users are prohibited from accessing and modifying this part, which is Indicated in gray in *Section 2.1 Block0 Area Register Detailed List* in this document. For the accessible part of Block 0, users can access it through the API functions rather than access through direct addressing.

Function Name	Description
sys_write_hv_reg	Write by address
sys_read_hv_reg	Read by address
sys_set_hv_reg	Set by bit address (set bit value)

Notes:

1. *These 3 functions provide direct operations on Block 0 area (directly access via API functions). See AN282 CMT216xA API Library Usage Guide for details.*
2. *The associated API functions of the CMT216xA peripheral modules will access the corresponding inperipheral registers in Block 0 as well, which is invisible to users.*

- **Block 1**: this area contains two sub-areas, Bank 0 and Bank 1 with an access address range of 0x80 ~ 0xFF, which is partially accessible to users as well. The inaccessible part is used to store on-chip system key parameters. Users are prohibited from accessing and modifying this part, which is Indicated in gray in Section *2.2 Block 1 Area Register Detailed List* in this document. For the accessible part of Block 1, users can access it th rough direct addressing, however, users need to ensure that the correct switching between Bank0 and Bank1 before accessing, otherwise it will result in incorrect access to the sub-areas.

Notes:

1. *In the Block 1 area, Bank 0 and Bank 1 switching is performed by calling the API function sys_set_sfr_bank.*
2. *When operating Block1 directly in the software, it is highly recommended to switch the target bank of the corresponding register, since the CMT216xA API functions will perform corresponding bank switch as required during function call, however there's no bank switching back operation to save function execution time. Fortunately, users rarely access Block 1 registers directly, in fact most of the registers are accessed through API function calling.*
3. *The registers related to the 8051 core in Bank0 of Block1 (marked in orange in Section 2.2.1 Bank0 Sub-Registrar Register Detailed List) can be accessed directly at any time without concerning bank switching.*

The CMT216xA register area arrangement is shown in the below figure.

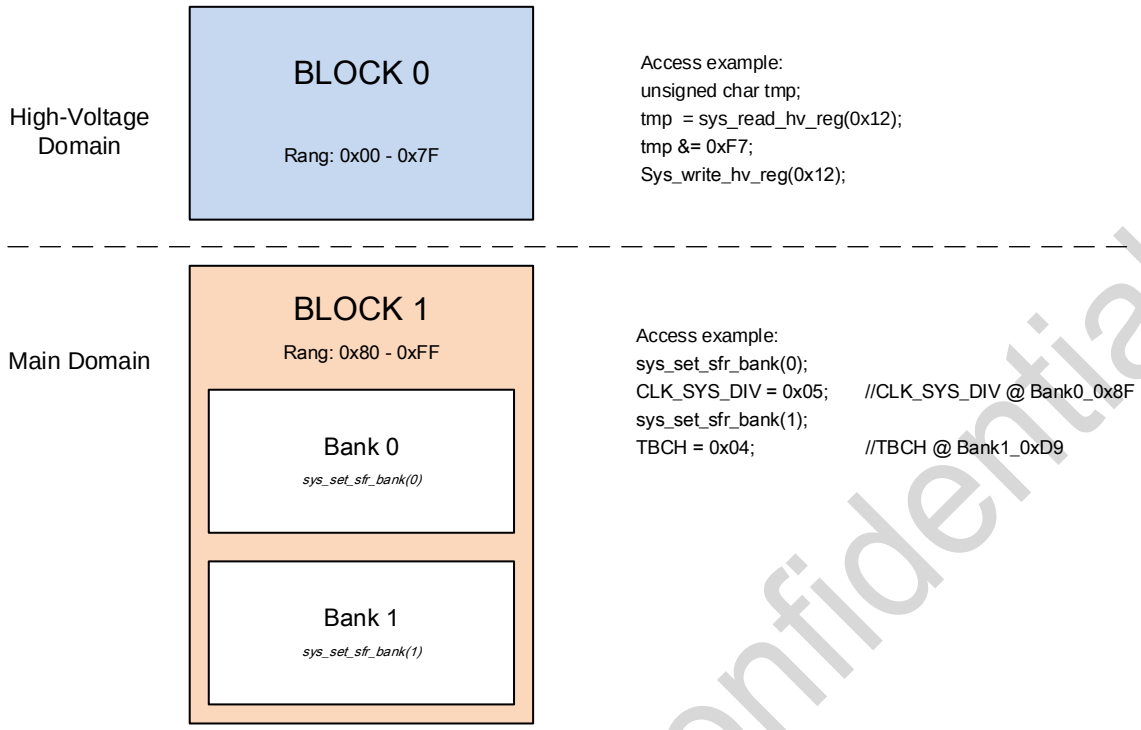

Figure1. CMT216xA Register Area Arrangement

Notes:

1. *The Block 0 SFR registers in the high-voltage domian do not change with the operating state of the CMT216xA (operating, sleep, etc.). So it just needs to be configured once upon first power-up with no need for repeated configurations for saving software initialization time.*
2. *The Block 1 SFR registers in the main domian will be lost when CMT216xA entering Shut Down (short for SDN, by calling the API function sys_shutdown), namely the register contents will be restored to default values. They need to be configured again upon next wake-up (code loading). Therefore, every time the program re-runs, they need to be configured again, rather than just be configure once upon the first power-up.*
3. *For more details on the terms of ShutDown, first power-up, etc, please see CMT216xA Datasheet or related AN documents.*

2 Register Details

2.1 Block 0 Area Register Details

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	RW	CUS_AFE1								
0x01	RW	CUS_AFE2								
0x02	RW	CUS_AFE3								
0x03	RW	CUS_AFE4	AFE_IA2_GX[1:0]							
0x04	RW	CUS_AFE5								
0x05	RW	CUS_AFE6			AFE_IA1_GX[2:0]					
0x06	RW	CUS_AFE7						AFE_SEN_CHX[2:0]		
0x07	RW	CUS_AFE8				HFOSC_CLK_EN[1:0]		LFOSC_LFXO_SEL	PD_LFXO	PD_LFOSC
0x08	RW	CUS_AFE9	LPOA0_VCM_DIS	LPOA1_VCM_DIS	AFE_IA_VCMX	AFE_OA_VCMX[1:0]		AFE_OA_OUTX[1:0]		AFE_IA1_CX
0x09	RW	CUS_AFE10	AFE_OA0_OX	AFE_OA0_NX[1:0]		AFE_OA0_PX[2:0]			AFE_OA0_NA_GX[1:0]	
0x0A	RW	CUS_AFE11	SAR_DIRECT_DIS	AFE_OA1_OX[1:0]		AFE_OA1_NX[1:0]		AFE_OA1_PX[2:0]		
0x0B	RW	CUS_AFE12	LDO_PIR_RAILB	AFE_OA2_OX[1:0]		AFE_OA2_NX[1:0]		AFE_OA2_PX[2:0]		
0x0C	RW	CUS_AFE13	LDO_PIR_VO_SEL[1:0]		SAR_INX[3:0]				SAR_REFX[1:0]	
0x0D	RW	CUS_AFE14	PD_AFE_OACMI	PIR_ST	PD_AFE_OSADJ	PD_AFE_IACMO	PD_SAR	PD_AFE_OA2	PD_AFE_OA1	PD_AFE_OA0
0x0E	RW	CUS_AFE15	LDO_SAR_VO_SEL[1:0]		LDO_SAR_RAILB	PD_BG	SAR_LBD_DIS	SAR_REF_DIS	PD_LDO_SAR	PD_AFE_VTR
0x0F	RW	CUS_AFE16	SAR_MBC0	SAR_MBC1	SAR_STM[1:0]		PD_LDO_PIR	PD_PIR_VTR	PD_LPOA1	PD_LPOA0
0x10	RW	CUS_AFE17	HDRV_SEL[4:0]					DRV_ENH	DRV_MAN_EN	PD_DRV
0x11	RW	CUS_AFE18		NDRV_SEL[3:0]				NDRV_EN	HDRV_EN	LDO_PIR_OE
0x12	RW	CUS_LFRX3	PD_P25	PD_P50	LFRX_AGC_IN[1:0]		LFRX_AGC_VHREF[3:0]			
0x13	RW	CUS_LFRX4		PD_PULLUP2	LFRX_AGC_CNT[1:0]		LFRX_AGC_VLREF[3:0]			
0x14	RW	CUS_LFRX5	LFRX_CADET_WIN[1:0]		LFRX_CADET_OK_CNT[1:0]		LFRX_PEAKDET_CLK[1:0]		LFRX_DATA_CLK[1:0]	

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15	RW	CUS_LFRX6	LFRX_DATA_R0[1:0]		LFRX_DATA_R1[1:0]		LFRX_PEAKDET_C[1:0]			
0x16	RW	CUS_LFRX7	LFRX_DATA_C1[3:0]				LFRX_DATA_C0[3:0]			
0x17	RW	CUS_LFRX8	LFRX_DATA_C3[3:0]				LFRX_DATA_C2[3:0]			
0x18	RW	CUS_LFRX9	LFRX_CMP_NOISE_MASK	LFRX_CMP_SW	LFRX_RSSIAMP_IBIAS[2:0]			LFRX_PGA_IBIAS[2:0]		
0x19	RW	CUS_LFRX10	LFRX_CMP_REF[3:0]				LFRX_DEMOD_TH_HOLD	LFRX_RSSIREC_IBIAS[2:0]		
0x1A	RW	CUS_LFRX11	LFRX_SNRDET_INVALID_WIN[1:0]		LFRX_SNRDET_VALID_WIN[1:0]		LFRX_SNRDET_SNR[3:0]			
0x1B	RW	CUS_LFRX12	LFRX_MEAS_SOURCE	LFRX_OSC_VREF[1:0]		LFRX_CH_Z	LFRX_CH_Y	LFRX_CH_X	LFRX_STARTUP_MANUAL[1:0]	
0x1C ~ 0x1D, inaccessible to users										
0x1E	RW	CUS_SNOOZE1	SNOOZE_TIMER_M_SLEEP[7:0]							
0x1F	RW	CUS_SNOOZE2	SNOOZE_UTH[9:8]		SNOOZE_DTH[9:8]		SNOOZE_TIMER_R_SLEEP[3:0]			
0x20	RW	CUS_SNOOZE3	SNOOZE_UTH[7:0]							
0x21	RW	CUS_SNOOZE4	SNOOZE_DTH[7:0]							
0x22	RW	CUS_SNOOZE5	SAR_CKX[1:0]				DWTH_WK_EN	UPTH_WK_EN	WOUT_WK_EN	WIN_WK_EN
0x23	R	CUS_SNOOZE6	GPIO_HOLD				DWTH_WK_INT	UPTH_WK_INT	WOUT_WK_INT	WIN_WK_INT
0x24	RW	CUS_PADCTL1	GPIO3_MODE[1:0]		GPIO2_MODE[1:0]		GPIO1_MODE[1:0]		GPIO0_MODE[1:0]	
0x25	RW	CUS_PADCTL2	GPIO7_MODE[1:0]		GPIO6_MODE[1:0]		GPIO5_MODE[1:0]		GPIO4_MODE[1:0]	
0x26	RW	CUS_PADCTL3	GPIO11_MODE[1:0]		GPIO10_MODE[1:0]		GPIO9_MODE[1:0		GPIO8_MODE[1:0]	
0x27	RW	CUS_PADCTL4	GPIO15_MODE[1:0]		GPIO14_MODE[1:0]		GPIO13_MODE[1:0]		GPIO12_MODE[1:0]	
0x28	RW	CUS_PADCTL5	GPIO7_CNF	GPIO6_CNF	GPIO5_CNF	GPIO4_CNF	GPIO3_CNF	GPIO2_CNF	GPIO1_CNF	GPIO0_CNF
0x29	RW	CUS_PADCTL6	GPIO15_CNF	GPIO14_CNF	GPIO13_CNF	GPIO12_CNF	GPIO11_CNF	GPIO10_CNF	GPIO9_CNF	GPIO8_CNF
0x2A	RW	CUS_PADCTL7	GPIO7_IOC	GPIO6_IOC	GPIO5_IOC	GPIO4_IOC	GPIO3_IOC	GPIO2_IOC	GPIO1_IOC	GPIO0_IOC
0x2B	RW	CUS_PADCTL8	GPIO15_IOC	GPIO14_IOC	GPIO13_IOC	GPIO12_IOC	GPIO11_IOC	GPIO10_IOC	GPIO9_IOC	GPIO8_IOC
0x2C	RW	CUS_PADCTL9	GPIO7_IDR	GPIO6_IDR	GPIO5_IDR	GPIO4_IDR	GPIO3_IDR	GPIO2_IDR	GPIO1_IDR	GPIO0_IDR
0x2D	RW	CUS_PADCTL10	GPIO15_IDR	GPIO14_IDR	GPIO13_IDR	GPIO12_IDR	GPIO11_IDR	GPIO10_IDR	GPIO9_IDR	GPIO8_IDR
0x2E	RW	CUS_PADCTL11	GPIO7_ODR	GPIO6_ODR	GPIO5_ODR	GPIO4_ODR	GPIO3_ODR	GPIO2_ODR	GPIO1_ODR	GPIO0_ODR

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2F	RW	CUS_PADCTL12	GPIO15_ODR	GPIO14_ODR	GPIO13_ODR	GPIO12_ODR	GPIO11_ODR	GPIO10_ODR	GPIO9_ODR	GPIO8_ODR
0x30 ~ 0x33，inaccessible to users										
0x34	RW	CAL_LFRX_TCAP2				LFRX_TCAP_Z[4:0]				
0x35	RW	CAL_LFRX_TCAP1				LFRX_TCAP_Y[4:0]				
0x36	RW	CAL_LFRX_TCAP0				LFRX_TCAP_X[4:0]				
0x37	RW	CAL_LFRX_OSC_CODE		LFRX_OSC_IBIAS[6:0]						
0x38 ~ 0x43, inaccessible to users										
0x44	RW	INT_SYSCTL3			S3S_DISABLE					
0x45	RW									
0x46	RW	CUS_SYSCTL1	TIMER_M_SLEEP[7:0]							
0x47	RW	CUS_SYSCTL2	TIMER_M_SLEEP[11:8]				TIMER_R_SLEEP[3:0]			
0x48 ~ 0x4F, 8 Bytes HVRAM for user										
0x50	RW	CUS_SYSCTL3	LED_INV	AFE_IR_EN	SNOOZE_EN	SNOOZE_DEBUG_EN	LFRX_DEBUG_EN	LFRX_EN	SLPT_WAKEUP_MODE	SLEEP_TIMER_EN
0x51	RW	CUS_SYSCTL4	LFRX_MODE[1:0]		LFRX_SIGNAL_OK_TYPE	LFRX_TIMER_EXTEND_MODE[1:0]		DUTY_CYCLE_METHOD	LFRX_DUTY_CYCLE_EN	ALWAYS_LFRX
0x52	RW	CUS_SYSCTL5	LFRX_TIMER_M_RX_T1[4:0]					LFRX_TIMER_R_RX_T1[2:0]		
0x53	RW	CUS_SYSCTL6	LFRX_TIMER_M_RX_T2[4:0]					LFRX_TIMER_R_RX_T2[2:0]		
0x54	RW	CUS_SYSCTL7	LFRX_TIMER_M_SLEEP[7:0]							
0x55	RW	CUS_SYSCTL8			LFRX_WAKEUP_AUTOCLR_DIS	LFRX_WAKEUP_MODE[1:0]		LFRX_TIMER_R_SLEEP[2:0]		
0x56	RW	CUS_SYSCTL9	LFRX_RSSI_MEAS_DIS	LFRX_DBUF_DIS	LFRX_SNRDET_WIN[2:0]			LFRX_MEAS_WIN[2:0]		
0x57	RW	CUS_SYSCTL10						GO_LFRX_DECODE	GO_LFRX_LISTEN	GO_LFSLEEP
0x58	RW	CUS_LFRX15	LFRX_DBUF_LENGTH[2:0]			LFRX_WKID_EN	LFRX_WKID_LENGTH[1:0]		LFRX_SYNC_LENGTH[1:0]	
0x59	RW	CUS_LFRX16	LFRX_ANT_MODE[1:0]		LFRX_HOLD_RST_S	LFRX_SNRDET_REF	LFRX_MAN_TYPE	LFRX_WKID_MAN_E	LFRX_DIG_DATAOU	LFRX_DATA_MA

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					EL	IN_SEL		N	T_SEL	N_EN
0x5A	RW	CUS_LFRX17	LFRX_SYNC_VALUE[7:0]							
0x5B	RW	CUS_LFRX18	LFRX_SYNC_VALUE[15:8]							
0x5C	RW	CUS_LFRX19	LFRX_SYNC_VALUE[23:16]							
0x5D	RW	CUS_LFRX20	LFRX_SYNC_VALUE[31:24]							
0x5E	RW	CUS_LFRX21	LFRX_WKID_VALUE[7:0]							
0x5F	RW	CUS_LFRX22	LFRX_WKID_VALUE[15:8]							
0x60	RW	CUS_LFRX23	LFRX_WKID_VALUE[23:16]							
0x61	RW	CUS_LFRX24	LFRX_WKID_VALUE[31:24]							
0x62	RW	CUS_LFRX25	LFRX_DATAOUT_SEL	LFRX_DECODE_SEQ	LFRX_SIGNAL_OK_AUTOCLR_DIS	LFRX_AGC_EN	LFRX_AGC_STEP	LFRX_AGC_CNT_TH[2:0]		
0x63	RW	CUS_LFRX26	LFRX_DQRES[3:0]				LFRX_AGC_MIN_INDEX[3:0]			
0x64	RW	CUS_LFRX27	LFRX_DR_SEL[3:0]					LFRX_ENABLE_MODE		LFRX_AGC_START_SEL
0x65	RW	CUS_LFRX28	LFRX_CADET_TH_H[7:0]							
0x66	RW	CUS_LFRX29	LFRX_CADET_TH_L[7:0]							
0x67	RW	CUS_LFRX30	LFRX_SIGNAL_OK_CLR_TH[7:0]							
0x68	RW	CUS_SYSCTL11	SLPT_MANU_RSTN			SNOOZE_MANU_CLR	LBD_MANU_CLR	LFRX_MANU_CLR	SLPT_MANU_CLR	BUT_MANU_CLR
0x69	R	CUS_SYSCTL12		SNOOZE_WAKEUP		WKID_PASS	SYNC_PASS	LFRX_SIGNAL_OK	SLEEP_TIMESUP	KEY_LAUNCH
0x6A	RW	CUS_SYSCTL13	LBD_STATUS(IN)	LBD_FINISH(IN)	LBD_AVG_SEL	LBD_ENABLE	SAR_DATA_UPDATE	SAR_MSTART	SAR_TRIGGER	SAR_CLK_EN
0x6B	R	CUS_SYSCTL14	SAR_DATA[11:4]							
0x6C	R	CUS_SYSCTL15					SAR_DATA[3:0]			
0x6D	RW	CUS_SYSCTL16	LBD_TH[7:0]							
0x6E	R	CUS_SYSCTL17	LBD_RESULT[7:0]							
0x6F	RW	CUS_SYSCTL18					PAD_GROUP2_EN	PAD_GROUP1_EN	LFOSC_CLKOUT_EN	HFOSC_CLKOUT_EN

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	RW	CUS_SYSCTL19	LFRX_OSC_OUT_EN	IRLED_DOUT_EN						
0x71	RW	CUS_SYSCTL20		OTP_CP_VCC_SELN[1:0]		OTP_CP_VTH_SEL	GPIO16_ODR	GPIO16_ODR	GPIO16_MODE[1:0]	
0x72	RW	CUS_LFRX31			LFRX_AGC_INDEX[5:0](IN)					
0x73	RW	CUS_LFRX32	MAN_DECODE _ERR_FLAG	LFRX_MEAS_OUT[2:0]			LFRX_IBIAS_ CAL_OVTS_FLAG	LFRX_TCAP2/1/0_CAL_OVTS_FLAG		
0x74	RW	CUS_LFRX33	LFRX_DATA_LENGTH[7:0]							
0x75	RW	CUS_RESV0	Reserved, can be use as HVRAM for user							
0x76	RW	CUS_RESV1								
0x77	RW	CUS_RESV2								
0x78	RW	CUS_RESV3	inaccessible to users							
0x79	RW	CUS_RESV4	inaccessible to users							
0x7A	RW	CUS_RESV5	LPOA0_PIN_DIS	LPOA1_PIN_DIS	WDT_REFRESH	WDT_START	WDT_RESET_TH[2:0]			WDT_DIS
0x7B ~ 0x7F，inaccessible to users										

Notes:

This color indicates inaccessible areas
This color indicates it can be used to store variables that cannot be lost, namely it supports to save variable values in ShutDown mode and they can be read again upon next wake-up.

2.2 Block 1 Area Register List

2.2.1 Bank 0 Sub-area Register List

Addr	TYP	名称	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x80	RW	P0	P0_IN[7:0] or P0_OUT[7:0]							
0x81	RW	SP	SP[7:0]							
0x82	RW	DPL	DPTR[7:0]							
0x83	RW	DPH	DPTR[15:8]							
0x84 ~ 0x86, inaccessible to users										
0x87	RW	PCON	SMOD1	SMOD0			GF1	GF0	STOP	IDLE
0x88	RW	TCON	TF1	TR1			IE1	IT1	IE0	IT0
0x89	RW	TMOD	GATE1	C_T1	M1[1:0]					
0x8A	RW	inaccessible to users								
0x8B	RW	TL1	TL1[7:0]							
0x8C	RW	inaccessible to users								
0x8D	RW	TH1	TH1[7:0]							
0x8E	RW	inaccessible to users								
0x8F	RW	CLK_SYS_DIV		LFRX_MCU_RCLK	LFRX_MCU_RDATA		CLK_SYS_DIV[3:0]			
0x90	RW	inaccessible to users								
0x91	RW	SPI_CTL1_H	BIDI_MODE	BIDI_OE	RX_ONLY	DFF	TXDMAEN	SSOE	SSM	SSI
0x92	RW	SPI_CTL1_L	LSB_FIRST	SPE	BR[2:0]			MSTR	CPOL	CPHA
0x93	RW	SPI_CTL2_H								
0x94	RW	inaccessible to users								
0x95	RW	SPI_DATA_H	SPI_TXDATA[15:8]							
0x96	RW	SPI_DATA_L	SPI_TXDATA[7:0]							
0x97	RW	USART_CTL								USART_SEL
0x98	RW	SCON0	FE0/SM00	SM10	SM20	REN0	TB80	RB80	TI0	RI0

Addr	TYP	名称	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x99	RW	SBUF0	SBUF0[7:0]							
0x9A	RW	TACLK_DIV_H	TACLK_DIV[15:8]							
0x9B	RW	TACLK_DIV_L	TACLK_DIV[7:0]							
0x9C	RW	TACH						TA_START	TACCI3	TACCI2
0x9D	RW	TACL				TA_CNT_MODE[1:0]		TA_CLR	TMR_IE	TMR_IFG
0x9E	R	TACNT_H	TIMERA_CNT[15:8]							
0x9F	R	TACNT_L	TIMERA_CNT[7:0]							
0xA0	RW	inaccessible to users								
0xA1	RW	TACCR0H	TACCR0[15:8]							
0xA2	RW	TACCR0L	TACCR0[7:0]							
0xA3	RW	TACCTL0H		TACCR0_CCI	TACCR0_SCCI	TACCR0_CM[1:0]		TACCR0_CCIS[1:0]		TACCR0_CAP
0xA4	RW	TACCTL0L	TACCR0_SCS	TACCR0_OUTMODE[2:0]			TACCR0_IE	TACCR0_OUT	TACCR0_COV	TACCR0_IFG
0xA5	RW	TACCR1H	TACCR1[15:8]							
0xA6	RW	TACCR1L	TACCR1[7:0]							
0xA7	RW	inaccessible to users								
0xA8	RW	IEN0	EA			ES0	ET1	EX1		EX0
0xA9	RW	TACCTL1H		TACCR1_CCI	TACCR1_SCCI	TACCR1_CM[1:0]		TACCR1_CCIS[1:0]		TACCR1_CAP
0xAA	RW	TACCTL1L	TACCR1_SCS	TACCR1_OUTMODE[2:0]			TACCR1_IE	TACCR1_OUT	TACCR1_COV	TACCR1_IFG
0xAB	RW	TACCR2H	TACCR2[15:8]							
0xAC	RW	TACCR2L	TACCR2[7:0]							
0xAD	RW	TACCTL2H		TACCR2_CCI	TACCR2_SCCI	TACCR2_CM[1:0]		TACCR2_CCIS[1:0]		TACCR2_CAP
0xAE	RW	TACCTL2L	TACCR2_SCS	TACCR2_OUTMODE[2:0]			TACCR2_IE	TACCR2_OUT	TACCR2_COV	TACCR2_IFG
0xAF	RW	IRQ0_SEL		IRQ_SW[0]	IRQ0_SEL[5:0]					
0xB0	RW	IRQ1_SEL		IRQ_SW[1]	IRQ1_SEL[5:0]					
0xB1	RW	IRQ2_SEL		IRQ_SW[2]	IRQ2_SEL[5:0]					
0xB2	RW	IRQ3_SEL		IRQ_SW[3]	IRQ3_SEL[5:0]					
0xB3	RW	IRQ4_SEL		IRQ_SW[4]	IRQ4_SEL[5:0]					

Addr	TYP	名称	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB4	RW	IRQ5_SEL		IRQ_SW[5]	IRQ5_SEL[5:0]					
0xB5	RW	IRQ6_SEL		IRQ_SW[6]	IRQ6_SEL[5:0]					
0xB6	RW	IRQ7_SEL		IRQ_SW[7]	IRQ7_SEL[5:0]					
0xB7	RW	TIMER_IN_SEL	T1_GPIO_SEL[3:0]				RXD0_IN_GPIO_SEL[3:0]			
0xB8	RW	IPL0				IPL0.4	IPL0.3	IPL0.2	IPL0.1	IPL0.0
0xB9	RW	TACCI_SEL	TACCI1_GPIO_SEL[3:0]				TACCI0_GPIO_SEL[3:0]			
0xBA	RW	SPI_IN_SEL0	SCK_IN_SEL[3:0]				NSS_IN_SEL[3:0]			
0xBB	RW	SPI_IN_SEL1	MOSI_IN_SEL[3:0]				MISO_IN_SEL[3:0]			
0xBC	RW	P0_IN_SEL0	PORT01_IN_GPIO_SEL[3:0]				PORT00_IN_GPIO_SEL[3:0]			
0xBD	RW	P0_IN_SEL1	PORT03_IN_GPIO_SEL[3:0]				PORT02_IN_GPIO_SEL[3:0]			
0xBE	RW	P0_IN_SEL2	PORT05_IN_GPIO_SEL[3:0]				PORT04_IN_GPIO_SEL[3:0]			
0xBF	RW	P0_IN_SEL3	PORT07_IN_GPIO_SEL[3:0]				PORT06_IN_GPIO_SEL[3:0]			
0xC0	RW	GPIO_IN_R_H	GPIO_IN_R[15:8](IN)							
0xC1	RW	GPIO_IN_R_L	GPIO_IN_R[7:0](IN)							
0xC2	RW	GPIO_OUT_R_H	GPIO_OUT_R[15:8]							
0xC3	RW	GPIO_OUT_R_L	GPIO_OUT_R[7:0]							
0xC4	RW	GPIO_OUT_SEL0	GPIO1_OUT_SEL[3:0]				GPIO0_OUT_SEL[3:0]			
0xC5	RW	GPIO_OUT_SEL1	GPIO3_OUT_SEL[3:0]				GPIO2_OUT_SEL[3:0]			
0xC6	RW	GPIO_OUT_SEL2	GPIO5_OUT_SEL[3:0]				GPIO4_OUT_SEL[3:0]			
0xC7	RW	GPIO_OUT_SEL3	GPIO7_OUT_SEL[3:0]				GPIO6_OUT_SEL[3:0]			
0xC8	RW	GPIO_OUT_SEL4	GPIO9_OUT_SEL[3:0]				GPIO8_OUT_SEL[3:0]			
0xC9	RW	GPIO_OUT_SEL5	GPIO11_OUT_SEL[3:0]				GPIO10_OUT_SEL[3:0]			
0xCA	RW	GPIO_OUT_SEL6	GPIO13_OUT_SEL[3:0]				GPIO12_OUT_SEL[3:0]			
0xCB	RW	GPIO_OUT_SEL7	GPIO15_OUT_SEL[3:0]				GPIO14_OUT_SEL[3:0]			
0xCC	RW	LED_CTL	SAR_DATA_UPDATE	LED_ON	LED_OUT_SEL	PWM_RATE_SEL	PWM_INTERVAL_SEL[3:0]			
0xCD ~ 0xCF, inaccessible to users										
0xD0	RW	PSW	CY	AC	F0	RS[1:0]		OV	F1	P

Addr	TYP	名称	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD1 ~ 0xDC, inaccessible to users										
0xDD	RW	GPIO_IN_R_D1								GPIO_IN_R[16]
0xDE	RW	GPIO_OUT_R_D1								GPIO_OUT_R[16]
0xDF	RW	inaccessible to users								
0xE0	RW	ACC	ACC[7:0]							
0xE1 ~ 0xE5, inaccessible to users										
0xE6	RW	IEN1	EX7	EX6	EX5	EX4	EX3	EX2		
0xE7 ~ 0xEF, inaccessible to users										
0xF0	RW	B	B[7:0]							
0xF1	RW	IRCON1	IE7	IE6	IE5	IE4	IE3	IE2		
0xF2 ~ 0xF5, inaccessible to users										
0xF6	RW	IPL1	IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2		
0xF7 ~ 0xFE, inaccessible to users										
0xFF	RW	SYS_CTL	SFR_CLK_GATE_EN							

Notes:

This color indicates inaccessible areas.
This color indicate the original 8051 core register, supporting bit range and direct access (with no need for register bank switching)

2.2.2 Bank 1 Sub-area Register List

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x80 ~ 0x8D, inaccessible										
0x8E	RW	PA_POWER_TH_9		PA_POWER_TH_9[6:0]						
0x8F	RW	PA_POWER_TH_8		PA_POWER_TH_8[6:0]						
0x90	RW	PA_POWER_TH_7		PA_POWER_TH_7[6:0]						
0x91	RW	PA_POWER_TH_6		PA_POWER_TH_6[6:0]						
0x92	RW	PA_POWER_TH_5		PA_POWER_TH_5[6:0]						
0x93	RW	PA_POWER_TH_4		PA_POWER_TH_4[6:0]						
0x94	RW	PA_POWER_TH_3		PA_POWER_TH_3[6:0]						
0x95	RW	PA_POWER_TH_2		PA_POWER_TH_2[6:0]						
0x96	RW	PA_POWER_TH_1		PA_POWER_TH_1[6:0]						
0x97	RW	PA_POWER_TH_0		PA_POWER_TH_0[6:0]						
0x98 ~ 0xA8, inaccessible										
0xA9	RW	TX_SYM_GROUP	TX_SYM_GROUP[7:0] / TX_DIRECT_DATA[0]							
0xAA	RW	TX_SYM_CTL		TX_DIRECT_EN	TX_GROUP_WIDTH[2:0]			TX_SYM_ENDIAN	TX_SYM_CTRL[1:0]	
0xAB	RW	TX_PKT_CTL					RAMP_EN	TX_MODU	FREQ_DEV_INV	GUASS_ON
0xAC	RW	SYMBOL_TIME_H	SYMBOL_TIME[15:8]							
0xAD	RW	SYMBOL_TIME_L	SYMBOL_TIME[7:0]							
0xAE	RW	FREQ_DEV_H	FREQ_DEV[15:8]							
0xAF	RW	FREQ_DEV_L	FREQ_DEV[7:0]							
0xB0	RW	RAMP_STEP_TIME_H		RAMP_STEP_TIME[14:8]						
0xB1	RW	RAMP_STEP_TIME_L	RAMP_STEP_TIME[7:0]							
0xB2	RW	inaccessible								
0xB3	RW	PA_IDAC_CODE			PA_IDAC_CODE[5:0]					
0xB4	RW	PA_CTL0				PA_DIFF_SEL	PA_RCRAMP_SELB	PA_RAMP_RSEL[2:0]		
0xB5	RW	inaccessible								

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB6	RW	VCO_CTL0				VCO_GAIN_CODE[2:0]			PLL_BW_SEL[1:0]	
0xB7	RW	VCO_CTL1	VCO_HBAND	PDCPLF_CPBIAS_CODE	DIVX_CODE[1:0]		DIVX_SEL[3:0]			
0xB8	RW	inaccessible								
0xB9	RW	PLLN	PLLN_CFG[7:0]							
0xBA	RW	PLLK_H	PLLK_CFG[15:8]							
0xBB	RW	PLLK_L	PLLK_CFG[7:0]							
0xBC	RW	inaccessible								
0xBD	RW	inaccessible								
0xBE	RW	RNG_CTL				RNG_SUM_VLD				RNG_START
0xBF	RW	RNG_SUM	RNG_SUM(IN)							
0xC0	RW	LBD_CTL					LBD_FLAG	LBD_VTH_SEL	LBD_POR_EN	LBD_ON
0xC1	RW	LFRX_IF_TH_H						LFRX_TBCCI0_SEL	LFRX_TACCI1_SEL	LFRX_TACCI0_SEL
0xC2	RW	inaccessible								
0xC3	RW	LFRX_IF_TH_L	LFRX_ANT_REF[7:0]							
0xC4 ~ 0xD6, inaccessible										
0xD7	RW	TBCLK_DIV_H	TBCLK_DIV[15:8]							
0xD8	RW	TBCLK_DIV_L	TBCLK_DIV[7:0]							
0xD9	RW	TBCH						TB_START	TBCCI3	TBCCI2
0xDA	RW	TBCL				TB_CNT_MODE[1:0]		TB_CLR	TMRB_IE	TMRB_IFG
0xDB	RW	TBCCR0H	TBCCR0[15:8]							
0xDC	RW	TBCCR0L	TBCCR0[7:0]							
0xDD	RW	TBCCTL0H		TBCCR0_CCI	TBCCR0_SCCI	TBCCR0_CM[1:0]		TBCCR0_CCIS[1:0]		TBCCR0_CAP
0xDE	RW	TBCCTL0L	TBCCR0_SCS	TBCCR0_OUTMODE[2:0]			TBCCR0_IE	TBCCR0_OUT	TBCCR0_COV	TBCCR0_IFG
0xDF	RW	TBCCR1H	TBTACCR1[15:8]							
0xE0	RW	inaccessible								
0xE1	RW	TBCCR1L	TBTACCR1[7:0]							
0xE2	RW	TBCCTL1H		TBCCR1_CCI	TBCCR1_SCCI	TBCCR1_CM[1:0]		TBCCR1_CCIS[1:0]		TBCCR1_CAP

Addr	TYP	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE3	RW	TBCCTL1L	TBCCR1_SCS	TBCCR1_OUTMODE[2:0]			TBCCR1_IE	TBCCR1_OUT	TBCCR1_COV	TBCCR1_IFG
0xE4	RW	TBCCR2H	TBTACCR2[15:8]							
0xE5	RW	TBCCR2L	TBTACCR2[7:0]							
0xE6	RW	inaccessible								
0xE7	RW	TBCCTL2H		TBCCR2_CCI	TBCCR2_SCCI	TBCCR2_CM[1:0]		TBCCR2_CCIS[1:0]		TBCCR2_CAP
0xE8	RW	TBCCTL2L	TBCCR2_SCS	TBCCR2_OUTMODE[2:0]			TBCCR2_IE	TBCCR2_OUT	TBCCR2_COV	TBCCR2_IFG
0xE9	RW	TBCCI_SEL	TBCCI1_GPIO_SEL[3:0]				TBCCI0_GPIO_SEL[3:0]			
0xEA	R	TBCNT_H	TIMERB_CNT[15:8]							
0xEB	R	TBCNT_L	TIMERB_CNT[7:0]							
0xEC ~ 0xFF, inaccessible										

Notes：

This color indicates inaccessible areas.

3 Register Details

3.1 T8051 XC3 Core Register Set

Table 2. 8051 Core Register Set

Name	Storage Area	Sub-area	Address	Reset	Function
P0	Block1	Bank0	0x80	0x00	Port0 register, support bit access, corresponding to the 8 core ports, P0.0–P0.7 [1].
SP	Block1	Bank0	0x81	0x00	Stack pointer register
DPL	Block1	Bank0	0x82	0x00	Data pointer (DPTR) register lower 8 bits
DPH	Block1	Bank0	0x83	0x00	Data pointer (DPTR) register higher 8 bits
PCON	Block1	Bank0	0x87	0x00	Power control register
TCON	Block1	Bank0	0x88	0x00	Timer1 control register (see *Section 3.2 Timer1 Register Set* for details)
TMOD	Block1	Bank0	0x89	0x00	Timer1 operating mode register (see *Section 3.2 Timer1 Register Set* for details)
TL1	Block1	Bank0	0x8B	0x00	The lower 8 bits of the Timer1 register (see *Section 3.2 Timer1 Register Set* for details)
TH1	Block1	Bank0	0x8D	0x00	The Timer1 register higher 8 bits (*Section 3.2 Timer1 Register Set* for details).
SCON0	Block1	Bank0	0x98	0x00	Serial port 0 control register (see *Section 3.8 UART Register Set* for deails)
SBUF0	Block1	Bank0	0x99	0x00	Serial 0 data buffer register (see *Section 3.8 UART Register Set* for deails)
IEN0	Block1	Bank0	0xA8	0x00	Interrupt enabling register 0
IPL0	Block1	Bank0	0xB8	0x00	Interrupt priority register 0
PSW	Block1	Bank0	0xD0	0x00	Program status/flag register
ACC	Block1	Bank0	0xE0	0x00	Accumulator register
IEN1	Block1	Bank0	0xE6	0x00	Interrupt enabling register 1
B	Block1	Bank0	0xF0	0x00	B register
IRCON1	Block1	Bank0	0xF1	0x00	Peripheral interrupt request flag register
IPL1	Block1	Bank0	0xF6	0x00	Interrupt priority register 1

Notes: Here, P0 is the core port0, the mapping between P0 and CMT216xA GPIOs is configurable.Other words, P0.0 does not nessessary refer to GPIO0. For the mapping between GPIO and P0, see CMT216xA User Guide for more details.

- **PCON Register**

PCON Reset value：0x00

7	6	5	4	3	2	1	0
SMOD1	SMOD0	--	--	GF1	GF0	STOP	IDLE

Name		Decription	Type
7	SMOD1	Serial port 0 double baud rate control bit. Setting to 1 valid when serial port 0 operates in mode 1/2/3 .	R/W
6	SMOD0	Serial port 0 frame error (FE) selection bit: When set to 1, read/write SCON0.7 as the FE flag bit. When set to 0, read/write SCON0.7 as the SM0 flag bit.	R/W
5:4	--	Unused, read as 0	R
3	GF1	General flag 1	R/W
2	GF0	General flag 0	R/W
1	STOP	STOP mode control bit [1]	R/W
0	IDLE	IDLE mode control bit [1]	R/W

Note: The STOP or IDLE mode only makes the 8051 core enter the power saving mode, but does not mean the whole CMT216xA SoC system enters the power saving mode. If it is required the entire system to enter power saving, the API function sys_shutdown should be called.

- **PSW Register**

PSW Reset value：0x00

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P

Name		Decription	Type
7	CY	Carrying flag	R/W
6	AC	Assisting carrying flag	R/W
5	F0	General flag 0, user operable	R/W
4:3	RS[1:0]	Operating register set selection: 2'b00: 0x00-0x07 2'b01:0x08-0x0F 2'b10:0x10-0x17 2'b11: 0x18-0x1F	R/W
2	OV	Signed calculation overflow bit	R/W
1	F1	General flag 1, user operable	R/W
0	P	ACC parity indication bit	R

- **IRCON1 register**

IRCON1 Reset value：0x00

7	6	5	4	3	2	1	0
IE7	IE6	IE5	IE4	IE3	IE2	-	--

Name		Decription	Type
7	IE7	External interrupt 7 request flag	R/W
6	IE6	External interrupt 6 request flag	R/W
5	IE5	External interrupt 5 request flag	R/W

Name		Decription	Type
4	IE4	External interrupt 4 request flag	R/W
3	IE3	External interrupt 3 request flag	R/W
2	IE2	External interrupt 2 request flag	R/W
1:0	--	Unused, read as 0	R

- **IEN0 register**

IEN0 Reset value：0x00

7	6	5	4	3	2	1	0
EA	--	--	ES0	ET1	EX1	--	EX0

Name		Decription	Type
7	EA	General interrupt enabling bit. It is valid when setting to 1.	R/W
6:5	-	Unused, read as 0.	R
4	ES0	Serial port 0 interrupt enabling bit. It is valid when setting to 1.	R/W
3	ET1	Timer 1 interrupt enabling bit. It is valid when setting to 1.	R/W
2	EX1	External interrupt 1 enabling bit. It is valid when setting to 1.	R/W
1	-	Unused, read as 0.	R/W
0	EX0	External interrupt 0 enabling bit. It is valid when setting to 1.	R

- **IEN1 register**

IEN1 Reset value：0x00

7	6	5	4	3	2	1	0
EX7	EX6	EX5	EX4	EX3	EX2	--	--

Name		Decription	Type
7:2	Exn	External interrupt n enabling bit. It is valid when setting to 1.	R/W
1:0	-	Unused, read as 0.	R

Notes: The interrupt is different from the ShutDown (SDN) mode wakeup. Please refer to CMT216xA User Guide for more details.

- **IPL0 Register**

IPL0 Reset value：0x00

7	6	5	4	3	2	1	0
--	--	--	IPL0.4	IPL0.3	IPL0.2	--	IPL0.0

Name		Decription	Type
7:5	-	Unused, read as 0.	R
4	IPL0.4	Series port 0 priority. Setting to 1 represents the highest priority.	R/W
3	IPL0.3	Timer 1 priority. Setting to 1 represents the highest priority.	R/W
2	IPL0.2	External interrupt 1 priority. Setting to 1 represents the highest priority.	R/W
1	-	Unused, read as 0.	R/W
0	IPL0.0	External interrupt 0 priority. Setting to 1 represents the highest priority.	R

- **IPL1 register**

IPL1 Reset value：0x00

7	6	5	4	3	2	1	0
IPL1.7	IPL1.6	IPL1.5	IPL1.4	IPL1.3	IPL1.2	--	--

Name		Decription	Type
7:2	IPL1[7:2]	External interrupt 7~2 priority. Setting to 1 represents the highest priority.	R/W
1:0	-	Unused, read as 0.	R

3.2 Timer1 Register Set

Table 3. Timer1 Module Register Set List

Name	Area	Sub-area	Address	Reset	Function
TCON	Block1	Bank0	0x88	0x00	Timer1 control register
TMOD	Block1	Bank0	0x89	0x00	Timer1 operating mode register
TL1	Block1	Bank0	0x8B	0x00	Timer1 register lower 8 bits
TH1	Block1	Bank0	0x8D	0x00	Timer1 register higher 8 bits
TIMER_IN_SEL	Block1	Bank0	0xB7	0x00	Timer1 input selection register

- **TCON Register**

TCON Reset value：0x00

7	6	5	4	3	2	1	0
TF1	TR1	--	--	IE1	IT1	IE0	IT0

Name		Decription	Type
7	TF1	Timer 1 overflow bit. Set to 1 by the hardware when Timer1 timer/counter overflows.	R/W
6	TR1	Timer 1 timer/counter enabling and operating bit	R/W
5:4	-	Unused, read as 0.	R
3	IE1	External interrupt 1 enabling bit.	R/W
2	IT1[1]	External interrupt 1 triggering mode. Set to 0, level triggering Set to 1, edge triggering	R/W
1	IE0	External interrupt 0 enabling bit.	R/W
0	IT0[1]	External interrupt 0 triggering mode. Set to 0, level triggering Set to 1, edge triggering	R/W

Notes: The triggering mode of external interrupt 0 and external interrupt 1 is other than the one of traditional 51 core, namely, the level and edge modes are supported. See the IRQn_SEL register description in Section 3.16 IRQn_SEL for details.

- **TMOD register**

TMOD Reset value：0x00

7	6	5	4	3	2	1	0
GATE1	C/T1	M1[1]	M1[0]	--	--	--	--

Name		Decription	Type
7	GATE1	Timer 1 gate bit. When set to 1, the T1 input source is valid only when Timer1 operates in the counting mode.	R/W
6	C/T1	Timer 1 count / timing selection bit. Set to 0, select the up-count mode of the internal clock source. Set to 1, select the up-count mode triggered by T1 falling edge input	R/W
5:4	M1[1:0]	Timer1 operating mode selection： 2'b00: Mode 0, 8-bit timing/counting mode with 5-bit prescaler. 2'b01: Mode 1, 16-bit timing/counting mode.	R/W

Name		Decription	Type
		2'b10: Mode 2, 8-bit timing/counting mode with reloading. 2'b11: Mode 3, unused, Timer 1 stops.	
3:0	-	Unused, read as 0.	R

- **TL1/TH1, timer1 counter register**

TL1 & TH1 Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TH1[7:0]							
L	TL1[7:0]							

Name	Decription	Type
TH1	Timer1 higher 8-bit count value	R/W
TL1	Timer1 lower 8-bit count value	R/W

- **TIMER_IN_SEL register**

TIMER_IN_SEL Reset value：0x00

7	6	5	4	3	2	1	0
T1_GPIO_SEL[3:0]				RXD0_IN_GPIO_SEL[3:0]			

Name		Decription	Type
7:4	T1_GPIO_SEL	Timer1 external input signal selection. Can map to GPIO[15:0]. 4’b0000, corresponding to GPIO0, namely A0 pin. 4’b0001, corresponding to GPIO1, namely A1 pin. …… 4’b01114’b0001, corresponding to GPIO7, namely A7 pin. 4’b1000, corresponding to GPIO8, namely A8 pin. 4’b1001, , corresponding to GPIO9, namely A9 pin. …… 4’b1111, , corresponding to GPIO15, namely B7 pin.	R/W

3.3 GPIO Register Set

Table 4. GPIO Register Set List

Name	Area	Sub-area	Address	Reset	Function
CUS_PADCTL1	Block0	--	0x24	0xFF	GPIO0 ~ GPIO15 port mode has the following 3 methods: 1. Push-pull output mode or open-drain output mode. 2. Digital input mode (configurable pull-up/ pull-down) or 3. Analog input and output mode. 4. Floating (default).
CUS_PADCTL2	Block0	--	0x25	0xFF	
CUS_PADCTL3	Block0	--	0x26	0x7F	
CUS_PADCTL4	Block0	--	0x27	0xFF	
CUS_PADCTL5	Block0	--	0x28	0x00	GPIO0 ~ GPIO15 port mode configuration register 1, responsible for input pull-up/pull-down selection or output push-pull/open-drain configuration
CUS_PADCTL6	Block0	--	0x29	0x00	
CUS_PADCTL7	Block0	--	0x2A	0x00	GPIO0 ~ GPIO15 port IO change interrupt/wake-up enabling register
CUS_PADCTL8	Block0	--	0x2B	0x00	
CUS_PADCTL9	Block0	--	0x2C	0x00	GPIO0 ~ GPIO15 input status saving register, used for IOC function port status transition comparison
CUS_PADCTL10	Block0	--	0x2D	0x00	
CUS_PADCTL11	Block0	--	0x2E	0x00	GPIO0 ~ GPIO15 port mode configuration register 2, responsible for input pull-up/pull-down enabling and output status saving (output mode)
CUS_PADCTL12	Block0	--	0x2F	0x00	
CUS_SYSCTL11	Block0	--	0x68	0x80	System control register 11.
CUS_SYSCTL12	Block0	--	0x69	0x00	System control register 12.
CUS_SYSCTL20	Block0	--	0x71	0x13	System control register 20
CUS_LFRX3	Block0	--	0x12	0x2A	Low frequency wake-up receiving register 3
CUS_LFRX4	Block0	--	0x13	0x55	Low frequency wake-up receiving register 3
CUS_SNOOZE6	Block0	--	0x23	0x00	SNOOZE configuration register 6
P0	Block1	Bank0	0x80	0x00	8051 core Port 0 register
TIMER_IN_SEL	Block1	Bank0	0xB7	0x00	Timer1 input and GPIO mapping registers, see Section 3.2 for details.
TACCI_SEL	Block1	Bank0	0xB9	0x00	Timer A capture module CCI and GPIO mapping, see Section 3.9 for details.
SPI_IN_SEL0	Block1	Bank0	0xBA	0x00	SPI input signal and GPIO mapping configuration register 0, see Section 3.7 for details.
SPI_IN_SEL1	Block1	Bank0	0xBB	0x00	The SPI input signal and GPIO mapping configuration register 1, see Section 3.7 for details.
P0_IN_SEL0	Block1	Bank0	0xBC	0x00	GPIO[15:0] mapping selection configuration register, when Port0[7:0] is used as the input mode.
P0_IN_SEL1	Block1	Bank0	0xBD	0x00	
P0_IN_SEL2	Block1	Bank0	0xBE	0x00	
P0_IN_SEL3	Block1	Bank0	0xBF	0x00	
GPIO_IN_R_H	Block1	Bank0	0xC0	0x00	GPIO0 ~ GPIO15 input read register (Note: this register does not support bit access mode)
GPIO_IN_R_L	Block1	Bank0	0xC1	0x00	
GPIO_OUT_R_H	Block1	Bank0	0xC2	0x00	GPIO0 ~ GPIO15 output control register (Note: this register does not support bit access mode)
GPIO_OUT_R_L	Block1	Bank0	0xC3	0x00	
GPIO_OUT_SEL0	Block1	Bank0	0xC4	0x00	Function selection register when GPIO0 ~ GPIO15 is used

Name	Area	Sub-area	Address	Reset	Function
GPIO_OUT_SEL1	Block1	Bank0	0xC5	0x00	as output function
GPIO_OUT_SEL2	Block1	Bank0	0xC6	0x00	
GPIO_OUT_SEL3	Block1	Bank0	0xC7	0x00	
GPIO_OUT_SEL4	Block1	Bank0	0xC8	0x00	
GPIO_OUT_SEL5	Block1	Bank0	0xC9	0x00	
GPIO_OUT_SEL6	Block1	Bank0	0xCA	0x00	
GPIO_OUT_SEL7	Block1	Bank0	0xCB	0x00	
LED_CTL	Block1	Bank0	0xCC	0x00	LED module control register, see section 3.4 for details.
GPIO_IN_R_D1	Block1	Bank0	0xDD	0x00	GPIO16 (namely D1) input access register
GPIO_OUT_R_D1	Block1	Bank0	0xDE	0x00	PIO16 (namely D1) output access register
TBCCI_SEL	Block1	Bank1	0xE9	0x00	TimerB capture module CCI and GPIO mapping, see section 3.9 for details.

Notes: This document focuses on the function description of each register. As the CMT216xA SoC on-chip GPIO configuration quite is flexible and rich, it is recommended that users read GPIO realted sections in CMT216xA User Guide and to better understand the function of the above registers.

- **CUS_PADCTL1 ~ CUSPADCTL4 register set**

CUS_PADCTL1 ~ 4 Reset value：0xFF, 0xFF, 0xF7, 0xFF

	7 6	5 4	3 2	1 0
1	GPIO3_MODE[1:0]	GPIO2_MODE[1:0]	GPIO1_MODE[1:0]	GPIO0_MODE[1:0]
2	GPIO7_MODE[1:0]	GPIO6_MODE[1:0]	GPIO5_MODE[1:0]	GPIO4_MODE[1:0]
3	GPIO11_MODE[1:0]	GPIO10_MODE[1:0]	GPIO9_MODE[1:0]	GPIO8_MODE[1:0]
4	GPIO15_MODE[1:0]	GPIO14_MODE[1:0]	GPIO13_MODE[1:0]	GPIO12_MODE[1:0]

Name	Decription	Type
GPIOn_MODE	GPIOn operating mode selection. 2'b00: analog input/output 2'b01: digital input 2'b10: digital output 2'b11: floating internally, high impedance (default value except GPIO9)	R/W

Notes: When the power supply voltage of the chip is lower than the lower limit of the operating voltage (less than 2.0 V), the GPIO configuration is restored to the default state, namely the floating internally, and the high impedance state externally . However, for B0 ~ B4 specially as simulation and programming pins, the status is different. In this case, B0, B1, B2, and B4 show a pull-up high state and B3 shows a pull-down low state.

- **CUS_PADCTL5 ~ CUSPADCTL6 register set**

CUS_PADCTL5 ~ 6 Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
5	GPIO7_CNF	GPIO6_CNF	GPIO5_CNF	GPIO4_CNF	GPIO3_CNF	GPIO2_CNF	GPIO1_CNF	GPIO0_CNF
6	GPIO15_CNF	GPIO14_CNF	GPIO13_CNF	GPIO12_CNF	GPIO11_CNF	GPIO10_CNF	GPIO9_CNF	GPIO8_CNF

Name	Decription	Type
GPIOn_CNF	● When GPIOn_MODE[1:0] = 2'b01 and GPIO is in digital input mode, – GPIOn_CNF = 0, it provides a pull-up resistor. – GPIOn_CNF = 1, it provides a pull-down resistor. ● When GPIOn_MODE[1:0] = 2'b10 and GPIO is in digital output mode, – GPIOn_CNF= 0, it provides push-pull output. – GPIOn_CNF= 1, it provides open-drain output	R/W

- **CUS_PADCTL7 ~ CUSPADCTL8 register set**

CUS_PADCTL7 ~ 8 Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
7	GPIO7_IOC	GPIO6_ IOC	GPIO5_ IOC	GPIO4_IOC	GPIO3_ IOC	GPIO2_ IOC	GPIO1_ IOC	GPIO0_ IOC
8	GPIO15_ IOC	GPIO14_ IOC	GPIO13_ IOC	GPIO12_ IOC	GPIO11_ IOC	GPIO10_IOC	GPIO9_ IOC	GPIO8_ IOC

Name	Decription	Type
GPIOn_IOC	Set to 0 to disable the IOC interrupt/wake-up function of the GPIOn port. Set to 1 to enable the IOC interrupt/wake-up function of the GPIOn port.	R/W

- **CUS_PADCTL9 ~ CUSPADCTL10 register set**

CUS_PADCTL9 ~ 10 Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
9	GPIO7_IDR	GPIO6_ IDR	GPIO5_ IDR	GPIO4_ IDR	GPIO3_ IDR	GPIO2_ IDR	GPIO1_ IDR	GPIO0_ IDR
10	GPIO15_ IDR	GPIO14_ IDR	GPIO13_ IDR	GPIO12_ IDR	GPIO11_ IDR	GPIO10_IDR	GPIO9_ IDR	GPIO8_ IDR

Name	Decription	Type
GPIOn_IDR	GPIOn input status saving register Set to 0, input is 0, generate interrupt or wake up the chip when input is detected changing to 1. Set to 1, input is 1, generate interrupt or wake up the chip when input is detected changing to 0.	R/W

- **CUS_PADCTL11 ~ CUSPADCTL12 register set**

CUS_PADCTL11 ~ 12 Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
9	GPIO7_ODR	GPIO6_ ODR	GPIO5_ ODR	GPIO4_ ODR	GPIO3_ ODR	GPIO2_ ODR	GPIO1_ ODR	GPIO0_ ODR
10	GPIO15_ ODR	GPIO14_ ODR	GPIO13_ ODR	GPIO12_ ODR	GPIO11_ ODR	GPIO10_ ODR	GPIO9_ ODR	GPIO8_ ODR

Name	Decription	Type
GPIOn_ODR	GPIOn mode configuration 2. ● When GPIOn_MODE[1:0] = 2'b01 and GPIO is in digital input mode: – GPIOn_ ODR = 0, it provides a pull-up resistor. – GPIOn_ ODR = 1, it provides a pull-down resistor. ● When GPIOn_MODE[1:0] = 2'b10 and GPIO is in digital output mode: – GPIOn_ ODR = 0, both push-pull output and open-drain output output 0[1]. – GPIOn_ ODR = 1, push-pull output outputs 1, open-drain output has no output[1].	R/W

Notes

[1]. When the CMT216xA enters the Shut Down mode, part of the Block1 register will be reset, so the GPIO status can only be saved through the GPIO associated register in Block0, such as the output high/low state, the input with pull-up/pull-down. GPIOn_ODR is responsible for the function that, in Shut Down mode, it retains the status of whether the input port is with pull-up or pull-down, or whether the port outputs high or low. See CMT216xA User Guide for more details.

- **CUS_SYSCTL11 Register**

CUS_SYSCTL11 Reset value: 0x80

7	6	5	4	3	2	1	0
SLPT_MANU_RSTN	Reserved	Reserved	SNOOZE_MANU_CLR	LBD_MANU_CLR	LFRX_MANU_CLR	SLPT_MANU_CLR	BUT_MANU_CLR

Name		Decription	Type
0	BUT_MANU_CLR	In SDN mode, the IOC interrupt manual clearing bit. When it is set to 1, it is automatially cleared.	R/W

- **CUS_SYSCTL12 Register**

CUS_SYSCTL12 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	SNOOZE_WAKEUP		WKID_PASS	SYNC_PASS	LFRX_SIGNAL_OK	SLEEP_TIMESUP	KEY_LAUNCH

Name		Decription	Type
0	KEY_LAUNCH	IOC triggering being active flag. It is active when being read as 1.	R

- **CUS_SYSCTL20 Register**

CUS_SYSCTL20 Reset value：0x13

7	6	5	4	3	2	1	0
Reserved	OTP_CP_VCC_SELN[1:0]		OTP_CP_VTH_SEL	GPIO16_ODR	GPIO16_CNF	GPIO16_MODE[1:0]	

Name		Decription	Type
3	GPIO16_ODR	For GPIO16 ODR configuration, please refer to GPIO[15:0] ODR configuration.	R/W
2	GPIO16_CNF	For GPIO16 CNF configuration, please refer to GPIO[15:0] CNF configuration.	R/W
1:0	GPIO16_MODE	For GPIO16 mode configuration, please refer to GPIO[15:0] mode configuration.	R/W

- **CUS_LFRX3 Register**

CUS_LFRX3 Reset value：0x2A

7	6	5	4	3	2	1	0
PD_P25	PD_P50	LFRX_AGC_IN[1:0]		LFRX_AGC_VHREF[3:0]			

Name		Decription	Type
7	PD_P25	Configure the output port load capacity. It is a common configuration of GPIO[16:0]: 2'b00, high speed (default). 2'b01, meduim speed. 2'b10, low speed. 2'b11, super-low speed.	R/W
6	PD_P50		R/W

- **CUS_LFRX4 Register**

CUS_LFRX4 Reset value：0x55

7	6	5	4	3	2	1	0
Reserved	PD_PULLUP2	LFRX_AGC_CNT[1:0]		LFRX_AGC_VLREF[3:0]			

Name		Decription	Type
6	PD_PULLUP2	Valid for all GPIO[16:0]. Set to 0 to enable the 500 kΩ pull-up resistor[1] Set to 1 to disable 500 kΩ pull-up resistor	R/W

Notes [1]：

1. *The 500 kΩ is a weak pull-up, which is disabled by default. The pull-up mentioned above is a standard pull-up, which is about 47 kΩ;*
2. *The difference is that the standard pull-up supports independent enabling/disabling per each GPIOn, however the weak pull-up is enabled or disabled as a whole.*
3. *If both the 2 types of pull-ups are enabled at the same time, they are in parallel.*

- **CUS_SNOOZE6 Register**

CUS_SNOOZE6 Reset value：0x00

7	6	5	4	3	2	1	0
GPIO_HOLD	Reserved	Reserved	Reserved	DWTH_WK_INT	UPTH_WK_INT	WOUT_WK_INT	WIN_WK_INT

Name		Decription	Type
7	GPIO_HOLD	GPIO[16:0] output mapping value selection[1]: – Se to 0, output the digital output mapping value. – Se to 1, output the value of GPIOn_ODR register.	R/W

Notes[1]. It is recommended to configure the output port status that is required to be retained in GPIOn_ODR before entering Shut Down mode, then set GPIO to 1 and enter the Shut Down mode. Upon waking-up (to Active mode), clear this bit for operation convenience. See the CMT216xA User Guide for details.

- **P0_IN_SEL0 ~ P0_IN_SEL3 register set**

P0_IN_SEL0/1/2/3 Reset value：0x00/0x00/0x00/0x00

	7	6	5	4	3	2	1	0
0	PORT01_IN_GPIO_SEL[3:0]				PORT00_IN_GPIO_SEL[3:0]			
1	PORT03_IN_GPIO_SEL[3:0]				PORT02_IN_GPIO_SEL[3:0]			
2	PORT05_IN_GPIO_SEL[3:0]				PORT04_IN_GPIO_SEL[3:0]			
3	PORT07_IN_GPIO_SEL[3:0]				PORT06_IN_GPIO_SEL[3:0]			

Name	Decription	Type
PORT0n_IN_GPIO_SEL	When 8051core Port0 is input port, the mapping with GPIOn is: 4’b0000, map to GPIO0 input, corresponding to the A0 pin. 4’b0001, map to GPIO1 input, corresponding to the A11pin. 4’b0010, map to GPIO2 input, corresponding to the A2 pin. …… 4’b0111, map to GPIO7 input, corresponding to the A7 pin. 4’b1000, map to GPIO8 input, corresponding to the B0 pin. …… 4’b1110, map to GPIO14 input, corresponding to the B6 pin. 4’b1111, map to GPIO15 input, corresponding to the B7 pin.	R/W

- **GPIO_IN_R_H/GPIO_IN_R_L register set**

GPIO_IN_R_H/L Reset value：0x00/0x00

	7	6	5	4	3	2	1	0
H	GPIO_IN_R[15:8](IN)							
L	GPIO_IN_R[7:0](IN)							

Name	Decription	Type
GPIO_IN_R[15:0]	GPIOn input mode mapping register. The range of n is 0 ~ 15.	R/W

- **GPIO_OUT_R_H/GPIO_OUT_R_L register set**

GPIO_OUT_R_H/L Reset value：0x00/0x00

	7	6	5	4	3	2	1	0
H	GPIO_OUT_R[15:8](IN)							
L	GPIO_OUT_R[7:0](IN)							

Name	Decription	Type
GPIO_OUT_R[15:0]	GPIOn output mode mapping register. The range of n is 0 ~ 15.	R/W

- **GPIO_IN_R_D1**

GPIO_IN_R_D1 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved							GPIO_IN_R[16]

Name	Decription	Type
GPIO_IN_R[16]	GPIO16 (namely D1) input mode mapping register	R

- **GPIO_OUT_R_D1**

GPIO_OUT_R_D1 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved							GPIO_OUT_R[16]

Name	Decription	Type
GPIO_OUT_R[16]	GPIO16 (namely D1) output mode mapping register.	R/W

- **GPIO_OUT_SEL0 ~ GPIO_OUT_SEL7 register set**

GPIO_OUT_SEL0～GPIO_OUT_SEL7 Reset value: all 0x00

	7	6	5	4	3	2	1	0
0	GPIO1_OUT_SEL[3:0]				GPIO0_OUT_SEL[3:0]			
1	GPIO3_OUT_SEL[3:0]				GPIO2_OUT_SEL[3:0]			
2	GPIO5_OUT_SEL[3:0]				GPIO4_OUT_SEL[3:0]			
3	GPIO7_OUT_SEL[3:0]				GPIO6_OUT_SEL[3:0]			
4	GPIO9_OUT_SEL[3:0]				GPIO8_OUT_SEL[3:0]			
5	GPIO11_OUT_SEL[3:0]				GPIO10_OUT_SEL[3:0]			
6	GPIO13_OUT_SEL[3:0]				GPIO12_OUT_SEL[3:0]			
7	GPIO15_OUT_SEL[3:0]				GPIO14_OUT_SEL[3:0]			

<table>
<tr><th>Name</th><th>Decription</th><th>Type</th></tr>
<tr><td>GPIOn_OUT_SEL</td><td>The mapping configuration of GPIOn when it operates as output:
<table>
<tr><th>Value</th><th>Binary</th><th>Function Description</th></tr>
<tr><td>0</td><td>4’b0000</td><td>Map to GPIO_OUT_R[15:0], namely control input status through the 2 registers, GPIO_OUT_R_H/L with one-to-one correspondence. For example, GPIO1 is corresponding to GPIO_OUT_R_L Bit1. This is the default value of GPIOn output.</td></tr>
<tr><td>1</td><td>4’b0001</td><td>Map to Port0 output. Both GPIO[7:0] and GPIO[15:8] can be configured to the corresponding Port0[7:0] with one-to-one correspondence. For example, GPIO7 or GPIO15 can be mapped to Port0.7, and GPIO10 or GPIO2 can be mapped to Port0.2. When this value is selected, GPIOn can be controlled through Port0.n output control.s</td></tr>
<tr><td>2</td><td>4’b0010</td><td>Map to TB_OUT0, TimerB captures/compares module 0 output.</td></tr>
<tr><td>3</td><td>4’b0011</td><td>Map to TB_OUT1, TimerB capture/compare module 1 output.</td></tr>
<tr><td>4</td><td>4’b0100</td><td>Map to TB_OUT2, TimerB capture/compare module 2 output.</td></tr>
<tr><td>5</td><td>4’b0101</td><td>Map to NSS_OUT, SPI module master mode chip selection output.</td></tr>
<tr><td>6</td><td>4’b0110</td><td>Map to SCK_OUT, SPI module master mode clock output.</td></tr>
<tr><td>7</td><td>4’b0111</td><td>Map to MISO_OUT, SPI module Slave mode data output.</td></tr>
<tr><td>8</td><td>4’b1000</td><td>Map to MOSI_OUT, SPI module Master mode data output.</td></tr>
<tr><td>9</td><td>4’b1001</td><td>Map to RxD0_OUT, UART module output enabling signal.</td></tr>
<tr><td>10</td><td>4’b1010</td><td>Map to TxD_OUT, UART module clock or data output.</td></tr>
<tr><td>11</td><td>4’b1011</td><td>Map to TA_OUT0, TimerA captures/compares module 0 output.</td></tr>
<tr><td>12</td><td>4’b1100</td><td>Map to TA_OUT1, TimerA capture/compare module 1 output.</td></tr>
<tr><td>13</td><td>4’b1101</td><td>Map to TA_OUT2, TimerA capture/compare module 2 output.</td></tr>
<tr><td>14</td><td>4’b1110</td><td>Map to LED_OUT_LV, the PWM output generated by LED module.</td></tr>
<tr><td>15</td><td>4’b1111</td><td>Map to T1_OV, overflow flag of Timer1 module.</td></tr>
</table></td><td>R/W</td></tr>
</table>

3.4 LED Module

Table 5. LED Module Register Set List

Name	Area	Sub-area	Address	Reset	Function
CUS_SYSCTL3	Block0	--	0x50	0x00	System control register 3
LED_CTL	Block1	Bank0	0xCC	0x00	LED control register

- **CUS_SYSCTL3 Register**

CUS_SYSCTL3 Reset value：0x00

7	6	5	4	3	2	1	0
LED_INV	AFE_IR_EN	SNOOZE_EN	SNOOZE_DEBUG_EN	LFRX_DEBUG_EN	LFRX_EN	SLPT_WAKEUP_MODE	SLEEP_TIMER_EN

Name		Decription	Type
7	LED_INV	LED module output direction enabling Set to 0, high level is normal state and low level drives LED. Set to 1, low level is normal state and high level drives LED.	R/W

- **LED_CTL Register**

LED_CTL Reset value：0x00

7	6	5	4	3	2	1	0
SAR_DATA_UPDATE	LED_ON	LED_OUT_SEL	PWM_RATE_SEL	PWM_INTERVAL_SEL[3:0]			

Name		Decription	Type
6	LED_ON	LED module enabling. 0: disable. 1, enable.	R/W
5	LED_OUT_SEL	LED module output mode selection: Set to 0, output TX baseband data. Set to 1, output PWM signal.	R/W
4	PWM_RATE_SEL	PWM frequency selection (if LED_OUT_SEL selects the PWM signal as valid signal): Set to 0, PWM is 3.34 kHz. Set to 1, PWM is 6.68 kHz.	R/W
3:0	PWM_INTERVAL_SEL	PWM duty cycle selection, ranging from 0 to 15 with 16 levels of duty cycle, each level increasing by 1 / 16.	R/W

3.5 S3S Programming Interface

Table 6. SPI Module Register Set List

Name	Area	Sub-area	Address	Reset	Function
INT_SYSCTL3	Block0	--	0x44		INT system control register 3

- **INT_SYSCTL3 register**

INT_SYSCTL3 Reset value: 0xC4

7	6	5	4	3	2	1	0
Reserved	Reserved	S3S_DISABLE	Reserved				

Name		Decription	Type
5	S3S_DISABLE	S3S debug port function enabling control (control PB1 ~ PB4, namely GPIO9 ~ GPIO12). Set to 0, the S3S debug port is used as a programming port. Set to 1, S3S is used as GPIO.	R/W

3.6 LBD Module

Table 7. LBD Module Register Set List

Name	Area	Sub-area	Address	Reset	Function
CUS_SYSCTL11	Block0	--	0x68	0x80	System control register 11
CUS_SYSCTL13	Block0	--	0x6A	0x00	System control register 13
CUS_SYSCTL16	Block0	--	0x6D	0x00	System control register 16
CUS_SYSCTL17	Block0	--	0x6E	0x00	System control register 17
LBD_CTL	Block1	Bank1	0xC0	0x24	LBD control register

- **CUS_SYSCTL11 register**

CUS_SYSCTL11 Reset value：0x80

7	6	5	4	3	2	1	0
SLPT_MANU_RSTN	Reserved	Reserved	SNOOZE_MANU_CLR	LBD_MANU_CLR	LFRX_MANU_CLR	SLPT_MANU_CLR	BUT_MANU_CLR

Name		Decription	Type
3	LBD_MANU_CLR	When the low voltage detection is completed, it needs clear the end flag manually. When set to 1, the system clears it automatically.	R/W

- **CUS_SYSCTL13 register**

CUS_SYSCTL13 Reset value：0x00

7	6	5	4	3	2	1	0
LBD_STATUS	LBD_FINISH	LBD_AVG_SEL	LBD_ENABLE	Reserved	SAR_MSTART	SAR_TRIGGER	SAR_CLK_EN

Name		Decription	Type
7	LBD_STATUS	Low voltage detection results. Read as 0, the power supply voltage is higher than the set threshold. Read as 1, the power supply voltage is lower than the set threshold.	R
6	LBD_FINISH	Low voltage detection end flag.	R
5	LBD_AVG_SEL	Low voltage detection result (LBD_RESULT) sampling times selection. Set to 0, average the the results of 8 successive samplings Set to 1, sample once for measurement.	R/W
4	LBD_ENABLE	Set to 0, LBD module is disabled. Set to 1, LBD module is enabled.	R/W

- **CUS_SYSCTL16 register**

CUS_SYSCTL16 Reset value：0x00

7	6	5	4	3	2	1	0
LBD_TH[7:0]							

Name	Decription	Type
LBD_TH	Low voltage detection comparison threshold	R/W

- **CUS_SYSCTL17 register**

CUS_SYSCTL17 Reset value：0x00

7	6	5	4	3	2	1	0
LBD_RESULT[7:0]							

Name	Decription	Type
LBD_RESULT	Low voltage detection result	R

Note: The low-voltage detection module uses VBG (1.2V) as the reference voltage and measures VBAT / 4 (VDD / 4), so setting LBD_TH or reading LBD_RESULT is calculated according to the following formulas.

$$\text{LBD\_TH} = \frac{V_{\text{LBD}_{TH}}}{4.8} \times 255$$

$$V_{BAT} = \frac{LBD\_RESULT}{255} \times 4.8V$$

- **LBD_CTL register**

LBD_CTL Reset value：0x24

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	LBD_FLAG	LBD_VTH_SEL	LBD_POR_EN	LBD_ON

Name		Decription	Type
3	LBD_FLAG	Voltage monitoring flag. Read as 0, in normal. Read as 1, voltage is lower than the monitoring threshold.	R
2	LBD_VTH_SEL	Voltage monitoring threshold selection. Set to 0, the monitoring threshold is 1.8 V. Set to 1, the monitoring threshold is 2.0 V.	R/W
1	LBD_POR_EN	Whether the power supply resets the chip when the power supply voltage is lower than the monitoring threshold (LBD_VTH_SEL selection). Set to 0, not reset. Set to 1, reset (this reset is equivalent to re-poweron).	R/W
0	LBD_ON	Set to 0, the power supply voltage monitoring is disabled. Set to 1, the power supply voltage monitoring is enabled.	R/W

Notes:

1. *Suggest users call the API sys_start_stop_supply_voltage_supervision to configure of LBD monitoring rather than configure this register directly since the LBD voltage monitoring function still requires other related configurations.*
2. *Users can either read LBD_FLAG or call the API call the API function sys_read_result_from_supply_voltage_supervision to query the voltage monitoring status.*

3.7 SPI Register Set

Table 8. SPI Module Register Set List

Name	Area	Sub-area	Address	Reset	Function
SPI_CTL1_H	Block1	Bank0	0x91	0x00	SPI module control register1 higher byte
SPI_CTL1_L	Block1	Bank0	0x92	0x00	SPI module control register1 lower byte
SPI_CTL2_H	Block1	Bank0	0x93	0x02	SPI module control register2 higher byte
SPI_DATA_H	Block1	Bank0	0x95	0x00	SPI module data higher byte
SPI_DATA_L	Block1	Bank0	0x96	0x00	SPI module data lower byte
SPI_IN_SEL0	Block1	Bank0	0xBA	0x00	SPI input signal and GPIO mapping register0
SPI_IN_SEL1	Block1	Bank0	0xBB	0x00	SPI input signal and GPIO mapping register1

- **SPI_CTL1_H register**

SPI_CTL1_H Reset value：0x00

7	6	5	4	3	2	1	0
BIDI_MODE	BIDI_OE	RX_ONLY	DFF	TXDMAEN	SSOE	SSM	SSI

Name		Decription	Type
7	BIDI_MODE	SPI module bidirectional data mode selection: Set to 0, select 2-wire bidirectional mode, namely, 4-wire SPI mode. Set to 1, select single line bidirectional mode, namely, 3-wire SPI mode.	R/W
6	BIDI_OE	Data line output direction in the single line bidirectional mode (BIDI_MODE = 1): Set to 0, the output is disabled (receiving-only mode). Set to 1, the output is enabled (sending-only mode). Note: in the single line bidirectional mode, on the host side, if the host is the sender, the data line is mosi. Otherwise, the data line is miso. On the slave side, if the slave is the sender, the data line is miso. Otherwise, the data line is mosi	R/W
5	RX_ONLY	In the 2-line bidirectional mode (BIDI_MODE = 0), for multiple slave configuration, set this bit to 1 to let only the accessed slave devices output, so that no data conflicts will occur in the data line. Set to 0, full duplex (transmiting and receiving); Set to 1, disable output (receiving-only);	R/W
4	DFF	Data frame format selection. Set to 0, transmit or receive using a 8-bit data frame format. Set to 1, transmit or receive using a 16-bit data frame format.	R/W
3	TXDMAEN	SPI DMA function enabling bit: Set to 0, disable the DMA function. Set to 1, enable the DMA function.	R/W
2	SSOE	SS output enabling: Set to 0 to disable SS output in the master mode. The device can operate in the multi-master mode. Set to 1,enable SS output in the master mode, the device can not operate in the multi-master mode.	R/W

Name		Decription	Type
1	SSM	Software slave device management. When set to 1, the level on the NSS pin is determined by the value of the SSI bit. Set to 0, disable software slave device management. Set to 1, enable software slave device management.	R/W
0	SSI	Internal slave device selection. Valid when SSM = 1. It determines the level on the NSS. The IO operation on the NSS pin is invalid in this case.	R/W

- **SPI_CTL1_L register**

SPI_CTL1_L Reset value：0x00

7	6	5	4	3	2	1	0
LSB_FIRST	SPE	BR[2:0]			MSTR	CPOL	CPHA

Name		Decription	Type
7	LSB_FIRST	Frame format selection. Set to 0, transmit MSB first. Data shifts to the left. Set to 1, transmit LSB first. Data shifts to the right.	R/W
6	SPE	SPI module enabling bit: Set to 0, disable SPI module. Set to 1, enable SPI module.	R/W
5:3	BR[2:0]	SPI baud rate selection (F_{PCLK} system clock, detault as 24 MHz). 3'b000, baud rate is F_{PCLK}/2. 3'b001, baud rate is F_{PCLK} /8. 3'b010, baud rate is F_{PCLK} /16. 3'b011, baud rate is F_{PCLK} /24. 3'b100, baud rate is F_{PCLK} /32. 3'b101, baud rate is F_{PCLK} /64. 3'b110, baud rate is F_{PCLK} /128. 3'b111, baud rate is F_{PCLK} /256.	R/W
2	MSTR	Master and slave mode selection. Set to 0, configure as slave mode. Set to 1, configure as master mode.	R/W
1	CPOL	SPI clock polarity. Set to 0, in the idle state, SCK remains low. Set to 1, in the idle state, SCK remains high.	R/W
0	SSOE	SPI clock phase. Set to 0, data sampling begins on the first clock edge. Set to 1, data sampling begins on the second clock edge.	R/W

Notes: When data communication is ongoing, cannot modify this register's value.

- **SPI_CTL2_H register**

SPI_CTL2_H Reset value：0x02

7	6	5	4	3	2	1	0
Reserved					SPI_BUSY	SPI_TXE	SPI_RXNE

Name		Decription	Type
2	SPI_BUSY	SPI busy flag. Read as 0, SPI not busy. Read as 1, SPI busy in communication, or tranmission buffer not empty. Notes: This bit is set or reset by the hardware. In the master mode with receiving-only (single line bidirectional), it is forbidden to check the flag.	R/W
1	SPI_TXE	SPI transmitting buffer not empty. Read as 0, transmitting buffer not empty. Read as 1, transmitting buffer empty.	R/W
0	SPI_RXNE	SPI receiving buffer not empty. Read as 0, receiving buffer not empty. Read as 1, receiving buffer empty.	R/W

- **SPI_DATA_H/SPI_DATA_L register set**

SPI_CTL2_H/L Reset value：0x00/0x00

	7	6	5	4	3	2	1	0
H	SPI_DATA[15:8]							
L	SPI_DATA[7:0]							

Name	Decription	Type
SPI_TXDATA	SPI data register, buffering data to be sent or received. The data register has two buffers, one for writing (sending buffer), the other for reading (receiving buffer). A write operation writes data to the sending buffer; a read operation returns the data in the receiving buffer.	R/W

- **SPI_IN_SEL0/SPI_IN_SEL1 register set**

SPI_IN_SEL0/1 Reset value：0x00/0x00

	7	6	5	4	3	2	1	0
0	SCK_IN_SEL[3:0]				NSS_IN_SEL[3:0]			
1	MOSI_IN_SEL[3:0]				MISO_IN_SEL[3:0]			

Name	Decription	Type
NSS_IN_SEL	In SPI bus slave mode, chip selection input signal maps to GPIO[15:0]	R/W
SCK_IN_SEL	In SPI bus Slave mode, clock input signal maps to GPIO[15:0]	R/W
MISO_IN_SEL	In SPI bus Master mode, data input signal maps GPIO[15:0]	R/W
MOSI_IN_SEL	In SPI bus Slave mode, data input signal maps to GPIO[15:0]	R/W

Notes:

1. The selection mapping is as follows.
   4’b0000, mapping to GPIO0 input, corresponding to A0 pin.
   4’b0001, mapping to GPIO1 input, corresponding to A1 pin.
   -4’b0010, mapping to GPIO2 input, corresponding to A2 pin.
   ...
   4’b0111, mapping to GPIO7 input, corresponding to A7 pin.
   4’b1000, mapping to GPIO8 input, corresponding to B0 pin.
   ...
   4’b1110, mapping to GPIO14 input, corresponding to B6 pin.
   4’b1111, mapping to GPIO15 input, corresponding to B7 pin.

3.8 UART Register Set

Table 9. UART Register Set List

Name	Area	Sub-area	Address	Reset	Function
SCON0	Block1	Bank0	0x98	0x00	Series port 0 control register.
PCON	Block1	Bank0	0x87	0x00	Power consumption control register, refer to Section 3.1 for details.
SBUF0	Block1	Bank0	0x99	0x00	Port 0 data buffer register.
USART_CTL	Block1	Bank0	0x97	0x00	UART control register.
TIMER_IN_SEL	Block1	Bank0	0xB7	0x00	Timer1 input selection register.

- **SCON0 Register**

SCON0 Reset value：0x00

7	6	5	4	3	2	1	0
FE0/SM00	SM10	SM20	REN0	TB80	RB80	TI0	RI0

Name		Decription	Type
7	FE0	Series port 0 frame error flag. When PON.6 = 1, access is valid. When an incorrect STOP bit is received, it is set to 1 by the hardware automatically.	R/W
7	SM00	Series port 0 mode configuration Bit0. When PCON.6 = 0, access is valid. Cooperate with SM10 and SM20 series port 0 operating mode configuration.	R/W
6	SM10	Series port 0 mode configuration bit1: SM00 / SM10 / Mode / Description 0 / 0 / 0 / Synchronous shift register. Fix to F_{PCLK}/12 baud rate. 0 / 1 / 1 / 8-bit UART, configurable baud rate and clock generated by Timer1. 1 / 0 / 2 / 9-bit UART, F_{PCLK}/64 or F_{PCLK}/32 baud rate. 1 / 1 / 3 / 9-bit UART, baud rate is configurable and clock is generated by Timer1.	R/W
5	SM20	Series port 0 mode configuration bit2, namely multimachine control bit.	R/W
4	REN0	Serial receiving enabling bit. In the UART mode, set to 1 to enable receiving. In mode 0, set to start data input transfer. Must clear it to 0 to enable data output transfer (write to SBUF0)	R/W
3	TB80	The 9th bit of 9-bit transmitting mode.	R/W
2	RB80	The 9th bit of 9-bit receiving mode.	R/W
1	TI0	Series port 0 transmitting interrupt flag.	R/W
0	RI0	Series port 0 receiving interrupt flag.	R/W

- **SBUF0 register**

SBUF0 Reset value：0x00

7	6	5	4	3	2	1	0
SBUF0[7:0]							

Name	Decription	Type
SBUF0	Series port 0 data buffer	R/W

- **USART_CTL register**

USART_CTL Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UART_SEL

Name		Decription	Type
0	UART_SEL	UART baud rate ehancement control bit. Set to 0, disable. Set to 1, enable.	R/W

Notes: When this bit is set, the preset frequency division by 12 of timer1 is closed. In this case, for UART1 and UART3 modes, it can fulfill multiple more accurate baud rates. Refer to CMT216xA User Guide for more details.

- **TIMER_IN_SEL register**

TIMER_IN_SEL Reset value：0x00

7	6	5	4	3	2	1	0
T1_GPIO_SEL[3:0]				RXD0_IN_GPIO_SEL[3:0]			

Name		Decription	Type
3:0	RXD0_IN_GPIO_SEL	UART0 external input signal selection, with configurably mapping to GPIO[15:0]. 4’b0000, corresponding to GPIO0, namely A0 pin. 4’b0001, corresponding to GPIO1, namely A1 pin. ... 4’b0111, corresponding to GPIO7, namely A7 pin. 4’b1000, corresponding to GPIO8, namely B0 pin. 4’b1001, corresponding to GPIO9, namely B1 pin. ... 4’b1111, corresponding to GPIO15, namely B7 pin.	R/W

3.9 16-Bit TimeA and TimerB Register Set

Table 10. 16-Bit TimerA and TimerB Register Set

Name	Area	Sub-area	Address	Reset	Function
TACLK_DIV_H	Block1	Bank0	0x9A	0x00	TimerA clock source frequency division register
TACLK_DIV_L	Block1	Bank0	0x9B	0x00	
TACH	Block1	Bank0	0x9C	0x00	TimerA control register
TACL	Block1	Bank0	0x9D	0x00	
TACNT_H	Block1	Bank0	0x9E	0x00	TimerA 16-bit real-time count register
TACNT_L	Block1	Bank0	0x9F	0x00	
TACCR0H	Block1	Bank0	0xA1	0x00	TimerA capture/compare module 0 register
TACCR0L	Block1	Bank0	0xA2	0x00	
TACCTL0H	Block1	Bank0	0xA3	0x40	TimerA capture/compare module 0 control register
TACCTL0L	Block1	Bank0	0xA4	0x00	
TACCR1H	Block1	Bank0	0xA5	0x00	TimerA capture/compare module 1 register
TACCR1L	Block1	Bank0	0xA6	0x00	
TACCTL1H	Block1	Bank0	0xA9	0x40	TimerA capture/compare module 1 control register
TACCTL1L	Block1	Bank0	0xAA	0x00	
TACCR2H	Block1	Bank0	0xAB	0x00	TimerA capture/compare module 2 register
TACCR2L	Block1	Bank0	0xAC	0x00	
TACCTL2H	Block1	Bank0	0xAD	0x40	TimerA capture/compare module 2 control register
TACCTL2L	Block1	Bank0	0xAE	0x00	
TACCI_SEL	Block1	Bank0	0xB9	0x00	TimerA capture module CCI and GPIO mapping
TBCLK_DIV_H	Block1	Bank1	0xD7	0x00	TimerB clock source frequency division register
TBCLK_DIV_L	Block1	Bank1	0xD8	0x00	
TBCH	Block1	Bank1	0xD9	0x00	TimerB control register
TBCL	Block1	Bank1	0xDA	0x00	
TBCCR0H	Block1	Bank1	0xDB	0x00	TimerB capture/compare module 0 register
TBCCR0L	Block1	Bank1	0xDC	0x00	
TBCCTL0H	Block1	Bank1	0xDD	0x40	TimerB capture/compare module 0 control register
TBCCTL0L	Block1	Bank1	0xDE	0x00	
TBCCR1H	Block1	Bank1	0xDF	0x00	TimerB capture/compare module 1 register
TBCCR1L	Block1	Bank1	0xE1	0x00	
TBCCTL1H	Block1	Bank1	0xE2	0x40	TimerB capture/compare module 1 control register
TBCCTL1L	Block1	Bank1	0xE3	0x00	
TBCCR2H	Block1	Bank1	0xE4	0x00	TimerB capture/compare module 2 register
TBCCR2L	Block1	Bank1	0xE5	0x00	
TBCCTL2H	Block1	Bank1	0xE7	0x40	TimerB capture/compare module 2 control register
TBCCTL2L	Block1	Bank1	0xE8	0x00	
TBCCI_SEL	Block1	Bank1	0xE9	0x00	TimerB capture module CCI and GPIO mappin, see Section 3.7 for details.
TBCNT_H	Block1	Bank1	0xEA	0x00	TimerB 16-bit real-time count register

Name	Area	Sub-area	Address	Reset	Function
TBCNT_L	Block1	Bank1	0xEB	0x00	

- **TACLK_DIV, TimerA clock source division register**

TACLK_DIV_H & TACLK_DIV_L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TACLK_DIV[15:8]							
L	TACLK_DIV[7:0]							

Name	Decription	Type
TACLK_DIV	TimerA clock source division factor. TACLK = FPCLK/TACLK_DIV, FPCLK is system clock, defualt as 24MHz. The TACLK_DIV range is 1～65535.	R/W

- **TACH, TimerA control register higher byte**

TACH Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	TA_START	TACCI3	TACCI2

Name		Decription	Type
2	TA_START	TimerA enabling bit. Set to 1, enable the TimerA module. Set to 0, disable the TimerA module.	R/W
1	TACCI3	Software configurable capture source input 3.	R/W
0	TACCI2	Software configurable capture source input 2.	R/W

- **TACL and TimerA control register lower byte**

TACL Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	TA_CNT_MODE[1:0]		TA_CLR	TMRA_IE	TMRA_IFG

Name		Decription	Type
4:3	TA_CNT_MODE	TimerA count mode selection. 2'b00, Stop mode, TimerA stopping count mode. 2'b01, Up mode, TimerA up count mode. 2'b10, Continuous mode, TimerA continuous count mode. 2'b11, Up / Down mode, Timer up and down count mode.	R/W
2	TA_CLR	TimerA clearing control bit. When set, it will reset TACNT, count direction, TACLK_DIV_H, TACLK_DIV_L, and TimerA related registers except register TACH/TACL.	R/W
1	TMRA_IE	TimerA interrupt enabling bit. When set to 1, run TimerA count interrupt request.	R/W
0	TMRA_IFG	TimerA counts the interrupt flag, which is set when the TACNT count returns to 0 again.	R/W

- **TACNT_H/TACNT_L, TimerA real-time count register**

TACNT_H & TACNT_L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TACNT[15:8]							
L	TACNT[7:0]							

Name	Decription	Type
TACNT	TimerA's real-time count value, read-only register, can be cleared by TA_CLR	R

- **TACCR0H/TACCR0L, TimerA capture/compare module 0 register**

TACCR0H & TACCR0L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TACCR0[15:8]							
L	TACCR0[7:0]							

Name	Decription	Type
TACCR0	TimerA capture/compare module 0 register. In compare mode, it saves the data that TACNT needs to compare with. In capture mode, it saves the count value of Timer A upon successful capture.	R/W

- **TACCTL0H, TimerA capture/compare module 0 control register higher byte**

TACCTL0H Reset value：0x40

7	6	5	4 3	2 1	0
Reserved	TACCR0_CCI	TACCR0_SCCI	TACCR0_CM[1:0]	TACCR0_CCIS[1:0]	TACCR0_CAP

Name		Decription	Type
6	TACCR0_CCI	The value of the selected capture source, which can be read by the software.	R
5	TACCR0_SCCI	When EQUx is valid, the selected captured value is stored and can be read by software.	R
4:3	TACCR0_CM	Capture mode selection. 2'b00, not captured. 2'b01, capture the rising edg. 2'b10, capture the falling edge. 2'b11, capture double edges.	R/W
2:1	TACCR0_CCIS	Capture source selection. 2'b00, TACCI0. 2'b01, TACCI1. 2'b10, TACCI2. 2'b11, TACCI3. Among them, TACCI0 and TACCI1 are from GPIO mapping (see TACCI_SELregister), TACCCI2 and TACCI3 are from register (see TACHregister);	R/W
0	TACCR0_CAP	Set to 0 to select the comparison mode. Set to 1, select the capture mode.	R/W

- **TACCTL0L, TimerA capture/compare module 0 control register lower byte**

TACCTL0L Reset value：0x00

7	6	5	4	3	2	1	0
TACCR0_SCS	TACCR0_OUTMODE[2:0]			TACCR0_IE	TACCR0_OUT	TACCR0_COV	TACCR0_IFG

Name		Decription	Type
7	TACCR0_SCS	Set to 0, the selected capture source is not synchronized with the system clock. Set to 1, the selected capture source is synchronized with the system clock.	R/W
6:4	TACCR0_OUTMODE	Output mode selection: 3'b000, direct output mode. 3'b001, set output mode. 3'b010, reverse/reset output mode. 3'b011, set/reset output mode; 3'b100, reverse output mode. 3'b101, reset output mode. 3'b110, reverse /set output mode. 3'b111, reset /set output mode. Note: The function is explained in detail in the Section *TimerA / B* in *CMT16xA User Guide*.	R/W
3	TACCR0_IE	TimerA capture/compare module 0 interrupt enabling bit	R/W
2	TACCR0_OUT	Can only be used in output mode 0 (TACCR0_OUTMODE=0), get throught directly to the corresponding output signal	R/W
1	TACCR0_COV	Capture overflow flag. Reading as 1 means that the previous capture source triggering result is not read yet, the current trigger source is captured currently, and software clearing is required.	R/W
0	TACCR0_IFG	TimerA capture/compare 0 interrupt flag	R/W

- **TACCR1H/TACCR1L, TimerA capture/compare module1 register**

TACCR1H & TACCR1L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TACCR1[15:8]							
L	TACCR1[7:0]							

Name	Decription	Type
TACCR1	TimerA capture/compare module1 register. In compare mode, it saves the data required to be compared with TACNT. In capture mode, it saves the current count value of Timer A.	R/W

- **TACCTL1H, TimerA capture/compare module1control register higher byte**

TACCTL1H Reset value：0x40

7	6	5	4	3	2	1	0
Reserved	TACCR1_CCI	TACCR1_SCCI	TACCR1_CM[1:0]		TACCR1_CCIS[1:0]		TACCR1_CAP

Name		Decription	Type
6	TACCR1_CCI	The selected capture source value. Can be read by the software.	R
5	TACCR1_SCCI	When EQUx is valid, it saves the selected capture value. Can be read by the software.	R
4:3	TACCR1_CM	Capture mode selection. 2'b00, not capture. 2'b01, capture on the rising edge. 2'b10, capture on the falling edge. 2'b11, capture on both edges.	R/W
2:1	TACCR1_CCIS	Capture source selection. 2'b00, TACCI0. 2'b01, TACCI1. 2'b10, TACCI2. 2'b11, TACCI3. Among them, TACCI0 and TACCI1 come from GPIO mapping (see TACCI_SEL register for details). TACCCI2 and TACCI3 come from register (see TACH register for details).	R/W
0	TACCR1_CAP	Set to 0, select compare mode. Se to 1, select capture mode.	R/W

- **TACCTL1L, Timer A capture/compare module1 control register lower byte**

TACCTL1L Reset value：0x00

7	6	5	4	3	2	1	0
TACCR1_SCS	TACCR1_OUTMODE[2:0]			TACCR1_IE	TACCR1_OUT	TACCR1_COV	TACCR1_IFG

Name		Decription	Type
7	TACCR1_SCS	Set to 0, the selected capture source is not be synchronized with the system clock. Set to 1, the selected capture source is synchronized with the system clock.	R/W
6:4	TACCR1_OUTMODE	Output mode selection: 3’b000, direct output mode. 3’b001, set output mode. 3’b010, reverse/reset output mode. 3’b011, set/reset output mode; 3’b100, reverse output mode. 3’b101, reset output mode. 3’b110, reverse /set output mode. 3’b111, reset /set output mode. Note: The function is explained in detail in the Section TimerA / B in CMT16xA User Guide.	R/W

Name		Decription	Type
3	TACCR1_IE	TimerA capture/compare module 1 interrupt enabling bit.	R/W
2	TACCR1_OUT	Can only be used in output mode 0 (TACCR1_OUTMODE=0), get through directly to the corresponding output signal.	R/W
1	TACCR1_COV	Capture overflow flag. Reading as 1 means that the previous capture source triggering result is not read yet, the current trigger source is captured currently, and software clearing is required.	R/W
0	TACCR1_IFG	TimerA capture/compare 1 interrupt flag	R/W

- **TACCR2H/TACCR2L, TimerA capture/compare module 2 register**

TACCR2H & TACCR2L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TACCR2[15:8]							
L	TACCR2[7:0]							

Name	Decription	Type
TACCR2	TimerA capture/compare module 2 register, in compare mode, saves the data that TACNT needs to compare with. In capture mode, saves the count value of Timer A upon successful capture.	R/W

- **TACCTL2H, Timer A capture/compare module 2 control register higher byte**

TACCTL2H Reset value：0x40

7	6	5	4	3	2	1	0
Reserved	TACCR2_CCI	TACCR2_SCCI	TACCR2_CM[1:0]		TACCR2_CCIS[1:0]		TACCR2_CAP

Name		Decription	Type
6	TACCR2_CCI	The value of the selected capture source, which can be read by the software.	R
5	TACCR2_SCCI	When EQUx is valid, the selected captured value is stored and can be read by the software.	R
4:3	TACCR2_CM	Capture mode selection. 2'b00, not captured. 2'b01, capture the rising edge. 2'b10, capture the falling edge. 2'b11, capture double edges.	R/W
2:1	TACCR2_CCIS	Capture source selection. 2'b00, TACCI0. 2'b01, TACCI1. 2'b10, TACCI2. 2'b11, TACCI3. Among them, TACCI0 and TACCI1 are from GPIO mapping (see TACCI_SEL register), TACCCI2 and TACCI3 are from register (see TACHregister).	R/W
0	TACCR2_CAP	Set to 0, select the comparison mode. Set to 1, select the capture mode.	R/W

- **TACCTL2L, Timer A capture/compare module 2 control register lower byte**

TACCTL2L Reset value：0x00

7	6	5	4	3	2	1	0
TACCR2_SCS	TACCR2_OUTMODE[2:0]			TACCR2_IE	TACCR2_OUT	TACCR2_COV	TACCR2_IFG

Name		Decription	Type
7	TACCR2_SCS	Set to 0, the selected capture source is not be synchronized with the system clock. Set to 1, the selected capture source is synchronized with the system clock.	R/W
6:4	TACCR2_OUTMODE	Output mode selection: 3'b000, direct output mode. 3'b001, set output mode. 3'b010, reverse/reset output mode. 3'b011, set/reset output mode; 3'b100, reverse output mode. 3'b101, reset output mode. 3'b110, reverse /set output mode. 3'b111, reset /set output mode. Note: The function is explained in detail in the Section TimerA / B in CMT16xA User Guide.	R/W
3	TACCR2_IE	TimerA capture/compare module 2 interrupt enabling bit.	R/W
2	TACCR2_OUT	Can only be used in output mode 0 (TACCR1_OUTMODE=0), get through directly to the corresponding output signal.	R/W
1	TACCR2_COV	Capture overflow flag. Reading as 1 means that the previous capture source triggering result is not read yet, the current trigger source is captured currently, and software clearing is required.	R/W
0	TACCR2_IFG	TimerA capture/compare 2 interrupt flag	R/W

- **TACCI_SEL, TimerA input signal Selection**

TACCI_SEL Reset value：0x00

7	6	5	4	3	2	1	0
TACCI1_GPIO_SEL [3:0]				TACCI0_GPIO_SEL[3:0]			

Name	Decription	Type
TACCI0_GPIO_SEL[3:0]	TACCI0 input signal mapping to GPIO[15:0]	R/W
TACCI1_GPIO_SEL[3:0]	TACCI1 input signal mapping to GPIO[15:0]	R/W

Notes: TACCI0 and TACCI1 input signals are mapped as follows.

4'b0000, corresponding to GPIO0, namely A0 pin.

4'b0001, corresponding to GPIO1, namely, A1 pin.

...

4'b0111, corresponding to GPIO7, namely A7 pin.

4'b1000, corresponding to GPIO8, namely B0 pin.

4'b1001, corresponding to GPIO9, namely B1 pin.

...

4’b1111, corresponding to GPIO15, namely B7 pin.

- **TBCLK_DIV, TimerB clock source frequency division register**

TBCLK_DIV_H & TBCLK_DIV_L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TBCLK_DIV[15:8]							
L	TBCLK_DIV[7:0]							

Name	Decription	Type
TBCLK_DIV	TimerB clock source division factor. TBCLK = FPCLK / TBCLK_DIV, FPCLK is the system clock, the default is 24 MHz. The TBCLK_DIV range is 1 ~ 65535.	R/W

- **TBCH, TimerB control register higher byte**

TBCH Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	TB_START	TBCCI3	TBCCI2

Name		Decription	Type
2	TB_START	TimerB enabling bit. Set to 1 to enable the TimerB module. Set to 0 to disable the TimerB module;	R/W
1	TBCCI3	Software configurable capture source input 3	R/W
0	TBCCI2	Software configurable capture source input 2	R/W

- **TBCL, TimerB control register lower byte**

TBCL Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	TB_CNT_MODE[1:0]		TB_CLR	TMRB_IE	TMRB_IFG

Name		Decription	Type
4:3	TB_CNT_MODE	TimerB counting mode selection. 2'b00, stop mode, namely TimerB stoping count mode. 2'b01, count up mode, namely TimerB up counting mode. 2'b10, continuous mode, namely TimerB continuous counting mode. 2'b11, up/down mode, namely TimerB up and down counting mode.	R/W
2	TB_CLR	TimerB clearing control bit. When set to 1, resets TBCNT, count direction,TBCLK_DIV_H, TBCLK_DIV_L, and other TimerB related registers except registerTBCH/TBCL.	R/W
1	TMRB_IE	TimerB interrupt enabling bit. When set to 1, run TimerB count interrupt request	R/W
0	TMRB_IFG	TimerB count interrupt flag, which is set to 1 when the TBCNT count returns to 0 again.	R/W

- **TBCNT_H/TBCNT_L, TimerB realtime count register**

TBCNT_H & TBCNT_L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TBCNT[15:8]							
L	TBCNT[7:0]							

Name	Decription	Type
TBCNT	TimerB real-time count value, read-only register, can be cleared by TB_CLR	R

- **TBCCR0H/TBCCR0L, TimerB capture/compare module 0 register**

TBCCR0H & TBCCR0L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TBCCR0[15:8]							
L	TBCCR0[7:0]							

Name	Decription	Type
TBCCR0	TimerB capture/compare module 0 register. In compare mode, it saves the data that TBCNT needs to compare with. In capture mode, it saves the count value of Timer B opun successful capture.	R/W

- **TBCCTL0H, TimerB capture/compare module 0 control register higher byte**

TBCCTL0H Reset value：0x40

7	6	5	4	3	2	1	0
Reserved	TBCCR0_CCI	TBCCR0_SCCI	TBCCR0_CM[1:0]		TBCCR0_CCIS[1:0]		TBCCR0_CAP

Name		Decription	Type
6	TBCCR0_CCI	The value of the selected capture source, which can be read by the software.	R
5	TBCCR0_SCCI	When EQUx is valid, the selected captured value is stored and can be read by the software;	R
4:3	TBCCR0_CM	Capture mode selection. 2'b00, not captured. 2'b01, capture the rising edge. 2'b10, capture the falling edge. 2'b11, capture both edges.	R/W
2:1	TBCCR0_CCIS	Capture source selection. 2'b00, TBCCI0. 2'b01, TBCCI1. 2'b10, TBCCI2. 2'b11, TBCCI3. Among them, TBCCI0 and TBCCI1 are from GPIO mapping (see TBCCI_SEL register), TBCCCI2 and TBCCI3 are from register (see TBCH register).	R/W
0	TBCCR0_CAP	Set to 0 to select the compare mode. Set to 1, select the capture mode.	R/W

- **TBCCTL0L, TimerB capture/compare module 0 control register lower byte**

TBCCTL0L Reset value：0x00

7	6	5	4	3	2	1	0
TBCCR0_SCS	TBCCR0_OUTMODE[2:0]			TBCCR0_IE	TBCCR0_OUT	TBCCR0_COV	TBCCR0_IFG

Name		Decription	Type
7	TBCCR0_SCS	Set to 0, the selected capture source is not synchronized with the system clock. Set to 1, the selected capture source is synchronized with the system clock.	R/W
6:4	TBCCR0_OUTMODE	Output mode selection: 3'b000, direct output mode. 3'b001, set output mode. 3'b010, reverse/reset output mode. 3'b011, set/reset output mode; 3'b100, reverse output mode. 3'b101, reset output mode. 3'b110, reverse /set output mode. 3'b111, reset /set output mode. Note: The function is explained in detail in the Section TimerA / B in CMT16xA User Guide.	R/W
3	TBCCR0_IE	TimerB capture/compare module 0 interrupt enabling bit	R/W
2	TBCCR0_OUT	Can only be used in output mode 0 (TBCCR0_OUTMODE=0), get through directly to the corresponding output signal	R/W
1	TBCCR0_COV	Capture overflow flag. Reading as 1 means that the previous capture source triggering result is not read yet, the current trigger source is captured currently, and software clearing is required.	R/W
0	TBCCR0_IFG	TimerB capture/compare 0 interrupt flag.	R/W

- **TBCCR1H/TBCCR1L, TimerB capture/compare module 1 register**

TBCCR1H & TBCCR1L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TBCCR1[15:8]							
L	TBCCR1[7:0]							

Name	Decription	Type
TBCCR1	TimerB capture/compare module 1 register. In compare mode, it saves the data that TACNT needs to compare with. In capture mode, it saves the count value of Timer B upon successful capture.	R/W

- **TBCCTL1H, TimerB capture/compare module 0 control register higher byte**

TBCCTL1H Reset value：0x40

7	6	5	4	3	2	1	0
Reserved	TBCCR1_CCI	TBCCR1_SCCI	TBCCR1_CM[1:0]		TBCCR1_CCIS[1:0]		TBCCR1_CAP

Name		Decription	Type
6	TBCCR1_CCI	The value of the selected capture source, which can be read by the software.	R
5	TBCCR1_SCCI	When EQUx is valid, the selected captured value is stored and can be read by software.	R
4:3	TBCCR1_CM	Capture mode selection. 2'b00, not captured. 2'b01, capture the rising edge. 2'b10, capture the falling edge. 2'b11, capture both edges.	R/W
2:1	TBCCR1_CCIS	Capture source selection. 2'b00, TACCI0. 2'b01, TACCI1. 2'b10, TACCI2. 2'b11, TACCI3. Among them, TACCI0 and TACCI1 are from GPIO mapping (see TACCI_SELregister), TACCCI2 and TACCI3 are from register (see TACHregister);	R/W
0	TBCCR1_CAP	Set to 0 to select the comparison mode. Set to 1, select the capture mode.	R/W

- **TBCCTL1L, TimerB capture/compare module 1 control register lower byte**

TBCCTL1L Reset value：0x00

7	6	5	4	3	2	1	0
TBCCR1_SCS	TBCCR1_OUTMODE[2:0]			TBCCR1_IE	TBCCR1_OUT	TBCCR1_COV	TBCCR1_IFG

Name		Decription	Type
7	TBCCR1_SCS	Set to 0, the selected capture source is not synchronized with the system clock. Set to 1, the selected capture source is synchronized with the system clock.	R/W
6:4	TBCCR1_OUTMODE	Output mode selection: 3’b000, direct output mode. 3’b001, set output mode. 3’b010, reverse/reset output mode. 3’b011, set/reset output mode; 3’b100, reverse output mode. 3’b101, reset output mode. 3’b110, reverse /set output mode. 3’b111, reset /set output mode. Note: The function is explained in detail in the Section TimerA / B in CMT16xA User Guide.	R/W
3	TBCCR1_IE	TimerB capture/compare module 1 interrupt enabling bit	R/W
2	TBCCR1_OUT	Can only be used in output mode 0 (TACCR1_OUTMODE=0), get through directly to the corresponding output signal	R/W
1	TBCCR1_COV	Capture overflow flag. Reading as 1 means that the previous capture source triggering result is not read yet, the current trigger source is captured currently, and software clearing	R/W

Name		Decription	Type
		is required.	
0	TBCCR1_IFG	TimerB capture/compare 1 interrupt flag.	R

- **TBCCR2H/TBCCR2L, TimerB capture/compare module 2 register**

TBCCR2H & TBCCR2L Reset value：0x00, 0x00

	7	6	5	4	3	2	1	0
H	TBCCR2[15:8]							
L	TBCCR2[7:0]							

Name	Decription	Type
TBCCR2	TimerB capture/compare module 2 register. In compare mode, saves the data that TACNT needs to compare with. In capture mode, saves the count value of Timer B upon successful capture.	R/W

- **TBCCTL2H, TimerB capture/compare module 2 control register higher byte**

TBCCTL2H Reset value：0x40

7	6	5	4	3	2	1	0
Reserved	TBCCR2_CCI	TBCCR2_SCCI	TBCCR2_CM[1:0]		TBCCR2_CCIS[1:0]		TBCCR2_CAP

Name		Decription	Type
6	TBCCR2_CCI	The selected capture source value. Can be read by the software.	R
5	TBCCR2_SCCI	When EQUx is valid, it saves the selected capture value. Can be read by the software.	R
4:3	TBCCR2_CM	Capture mode selection. 2'b00, not capture 2'b01, capture on the rising edge. 2'b10, capture on the falling edge. 2'b11, capture on both edges.	R/W
2:1	TBCCR2_CCIS	Capture source selection. 2'b00, TBCCI0. 2'b01, TBCCI1. 2'b10, TBCCI2. 2'b11, TBCCI3. Among them, TBCCI0 and TBCCI1 come from GPIO mapping (see TACCI_SELregister for details). TBCCCI2 and TBCCI3 come from register（See TBCHregister for details.	R/W
0	TBCCR2_CAP	Set to 0 to select the comparison mode. Set to 1, select the capture mode.	R/W

- **TBCCTL2L, Timer B capture/compare module2 control register lower byte**

TBCCTL2L Reset value：0x00

7	6	5	4	3	2	1	0
TBCCR2_SCS	TBCCR2_OUTMODE[2:0]			TBCCR2_IE	TBCCR2_OUT	TBCCR2_COV	TBCCR2_IFG

Name		Decription	Type
7	TBCCR2_SCS	Set to 0, the selected capture source is not be synchronized with the system clock. Set to 1,the selected capture source is synchronized with the system clock	R/W
6:4	TBCCR2_OUTMODE	Output mode selection: 3'b000, direct output mode. 3'b001, set output mode. 3'b010, reverse/reset output mode. 3'b011, set/reset output mode; 3'b100, reverse output mode. 3'b101, reset output mode. 3'b110, reverse /set output mode. 3'b111, reset /set output mode. Note: The function is explained in detail in the Section TimerA / B in CMT16xA User Guide.	R/W
3	TBCCR2_IE	TimerB capture/compare module 2 interrupt enabling bit	R/W
2	TBCCR2_OUT	Can only be used in output mode 0（TBCCR2_OUTMODE=0）,pass directly to the corresponding output signal	R/W
1	TBCCR2_COV	Capture overflow flag. Reading as 1 means that the previous capture source triggering result is not read yet, the current trigger source is captured currently, and software clearing is required.	R/W
0	TBCCR2_IFG	TimerB capture/compare 2 interrupt flag	R/W

- **TBCCI_SEL, TimerB input signal selection**

TBCCI_SEL Reset value：0x00

7	6	5	4	3	2	1	0
TBCCI1_GPIO_SEL [3:0]				TBCCI0_GPIO_SEL[3:0]			

Name	Decription	Type
TBCCI0_GPIO_SEL[3:0]	TBCCI0 input signal mapping to GPIO[15:0]	R/W
TBCCI1_GPIO_SEL[3:0]	TBCCI1 input signal mapping to GPIO[15:0]	R/W

Notes:

Timer1 external input signal selection. Can map to GPIO[15:0].

4'b0000, corresponding to GPIO0, namely A0 pin.

4'b0001, corresponding to GPIO1, namely A1 pin.

……

4'b01114'b0001, corresponding to GPIO7, namely A7 pin.

4'b1000, corresponding to GPIO8, namely A8 pin.

4'b1001, , corresponding to GPIO9, namely A9 pin.

……

4'b1111, , corresponding to GPIO15, namely B7 pin.

3.10 3D Low-frequency Wakeup Register Set

Table 11. 3D Low-frequency Wakeup Register Set

Name	Storage Area	Sub-area	Address	Reset	Function
CUS_LFRX3	Block0	--	0x12	0x2A	Low-frequency wakeup configuration register3
CUS_LFRX4	Block0	--	0x13	0x55	Low-frequency wakeup configuration register4
CUS_LFRX5	Block0	--	0x14	0x8F	Low-frequency wakeup configuration register5
CUS_LFRX6	Block0	--	0x15	0xFE	Low-frequency wakeup configuration register6
CUS_LFRX7	Block0	--	0x16	0x61	Low-frequency wakeup configuration register7
CUS_LFRX8	Block0	--	0x17	0xB3	Low-frequency wakeup configuration register8
CUS_LFRX9	Block0	--	0x18	0xE4	Low-frequency wakeup configuration register9
CUS_LFRX10	Block0	--	0x19	0xEF	Low-frequency wakeup configuration register10
CUS_LFRX11	Block0	--	0x1A	0x15	Low-frequency wakeup configuration register11
CUS_LFRX12	Block0	--	0x1B	0x13	Low-frequency wakeup configuration register12
CAL_LFRX_TCAP2	Block0	--	0x34	0x10	Low-frequency wakeup Internal matching capacitor register2 (Z-axis antenna)
CAL_LFRX_TCAP1	Block0	--	0x35	0x10	Low-frequency wakeup Internal matching capacitor register1 (Y-axis antenna)
CAL_LFRX_TCAP0	Block0	--	0x36	0x10	Low-frequency wakeup Internal matching capacitor register0 (X-axis antenna)
CAL_LFRX_OSC_CODE	Block0	--	0x37	0x00	NA
CUS_SYSCTL3	Block0	--	0x50	0x00	System control register3
CUS_SYSCTL4	Block0	--	0x51	0x01	System control register4
CUS_SYSCTL5	Block0	--	0x52	0x00	System control register5, low-frequency receiving duty-cycle receiving T1 setting
CUS_SYSCTL6	Block0	--	0x53	0x00	System control register6, low- frequency receiving duty-cycle receiving T2 setting
CUS_SYSCTL7	Block0	--	0x54	0x00	System control register7, low-frequency receiving duty-cycle sleepint time setting 1
CUS_SYSCTL8	Block0	--	0x55	0x10	Low- frequency receiving duty-cycle sleepint time setting 2
CUS_SYSCTL9	Block0	--	0x56	0x29	System control register9
CUS_SYSCTL10	Block0	--	0x57	0x00	System control register10, Low- frequency receiving manual control state register
CUS_LFRX15	Block0	--	0x58	0x72	Low-frequency wakeup configuration register15
CUS_LFRX16	Block0	--	0x59	0xAD	Low-frequency wakeup configuration register16
CUS_LFRX17	Block0	--	0x5A	0x59	Low-frequency wakeup configuration register17, SyncValue[7:0]
CUS_LFRX18	Block0	--	0x5B	0x5A	Low-frequency wakeup configuration register18, SyncValue[15:8]
CUS_LFRX19	Block0	--	0x5C	0xA5	Low-frequency wakeup configuration register19, SyncValue[23:16]
CUS_LFRX20	Block0	--	0x5D	0x00	Low-frequency wakeup configuration register20, SyncValue[31:24]
CUS_LFRX21	Block0	--	0x5E	0x23	Low-frequency wakeup configuration register21, WakeupID[7:0]
CUS_LFRX22	Block0	--	0x5F	0x00	Low-frequency wakeup configuration register22, WakeupID[15:8]
CUS_LFRX23	Block0	--	0x60	0x00	Low-frequency wakeup configuration register23, WakeupID[23:16]

Name	Storage Area	Sub-area	Address	Reset	Function
CUS_LFRX24	Block0	--	0x61	0x00	Low-frequency wakeup configuration register24, WakeupID[31:24]
CUS_LFRX25	Block0	--	0x62	0x1C	Low-frequency wakeup configuration register25
CUS_LFRX26	Block0	--	0x63	0x50	Low-frequency wakeup configuration register26
CUS_LFRX27	Block0	--	0x64	0x31	Low-frequency wakeup configuration register27, low-frequency rate section
CUS_LFRX28	Block0	--	0x65	0x7C	Low-frequency wakeup configuration register28
CUS_LFRX29	Block0	--	0x66	0x65	Low-frequency wakeup configuration register29
CUS_LFRX30	Block0	--	0x67	0x1E	Low-frequency wakeup configuration register30
CUS_SYSCTL11	Block0	--	0x68	0x80	System control register11
CUS_SYSCTL12	Block0	--	0x69	0x00	System control register12
CUS_SYSCTL18	Block0	--	0x6F	0x00	System control register18
CUS_LFRX31	Block0	--	0x72	0x00	Low-frequency wakeup configuration register31
CUS_LFRX32	Block0	--	0x73	0x00	Low-frequency wakeup configuration register32
CUS_LFRX33	Block0	--	0x74	0x00	Low-frequency wakeup configuration register33
CLK_SYS_DIV	Block1	Bank0	0x8F	0x00	System clock division register
LFRX_IF_TH_H	Block1	Bank1	0xC1	0x00	Calibration frequency output capturing channel selection
LFRX_IF_TH_L	Block1	Bank1	0xC3	0x7D	Target frequency of Calibration

- **CUS_LFRX3 register**

CUS_LFRX3 Reset value：0x3F

7	6	5	4	3	2	1	0
PD_P25	PD_P50	LFRX_AGC_IN[1:0]		LFRX_AGC_VHREF[3:0]			

Name		Decription	Type
5:4	LFRX_AGC_IN	AGC input source select, generated by CMT216xA RFPDK	R/W
3:0	LFRX_AGC_VHREF	AGC reference upper threshold, generated by CMT216xA RFPDK	R/W

- **CUS_LFRX4 register**

CUS_LFRX4 Reset value：0x68

7	6	5	4	3	2	1	0
Reserved	PD_PULLUP2	LFRX_AGC_CNT[1:0]		LFRX_AGC_VLREF[3:0]			

Name		Decription	Type
5:4	LFRX_AGC_CNT	AGC detection count related to threshold, automatically generated by CMT216xA RFPDK.	R/W
3:0	LFRX_AGC_VLREF	AGC reference upper threshold, automatically generated by CMT216xA RFPDK	R/W

- **CUS_LFRX5 register**

CUS_LFRX5 Reset value：0x8F

7	6	5	4	3	2	1	0
LFRX_CADET_WIN[1:0]		LFRX_CADET_OK_CNT[1:0]		LFRX_PEAKDET_CLK[1:0]		LFRX_DATA_CLK[1:0]	

Name		Decription	Type
7:6	LFRX_CADET_WIN	Related to carrier frequency detection time window, automatically generated by CMT216xA RFPDK	R/W
5:4	LFRX_CADET_OK_CNT	Related to carrier frequency detection time window, automatically generated by CMT216xA RFPDK.	R/W
3:2	LFRX_PEAKDET_CLK	Related to carrier frequency detection time window, automatically generated by CMT216xA RFPDK.	R/W
1:0	LFRX_DATA_CLK	Demodulation data filter related configuration, automatically generated by CMT216xA RFPDK.	R/W

- **CUS_LFRX6 register**

CUS_LFRX6 Reset value：0xFE

7	6	5	4	3	2	1	0
LFRX_DATA_R0[1:0]		LFRX_DATA_R1[1:0]		LFRX_PEAKDET_C[1:0]		Reserved	

Name		Decription	Type
7:6	LFRX_DATA_R0	Demodulation data filter related configuration, automatically generated by CMT216xA RFPDK.	R/W
5:4	LFRX_DATA_R1	Demodulation data filter related configuration, automatically generated by CMT216xA RFPDK.	R/W
3:2	LFRX_PEAKDET_C	Peak detection related configuration, automatically generated by CMT216xA RFPDK.	R/W

- **CUS_LFRX7 register**

CUS_LFRX7 Reset value：0x61

7	6	5	4	3	2	1	0
LFRX_DATA_C1[3:0]				LFRX_DATA_C0[3:0]			

Name		Decription	Type
7:4	LFRX_DATA_C1	Demodulation data filter related configuration, automatically generated by CMT216xA RFPDK.	R/W
3:0	LFRX_DATA_C0	Demodulation data filter related configuration, automatically generated by CMT216xA RFPDK.	R/W

- **CUS_LFRX8 register**

CUS_LFRX8 Reset value：0xB3

7	6	5	4	3	2	1	0
LFRX_DATA_C3[3:0]				LFRX_DATA_C2[3:0]			

Name		Decription	Type
7:4	LFRX_DATA_C3	Demodulation data filter related configuration, automatically generated by CMT216xA RFPDK.	R/W

Name		Decription	Type
3:0	LFRX_DATA_C2	Demodulation data filter related configuration, automatically generated by CMT216xA RFPDK.	R/W

- **CUS_LFRX9 register**

CUS_LFRX9 Reset value：0xE4

7	6	5	4	3	2	1	0
LFRX_CMP_NOISE_MASK	LFRX_CMP_SW	LFRX_RSSIAMP_IBIAS[2:0]			LFRX_PGA_IBIAS[2:0]		

Name		Decription	Type
7	LFRX_AGC_CNT	Related to carrier frequency detection threshold configuration, automatically generated by CMT216xA RFPDK.	R/W
6	LFRX_AGC_VLREF	Related to carrier frequency detection threshold configuration, automatically generated by CMT216xA RFPDK.	R/W
5:3	LFRX_RSSIAMP_IBIAS	Related to signal link power configuration configuration, automatically generated by CMT216xA RFPDK.	R/W
2:0	LFRX_PGA_IBIAS	Signal link power configuration related configuration, automatically generated by CMT216xA RFPDK.	R/W

- **CUS_LFRX10 register**

CUS_LFRX10 Reset value：0xEF

7	6	5	4	3	2	1	0
LFRX_CMP_REF[3:0]				LFRX_DEMOD_TH_HOLD	LFRX_RSSIREC_IBIAS[2:0]		

Name		Decription	Type
7:4	LFRX_CMP_REF	Related to carrier frequency detection threshold, automatically generated by CMT216xA RFPDK.	R/W
3	LFRX_DEMOD_TH_HOLD	NA, fixed to 1.	R/W
2:0	LFRX_RSSIREC_IBIAS	Related to signal link power configuration, automatically generated by CMT216xA RFPDK.	R/W

- **CUS_LFRX11 register**

CUS_LFRX11 Reset value：0x15

7	6	5	4	3	2	1	0
LFRX_SNRDET_INVALID_WIN[1:0]		LFRX_SNRDET_VALID_WIN[1:0]		LFRX_SNRDET_SNR[3:0]			

Name		Decription	Type
7:6	LFRX_SNRDET_INVALID_WIN	SNR detection, invalid-window setting, automatically generated by CMT216xA RFPDK.	R/W
5:4	LFRX_SNRDET_VALID_WIN	SNR detection, effective-window setting, automatically generated by CMT216xA RFPDK.	R/W
3:0	LFRX_SNRDET_SNR	SNR detection, signal-to-noise ratio setting, automatically generated by CMT216xA RFPDK.	R/W

- **CUS_LFRX12 register**

CUS_LFRX12 Reset value：0x03

7	6	5	4	3	2	1	0
LFRX_MEAS_SOURCE	LFRX_OSC_VREF[1:0]		LFRX_CH_Z	LFRX_CH_Y	LFRX_CH_X	LFRX_STARTUP_MANUAL[1:0]	

Name		Decription	Type
7	LFRX_MEAS_SOURCE	Related to RSSI measurement, automatically generated by CMT216xA RFPDK	R/W
6:5	LFRX_OSC_VREF	Internal parameter, automatically generated by CMT216xA RFPDK	R/W
4	LFRX_CH_Z	In normal mode, channel Z enabling control. Set to 1 to enable.	R/W
3	LFRX_CH_Y	In normal mode, channel Y enabling control. Set to 1 to enable.	R/W
2	LFRX_CH_X	In normal mode, channel X enabling control. Set to 1 to enable.	R/W
1:0	LFRX_STARTUP_MANUAL	Internal parameter, users can ignore it. The default value is 3.	R/W

- **CUS_LFRX_TCAP2 register**

CUS_LFRX_TCAP2 Reset value：0x10

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LFRX_TCAP_Z[4:0]				

Name		Decription	Type
4:0	LFRX_TCAP_Z	Low-frequency wakeup tuning load capacitance in Z-axls antenna, ranging from 0 to 31 with 1.2 pF/Step.	R/W

- **CUS_LFRX_TCAP1 register**

CUS_LFRX_TCAP1 Reset value：0x10

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LFRX_TCAP_Y[4:0]				

Name		Decription	Type
4:0	LFRX_TCAP_Y	Low-frequency wakeup tuning load capacitance in Y-axls antenna, ranging from 0 to 31 with 1.2 pF/Step.	R/W

- **CUS_LFRX_TCAP0 register**

CUS_LFRX_TCAP0 Reset value：0x10

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LFRX_TCAP_X[4:0]				

Name		Decription	Type
4:0	LFRX_TCAP_X	Low-frequency wakeup tuning load capacitance in X-axls antenna, ranging from 0 to 31 with 1.2 pF/Step.	R/W

- **CUS_LFRX_OSC_CODE register**

CUS_LFRX_TCAP0 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	LFRX_OSC_IBIAS[6:0]						

Name		Decription	Type
6:0	LFRX_OSC_IBIAS	Internal parameter. The configuration value is generated by CMT216xA RFPDK.	R/W

- **CUS_SYSCTL3 register**

CUS_SYSCTL3 Reset value：0x00

7	6	5	4	3	2	1	0
LED_INV	AFE_IR_EN	SNOOZE_EN	SNOOZE_DEBUG_EN	LFRX_DEBUG_EN	LFRX_EN	SLPT_WAKEUP_MODE	SLEEP_TIMER_EN

Name		Decription	Type
3	LFRX_DEBUG _EN	Low-frequency wakeup module simulating mode enabling. Set to 0 to disable the low frequency module simulating mode. Set to 1 to enable the low frequency mode simulating mode (used when performing online debugging).	R/W
2	LFRX_EN	Low frequency wake-up module enabling control. Set to 0 to disable the low-frequency wakeup module. Set to 1 to enable the low-frequency wakeup module.	R/W

- **CUS_SYSCTL4 register**

CUS_SYSCTL4 Reset value：0x01

7	6	5	4	3	2	1	0
LFRX_MODE[1:0]		LFRX_SIGNAL_OK_TYPE	LFRX_TIMER_EXTEND_MODE[1:0]		DUTY_CYCLE_METHOD	LFRX_DUTY_CYCLE_EN	ALWAYS_LFRX

Name		Decription	Type
7:6	LFRX_MODE	Low-frequency wakeup mode selection. 2'b00, LFRX_WAKEUP is only used to wake up the core. 2'b01, LFRX_WAKEUP is only used to wake up the external MCU, and the internal MCU can be uses asother functions. 2'b10, LFRX_WAKEUP is only used to wake up the external MCU, the internal MCU is not used. 2'b11, invalid configuration, unavailable.	R/W
5	LFRX_SIGNAL_OK_TYPE	Low-frequency signal detection method. Set to 0, use carrier (carrier duration) detection mode. Set to 1, use signal to noise ratio (SNR) detection mode.	R/W
4:3	LFRX_TIMER_EXTEND_MODE	In low-frequency duty cycle delay mode, the condition selection for T1 time being extended to T2 (pre-condition is DUTY_CYCLE_METHOD=0). 2'b00, signal detection being satisfied (lfrx_signal_ok). 2'b01, sync word matching (sync_pass). 2'b10, wakeup ID matching (wkid_pass.; 2'b11, signal strength being satisfied (dbmdet_ok).	R/W
2	DUTY_CYCLE_METHOD	Low-frequency receiving duty cycle mode selection (pre-condition is LFRX_DUTY_CYCLE_EN=1) Set to 0, adopt automatic delay mode (need to set T1 and T2 for low-frequency receiving). Set to 1, adopt fixed duty cycle mode (only need to set T1 for low-frequency receiving)	R/W
1	LFRX_DUTY_CYCLE_EN	Set to 0, disable the duty cycle mode of low frequency receiving. Set to 1, enable the duty cycle mode of low frequency receiving.	R/W
0	ALWAYS_LFRX	Set to 0, adopt non-long-receiving mode for low-frequency receiving. Set to 1, adopt long-receiving mode for low-frequency receiving.	R/W

- **CUS_SYSCTL5 register**

CUS_SYSCTL5 Reset value：0x00

7	6	5	4	3	2	1	0
LFRX_TIMER_M_RX_T1[4:0]					LFRX_TIMER_R_RX_T1[2:0]		

Name		Decription	Type
7:3	LFRX_TIMER_M_RX_T1	In low-frequency receiving duty cycle mode, receive the M value of the T1 window with a configuration range of 0-31.	R/W
2:0	LFRX_TIMER_R_RX_T1	In low-frequency receiving duty cycle mode, receive the R value of the T1 window with a configuration range of 0-7.	R/W

Notes:

1. The T1 window of low-frequency receiving duty cycle mode meets the below calculation formular.

$$LFRX_{T1} = M \times 2^{(R+1)} \times 500\ us$$

In above, M is the value of LFRX_TIMER_M_RX_T1，R is the value of LFRX_TIMER_R_RX_T1. 500 us corresponds to the internal 32 kHz clock. When external 32.768 kHz crystal oscillator is used, the time unit is 488 us.

- **CUS_SYSCTL6 register**

CUS_SYSCTL6 Reset value：0x00

7	6	5	4	3	2	1	0
LFRX_TIMER_M_RX_T2[4:0]					LFRX_TIMER_R_RX_T2[2:0]		

Name		Decription	Type
7:3	LFRX_TIMER_M_RX_T2	In low-frequency receiving duty cycle mode, receive the M value of the T2 window with a configuration range of 0-31.	R/W
2:0	LFRX_TIMER_R_RX_T2	In low-frequency receiving duty cycle mode, receive the R value of the T2 window with a configuration range of 0-7.	R/W

Notes:

1. *The T2 window of low-frequency receiving duty cycle mode meets the below calculation formular.*

$$LFRX_{T2} = M \times 2^{(R+1)} \times 500\ uS$$

In above, M is the value of LFRX_TIMER_M_RX_T2，R is the value of LFRX_TIMER_R_RX_T2. 500 us corresponds to the internal 32 kHz clock. When external 32.768 kHz crystal oscillator is used, the time unit is 488 us.

- **CUS_SYSCTL7 register**

CUS_SYSCTL7 Reset value：0x00

7	6	5	4	3	2	1	0
LFRX_TIMER_M_SLEEP[7:0]							

Name		Decription	Type
7:0	LFRX_TIMER_M_SLEEP	In low-frequency receiving duty cycle mode, the M value of the sleep window with a configuration range of 0-255.	R/W

Notes:

1. The sleep window of low-frequency receiving duty cycle mode meet the below calculation formular.

$$LFRX_{SLEEP} = M \times 2^{(R+1)} \times 500\ uS$$

In above, M is the value of LFRX_TIMER_M_SLEEP, R is the value of LFRX_TIMER_R_SLEEP. 500 us corresponds to the internal 32 kHz clock. When external 32.768 kHz crystal oscillator is used, the time unit is 488 us.

- **CUS_ SYSCTL8 register**

CUS_SYSCTL8 Reset value：0x10

7	6	5	4	3	2	1	0
Reserved	Reserved	LFRX_WAKEUP_AUTOCLR_DIS	LFRX_WAKEUP_MODE[1:0]		LFRX_TIMER_R_SLEEP[2:0]		

Name		Decription	Type
5	LFRX_WAKEUP_AUTOCLR_DIS	After LFRX_WAKEUP is valid, namely, wakeup is valid, the signal_ok auto-clear function is automatically disabled. Set to 0, once the set time window of Signal_Ok Auto Clear Time is met, automatic clearing will be performed immediately, and it will return from Decode state to Listen state; Set to 1, that is, namely the MCU is wakened, the function of automatically clearing signal_ok is immediately disabled, and let the MCU set the clearing signal LFRX_MANU_CLR to 1 at an appropriate time. If the MCU is not woken up yet, the automatic clearing function is always effective.	R/W
4:3	LFRX_WAKEUP_MODE	Mode selection for low-frequency wakeup. 2'b00, signal detection being satisfied (lfrx_signal_ok). 2'b01, sync word matching (sync_pass). 2'b10, wakeup ID matching (wkid_pass). 2'b11, invalid configuration.	R/W
2:0	LFRX_TIMER_R_SLEEP	The R value of low-frequency receiving duty cycle mode with a configuration range of 0-7.	R/W

Notes:

- *The sleep window of low-frequency receiving duty cycle mode meet the below calculation formular.*

$$LFRX_{SLEEP} = M \times 2^{(R+1)} \times 500\ us$$

M is the value of LFRX_TIMER_M_SLEEP，R is the value of LFRX_TIMER_R_SLEEP. 500 us corresponds to the internal 32 kHz clock. When external 32.768 kHz crystal oscillator is used, the time unit is 488 us.

- **CUS_ SYSCTL9 register**

CUS_SYSCTL9 Reset value：0x29

7	6	5	4	3	2	1	0
LFRX_RSSI_MEAS_DIS	LFRX_DBUF_DIS	LFRX_SNRDET_WIN[2:0]			LFRX_MEAS_WIN[2:0]		

Name		Decription	Type
7	LFRX_RSSI_MEAS_DIS	RSSI measurement related settings. The configurations are generated by RFPDK.	R/W
6	LFRX_DBUF_DIS	Set to 0, enable data stream output delay fucntion after low-frequency wakeup [1] (default); Set to 1, disable data stream output delay fucntion after low-frequency wakeup.	R/W
5:3	LFRX_SNRDET_WIN	SNR detection related settings. The configurations are generated by RFPDK.	R/W
2:0	LFRX_MEAS_WIN	RSSI measurement related settings. The configurations are generated by RFPDK.	R/W

Notes: The data stream output delay fucntion after wakeup is required to match the OTP code loading time when waking up, to

make sure the code has been loaded and running upon data stream output (the software can receive from the first data bit correctly). When this feature is enabled, users can set the buffer depth of the delay, namely the delay time (time converted according to the low-frequency data rate).

- **CUS_ SYSCTL10 register**

CUS_SYSCTL10 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	GO_LFRX_DECODE	GO_LFRX_LISTEN	GO_LFSLEEP

Name		Decription	Type
2	GO_LFRX_DECODE	In decode-only mode (namely LFRX_ENABLE_MODE = 1), setting this bit to 1 indicates a jump to (LFRX) DECODE mode.	R/W
1	GO_LFRX_LISTEN	Setting this bit to 1 indicates a jump to the (LFRX) LISTEN state.	R/W
0	GO_LFSLEEP	Setting this bit to 1 indicates a jump to the (LFRX) SLEEP state.	R/W

Note: This register provides a manual control of the low-frequency state mode (ie user software control). This manual mode is not recommended for normal use of low frequency module. If users need to manually control the low-frequency module per specific requirements, please contact CMOSTEK engineers.

- **CUS_LFRX15 register**

CUS_LFRX15 Reset value：0x72

7	6	5	4	3	2	1	0
LFRX_DBUF_LEGNTH[2:0]			LFRX_WKID_EN	LFRX_WKID_LENGTH[1:0]		LFRX_SYNC_LENGTH[1:0]	

Name		Decription	Type
7:5	LFRX_DBUF_LENGTH	The depth of output delay after wakeup (precondition is LFRX_DBUF_DIS=0) with a range of 0-7. The unit is byte, namely, the conversion of the delay time according to the set data rate.	R/W
4	LFRX_WKID_EN	Set to 0, disable ID matching function. Set to 1, enable ID matching function.	R/W
3:2	LFRX_WKID_LENGTH	The length selection of matching ID: 2'b00, 1-Byte 2'b01, 2-Byte 2'b10, 3-Byte 2'b11, 4-Byte	R/W
1:0	LFRX_SYNC_LENGTH	The length selection of sync word. 2'b00, 1-Byte is valid. LF_SYNC_VALUE[7:0]. 2'b01, 2-Byte is valid. LF_SYNC_VALUE[15:0]. 2'b10, 3-Byte is valid. LF_SYNC_VALUE[23:0]. 2'b11, 4-Byte is valid . LF_SYNC_VALUE[31:0].	R/W

- **CUS_LFRX16 register**

CUS_LFRX16 Reset value：0xAD

7	6	5	4	3	2	1	0
LFRX_ANT_MODE[1:0]		LFRX_HOLD_RST_SEL	LFRX_SNRDET_REFIN_SEL	LFRX_MAN_TYPE	LFRX_WKID_MAN_EN	LFRX_DIG_DATAOUT_SEL	LFRX_DATA_MAN_EN

Name		Decription	Type
7:6	LFRX_ANT_MODE	The mode selection of low-frequency wake-up antenna: 2'b00 and 2'b01, non-scanning antenna modes (X, Y, and Z-axis antennas can be individually enabled and controlled). 2'b10, X and Y-axis scanning antenna pattern. 2'b11, X, Y and Z-axis scanning antenna patterns.	R/W
5	LFRX_HOLD_RST_SEL	The configuration is generated by RFPDK. Not suggest users change them.	R/W
4	LFRX_SNRDET_REFIN_SEL	The SNR detection related settings. The configuration is generated by RFPDK. Not suggest users change them.	R/W
3	LFRX_MAN_TYPE	The polarity selection when the low-frequency data Manchester code is valid (LFRX_DATA_MAN_EN=1). Set to 0, 01 represents logic 1, and 10 represents logic 0. Set to 1, 10 represents logic 1, and 01 represents logic 0.	R/W
2	LFRX_WKID_MAN_EN	Set to 0, the low-frequency wakeup ID is not encoded (namely adopt NRZ code by default). Set to 1, the low-frequency wakeup ID is Manchester coded.	R/W
1	LFRX_DIG_DATAOUT_SEL	Low-frequency demodulation data stream output stage selection. Set to 0, the low frequency demodulated data stream is output after waking up. Set to 1, the low frequency demodulated data code stream is output upon invalid signal detection(carrier detection) Note: this setting is valid when LFRX_DATAOUT_SEL=0.	R/W
0	LFRX_DATA_MAN_EN	Set to 0, the low-frequency payload data is not encoded (namely adopt NRZ encoding by default). Set to 1, the low frequency load data is Manchester coded.	R/W

- **CUS_LFRX17 - CUS_LFRX20 register set**

CUS_LFRX17 - 20 Reset value：0x59, 0x5A, 0xA5, 0x00

	7	6	5	4	3	2	1	0
17	LFRX_SYNC_VALUE[7:0]							
18	LFRX_SYNC_VALUE[15:8]							
19	LFRX_SYNC_VALUE[23:16]							
20	LFRX_SYNC_VALUE[31:24]							

Name	Decription	Type
LFRX_SYNC_VALUE	Low frequency data sync word configuration value, can configure as 8/16/24/32 Symbols. *Note: only the NRZ encoding format is used.*	R/W

- **CUS_LFRX21 - CUS_LFRX24 register set**

CUS_LFRX21 - 24 Reset value：0x23, 0x00, 0x00, 0x00

	7	6	5	4	3	2	1	0
21	LFRX_WKID_VALUE[7:0]							
22	LFRX_ WKID _VALUE[15:8]							
23	LFRX_ WKID _VALUE[23:16]							
24	LFRX_ WKID _VALUE[31:24]							

Name	Decription	Type
LFRX_WKID_VALUE	The low-frequency data wakeup ID configuration value, can configure as 8/16/24/32 bits. *Note: Manchester encoding can be used with LFRX_WKID_MAN_EN configuration. NRZ is used by default. If Manchester encoding is used, the above value is the value after Manchester encoding.*	R/W

- **CUS_LFRX25 register**

CUS_LFRX25 Reset value：0x1C

7	6	5	4	3	2 1 0
LFRX_DATAOUT_SEL	LFRX_DECODE_SEQ	LFRX_SIGNAL_OK_AUTOCLR_DIS	LFRX_AGC_EN	LFRX_AGC_STEP	LFRX_AGC_CNT_TH[2:0]

Name		Decription	Type
7	LFRX_DATAOUT_SEL	Low-frequency demodulation data output mode selection. Set to 0, the output as data rate clock synchronization mode (default). Set to 1, output as RAW DATA mode.	R/W
6	LFRX_DECODE_SEQ	The matching sequence of wakeup IDs. Set to 0, higher bit data first in (data shift to the left) (default). Set to 1, lower bit data first in (data shift to the right).	R/W
5	LFRX_SIGNAL_OK_AUTOCLR_DIS	Set to 0, enable automatic LFRX_SIGNAL_OK clearing. Set to 1, disable automatic LFRX_SIGNAL_OK clearing.	R/W
4	LFRX_AGC_EN	Set to 0, disable low-frequency demodulation AGC. Set to 1, enable low-frequency demodulation AGC.	R/W
3	LFRX_AGC_STEP	AGC adjustment step selection (when LFRX_AGC_EN=1). Set to 0, the adjustment step is 3 dB / Step. Set to 1, the adjustment step is 6 dBm / Step.	R/W
2:0	LFRX_AGC_CNT_TH	AGC restoring time. The configuration is generated by RFPDK.	R/W

- **CUS_LFRX26 register**

CUS_LFRX26 Reset value：0x50

7	6	5	4	3	2	1	0
LFRX_DQRES[3:0]				LFRX_AGC_MIN_INDEX[3:0]			

Name		Decription	Type
7:4	LFRX_DQRES	Antenna's Q-factor reducing resistor configuration. The configuration is generated by RFPDK.	R/W
3:0	LFRX_AGC_MIN_INDEX	The minimum AGC gain configuration. The configuration is generated by RFPDK.	R/W

- **CUS_LFRX27 register**

CUS_LFRX27 Reset value：0x31

7	6	5	4	3	2	1	0
LFRX_DR_SEL[3:0]				Reserved	LFRX_ENABLE_MODE	Reserved	LFRX_AGC_START_SEL

Name		Decription	Type
7:4	LFRX_DR_SEL	Low-frequency rate selection. – 4'b1111: 1.00 kbps. – 4'b1110: 1.07 kbps. – 4'b1101: 1.14 kbps. – 4'b1100: 1.23 kbps. – 4'b1011: 1.33 kbps. – 4'b1010: 1.45 kbps. – 4'b1001: 1.60 kbps. – 4'b1000: 1.78 kbps. – 4'b0111: 2.00 kbps. – 4'b0110: 2.29 kbps. – 4'b0101: 2.67 kbps. – 4'b0100: 3.20 kbps. – 4'b0011: 4.00 kbps (default). – 4'b0010: 5.33 kbps. – 4'b0001: 8.00 kbps. – 4'b0000: cannot be used.	R/W
2	LFRX_ENABLE_MODE	Low-frequency module operating mode. Set to 0, Listen & Decode mode (default). Set to 1, Decode-only mode.	R/W
0	LFRX_AGC_START_SEL	Low-frequency module AGC startup selection. Set to 0, start in Listen mode. Set to 1, start in Decode mode.	R/W

- **CUS_LFRX28 register**

CUS_LFRX28 Reset value：0x7C

7	6	5	4	3	2	1	0
LFRX_CADET_TH_H[7:0]							

Name	Decription	Type
LFRX_CADET_TH_H	The upper limit value of carrier frequency detection tolerance window. The unit is the time of a carrier frequency cycle.	R/W

- **CUS_LFRX29 register**

CUS_LFRX29 Reset value：0x65

7	6	5	4	3	2	1	0
LFRX_CADET_TH_L[7:0]							

Name	Decription	Type
LFRX_CADET_TH_L	The lower limit value of carrier frequency detection tolerance window. The unit is the time of a carrier frequency cycle.	R/W

Notes:

LFRX_CADET_TH_H and LFRX_CADET_TH_L are a pair of carrier detection upper/lower window values. For instance, when the 125 kHz carrier detection window is configured as 906.25 us, the unit time is 8 us, reserving a margin of 10% for upper and lower window values .

$$LFRX\_CADET\_TH\_H = \frac{906.25us}{8us} \times 110\% = 124$$

$$LFRX\_CADET\_TH\_L = \frac{906.25us}{8us} \times 90\% = 101$$

- **CUS_LFRX30 register**

CUS_LFRX30 Reset value：0x1E

7	6	5	4	3	2	1	0
LFRX_SIGNAL_OK_CLR_TH[7:0]							

Name	Decription	Type
LFRX_SIGNAL_OK_CLR_TH	The perodic auto-reset window time value of the low-frequency module. The configuration is generated by RFPDK.	R/W

Notes:

This item is valid when the low-frequency auto-reset function is enabled. It is used to automatically reset the low-frequency module at regular intervals. After resetting, the low-frequency module retrieves the preset detection mode (carrier or SNR), synchronization word matching, wake-up ID matching, and so on.

- **CUS_SYSCTL11 register**

CUS_SYSCTL11 Reset value：0x80

7	6	5	4	3	2	1	0
SLPT_MANU_RSTN	Reserved	Reserved	SNOOZE_MANU_CLR	LBD_MANU_CLR	LFRX_MANU_CLR	SLPT_MANU_CLR	BUT_MANU_CLR

Name		Decription	Type
2	LFRX_MANU_CLR	Low-frequency wakeup manual clearing flag. Set to 1, the system automatically clears.	R/W

- **CUS_SYSCTL12 register**

CUS_SYSCTL12 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	SNOOZE_WAKEUP		WKID_PASS	SYNC_PASS	LFRX_SIGNAL_OK	SLEEP_TIMESUP	KEY_LAUNCH

Name		Decription	Type
4	WKID_PASS	Flag for matching ID detection valid In low-frequency data, valid when reading as 1.	R
3	SYNC_PASS	Flag for synch word detection valid In low-frequency data, valid when reading as 1.	R
2	LFRX_SIGNAL_OK	Flag for low-frequency carrier detection valid, valid when reading as 1.	R

- **CUS_LFRX31 register**

CUS_LFRX31 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	LFRX_AGC_INDEX[5:0]					

Name		Decription	Type
5:0	LFRX_AGC_INDEX	Low-frequency signal strength indication value, which is used to calculte RSSI value. See Section 4.4 in AN280 CMT216xA Low-frequency Receiving Function User Guide for details.	R

- **CUS_LFRX32 register**

CUS_LFRX32 Reset value：0x00

7	6 5 4	3	2	1	0
MAN_DECODE_ERR_FLAG	LFRX_MEAS_OUT[2:0]	LFRX_IBIAS_CAL_OVTS_FLAG	LFRX_TCAP2_CAL_OVTS_FLAG	LFRX_TCAP1_CAL_OVTS_FLAG	LFRX_TCAP0_CAL_OVTS_FLAG

Name		Decription	Type
7	MAN_DECODE_ERR_FLAG	Low-frequency demodulation data error indication, valid when reading as 1 (valid when Manchester is enabled).	R
6:4	LFRX_MEAS_OUT	NA, internal parameter. Users can ignore it.	R
3	LFRX_IBIAS_CAL_OVTS_FLAG	NA, internal parameter. Users can ignore it.	R
2	LFRX_TCAP2_CAL_OVTS_FLAG	Low-frequency Z-axis antenna tuning overflow flag	R
1	LFRX_TCAP1_CAL_OVTS_FLAG	Low-frequency Y-axis antenna tuning overflow flag	R
0	LFRX_TCAP0_CAL_OVTS_FLAG	Low-frequency X-axis antenna tuning overflow flag	R

- **CUS_LFRX33 register**

CUS_LFRX33 Reset value：0x01

7	6	5	4	3	2	1	0
LFRX_DATA_LENGTH[7:0]							

Name	Decription	Type
LFRX_DATA_LENGTH	Low-frequency data receiving length	R/W

- **CLK_SYS_DIV register**

CLK_SYS_DIV Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	LFRX_MCU_RCLK	LFRX_MCU_RDATA	Reserved	CLK_SYS_DIV[3:0]			

Name		Decription	Type
6	LFRX_MCU_RCLK	Low-frequency demodulation data synchronization clock flag, software accessible.	R
5	LFRX_MCU_RDATA	Low-frequency demodulation data flag, software accessible.	R

Notes:

1. *Both LFRX_MCU_RCLK and LFRX_MCU_RDATA can generate interrupts. Refer to the interrupt related sections CMT216xA User Guide for more details.*
2. *Suggest users use interrupt mode to collect low-frequency data bit by bit, especially for LFRX_MCU_RCLK. Since the synchronous clock is output at a preset rate, interrupt mode can respond in a timely manner. If the software query method is used, users should pay attention to the period of the software query interval to avoid asynchrony causing data loss.*

- **LFRX_IF_TH_H register**

LFRX_IF_TH_H Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	LFRX_TBCCI1_SEL	LFRX_TBCC0_SEL	LFRX_TACCI1_SEL	LFRX_TACCI0_SEL

Name		Decription	Type
3	LFRX_TBCCI1_SEL	Select CCI1 for outputting low-frequency resonance frequency to TimerB. Set to 1, select output. Set to 0, close.	R/W
2	LFRX_TBCCI0_SEL	Select CCI0 for low-frequency resonance frequency output to TimerB. Set to 1, select output. Set to 0, close.	R/W
1	LFRX_TACCI1_SEL	Select CCI1 for outputting low-frequency resonance frequency to TimerA: Set to 1, select output. Set to 0, close.	R/W
0	LFRX_TACCI0_SE	Select CCI0 for low-frequency resonance frequency output to TimerA. Set to 1, select output. Set to 0, close.	R/W

- **LFRX_IF_TH_L register**

LFRX_IF_TH_L Reset value：0x7D

7	6	5	4	3	2	1	0
LFRX_ANT_REF[7:0]							

Name	Decription	Type
LFRX_ANT_REF	The target frequency of antenna calibration. The default value is 125, namely 125 kHz.	R/W

3.11 Sub-1G Transmiter Module Register Set

Table 12. Sub-1G Transmiter Module Register List

Name	Storage Area	Sub-area	Address	Reset	Function
PA_POWER_TH_9	Block1	Bank1	0x8E	0x7F	Transmission power threshold register9
PA_POWER_TH_8	Block1	Bank1	0x8F	0x7F	Transmission power threshold register8
PA_POWER_TH_7	Block1	Bank1	0x90	0x7F	Transmission power threshold register7
PA_POWER_TH_6	Block1	Bank1	0x91	0x7F	Transmission power threshold register6
PA_POWER_TH_5	Block1	Bank1	0x92	0x7F	Transmission power threshold register5
PA_POWER_TH_4	Block1	Bank1	0x93	0x7F	Transmission power threshold register4
PA_POWER_TH_3	Block1	Bank1	0x94	0x7F	Transmission power threshold register3
PA_POWER_TH_2	Block1	Bank1	0x95	0x7F	Transmission power threshold register2
PA_POWER_TH_1	Block1	Bank1	0x96	0x7F	Transmission power threshold register1
PA_POWER_TH_0	Block1	Bank1	0x97	0x7F	Transmission power threshold register0
TX_SYM_GROUP	Block1	Bank1	0xA9	0x00	Transmission symbol register
TX_SYM_CTL	Block1	Bank1	0xAA	0x00	Transmission symbol control register
TX_PKT_CTL	Block1	Bank1	0xAB	0x40	Transmission mode control register
SYMBOL_TIME_H	Block1	Bank1	0xAC	0x00	Transmission data rate configuration register higher 8 bits
SYMBOL_TIME_L	Block1	Bank1	0xAD	0x00	Transmission data rate configuration register lower 8 bits
FREQ_DEV_H	Block1	Bank1	0xAE	0x00	Frequency deviation register higher 8 bits
FREQ_DEV_L	Block1	Bank1	0xAF	0x00	Frequency deviation register lower 8 bits
RAMP_STEP_TIME_H	Block1	Bank1	0xB0	0x00	RAMP configuration register higher 8 bits
RAMP_STEP_TIME_L	Block1	Bank1	0xB1	0x00	RAMP configuration register lower 8 bits
PA_IDAC_CODE	Block1	Bank1	0xB3	0x00	Transmission power configuration register
PA_CTL0	Block1	Bank1	0xB4	0x00	PA configuration/control register0
VCO_CTL0	Block1	Bank1	0xB6	0x0F	VCO control register0
VCO_CTL1	Block1	Bank1	0xB7	0x20	VCO control register1
PLLN	Block1	Bank1	0xB9	0x42	Phase-locked loop N value configuration register
PLLK_H	Block1	Bank1	0xBA	0xC1	Phase-locked loop K value register higher 8 bits
PLLK_L	Block1	Bank1	0xBB	0xC5	Phase-locked loop K value register lower 8 bits

- **PA_POWER_TH_0-9 register set**

PA_POWER_TH_0-9 Reset value：0x7F for all

7	6	5	4	3	2	1	0
PA_POWER_TH_n[7:0]							

Name	Decription	Type
PA_POWER_THn	Transmission power configuration according to each voltage level. When n = 0, transmit power configuration value at a voltage of 1.8 V. When n = 1, transmit power configuration value at a voltage of 2.0 V. When n = 2, transmit power configuration value at a voltage of 2.2 V. When n = 3, transmit power configuration value at a voltage of 2.4 V. When n = 4, transmit power configuration value at a voltage of 2.6 V. When n = 5, transmit power configuration value at a voltage of 2.8 V. When n = 6, transmit power configuration value at a voltage of 3.0 V. When n = 7, transmit power configuration value at a voltage of 3.2 V. When n = 8, transmit power configuration value at a voltage of 3.4 V. When n = 9, transmit power configuration value at a voltage of 3.6 V.	R/W

Note: The transmission power configuration value is related to users' target power value. It is recommended that users assign values according to the configuration values provided by the official configuration tool (software). Using improper values may affect transmission performance.

- **TX_SYM_GROUP register**

TX_SYM_GROUP Reset value：0x00

7	6	5	4	3	2	1	0
TY_SYM_GROUP[7:0] / TX_DIRECT_DATA[0]							

Name		Decription	Type
7:0	TX_SYM_GROUP	Register for buffer of data to be transmitted. In the packet mode, transmit data according to bit width defined by TX_GROUP_WIDTH. In the direct mode, the direct transmission is performed through setting Bit0 to 0 or 1.	R/W

- **TX_SYM_CTL register**

TX_SYM_CTL Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	TX_DIRECT_EN	TX_GROUP_WIDTH[2:0]			TX_SYM_ENDIAN	TX_SYM_CTRL[1:0]	

Name		Decription	Type
6	TX_DIRECT_EN	Direct mode enabling control. Set to 0, adopt packet mode. Set to 1, adopt direct mode.	R/W
5:3	TX_GROUP_WIDTH	Determine the TX_SYM_GROUP transmission bit width with a range of 1 - 8 bits.	R/W
2	TX_SYM_ENDIAN	Transmission data little/large endian mode selection. 3'b000, Bit0 of TX_SYM_GROUP is valid. 3'b001, Bit1-Bit0 of TX_SYM_GROUP is valid.	R/W

Name		Decription	Type
		3'b010, Bit2-Bit0 of TX_SYM_GROUP is valid. 3'b011, Bit3-Bit0 of TX_SYM_GROUP is valid. 3'b100, Bit4-Bit0 of TX_SYM_GROUP is valid. 3'b101, Bit5-Bit0 of TX_SYM_GROUP is valid. 3'b110, Bit6-Bit0 of TX_SYM_GROUP is valid. 3'b111, Bit7-Bit0 of TX_SYM_GROUP is valid.	
1:0	TX_SYM_CTRL	Transmission end mode selection. 2'b00, close transmission after the last bit transmission completes. 2'b01, keep transmitting the last bit after the last bit transmission completes. 2'b10, keep transmitting 0. 2'b11, keep transmitting 1.	R/W

Notes:

1. *The main difference between packet mode and direct mode is that the former needs to define the transmission buffer array in the code, transmission is done through relevant API functions, and transmission rate follows the set rate; while the direct mode does not need to define the transmission buffer data, and it is not limited to use the set transmission rate (suggest users fill a rate greater than the actual transmission rate in the configuration tool software), instead the transmission time is adjusted by software. Please refer to the Datasheet specifications and related AN documents for more details.*
2. *When using the API function tx_sym_transmit to implement the transmission function, the TX_SYM_CTRL setting is invalid, and it is processed according to the 2'b00 option, that is, the transmission function is closed after the transmission is completed.*

- **TX_PKT_CTL register**

TX_PKT_CTL Reset value：0x40

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RAMP_EN	TX_MODU	FREQ_DEV_INV	GUASS_ON

Name		Decription	Type
3	RAMP_EN	Set to 0, disable the RAMP function. Set to 1, enable the RAMP function.	R/W
2	TX_MODU	Modulation mode selection. Set to 0, OOK modulation mode. Set to 1, FSK modulation mode.	R/W
1	FREQ_DEV_INV	FSK mode data modulation polarity. Set to 0, +FDEV is 1, -FDEV is 0 (FDEV is the transmission frequency deviation). Set to 1, +FDEV is 0, -FDEV is 1.	R/W
0	GUASS_ON	Set to 0, disable FSK data Gaussian filtering. Set to 1, enable FSK data Gaussian filtering.	R/W

- **SYMBOL_TIME_H / L register set**

SYMBOL_TIME_H/L Reset value：0x00/0x00

	7	6	5	4	3	2	1	0
H	SYMBOL_TIME[15:8]							
L	SYMBOL_TIME[7:0]							

Name	Decription	Type
SYMBOL_TIME[15:0]	Transmission data rate configuration. FSK modulation, with a configurable range of 0.5 - 200 kbps. OOK modulation with a data rate range of 0.5 - 40 kbps.	R/W

Notes:

The rate calcualtion formula is as follows.

$$SYMBOL\_TIME = \frac{BR \times 2^{21}}{F_{XTAL}}$$

In above, FXTAL is crystal frequency, namely 26 MHz. In addition, users do not need to do te calculatation. The official configuration tool software can be used to automatically generate the target parameter results just by setting the target rate..

- **FREQ_DEV_H / L register set**

FREQ_DEV_H/L Reset value：0x00/0x00

	7	6	5	4	3	2	1	0
H	FREQ_DEV[15:8]							
L	FREQ_DEV[7:0]							

Name	Decription	Type
FREQ_DEV[15:0]	FSK transmission frequency deviation configuration.	R/W

- **RAMP_STEP_TIME_H / L register set**

RAMP_STEP_TIME_H/L Reset value：0x00/0x00

	7	6	5	4	3	2	1	0
H	RAMP_STEP_TIME[14:8]							
L	RAMP_STEP_TIME[7:0]							

Name	Decription	Type
RAMP_STEP_TIME[14:0]	PA RAMP step time register. The minimum step size is 76.9 ns, and the maximum step size is 20 us.	R/W

- **PA_IDAC_CODE register**

PA_IDAC_CODE Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	PA_IDAC_CODE[5:0]					

Name		Decription	Type
5:0	PA_IDAC_CODE	The transmit power IDAC configuration, co-working with the PA_POWER_TH_0-9 register set to determine the transmission power;	R/W

Note: The above register configuration values need to be set by the configuration tool (XLS file or GUI software) through set target parameters (such as operating frequency, rate, frequency diviation) by users then the tools will automatically convert them into register configurations.

- **PA _CTL0 register**

PA _CTL0 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	PA_DIFF_SEL	PA_RCRAMP_SELB	PA_RAMP_RSEL[2:0]		

Name		Decription	Type
4	PA_DIFF_SEL	PA operating mode selection. Set to 0, select the single-ended PA output. Set to 1, select the differential PA output.	R/W
3	PA_RCRAMP_SELB	PA RAMP RC filter enabling selection. Set to 0, enable the RC filter. Set to 1, disable the RC filter.	R/W
2:0	PA_RAMP_RSEL	PA RAMP RC filter parameter selection.	R/W

- **VCO _CTL0 register**

VCO _CTL0 Reset value：0x0F

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	VCO_GAIN_CODE[2:0]			PLL_BW_SEL[1:0]	

Name		Decription	Type
4:2	VCO_GAIN_CODE	The VCO gain configuration value.	R/W
1:0	PLL_BW_SEL	PLL bandwidth selection. Set to 0, select 210 kHz. Set to 1, select 150 kHz.	R/W

- **VCO _CTL1 register**

VCO _CTL1 Reset value：0x20

7	6	5	4	3	2	1	0
VCO_HBAND	PDCPLF_CPBIAS_CODE	DIVX_CODE[1:0]		DIVX_SEL[3:0]			

Name		Decription	Type
7	VCO_HBAND	VCO frequency band selection. Set to 0, select low frequency band. Set to 1, select high frequency band.	R/W
6	PDCPLF_CPBIAS_CODE	PDCPLF current control	R/W
5:4	DIVX_CODE	The two parameters determine the PLL frequency division ratio DIV_VALUE, and the VCO frequency is divided by the DIV_VALUE to the PA output frequency.	R/W
3:0	DIVX_SEL		R/W

- **PLLN / PLLK_H / PLLK_L register set**

PLLN / PLLK_ H/ PLLK_L Reset value：0x42 / 0xC1 / 0xC5

	7	6	5	4	3	2	1	0
N	PLLN [7:0]							
K_H	PLLK_H [15:8]							
K_L	PLLK_L [7:0]							

Name	Decription	Type
PLLN[7:0]	N value and K value of PLL configuration. This parameter is related to transmission power.	R/W
PLLK[15:0]		R/W

Notes:

1. *The above register configuration values need to be set by the configuration tool (XLS file or GUI software) through set target parameters (such as operating frequency, rate, frequency diviation) by users then the tools will automatically convert them into register configurations..*
2. *The PLL_K and PLL_N values in the phase-locked loop are calculated as follows:*

$$PLL\_N = INT\left(\frac{F_{RF} \times DIV\_VALUE}{F_{XO}}\right)$$

$$PLL\_K = \left(\frac{F_{RF} \times DIV\_VALUE}{F_{XO}} - PLL\_N\right) \times 2^{16}$$

In above,

- *DIV_VALUE is the frequency division from VCO frequency to PA output. It is determined by DIVX_CODE and DIVX_SEL in VCO_CTL1 register. Please refer to CMT216xA User Guide for details.*
- *FXO is the crystal oscillator frequency, which is 26 MHz;*
- *FRF is the target operating frequency.*

PLL_N is the integer part of the phase-locked loop, which is calculated and rounded according to the target frequency, the VCO frequency division value and the crystal frequency. Then calculate the PLL_K, the decimal part of the phase-locked loop.

3.12 Analog Front End（AFE）register Set

ULPOA & HSOA, SAR-ADC and SNOOZE are the 3 core analog front end parts.

Table 13. Analog Front End Register Set List

Name	Storage Area	Address	Reset	Function
CUS_AFE4	Block0	0x03	0x00	Gain Configuration Register-1
CUS_AFE6	Block0	0x05	0x80	Gain Configuration Register-2
CUS_AFE7	Block0	0x06	0x80	Bridge sensor interface configuration register
CUS_AFE9	Block0	0x08	0xC1	DC bias configuration register
CUS_AFE10	Block0	0x09	0x00	HSOA0 configuration register
CUS_AFE11	Block0	0x0A	0x00	HSOA1 configuration register
CUS_AFE12	Block0	0x0B	0x00	HSOA2 configuration register
CUS_AFE13	Block0	0x0C	0x84	Micro-power regulator output and ADC input configuration register
CUS_AFE14	Block0	0x0D	0xFF	AFE control register-1
CUS_AFE15	Block0	0x0E	0xB7	AFE control register-2
CUS_AFE16	Block0	0x0F	0x07	ADC conversion time configuration and LPOAs control register
CUS_AFE17	Block0	0x10		Constant current source drive control register-1
CUS_AFE18	Block0	0x11		Constant current source drive control register-2
CUS_SNOOZE1	Block0	0x1E	0x00	SNOOZE configuration register-1 (sleep cycle configuration 1)
CUS_SNOOZE2	Block0	0x1F	0x00	SNOOZE configuration register-2 (sleep cycle configuration 2)
CUS_SNOOZE3	Block0	0x20	0x00	SNOOZE interrupt threshold register-1 (trigger window upper limit configuration)
CUS_SNOOZE4	Block0	0x21	0x00	SNOOZE Interrupt Threshold Register-2 (trigger Window Lower Limit Configuration)
CUS_SNOOZE5	Block0	0x22	0x00	SNOOZE interrupt enabling and ADC clock frequency select register
CUS_SNOOZE6	Block0	0x23	0x00	SNOOZE interrupt flag register
CUS_SYSCTL3	Block0	0x50	0x00	System control register 3 (SNOOZE mode control register)
CUS_SYSCTL11	Block0	0x68	0x80	System control register 11 (software clearing flag control register)
CUS_SYSCTL12	Block0	0x69	0x00	System control register 12 (SNOOZE interrupt wake-up flag)
CUS_SYSCTL13	Block0	0x6A	0x00	ADC control register
CUS_SYSCTL14	Block0	0x6B	0x00	ADC data register-1
CUS_SYSCTL15	Block0	0x6C	0x00	ADC data register-2
CUS_SYSCTL19	Block0	0x70	0x70	System control register 19 (constant current source drive pulse output port control)
CUS_RESV5	Block0	0x7A	0x7A	LPOAs non-inverting input port configuration register

- **CUS_AFE4 register**

CUS_AFE4 Reset value：0x00

7	6	5	4	3	2	1	0
AFE_IA2_GX[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Name		Decription	Type
7:6	AFE_IA2_GX	Gain selection for internal HSOA0 used as a second amplifier or non-inverting amplifier of general-purpose instrumentation. 00, the gain is x1.0. 01, the gain is x1.5. 10, the gain is x2.0. 11, the gain is x3.0.	R/W

- **CUS_AFE6 register**

CUS_AFE6 Reset value：0x80

7	6	5	4	3	2	1	0
Reserved	Reserved	AFE_IA1_GX[2:0]			Reserved	Reserved	Reserved

Name		Decription	Type
5:3	AFE_IA1_GX	Gain selection for internal HSOA1 and HSOA2 used as a first amplifier or a non-inverting amplifier of general-purpose instrumentation. 3'b000, no gain setting, disabled when the amplifier is operating. 3'b001, the gain is x2. 3'b010, the gain is x4. 3'b011, the gain is x8. 3'b100, the gain is x16. 3'b101, the gain is x24. 3'b110, the gain is x32. 3'b111, the gain is x48.	R/W

- **CUS_AFE7 register**

CUS_AFE7 Reset value：0x80

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	AFE_SEN_CHX[2:0]		

Name		Decription	Type
2:0	AFE_SEN_CHX	Sensor channel selection: 3’b000, no channel selection. 3’b001, select external sensor channel 1, A1 and A2 pins as bridge sensor input, ASN and ASP pins as sensor power source; 3’b010, select external sensor channel 2, A3 and A4 pins as bridge sensor input, PSN and PSP pins as sensor power supply excitation source. 3’b011, select the internal temperature sensor channel. 3’b1xx, cannot use.	R/W

- **CUS_AFE9 register**

CUS_AFE9 Reset value：0xC1

7	6	5	4	3	2	1	0
ULPOA0_VCM_DIS	ULPOA1_VCM_DIS	AFE_IA_VCMX	AFE_OA_VCMX[1:0]		AFE_OA_OUTX[1:0]		AFE_IA1_CX

Name		Decription	Type
7	ULPOA0_VCM_DIS	ULPOA0 internal 0.6V selection configuration. Set to 0, connect the internal 0.6V reference to the non-inverting input of ULPOA0. Set to 1, not select.	R/W
6	ULPOA1_VCM_DIS	ULPOA1 internal 0.6V selection configuration. Set to 0, connect the internal 0.6V reference to the non-inverting input of ULPOA0. Set to 1, not select.	R/W
5	AFE_IA_VCMX	HSOAn reference voltage selection. Set to 0, select VDDA/10; Set to 1, select VDDA/2;	R/W
4:3	AFE_OA_VCMX	HSOAn non-inverting input DC bias voltage voltage selection: 2'b00, select VDDA/20. 2'b01, select VDDA/10. 2'b10, select VDDA/4. 2'b11, select VDDA/2.	R/W
2:1	AFE_OA_OUTX	Selection for HSOAn connecting ADC. 2'b00, no connection; 2'b01, connect HSOA0; 2'b10, connect HSOA1; 2'b11, connect HSOA2;	R/W
0	AFE_IA1_CX	HSOA1 and HSOA2 internal function selection: Set to 0, HSOA1 and HSOA2 are both as internal non-inverting amplifier amplifiers; Set to 1, HSOA1 and HSOA2 compose the internal instrument amplifier.	R/W

- **CUS_AFE10 register**

CUS_AFE10 Reset value：0x00

7	6	5	4	3	2	1	0
AFE_OA0_OX	AFE_OA0_NX[1:0]		AFE_OA0_PX[2:0]			AFE_OA0_NA_GX[1:0]	

Name		Decription	Type
7	AFE_OA0_OX	HSOA0 output channel selection. Set to 0, select channel 0 output. A gain amplification mode with configuring AFE_IA2_GX and AFE_OA0_NA_GX. Set to 1, select channel 1 output for floating mode.	R/W
6:5	AFE_OA0_NX	HSOA0 reverse input channel selection. 2'b00, no channel selection. 2'b01, select channel 1, namely no input connection. 2'b10, select channel 2. A gain amplification mode with configuring AFE_IA2_GX and AFE_OA0_NA_GX.	R/W

Name		Decription	Type
		2'b11, select channel 3, connect HSOA0 output as buffer amplifier.	
4:2	AFE_OA0_PX	HSOA0 non-inverting input channel selection. 3'b000, no channel selection. 3'b001, select channel 1, connect OA0_IP, selecting sampling channel through configuring SAR_INX. 3'b010, select channel 2, with HSOAs forming instrument amplifier. 3'b011, select channel 3, connect HSOA1 output. 3'b100, select channel 4, connect HSOA2 output. 3'b101, select channel 5, connect power supply battery sensor (VDD/ 4). 3'b110, select channel 6, internal signal, unavailable to users. 3'b111, select channel 7, connect internal DC bias voltage OA_VCMI.	R/W
1:0	AFE_OA0_NA_GX	HSOA0 non-inverting amplification gain selection, co-working with AFE_IA2_GX. 2'b00, inverting amplification. 2'b01, small gain non-inverting amplification. 2'b10, medium gain non-inverting amplification. 2'b11, high gain non-inverting amplification.	R/W

- **CUS_AFE11 register**

CUS_AFE11 Reset value：0x00

7	6	5	4	3	2	1	0
SAR_DIRECT_DIS	AFE_OA1_OX[1:0]		AFE_OA1_NX[1:0]		AFE_OA1_PX[2:0]		

Name		Decription	Type
7	SAR_DIRECT_DIS	ADC internal test control bit. When the ADC is used normally, it must be set to 1. Set to 0, internal test mode, for internal test only, unavailable to users. Set to 1, ADC normal operation mode.	R/W
6:5	AFE_OA1_OX	HSOA1 output channel selection. 2'b00, no channel selection. 2'b01, select channel 1, which can form non-inverting amplifier or instrument amplifier. 2'b10, select channel 2, connecting to the ASN pin. 2'b11, connect channel 1 and channel 2 at the same time, namely, map the HSOA1 output to the ASN pin and use it as the reverse input signal of HSOA0.	R/W
4:3	AFE_OA1_NX	HSOA1 inverting input channel selection. 2'b00, no channel selection. 2'b01, select channel 1, connecting to A4 pin (GPIO4). 2'b10, select channel 2, which can form non-inverting amplifier instrument amplifier. 2'b11, select channel 3, connecting HSOA1 output, using HSOA1 as buffer amplifier.	R/W
2:0	AFE_OA1_PX	HSOA1 non-inverting input channel selection. 3’b000, no channel selection. 3’b001, select 1 channel and connect to A3 pin (GPIO3). -3’b010, select 2 channels, connect to PSN pin. -3’b011, unavailable to users. -3’b100, select 3 channels, internal DC bias voltage OA_VCMI. -3’b101, select channel 1 and channel 3 at the same time. The A3 pin is connected to the internal OA_VCMI, connecting to the HSOA1 non-inverting input. -3’b110, select channel 2 and channel 3 at the same time. The PSN pin is connected to the internal OA_VCMI, connecting to the HSOA1 non-inverting input;	R/W

Name		Decription	Type
		3'b111, unavailable to users.	

- **CUS_AFE12 register**

CUS_AFE12 Reset value: 0x00

7	6 5	4 3	2 1 0
LDO_ULPOA_RAILB	AFE_OA2_OX[1:0]	AFE_OA2_NX[1:0]	AFE_OA2_PX[2:0]

Name		Decription	Type
7	LDO_ULPOA_RAILB	Bypass function selection of micro-power LDO_PIR regulator. Set to 0, bypass is enabled. Set to 1, bypass is disabled.	R/W
6:5	AFE_OA2_OX	HSOA2 output channel selection. 2'b00, no channel selection. 2'b01, select channel 1, forming instrument amplifier or non-inverting amplifier. 2'b10, select channel 2, connecting to the ASP pin. 2'b11, connect channel 1 and channel 2 at the same time, namely, map the HSOA2 output to the ASN pin and use it as the non-inverting input signal of HSOA0.	R/W
4:3	AFE_OA2_NX	HSOA2 inverting input channel selection. 2'b00, no channel selection. 2'b01, select channel 1, connecting to A2 pin (GPIO2). 2'b10, select channel 2, forming non-inverting amplifier or instrument amplifier. 2'b11, select channel 3, connecting HSOA2 output as buffer amplifier.	R/W
2:0	AFE_OA2_PX	HSOA2 non-inverting input channel selection. 3'b000, no channel selection. 3'b001, select channel 1, connecting to A1 pin (GPIO1). 3'b010, select channel 2, connecting to ASN pin. 3'b011, unavailable to users. 3'b100, select channel 3, connect to internal DC bias voltage OA_VCMI. 3'b101, connect channel 1 and channel 3 at the same time. A1 is connected to internal OA_VCMI, connecting to HSOA2 non-inverting input. 3'b110, connect channel 2 and channel 3 at the same time. ASN is connected to internal OA_VCMI, connecting to HSOA2 non-inverting input. 3'b111, unavailable to users.	R/W

- **CUS_AFE13 register**

CUS_AFE13 Reset value：0x80

7	6	5	4	3	2	1	0
LDO_ULPOA_VO_SEL[1:0]		SAR_INX[3:0]				SAR_REFX[1:0]	

Name		Decription	Type
7:6	LDO_ULPOA_VO_SEL	Selection of micro-power consumption LDO_PIR regulator output voltage VREG. 2'b00, select 1.8 V. 2'b01, select 2.0 V. 2'b10, select 2.2 V. 2'b11, select 2.4 V.	R/W
5:2	SAR_INX	HSOA0 non-inverting input channel selection: 4'b0000, no connection; 4'b0001, connect to A1 channel. 4'b0010, connect to A2 channel. 4'b0011, connect to A3 channel. 4'b0100, connect to A4 channel. 4'b0101, connect to A5 channel. 4'b0110, connect to A6 channel. 4'b0111, connect to A7 channel. 4'b1000, connect to B7 channel. 4'b1001, connect to B6 channel. 4'b1010, connect to B5 channel. 4'b1011, connect to ASN channel, or LPOA0 output channel. 4'b1100, connect to PSN channel, or LPOA1 output channel. 4'b1101, unavailable to users. 4'b1110, unavailable to users. 4'b1111, unavailable to users.	R/W
1:0	SAR_REFX	ADC reference voltage selection. 2'b00, select VDDA, which is the output of LDO_SAR regulator. 2'b01, select 1.2 V band gap reference (VBG), driving ADC with internal buffer; 2'b10, select to input external reference voltage from port B6, driving ADC with internal buffer. 2'b11, unavailable to users.	R/W

- **CUS_AFE14 register**

CUS_AFE14 Reset value：0xBF

7	6	5	4	3	2	1	0
PD_AFE_OACMI	PIR_ST	PD_AFE_OSADJ	PD_AFE_IACMO	PD_SAR	PD_AFE_OA2	PD_AFE_OA1	PD_AFE_OA0

Name		Decription	Type
7	PD_AFE_OACMI	HSOAn non-inverting input DC bias voltage output enabling. Set to 0, enable DC bias voltage output. Set to 1, disable DC bias voltage output.	R/W
6	ULPOA_ST	Micro-power regulator DC bias circuit startup control bit: Set to 0, enable (default). Set to 1, disable.	R/W
4	PD_AFE_IACMO	Instrumentation amplifier output reference voltage enabling. Set to 0, enable. Set to 1, disable.	R/W

Name		Decription	Type
3	PD_SAR	SAR-ADC enabling control. Set to 0, enable. Set to 1, disable.	R/W
2	PD_AFE_OA2	HSOA2 enabling control. Set to 0, enable. Set to 1, disable.	R/W
1	PD_AFE_OA1	HSOA1 enabling control. Set to 0, enable. Set to 1, disable.	R/W
0	PD_AFE_OA0	HSOA0 enabling control. Set to 0, enable. Set to 1, disable.	R/W

- **CUS_AFE15 register**

CUS_AFE15 Reset value：0xBF

7	6	5	4	3	2	1	0
LDO_SAR_VO_SEL[1:0]		LDO_SAR_RAILB	PD_BG	SAR_LBD_DIS	SAR_REF_DIS	PD_LDO_SAR	PD_AFE_VTR

Name		Decription	Type
7:6	LDO_SAR_VO_SEL	Internal LDO_SAR regulator output voltage selection. 2'b00, output 1.8 V. 2'b01, output 2.0 V. 2'b10, output 2.2 V. 2'b11, output 2.4 V.	R/W
5	LDO_SAR_RAILB	Bypass internal LDO_SAR regulator output. Set to 0, bypass the internal LDO regulator.VDDA supplies power for the chip in this case. Set to 1, do not bypass the internal l LDO_SAR regulator.	R/W
4	PD_BG	Built-in BandGap reference source (VBG) enabling control. Set to 0, enable BandGap (1.2 V). Set to 1, disable BandGap.	R/W
3	SAR_LBD_DIS	Supply power detection enabling. Set to 0, enable the LBD function. Set to 1, disable the LBD function.	R/W
2	SAR_REF_DIS	ADC reference voltage enabling. Set to 0, enable. Set to 1, disable.	R/W
1	PD_LDO_SAR	Internal LDO_SAR regulator enabling control. Set to 0, enable. Set to 1, disable.	R/W
0	PD_AFE_VTR	AFE DC bias enabling. When HSOAs or ADC in operating, it must be set to 0. Set to 0, enable. Set to 1, disable.	R/W

- **CUS_AFE16 register**

CUS_AFE16 Reset value：0x0F

7	6	5	4	3	2	1	0
SAR_MBC0	SAR_MBC1	SAR_STM[1:0]		PD_LDO_ULPOA	PD_ULPOA_VTR	PD_ULPOA1	PD_ULPOA0

Name		Decription	Type
7	SAR_MBC0	SAR-ADC second high bit conversion time selection. Set to 0, 1 ADC clock. Set to 1, 2 ADC clocks.	R/W
6	SAR_MBC1	SAR-ADC highest bit conversion time selection. Set to 0, 2 ADC clocks. Set to 1, 4 ADC clocks.	R/W
5:4	SAR_STM	SAR-ADC sampling time selection. 2'b00, 2 ADC clocks. 2'b01, 4 ADC clocks. 2'b10, 6 ADC clocks. 2'b11, 8 ADC clocks.	R/W
3	PD_LDO_ULPOA	Micro-power LDO_PIR regulator enabling. Set to 0, enable ULPOA's LDO Regulator output. Set to 1, disable ULPOA's LDO Regulator output.	R/W
2	PD_ULPOA_VTR	Micro-power circuit bias current enabling control. Set to 0, enable. When LDO_PIR Regulator or LPOAs are in operating, must set it to 0. Set to 1, disable.	R/W
1	PD_ULPOA1	Set to 0, enable ULPOA1. Set to 1, disable ULPOA1.	R/W
0	PD_ULPOA0	Set to 0, enable ULPOA0. Set to 1, disable ULPOA0.	R/W

- **CUS_SNOOZE1 register**

CUS_SNOOZE1 Reset value：0x00

7	6	5	4	3	2	1	0
SNOOZE_TIMER_M_SLEEP[7:0]							

Name	Decription	Type
SNOOZE_TIMER_M_SLEEP	In SNOOZE mode, the sleep timer calculates the M value periodcally.	R/W

Notes: The SNOOZE sleep time calculation formular is as below.

$$T_{SNOOZE} = M \times 2^{(R+1)} \times T_{CLK}$$

In above, TCLK is provided by the system LFOSC module. By default, the LFOSC clock source comes from the internal LPOSC, namely a 32 kHz low-power RC clock with TCLK as 31.25us. If the LFOSC clock selects external LXOSC, namely a 32.768 kHz crystal oscillator, the TCLK is is 30.5176 us.

- **CUS_SNOOZE2 register**

CUS_SNOOZE2 Reset value：0x00

7	6	5	4	3	2	1	0
SNOOZE_UTH[9:8]		SNOOZE_DTH[9:8]		SNOOZE_TIMER_R_SLEEP[3:0]			

Name		Decription	Type
7:6	SNOOZE_UTH	The higher 2 bits of the upper limit interrupt threshold of ADC detection window interrupt.	R/W
5:4	SNOOZE_DTH	The higher 2 bits of the lower limit interrupt threshold of ADC detection window interrupt.	R/W
3:0	SNOOZE_TIMER_M_SLEEP	In SNOOZE mode, the sleep timer calculates the R value periodically.	R/W

- **CUS_SNOOZE3 / 4 register set**

CUS_SNOOZE3 / 4 Reset value：0x00 / 0x00

	7	6	5	4	3	2	1	0
3	SNOOZE_UTH[7:0]							
4	SNOOZE_DTH[7:0]							

Name	Decription	Type
SNOOZE_UTH	The lower 8 bits of upper limit interrupt threshold of ADC detection window interrupt.	R/W
SNOOZE_DTH	The lower 8 bits of lower limit interrupt threshold of ADC detection window interrupt.	R/W

Note: SNOOZE_UTH and SNOOZE_DTH are 10-bit values, which will be compared to the upper 10 bits of the SAR-ADC sample.

- **CUS_SNOOZE5 register**

CUS_SNOOZE5 Reset value：0x40

7	6	5	4	3	2	1	0
SAR_CKX[1:0]		Reserved	Reserved	DWTH_WK_EN	UPTH_WK_EN	WOUT_WK_EN	WIN_WK_EN

Name		Decription	Type
7:6	SAR_CKX	ADC clock frequency selection: (recommend to use default frequency) 2'b00, select 0.5 MHz. 2'b01, select 1.0 MHz (default setting). 2'b10, select 1.5 MHz. 2'b11, select 2.0 MHz.	R/W
3	DWTH_WK_EN	Lower-limit interrupt enabling. Set to 0, disable. Set to 1, enable the interrupt wakeup when SAR_DATA[11:2] < SNOOZE_DTH.	R/W
2	UPTH_WK_EN	Upper-limit interrupt enabling. Set to 0, disable. Set to 1, enable the interrupt wakeup when SAR_DATA[11:2] > SNOOZE_UTH.	R/W
1	WOUT_WK_EN	Out-of-window interrupt enabling. Set to 0, disable. Set to 1 to enable the interrupt wakeup whenSAR_DATA[11:2] > SNOOZE_UTH or SAR_DATA[11:2] < SNOOZE_DTH.	R/W

Name		Decription	Type
0	WIN_WK_EN	In-window interrupt enabling. Set to 0, disable. Set to 1 to enable the interrupt wakeup when tSNOOZE_DTH < SAR_DATA[11:2] < SNOOZE_UTH.	R/W

- **CUS_SNOOZE6 register**

CUS_SNOOZE6 Reset value：0x00

7	6	5	4	3	2	1	0
GPIO_HOLD	Reserved	Reserved	Reserved	DWTH_WK_INT	UPTH_WK_INT	WOUT_WK_INT	WIN_WK_INT

Name		Decription	Type
3	DWTH_WK_INT	Lower-limit interrupt enabling. Read as 0, no interrupt occurs. Read as 1, interrupt is generated for SAR_DATA[11:2] < SNOOZE_DTH.	R
2	UPTH_WK_INT	Upper-limit interrupt enabling. Read as 0, no interrupt occurs. Read as 1, interrupt is generated for SAR_DATA[11:2] > SNOOZE_UTH.	R
1	WOUT_WK_INT	Out-of-window interrupt enabling. Read as 0, no interrupt occurs. Read as 1, interrupt is generated for when SAR_DATA[11:2] > SNOOZE_UTH or SAR_DATA[11:2] < SNOOZE_DTH.	R
0	WIN_WK_INT	In-window interrupt enabling. Read as 0, no interrupt occurs. Read as 1, interrupt is generated for SNOOZE_DTH < SAR_DATA[11:2] < SNOOZE_UTH.	R

- **CUS_SYSCTL3 register**

CUS_SYSCTL3 Reset value：0x00

7	6	5	4	3	2	1	0
LED_INV	AFE_IR_EN	SNOOZE_EN	SNOOZE_DEBUG_EN	LFRX_DEBUG_EN	LFRX_EN	SLPT_WAKEUP_MODE	SLEEP_TIMER_EN

Name		Decription	Type
6	AFE_IR_EN	In SNOOZE mode, the constant current source drive synchronous pulse output enabling Set to 0, disable Set to 1, enable.	R/W
5	SNOOZE_EN	SNOOZE mode enabling. Set to 0, disable the SNOOZE function. Set to 1, enable the SNOOZE function.	R/W
4	SNOOZE_DEBUG_EN	SNOOZE simulation debugging mode enabling. Set to 0, disable Set to 1, enable.	R/W

- **CUS_SYSCTL11 register**

CUS_SYSCTL11 Reset value: 0x00

7	6	5	4	3	2	1	0
SLPT_MANU_RSTN	Reserved	Reserved	SNOOZE_MANU_CLR	LBD_MANU_CLR	LFRX_MANU_CLR	SLPT_MANU_CLR	BUT_MANU_CLR

Name		Decription	Type
4	SNOOZE_MANU_CLR	When the system enables the SNOOZE function and it is woken up, it needs to manually set the bit to 1, which clears the interrupt flag processing, then the system resets the bit to 0 automatically.	R/W

- **CUS_SYSCTL12 register**

CUS_SYSCTL12 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	SNOOZE_WAKEUP		WKID_PASS	SYNC_PASS	LFRX_SIGNAL_OK	SLEEP_TIMESUP	KEY_LAUNCH

Name		Decription	Type
6	SNOOZE_WAKEUP	SNOOZE interrupt flag (namely wakeup/interrupt flag). Valid when read as 1.	R

- **CUS_SYSCTL13 register**

CUS_SYSCTL13 Reset value：0x00

7	6	5	4	3	2	1	0
LBD_STATUS	LBD_FINISH	LBD_AVG_SEL	LBD_ENABLE	SAR_DATA_UPDATE	SAR_MSTART	SAR_TRIGGER	SAR_CLK_EN

Name		Decription	Type
3	SAR_DATA_UPDATE	ADC conversion end flag: Read as 0, ADC conversion is not completed. Read as 1, the ADC conversion is completed, and it will be automatically cleared by hardware 3 ADC clock cycles afterit taking effect.	R
2	SAR_MSTART	ADC continuous conversion software trigger control. Set to 0, disable the ADC continuous conversion function. Set to 1, enable the ADC continuous conversion function.	R/W
1	SAR_TRIGGER	ADC one-shot conversion software trigger control. Set to 0, disable the ADC single conversion function. Set to 1, enable the ADC single conversion function.	R/W
0	SAR_CLK_EN	ADC clock enabling. Set to 0, disable the ADC conversion function. Set to 1, enable the ADC conversion function.	R/W

- **CUS_SYSCTL14 register**

CUS_SYSCTL14 Reset value：0x00

7	6	5	4	3	2	1	0
SAR_ADC_DATA[11:4]							

Name	Decription	Type
SAR_ADC_DATA	Higher 8 bits of SAR-ADC sample value.	R/W

- **CUS_SYSCTL15 register**

CUS_SYSCTL15 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SAR_ADC_DATA[3:0]			

Name		Decription	Type
3:0	SAR_ADC_DATA	lower 4 bits of SAR-ADC sample value.	R/W

- **CUS_RESV5 register**

CUS_RESV5 Reset value：0xC1

7	6	5	4	3	2	1	0
LPOA0_PIN_DIS	LPOA1_PIN_DIS	WDT_REFRESH	WDT_START	WDT_RESET_TH[2:0]			WDT_DIS

Name		Decription	Type
7	LPOA0_PIN_DIS	LPOA0 non-inverting input port connection control。 Set to 0, LPOA0 non-inverting input is connected to A6 pin。 Set to 1, the LPOA0 non-inverting input is disconnected from the A6 pin。	R/W
6	LPOA1_PIN_DIS	LPOA1 non-inverting input port connection control。 Set to 0, the non-inverting input of LPOA1 is connected to the B7 pin。 Set to 1, LPOA1 non-inverting input is disconnected from B7 pin。	R/W

3.13 Constant Current Source Driver Register Set

Table 14. Constant Current Source Driver Register Set List

Name	Storage Area	Sub-area	Address	Reset	Function
CUS_AFE17	Block0	--	0x10	0x01	Constant current source driver register 1
CUS_AFE18	Block0	--	0x11	0x00	Constant current source driver register 2
CUS_SYSCTL19	Block0	--	0x70	0x03	System control register 19 (constant current source driver pulse output port control)

- **CUS_AFE17 register**

CUS_AFE17 Reset value：0x01

7	6	5	4	3	2	1	0
HDRV_SEL[4:0]					DRV_ENH	DRV_MAN_EN	PD_DRV

Name		Decription	Type
7:3	HDRV_SEL	Enhanced constant current source driver current selection, valid when HDRV_EN is 1,	R/W
2	DRV_ENH	Enhanced constant current source driver current reference enhancement enabling (by 10%). Set to 0, disable. Set to 1, enable.	R/W
1	DRV_MAN_EN	Constant current source current driving stage enabling. Set to 0, disable. Set to 1, enable.	R/W
0	PD_DRV	Constant current source current reference circuit enabling. Set to 0, enable. Set to 1, disable.	R/W

Value	mA		Value	mA		Value	mA
5'b00000	0.0		5'b01011	94.3		5'b10110	187.8
5'b00001	8.5		5'b01100	103.2		5'b10111	195.6
5'b00010	17.0		5'b01101	111.3		5'b11000	207.3
5'b00011	25.4		5'b01110	120.0		5'b11001	215.4
5'b00100	34.5		5'b01111	128.2		5'b11010	223.6
5'b00101	42.9		5'b10000	138.5		5'b11011	231.4
5'b00110	51.2		5'b10001	146.7		5'b11100	240.3
5'b00111	59.2		5'b10010	155.0		5'b11101	248.1
5'b01000	69.5		5'b10011	163.0		5'b11110	256.0
5'b01001	77.8		5'b10100	171.8		5'b11111	263.7
5'b01010	86.2		5'b10101	179.8			

- **CUS_AFE18 register**

CUS_AFE18 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	NDRV_SEL[3:0]				NDRV_EN	HDRV_EN	LDO_PIR_OE

<table>
<tr><th colspan="2">Name</th><th>Decription</th><th>Type</th></tr>
<tr><td>7:3</td><td>NDRV_SEL</td><td>Ordinary constant current source driver current selection, valid when NDRV _EN is 1,

<table>
<tr><th>Value</th><th>Current(mA)</th><th></th><th>Value</th><th>Current(mA)</th></tr>
<tr><td>4’b0000</td><td>0.0</td><td rowspan="8"></td><td>4’b1000</td><td>22.0</td></tr>
<tr><td>4’b0001</td><td>2.8</td><td>4’b1001</td><td>24.8</td></tr>
<tr><td>4’b0010</td><td>5.6</td><td>4’b1010</td><td>27.6</td></tr>
<tr><td>4’b0011</td><td>8.4</td><td>4’b1011</td><td>30.4</td></tr>
<tr><td>4’b0100</td><td>11.3</td><td>4’b1100</td><td>33.3</td></tr>
<tr><td>4’b0101</td><td>14.1</td><td>4’b1101</td><td>36.0</td></tr>
<tr><td>4’b0110</td><td>17.0</td><td>4’b1110</td><td>38.8</td></tr>
<tr><td>4’b0111</td><td>19.7</td><td>4’b1111</td><td>41.5</td></tr>
</table></td><td>R/W</td></tr>
<tr><td>2</td><td>NDRV_EN</td><td>Ordinary constant current source driving stage enabling.
Set to 0, disable.
Set to 1, enable.</td><td>R/W</td></tr>
<tr><td>1</td><td>HDRV_EN</td><td>Enhanced constant current source driving stage enabling.
Set to 0, disable.
Set to 1, enable.</td><td>R/W</td></tr>
<tr><td>0</td><td>LDO_PIR_OE</td><td>Micro-power LDO_PIR regulator output enabling.
Set to 0, disable. The output of the micropower LDO_PIR regulator is disconnected from the VREG_OUT / D3 pin;
Set to 1, enable. The micro-power LDO_PIR regulator outputs voltage through the REG_OUT / D3 pin.</td><td>R/W</td></tr>
</table>

- **CUS_SYSCTL19 Register**

CUS_SYSCTL19 Reset value：0x00

7	6	5	4	3	2	1	0
LFRX_OSC_OUT_EN	IRLED_DOUT_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Name		Decription	Type
6	IRLED_CLK_EN	constant current source drive pulse output port enabling In SNOOZE mode (namely ADC sampling operating window enabling) Set to 0, disable Set to 1, enable. The synchronization pulse generated by the hardware is output through the B5 pin.	R/W

3.14 True Random Number Generation Module

Table 15. True Random Number Module Register Set List

Name	Storage Area	Sub-area	Address	Reset	Function
RNG_CTL	Block1	Bank1	0xBE	0x04	True Random Number Generation control register.
RNG_SUM	Block1	Bank1	0xBF	0x00	8-bit random number generation result.

- **RNG_CTL register**

RNG_CTL Reset value：0x04

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RNG_SUM_VLD	Reserved	Reserved	Reserved	RNG_START

Name		Decription	Type
4	RNG_SUM_VLD	The valid flag of random number generation.	R
0	RNG_START	The start flag of random number generation.	R/W

- **RNG_SUM register**

RNG_SUM Reset value：0x00

7	6	5	4	3	2	1	0
RNG_SUM[7:0]							

Name	Decription	Type
RNG_SUM	8-bit random number result	R

Notes: Whe using true random number function, users only need to call API sys_get_random_data. Refer to AN282 CMT216xA API Function Library User Guide for more details.

3.15 Watchdog (WDT) Register Set

Table 16 Watchdog (WDT) Register Set List

Name	Storage Area	Sub-area	Address	Reset	Function
CUS_RESV5	Block0	--	0x7A	0x01	Watchdog control register

- **CUS_RESV5 register**

CUS_RESV5 Reset value：0xC1

7	6	5	4	3	2	1	0
ULPOA0_PIN_DIS	ULPOA1_PIN_DIS	WDT_REFRESH	WDT_START	WDT_RESET_TH[2:0]			WDT_DIS

Name		Decription	Type
5	WDT_REFRESH	Set to 0, invalid. Set to 1, clear the watchdog circuit (feed dog).	R/W
4	WDT_START[1]	Set to 0, stop/pause watchdog. Set to 1, start watchdog.	R/W
3:1	WDT_RESET_TH	Watchdog timer threshold. 000, 32 ms. 001, 64 ms. 010, 128 ms. 011, 256 ms. 100, 512 ms. 101, 1s. 110, 2s. 111, 4s.	R/W
0	WDT_DIS[2]	Set to 0, enable the watchdog module . Set to 1, disable the watchdog module ..	R/W

Notes:

[1]. When the watchdog module is enabled, the watchdog counting can be started or stopped by WDT_START. It can also be paused during the counting and resumed to continue counting.

[2]. When the watchdog module is enabled, namely WDT_DIS = 0, the watchdog module clock is still running and consumes power even if the watchdog counting is paused by WDT_START.

[3]. The clock source of the watchdog is provided by LFOSC, please enable LFOSC when using the watchdog function.

3.16 Sleep Timer Module Register Set

Table 17. Sleep Timer Module Register Set List

Name	Storage Area	Sub-area	Address	Reset	Function
CUS_AFE8	Block0	--	0x07	0x53	Analog front end configuration register 8，clock configuration register
CUS_SYSCTL1	Block0	--	0x46	0x00	Sleep timer counting period register1
CUS_SYSCTL2	Block0	--	0x47	0x00	Sleep timer counting period register2
CUS_SYSCTL3	Block0	--	0x50	0x00	System control register3
CUS_SYSCTL11	Block0	--	0x68	0x80	System control register11
CUS_SYSCTL12	Block0	--	0x69	0x00	System control register12

- **CUS_AFE8 register**

CUS_AFE8 Reset value：0x53

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	HFOSC_CLK_SEL[1:0]		LFOSC_LFXO_SEL	PD_LFXO	PD_LFOSC

Name		Decription	Type
2	LFOSC_LFXO_SEL	Sleep timer clock source selection. Set to 0, select the internal 32 kHz low power oscillator. Set to 1, select the external 32.768 kHz crystal oscillator.	R/W
1	PD_LFXO	Set to 0, open 32.768 kHz crystal oscillator. Set to 1, close 32.768 kHz crystal oscillator.	R/W
0	PD_LFOSC	Set to 0, open 32 kHz internal low-power crystal oscillator. Set to 1, close 32 kHz internal low-power crystal oscillator.	R/W

- **CUS_SYSCTL1 register**

CUS_SYSCTL1 Reset value：0x00

7	6	5	4	3	2	1	0
TIMER_M_SLEEP[7:0]							

Name	Decription	Type
TIMER_M_SLEEP	The lower 7 bits of sleep timer's M value. See CUS_SYSCTL2 below for details.	R/W

- **CUS_SYSCTL2 register**

CUS_SYSCTL2 Reset value：0x00

7	6	5	4	3	2	1	0
TIMER_M_SLEEP[11:8]				TIMER_R_SLEEP[3:0]			

Name	Decription	Type
TIMER_M_SLEEP	The higher 4 bits of sleep timer's M value.	R/W
TIMER_R_SLEEP	The R value of sleep timer count period.	R/W

Notes: The sleep time timing period formula is as below.

$$T_{SLEEP} = M \times 2^{(R+1)} \times 31.25\ us$$

M is the value of TIMER_M_SLEEP，R is the value of TIMER_R_SLEEP, 31.25 us corresponds to the internal 32 kHz clock.

- **CUS_SYSCTL3 register**

CUS_SYSCTL3 Reset value：0x00

7	6	5	4	3	2	1	0
LED_INV	AFE_IR_EN	SNOOZE_EN	SNOOZE_DEBUG_EN	LFRX_DEBUG_EN	LFRX_EN	SLPT_WAKEUP_MODE	SLEEP_TIMER_EN

Name		Decription	Type
1	SLPT_WAKEUP_MODE	Sleep timer operating mode selection[1]. Set to 0, select RTC mode. Set to 1, select WAKEUP (wakeup only) mode.	R/W
0	SLEEP_TIMER_EN	Sleep timer enabling bit. Set to 0, disable sleep timer. Set to 1, enable sleep timer.	R/W

Notes: The difference between RTC mode and WAKEUP mode is as follows.

RTC is a continuous timing mode and generates a flag when reaching period end regardless of system status. If the system is running, an interrupt can be generated (if the corresponding interrupt is enabled). However, if the system is in ShutDown mode, it awakes the system first,then after code laoding ,it has processing according to the system software (such as re-entering the corresponding interrupt service). Therefore, the RTC mode is suitable for application senarios where strict timing is required. Generally, an external 32.768 kHz is recommended to produce a more accurate timing period in this case.

In WAKEUP mode (also known as wakeup-only mode), it only has timing when the system is in ShutDown mode. when the system is in non-ShutDown mode, it stops timing. Therefore, the main purpose is to wake up the system from ShutDown mode. The operation of WAKEUP mode is relatively simple with no interrupt service required. As the main function is to wakeup, It's more suitable for senarios with non-strict timing requirement, namely, it only needs to wake up the system winthin a certain period.

- **CUS_SYSCTL11 register**

CUS_SYSCTL11 Reset value：0x80

7	6	5	4	3	2	1	0
SLPT_MANU_RSTN	Reserved	Reserved	SNOOZE_MANU_CLR	LBD_MANU_CLR	LFRX_MANU_CLR	SLPT_MANU_CLR	BUT_MANU_CLR

Name		Decription	Type
7	SLPT_MANU_RSTN	When the system needs to reconfigure the sleep timer parameters, users need to reset the sleep timer. The specific operation is: set this bit to 0 first, and then set it to 1. This bit is set to 1 by default.	R/W
1	SLPT_MANU_CLR	When the system is woken up by the sleep timer (in RTC or WAKEUP mode), this bit needs to be manually set to 1, that is, the interrupt flag is cleared, then system automatically resets the bit to 0.	R/W

- **CUS_SYSCTL12 register**

CUS_SYSCTL12 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	SNOOZE_WAKEUP		WKID_PASS	SYNC_PASS	LFRX_SIGNAL_OK	SLEEP_TIMESUP	KEY_LAUNCH

Name		Decription	Type
1	SLEEP_TIMESUP	Sleep timer timing period full flag (namely wake/interrupt flag). Valid when reading as 1.	R

3.17 Interrupt Related Register Set

Table 18. Interrupt Related Register Set List

Name	Storage Area	Sub-area	Address	Reset	Function
TCON	Block1	Bank0	0x88	0x00	Timer1 control register (see *Section 3.2 Timer1 register set* for details)
IEN0	Block1	Bank0	0xA8	0x00	Interrupt enabling register0 (see *Section 3.1 8051 core register set* for details)
IPL0	Block1	Bank0	0xB8	0x00	Interrupt priority register0 (see *Section 3.1 8051 core register set* for details)
IEN1	Block1	Bank0	0xE6	0x00	Interrupt enabling register1 (see *Section 3.1 8051 core register set* for details)
IRCON1	Block1	Bank0	0xF1	0x00	Peripheral interrupt request flag register (see *Section 3.1 8051 core register set* for details)
IPL1	Block1	Bank0	0xF6	0x00	Interrupt priority register1 (see *Section 3.1 8051 core register set* for details)
IRQ0_SEL	Block1	Bank0	0xAF	0x00	external interrupt 0 configuration register
IRQ1_SEL	Block1	Bank0	0xB0	0x00	external interrupt 1 configuration register
IRQ2_SEL	Block1	Bank0	0xB1	0x00	external interrupt 2 configuration register
IRQ3_SEL	Block1	Bank0	0xB2	0x00	external interrupt 3 configuration register
IRQ4_SEL	Block1	Bank0	0xB3	0x00	external interrupt 4 configuration register
IRQ5_SEL	Block1	Bank0	0xB4	0x00	external interrupt 5 configuration register
IRQ6_SEL	Block1	Bank0	0xB5	0x00	external interrupt 6 configuration register
IRQ7_SEL	Block1	Bank0	0xB6	0x00	external interrupt 7 configuration register

- **IRQn_SEL register（n=[7:0]）**

IRQn_SEL Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved	IRQ_SW[n]	IRQn_SEL[5:0]					

Name		Decription	Type
6	IRQ_SW[n]	Interrupt polarity selection of external interrupt source n[1] Set to 0, the falling edge triggers the interrupt. Set to 1, the rising edge triggers the interrupt.	R/W
5:0	IRQn_SEL	External Interrupt triggering selection.	R/W

Value	Interrupt Source Signal	Polarity	Description
0x0F – 0x00	GPIO_IN_[15:0]	Depending on different port	GPIO[15:0] interrupt
0x10	SLEEP_TIMESUP	Rising edge	Sleep timer interrupt signal
0x11	LFRX_MCU_RCLK	Rising edge	Low frequency data clock interrupt signal
0x12	LFRX_MCU_RDATA	Depending on different data	Low frequency data interrupt signal
0x13	GPIO_IN_16	Depending on different port	GPIO16 port interrupt
0x14	WKID_PASS	Rising edge	Successful low frequency wakeup ID matching
0x15	SYNC_PASS	Rising edge	Successful low frequency sync word matching
0x16	SAR_DATA_UPDATE	Rising edge	ADC conversion complete interrupt
0x17	LFRX_SIGNAL_OK	Rising edge	Valid Low frequency carrier detection interrupt
0x18	TMRA_IFG	Rising edge	TimerA interrupt signal
0x19	TACCR0_IFG	Depending on different input	TimerA capture 0 interupt signal
0x1A	TACCR1_IFG	Depending on different input	TimerA capture 1 interupt signal
0x1B	TACCR2_IFG	Depending on different input	TimerA capture 2 interupt signal
0x1C	TX_SYM_EMPTY	Rising edge	High frequency transmission complete interrupt
0x1D	SPI_TXE	Rising edge	SPI bus transmission empty interrupt
0x1E	SPI_RXNE	Rising edge	SPI bus receiving non-empty interrupt
0x1F	TMRB_IFG	Rising edge	TimerB interrupt signal
0x20	TBCCR0_IFG	Depending on different input	TimerB capture 0 interrupt signal
0x21	TBCCR1_IFG	Depending on different input	TimerB capture 1 interrupt signal
0x22	TBCCR2_IFG	Depending on different input	TimerB capture 2 interrupt signal

Note [1]:

- *For external interrupt 2-7, it only supports the edge triggering mode and the interrupt polarity selection is matched according to the polarity in the interrupt source signal table.*
- *For external interrupts 0 and 1, when the edge-triggered interrupt is selected, the polarity selection is the same as that of the external interrupt 2-7. If the level triggering interrupt mode is selected, when IRQ_SW[0/1] = 0, it's ative low; when IRQ_SW[0/1] = 1, it's active high.*

3.18 System Related register Set

Table 19. System Related register Set

Name	Storage Area	Sub-area	Address	Reset	Function
CUS_AFE8	Block0	--	0x07	0x53	Analog front end configuration register8, clock configuration register
CUS_SYSCTL18	Block0	--	0x6F	0x00	System clock control register18, clock ourput control register
CUS_SYSCTL20	Block0	--	0x70		System control register19
CLK_SYS_DIV	Block0	--	0x71	0x13	System control register20
SYS_CTL	Block0	--	0x79		

- **CUS_AFE8 register**

CUS_AFE8 Reset value：0x53

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	HFOSC_CLK_SEL[1:0]		LFOSC_LFXO_SEL	PD_LFXO	PD_LFOSC

Name		Decription	Type
4:3	HFOSC_CLK_SEL[1]	Internal high speed RC (HFOSC) frequency selection. 2'b00, HFOSC = 3 MHz. 2'b01, HFOSC = 12 MHz. 2'b10 and 11, HFOSC = 24 MHz (default) .	R/W
2	LFOSC_LFXO_SEL	Sleep timer clock source selection. Set to 0, select the internal 32 kHz low power oscillator. Set to 1, select the external 32.768 kHz crystal oscillator.	R/W
1	PD_LFXO	Set to 0, open the 32.768 kHz cryatal oscillator. Set to 1, close the 32.768 kHz cryatal oscillator.	R/W
0	PD_LFOSC	Set to 0, open the 32 kHz low-power oscillator. Set to 1, close the 32 kHz low-power oscillator.	R/W

Notes:

1. *The system current consume is different for HFOSC when different frequencies are selected. For example, the current consumption of 24 MHz is greater than that of 12 MHz and the 12 MHz consumption current is greater than that of 3 MHz similarly. Please refer to the data sheet docuement for specific current consumption. In addition, HFOSC supports frequency switching during operatng, which can be set by calling the API function sys_set_hfosc_clk_sel. Moreover, it should be noted that HFOSC also serves as the clock source for some peripherals (such as Timer1, TimerA/B, etc.), so the modification will also affect the operating time of the associated peripherals.*
2. *After the clock frequency switching through HFOSC_CLK_SEL (or using the API function sys_set_hfosc_clk_sel), it is recommended to use the clock calibration function cal_hfosc_clk_high_coase_calibration to calibrate the clock.*

- **CUS_SYSCTL18 register**

CUS_SYSCTL18 Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	PAD_GROUP2_EN	PAD_GROUP1_EN	LFOSC_CLKOUT_EN	HFOSC_CLKOUT_EN

Name		Decription	Type
3	PAD_GROUP2_EN	Co-work with LFOSC_CLKOUT_EN and HFOSC_CLKOUT_EN, refer to the below table for details.	R/W
2	PAD_GROUP1_EN		
1	LFOSC_CLKOUT_EN	Low speed clock(intrnal 32 kHz or exteral 32.768 kHz) output enabling control. Set to 0, low speed clock does not output. Set to 1, low speed clock outputs. Refer to below table for the GPIO mapping.	R/W
0	HFOSC_CLKOUT_EN	High speed clock output (HFOSC) enabling control. Set to 0, high speed clock does not output. Set to 1, high speed clock outputs. Refer to below table for the GPIO mapping.	R/W

When LFOSC_CLKOUT_EN=1 or HFOSC_CLKOUT_EN=1，

PAD_GROUP1_EN	PAD_GROUP2_EN	Low Speed Clock GPIO Mapping
0	0	GPIO8, namey B0 pin (default)
1	0	GPIO4, namely A4 pin.
0	1	GPIO15, , namely B7pin.

Notes: Cannot set LFOSC_CLKOUT_EN and HFOSC_CLKOUT_EN to 1 at the same time.

- **CUS_SYSCTL20 register**

CUS_SYSCTL20 Reset value：0x13

7	6 5	4	3	2	1 0
Reserved	OTP_CP_VCC_SELN[1:0]	OTP_CP_VTH_SEL	GPIO16_ODR	GPIO16_CNF	GPIO16_MODE[1:0]

Name		Decription	Type
6:5	OTP_CP_VCC_SELN[1]	The Charge Pump selection when loading the OTP code. 2'b00, using the internal Charge Pump each time. 2'b01, smart mode, having VTH comparison to determine whether to use Charge Pump. 2'b10, Reserved, the user cannot select this item. 2'b11, disable the internal Charge Pump.	R/W
4	OTP_CP_VTH_SEL	VTH threshold selection in smart mode (OTP_CP_VCC_SELN=01). Set to 0, VTH is 2.4 V. Set to 0, VTH is 2.8 V.	R/W

Notes: After waking up from ShutDown mode, it loads the running code from OTP into PRAM. This loading process requires reliable power supply, therefore a ChargePump is provided internally. By default, Charge Pump operates upon each code loading. The loading process consumes extra Charge Pump current compared with current consumption of the operating state. If smart

mode is selected, it will compared VCC with the VTH setting. If it is higher than VTH, ChargePump is not used when loading code. Otherwise if it is lower than VTH, ChargePump will be used. If the internal ChargePump is disabled, it will use VCC power supply for each code loading, which is not recommended generally. This register will affect the system operation. Recommend users adopt the default settings. If the product has special requirements on power consumption, please verify the settings carefully!

- **CLK_SYS_DIV register**

CLK_SYS_DIV Reset value：0x00

7	6	5	4	3	2	1	0
Reserved	LFRX_MCU_RCLK	LFRX_MCU_RDATA	Reserved	CLK_SYS_DIV[3:0]			

Name		Decription	Type
3:0	CLK_SYS_DIV[1]	System clock division ratio selection (HFOSC division). 0xxx: 1; 1000: 2; 1001: 4; 1010: 8; 1011: 16; 1100: 32; 1101: 64; 1110: 128; 1111: 256	R/W

Note [1]: The HFOSC frequency division can be set by calling the API function sys_set_system_clk_divider.

- **SYS_CTL register**

SYS_CTL Reset value：0x00

7	6	5	4	3	2	1	0
SFR_CLK_GATE_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Name		Decription	Type
7	SFR_CLK_GATE_EN	SFR regisster clock threshold control. Set to 0, enable. Set to 1, disable.	R/W

Notes:

1. *This control bit is used to control the SFR register clock. If it is set to 1, the SFR register clock is stopped. At the same time, the access operation of the SFR register can no longer be performed, but it can save some power consumption during operation. For non-special scenarios, users are advised to use it with caution!*
2. *SFR mainly refers to the SFR registers in the Block0 and Block1 areas, but does not include the 8051 core register set (see Table 2 for details).*

4 Revise History

Table 20. Revise History Records

Version No.	Chapter	Description	Date
0.5	All	Initial version	2019-06-05
0.5E	All	Modify/add info	2019-12-25

5 Contacts

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