

CMT216xA RFPDK Operation Guide

Overview

This document discusses the operation guide of CMT216xA developing tool kit RFPDK, covering its hardware and software composition, functions and how to program the CMT216xA series chips using this tool.

The product models covered in the document are listed in the table below.

Table 1. Chip Models Supported by CMT216xA RFPDK

Chip Model	
CMT2160A	CMT2163A
CMT2168F02M	CMT2168A
CMT2189D	

Notes:

The CMT216xA RFPDK 5.01 or higher versions support only CMT216xA Programmer hardware V1.1 and higher versions and the firmware version V501 or higher versions. Please refer to figure 6 for displayed version information on GUI.

Table of Contents

1. CMT216xA RFPDK Introduction	3
2. CMT216xA RFPDK Toolkit Hardware and Software Composition	3
3. RFPDK Software Installation	4
4. CMT216xA RFPDK Hardware	4
4.1 CMT216xA Programmer	4
4.1.1 IDC 10P Connecting Line	4
4.1.2 LED Indicator Light	5
4.1.3 USB Socket	6
4.2 Hardware Connection	6
5. Flow for Chip Configuring and Programming Using RFPDK	6
6. RFPDK GUI Operation	7
6.1 Connection Status Information	7
6.2 OTP Configuration	9
6.3 Flash Configuration	13
6.4 Tx Configuration	15
6.4.1 Tx RF Set Configuration	16
6.4.2 Power Set Configuration	17
6.5 LFRx Configuration	18
6.5.1 Analog Configuration	19
6.5.2 Packet Configuration	20
6.5.3 Signal_OK Detect Configuration	21
6.5.4 System Control Configuration	22
6.5.5 GPIO Output Configuration	23
6.5.6 Output Result Auto-calculation	24
7. Firmware Upgrading and Downgrading	26
7.1 Firmware Upgrading	26
7.2 Firmware Downgrading	27
7.3 Handling of False Upgrading Across Different RFPDK Types	29
8. Revision History	30
9. Contacts	31





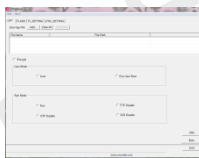
1. CMT216xA RFPDK Introduction

The CMT216xA RFPDK provides visualized configuration and programming function according to CMT216xA series chips. The CMT216xA RFPDK software adapts to run on Windows 2000, XP, 7 and 8 OS. The CMT216xA RFPDK software co-works with both the CMT216xA Programmer hardware and the CMT216xA EM module to accomplish configuration and programming functions for CMT216xA series chips.

2. CMT216xA RFPDK Toolkit Hardware and Software Composition

The CMT216xA RFPDK toolkit includes the following software and hardware.

Table 2 CMT216xA RFPDK Toolkit Hardware and Software Composition

Category	Image	Name	Function and Specification
Hardware		CMT216xA Programmer	CMT216xA series chip online configuration and programming.
		CMT216xA EM module	CMT216xA EM module with built-in CMT216xA series chip, targeting for chip evaluation.
		USB cable	USB male A connector -> USB male B connector, 1.5 m, connecting programmer to computer for importing chip configuration and program data.
		Programming connection cable	1 IDC 10P cable, connecting CMT216xA Programmer to CMT216xA EM module (chip pin).
Software		CMOSTEK CMT216xA RFPDK	Run on PC, providing visualized function of CMT216xA series chip's configuration, programming, exporting configuration and so on.

3. RFPDK Software Installation

▲ Important Information: before installing this software, users must have Windows local administrator role.

Double click the CMT216xA RFPDK installation icon below to install the CMT216xA RFPDK on user PC.



Figure 1. CMT216xA RFPDK Installation Icon

4. CMT216xA RFPDK Hardware

Please see Table2 for CMT216xA RFPDK hardware composition.

4.1 CMT216xA Programmer

CMT216xA Programmer targets for transferring user program and configuration data from RFPDK software to the CMT216xA EM module.

4.1.1 IDC 10P Connecting Line

IDC 10P cable can connect CMT216xA online programmer to CMT216xA EB series boards.

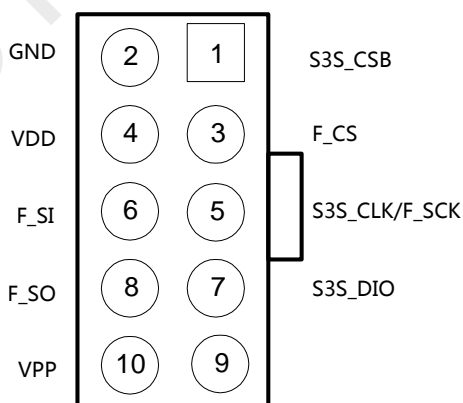


Figure 2. IDC 10P Cable Interface Schematic Diagram

Notes:

The above figure is the front view of facing the 10 sockets of the IDC 10-pin interface

Table 3. IDC 10P Connecting Line Signal Description

#	Name	Corresponding Chip Pin
1	S3S_CSB	B2
2	GND	GND
3	F_CS (Flash Chip Select)	-
4	VDD	VDD
5	S3S_CLK/F_CLK	B3/Flash Clock Input
6	F_SI (Flash Data Input)	-
7	S3S_DIO	B4
8	F_SO (Flash Data Output)	-
9	-	-
10	VPP	B1

4.1.2 LED Indicator Light

As shown in the figure below, CMT216xA Programmer provides 3 LED indicator lights representing 3 operating states with the specific operating state description shown in the table below.

**Figure 3. CMT216xA Programmer LED Indicator Light****Table 4. CMT216xA Programmer LED Indicator Light State Description**

Indicator Light	State Description	Color
Run	When it is detected that the CMT216xA Programmer is connected with PC, this light flashes. When it is programming to evaluation module, this light is on.	Green
Err	In the case of programming failure, this light turns on for 5 seconds.	Red
USB	When the CMT216xA Programmer is connected to PC successfully, this light is on.	Green

4.1.3 USB Socket

The CMT216xA Programmer provides a type B USB socket. The RFPDK toolkit provides an A -> B USB cable for connecting the CMT216xA Programmer to PC. The function of this USB socket is shown below.

- Connecting with PC, which provides power for the CMT216xA Programmer.
- Communicating with the RFPDK software installed on the PC.



Figure 4. USB Socket

4.2 Hardware Connection

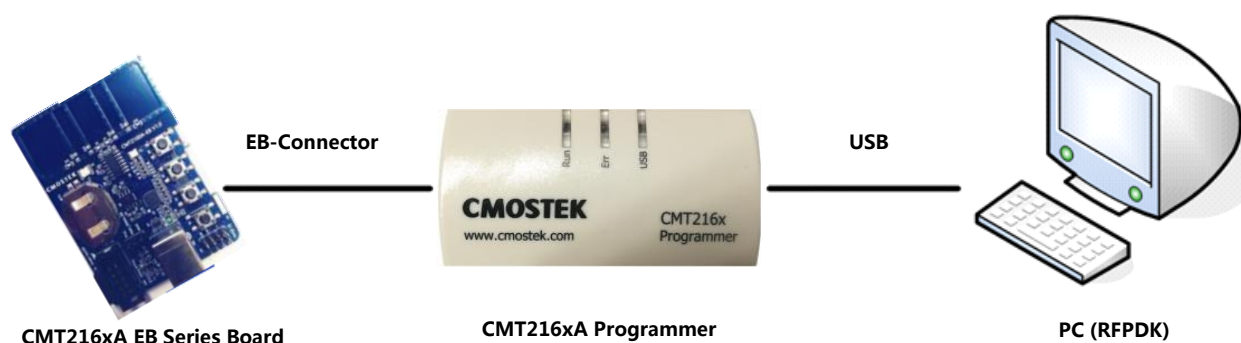


Figure 5. Hardware Connection

5. Flow for Chip Configuring and Programming Using RFPDK

Users can configure and program CMT216xA series chips using RFPDK following the steps below.

1. Connect hardware correctly as shown in Figure 5.
2. The system will install the CMT216xA Programmer driver on the connected PC. If the CMT216xA RFPDK software has already been installed, make sure not run the RFPDK software at this point.
3. Install the CMT216xA RFPDK software as specified in Section 3.
4. Run the CMT216xA RFPDK software then perform the CMT216xA series chip configuration and programming on RFPDK GUI. The CMT216xA EM module is ready to be used in application systems after users finish the above configuration and

programming.

6. RFPDK GUI Operation

6.1 Connection Status Information

The CMT216xA RFPDK can detect device connection status automatically and display the related information in the status area at the bottom of GUI as shown in the figure below.

According to the marked numbers in the figure below, the displayed status information details are described in the table below.

No.	Status Information	Description
①	CMT216x Programmer connection status	When it is connected successfully, it displays in green icon with <i>Connected</i> status. When it is not connected successfully, it displays in red icon with <i>Unconnected</i> status.
②	Chip connection status and chip unit ID	When the chip is identified successfully, it displays in green icon with chip unique ID (UUID). When the chip is not identified successfully, it displays in red icon with value 0.
③	Device type and version information	As shown in the example in the figure below, the meanings are as follows. CMT216x Programmer - <i>Programmer hardware type</i> V1.x - <i>CMT216x Programmer hardware version</i> (Firmware version = 501) - <i>CMT216x Programmer firmware version</i> Device: CMT2163F08M - <i>chip model</i>

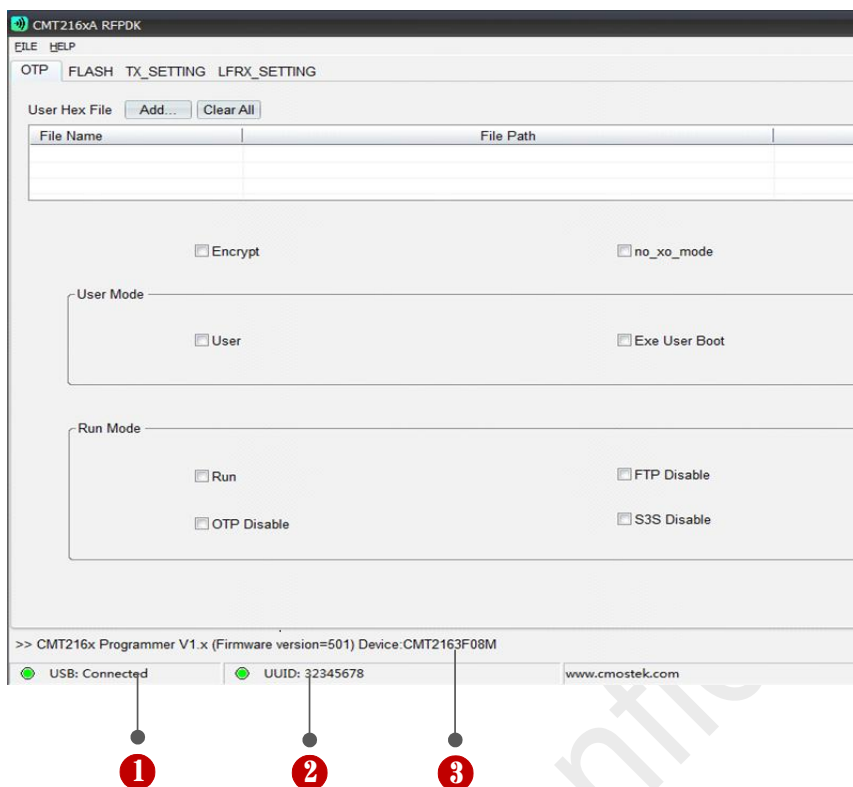


Figure 6. Connection Status - CMT216x Programmer Connection and Chip Identification Being Successful

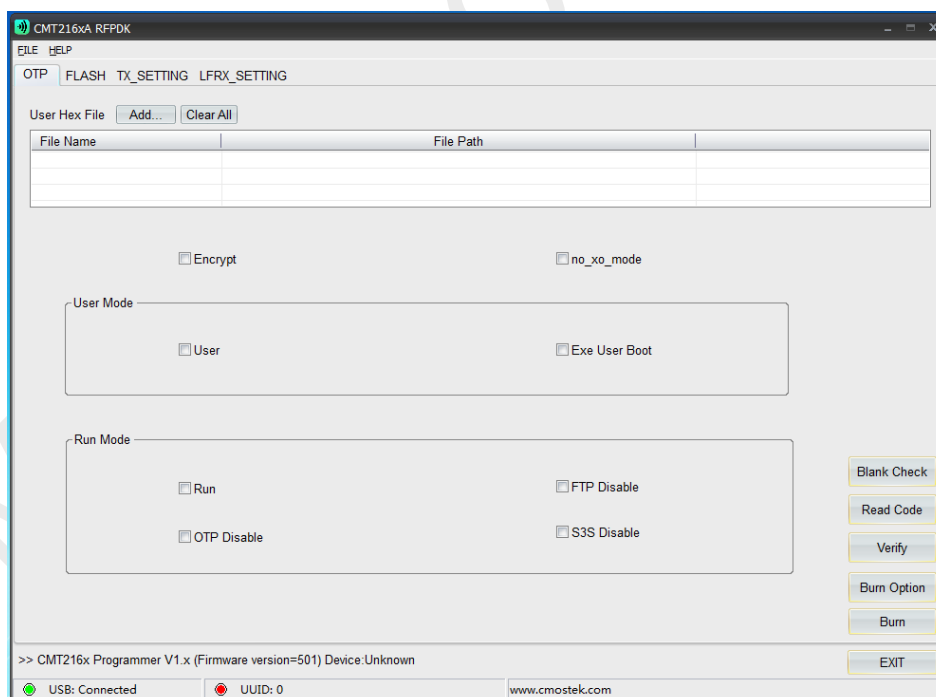


Figure 7. Connection Status - CMT216x Programmer Connection OK But Chip Identification Being Failed

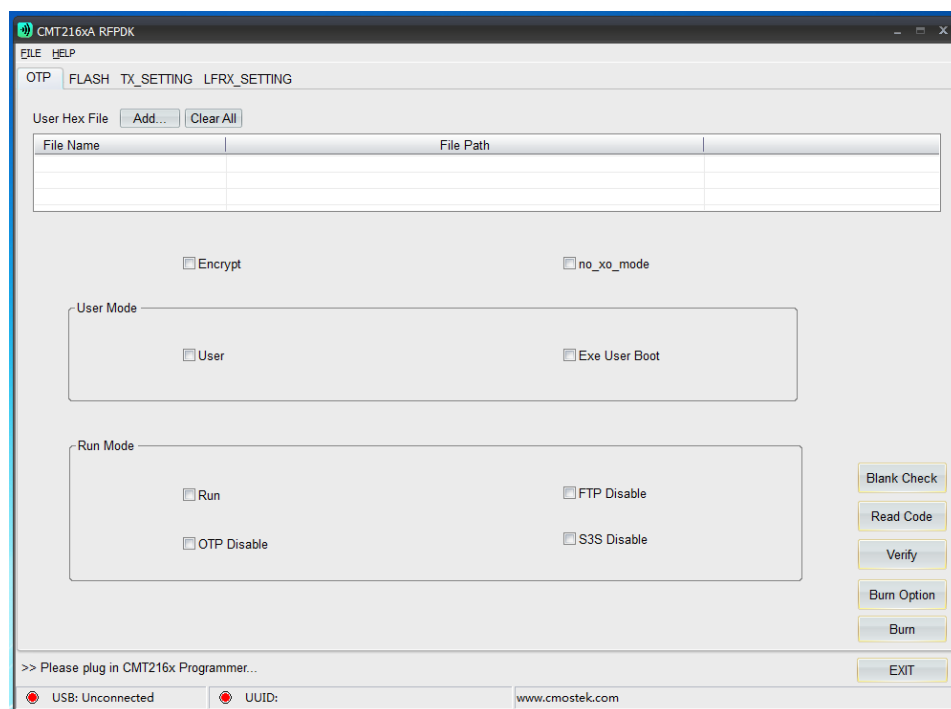


Figure 8. Connection Status - CMT216x Programmer Connection Being Failed
(not connected successfully or connected hardware type is mismatched)

6.2 OTP Configuration

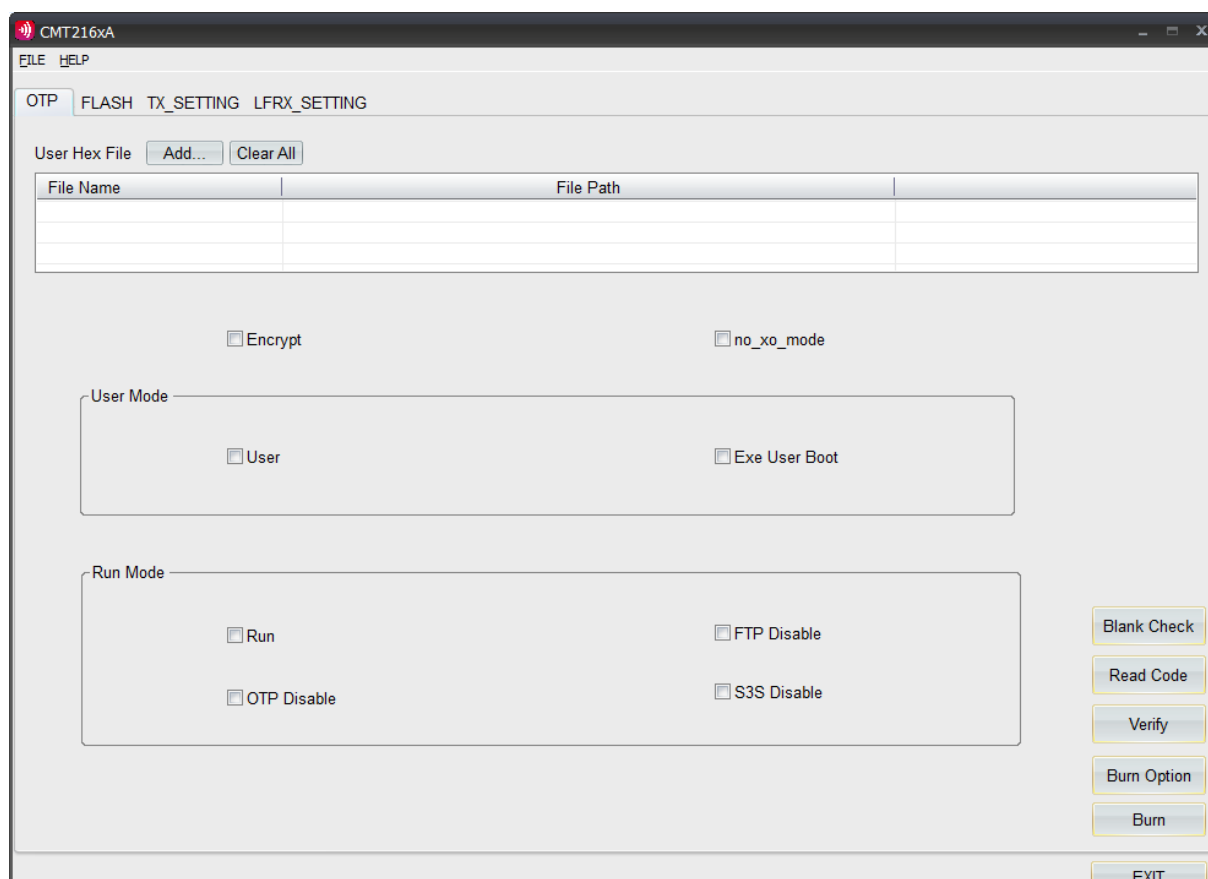


Figure 9. OTP Configuration GUI Button Description

Table 5. OTP Configuration GUI Button Description

No.	Button Name	Function
1	Add	Load user program.
2	Clear All	Clear loaded user program
3	Burn	Program the loaded user program to chip.
4	Exit	Exit RFPDK software.
5	Blank Check	<p>Check whether the chip is empty.</p> <ul style="list-style-type: none"> ● If the chip is empty, it indicates chip being empty. ● If the chip is not empty and S3S bus is not disabled, it indicates the chip not being empty and being readable. ● If the chip losses connection, it indicates connection problem or S3S bus being disabled.
6	Read Code	<p>The function to read chip program. Users can read out the program burnt into OTP if S3S bus is not disabled. When this button is pressed and the program is read out, the content will be displayed in a new window, and the content can be saved as a text file.</p> <ul style="list-style-type: none"> ● If the program on OTP is not encrypted, the content can be read directly.

		<ul style="list-style-type: none">● If the program on OTP is encrypted, the read out content will be decrypted using UUID, then the plane content after decryption will be displayed.
7	Verify	Check whether the burning is correct.
8	Burn Option	Select to burn only configuration to the chip but not program. For example, the chip operates in User mode currently and S3S bus is not disabled. By using this function, it can switch to operate in Run mode without re-burning program.

Table 6. OTP Configuration Data Field Description

No.	Configuration Item	Function Description
1	Encrypt	OTP encryption enabling. If it is checked, the user code is encrypted first before it is programmed to the chip. Refer to <i>AN290 CMT216xA User Guide</i> for more details.
2	No_xo_mode	The operating mode with the external crystal (26 MHz) absent. As the external crystal (26 MHz) is disabled, high-frequency transmission function is not supported consequently. This parameter is customized for specific customers who do not require high-frequency transmission thus the external 26 MHz crystal is not needed. If without the external 26 MHz crystal, high-frequency transmission and other associated functionalities will be affected, thus it is not suggested for users to apply this mode. If it is required, please contact CMOSTEK technical supporting.
3	User	User Mode Option. If it is checked, the chip will be programmed as <i>user Mode</i> . Refer to <i>AN290 CMT216xA user guide for the details of user more</i> .
4	Ext User Boot	The option for whether to run user code in user mode. If it is checked, the user code will run automatically. Otherwise, if it is unchecked, the user code will be loaded into PRAM, however not run.
5	Run	Run mode option. If it is checked, the chip will be programmed as run mode (product mode). Refer to <i>AN290 CMT216xA user guide for the details of run more</i> .
6	FTP Disable	FTP protection enabling. If <i>FTP Disable</i> and <i>OTP Disable</i> are checked when the chip is configured to be programmed as run mode, the protection mechanism is still available in re-test mode, namely FTP access is unpermitted. Refer to <i>AN290 CMT216xA user guide for the details of the protection mechanism and re-test more</i> .
7	OTP Disable	FTP protection enabling. If <i>FTP Disable</i> and <i>OTP Disable</i> are checked when the chip is configured to be programmed as run mode, the protection mechanism is still available in re-test mode, namely OTP access is unpermitted. Refer to <i>AN290 CMT216xA user guide for the details of the protection mechanism and re-test more</i> .
8	S3S Disable	S3S bus enabling. In run mode, if <i>S3S Disable</i> is checked, S3S programming bus and 1-wire are invalid and the chip is encrypted in this case, it cannot enter the re-test mode; otherwise if <i>S3S Disable</i> is unchecked, S3S and 1-wire can be started in a special way, the chip enters re-test mode in this case. Refer to <i>AN290 CMT216xA user guide for the details of re-test more</i> .

6.3 Flash Configuration

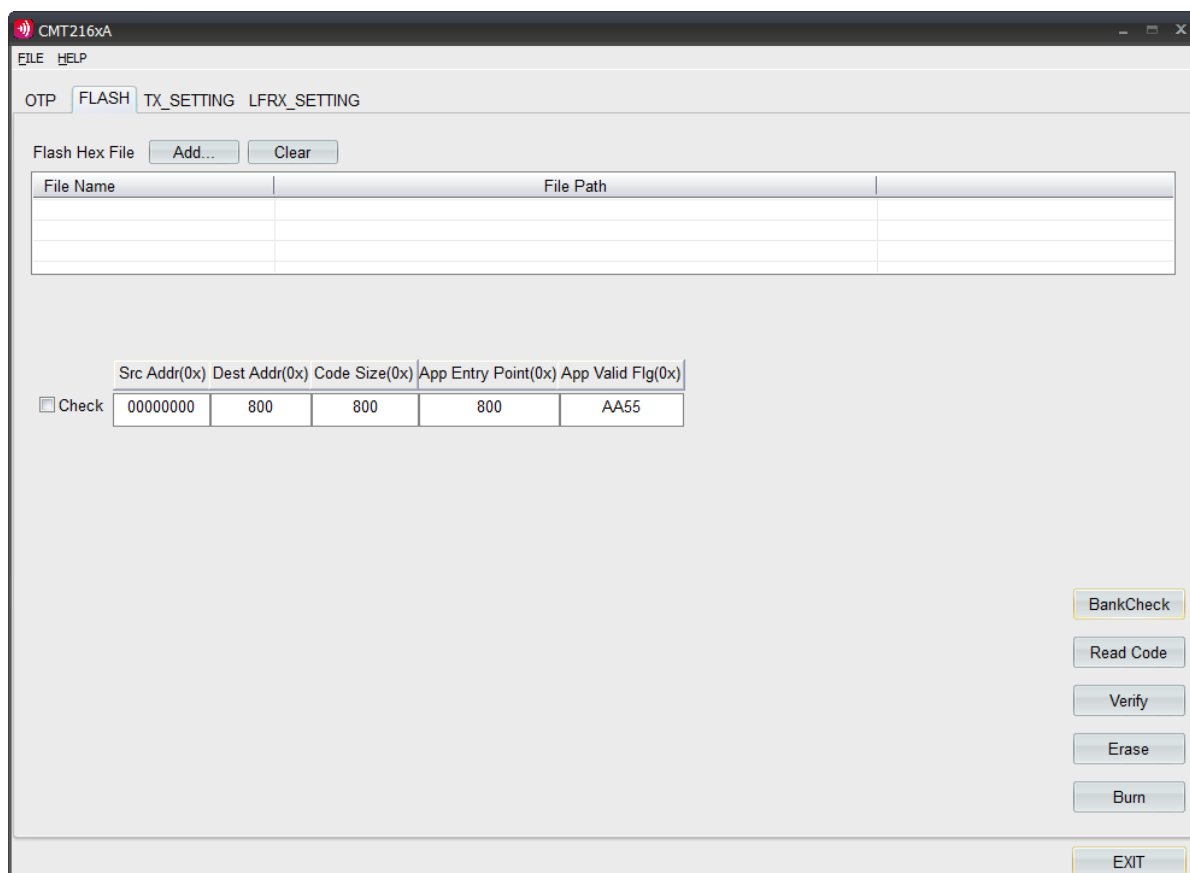


Figure 10. Flash Configuration GUI

Table 7. Flash Configuration GUI Button Description

No.	Button Name	Function
1	Add	Load Flash HEX file.
2	Clear	Clear the loaded Flash HEX file.
3	Burn	Program the loaded HEX file to the Flash.
4	Erase	Erase the HEX from the Flash.
5	Exit	Exit RFPDK software.
6	Blank Check	Check whether the chip is empty.
7	Read Code	The function to read chip program. When this button is pressed and the program is read out, the content will be displayed in a new window, and the content can be saved as a text file.
8	Verify	Check whether the burning is correct.

Table 8. Flash Configuration Data Field Description

No.	Configuration Item	Range	Default	Function Description
1	Check	Check / Uncheck	Uncheck	Whether or not program the configured address information on the right side into Flash. Check: the configured address parameters on the right side will be added into the Hex file and will be programmed into Flash. Uncheck: the configured address parameters on the right side will not be used, it will program only the content in the Hex file into Flash.
2	Src Addr		0000000C	The start address in Flash where the user code is stored.
3	Dest Addr		800	The start address in PRAM which the user code is copied to.
4	Code Size		800	The length of copied user code.
5	App Entry Point		800	The user program entry address that is skipped to after the Bootloader completes.
6	App Valid Flg		AA55	The flag that confirms the content in the information area is valid.

6.4 Tx Configuration

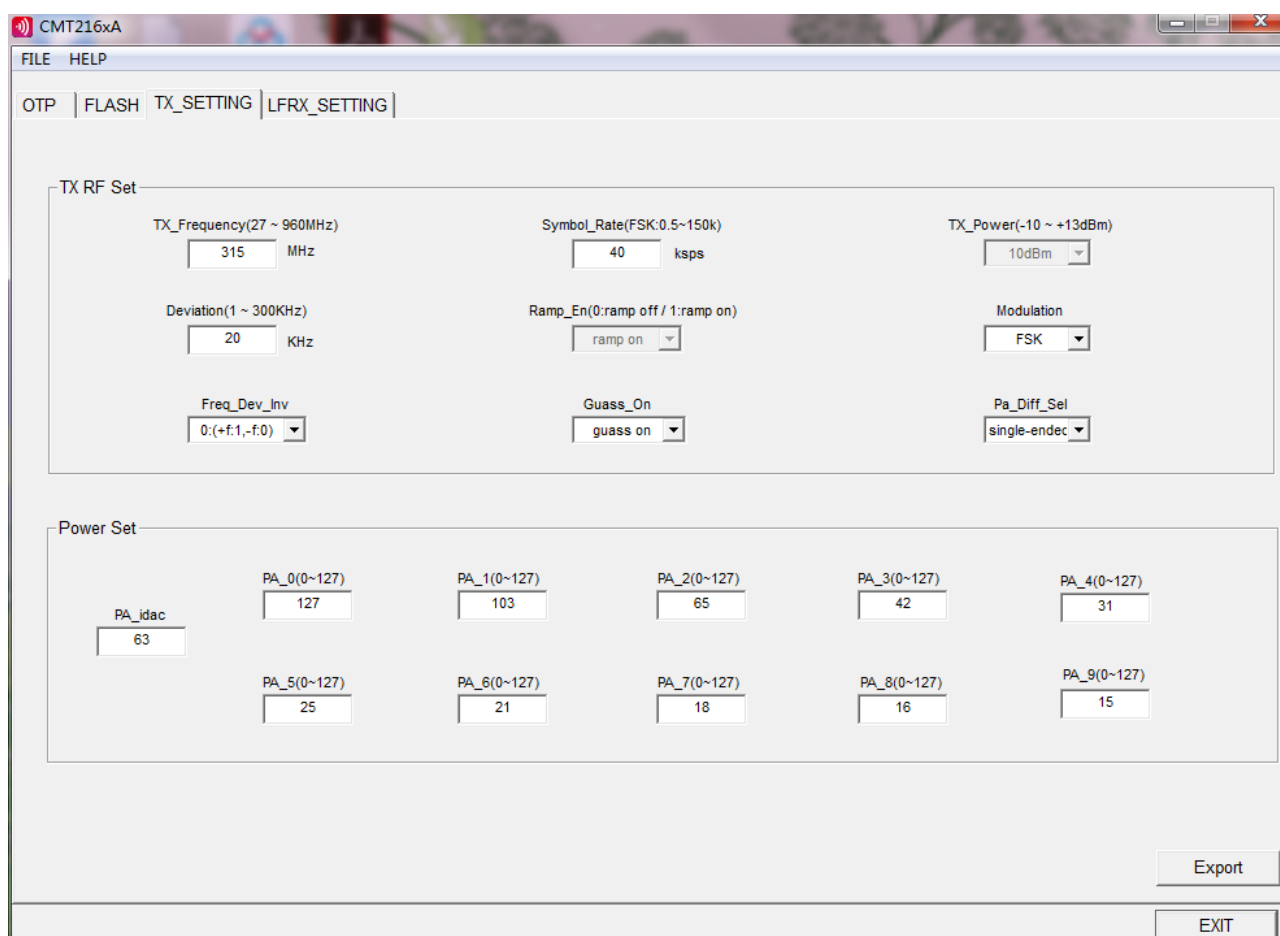


Figure 11. Tx Configuration GUI

Table 9. Tx Configuration GUI Button Description

No.	Button Name	Function
1	Export	Export Tx configuration file used for user application developing.
2	Exit	Export RFPDK software.

6.4.1 Tx RF Set Configuration

Figure 12. Tx RF Set Configuration GUI

Table 10. Tx RF Set Configuration Data Field Description

No.	Configuration Item	Range	Default	Function Description
1	Tx_Frequency	27 - 960 MHz	315	Tx frequency configuration.
2	Symbol_Rate	FSK: 0.5 - 150 kbps OOK: 0.5 - 40 kbps	40	Symbol rate configuration.
3	TX_Power	-10 ~ +13 dBm	10 dBm	Tx power configuration. This parameter is set with a fixed value, the specific Tx power configurations are provided in Section 6.3.2.
4	Deviation	1 - 200 kHz	20	Tx frequency deviation configuration.
5	Ramp_En	0: ramp off 1: ramp on	ramp on	Ramp function enabling.
6	Modulation		FSK	Modulation mode
7	Freq_Dev_inv	0: +f:1, -f:0, 1: +f:0, -f:1	0: (+f:1, -f:0)	FSK mode data modulation polarity option: 0: +F _{DEV} is 1, -F _{DEV} is 0; (F _{DEV} is Tx frequency deviation) 1, +F _{DEV} is 0, -F _{DEV} is 1.
8	Guass_On	Guass_off, Guass_on	Guass_on	FSK data GUASS filtering enabling.
9	Pa_Diff_Sel	Single-ended, Differential		PA operating mode selection; Single-ended, Single-ended PA output. Differential, differential PA output.

6.4.2 Power Set Configuration

Power Set

PA_idac 63	PA_0(0~127) 127	PA_1(0~127) 103	PA_2(0~127) 65	PA_3(0~127) 42	PA_4(0~127) 31
	PA_5(0~127) 25	PA_6(0~127) 21	PA_7(0~127) 18	PA_8(0~127) 16	PA_9(0~127) 15

Figure 13. Power Set Configuration GUI

Table 11. Power Set Configuration Data Field Description

No.	Configuration Item	Range	Default	Function Description
1	PA_idac	0 - 127	63	Tx power IDAC configuration. For instance, for Tx power of 10 dBm, the recommended value is 20.
2	PA_0(0~127)	0 - 127	127	Tx power configuration value for a voltage of 1.8 V.
3	PA_1(0~127)	0 - 127	103	Tx power configuration value for a voltage of 2.0 V.
4	PA_2(0~127)	0 - 127	65	Tx power configuration value for a voltage of 2.2 V.
5	PA_3(0~127)	0 - 127	42	Tx power configuration value for a voltage of 2.4 V.
6	PA_4(0~127)	0 - 127	31	Tx power configuration value for a voltage of 2.6 V.
7	PA_5(0~127)	0 - 127	25	Tx power configuration value for a voltage of 2.8 V.
8	PA_6(0~127)	0 - 127	21	Tx power configuration value for a voltage of 3.0 V.
9	PA_7(0~127)	0 - 127	18	Tx power configuration value for a voltage of 3.2 V.
10	PA_8(0~127)	0 - 127	16	Tx power configuration value for a voltage of 3.4 V.
11	PA_9(0~127)	0 - 127	15	Tx power configuration value for a voltage of 3.6 V.

6.5 LFRx Configuration

CMT216xA

FILE HELP

OTP FLASH TX_SETTING **LFRX_SETTING**

Analog

LFRX: On
 LFCLK: 32 kHz LFOSC
 AGC: On
 MAX Gain: Max
 De-Quality: 27Kohm
 Frequency(20~250): 125 kHz
 Symbol Rate(1~8): 4 kbps
 Power Consumption(0~9): 7
 L(0~1000): 7.2 mH
 Q(0~1000): 26
 TX Freq Accuracy(0~50): 5 %
 Demod_TH Stable Time(4~32): 8 sym

Packet Signal OK Detect System Control GPIO Output

Packet

Sync Size: 2Byte
 Sync Value(0~0xFFFFFFFF): 0x1234
 Wkid: On
 Wkid Size: 2Byte
 Wkid Value(0~0xFFFFFFFF): 0xabcd
 Data Size(1~256): 3 Byte
 Manchester Type: '10' is one
 Wkid Manchester: On
 Data Manchester: On
 Data Buffer: On
 Data Buffer Size: 2-byte

Output Result

T_Sleep_mS: mS
 T_settle_mS: mS
 T1_RX_mS: mS
 T2_RX_mS: mS
 BW_KHz: kHz
 BW_KHz_advice: kHz
 T_sync_mS: mS
 T_wkid_mS: mS
 T_data_mS: mS
 T_dbuf_mS: mS
 T_carrier_for_cadet_mS: mS
 T_carrier_for_RX_mS: mS
 T_preamble_for_snrdet_mS: mS
 T_preamble_for_RX_mS: mS
 signal_ok_autoclr_time: mS

Run Export C Export exp EXIT

Figure 14. LFRx Configuration GUI

Table 12. LFRx Configuration Data Field Description

No.	Button Name	Function
1	Export C	Export LFRx configuration file with .C format used for user application developing.
1	Export exp	Export LFRx configuration file with .exp format used for user application developing.
2	Exit	Exit RFPDK software.

6.5.1 Analog Configuration

The screenshot shows the 'Analog' configuration window with the following settings:

- LFRX:** On (dropdown)
- LFCLK:** 32kHz (dropdown)
- AGC:** On (dropdown)
- MAX Gain:** Max (dropdown)
- De-Quality:** 9.5Kohm (dropdown)
- Frequency(20~250):** 125 kHz (text input)
- Symbol Rate(1~8):** 4 kbps (text input)
- Power Consumption(0~9):** 7 (text input)
- L(0~1000):** 7.2 mH (text input)
- Q(0~1000):** 26 (text input)
- TX Freq Accuracy(0~50):** 5 % (text input)
- Demod_TH Stable Time(4~32):** 8 sym (text input)

Figure 15. Analog Configuration GUI

Table 13. Analog Configuration Data Field Description

No.	Configuration Item	Range	Default	Function Description
1	LFRX	Off/On	On	Rx enabling.
2	LFCLK	32 kHz, 32.768 kHz	32 kHz	Rx clock frequency option.
3	AGC	Off/On	On	Automatic gain control enabling.
4	Max Gain	Max, Max-3, Max-6, Max-9, Max-42 dB	Max	Max gain configuration.
5	De-Quality	1.2 -2000 kΩ	27 KΩ	Receiving antenna Q-reducing resistance value selection.
6	Frequency	20 ~ 250 kHz	125	Receiving frequency.
7	Symbol Rate	1 - 8 kbps	4	Receiving symbol rate.
8	Power Consumption	0 - 9	7	Receiving power consumption configuration.
9	L	0 - 1000 mH	7.2	Antenna inductance value configuration.
10	Q	0- 1000	26	Antenna inductor Q-value configuration.
11	Tx Freq Accuracy	0 - 50 %	5%	Tx frequency precision.
12	Demod_TH Stable Time	4 - 32 sym	8 sym	Demodulation threshold stabilization time configuration.

6.5.2 Packet Configuration

Packet

Sync Size 2Byte	Sync Value(0~0xFFFFFFFF) 12345678	Wkid On	Wkid Size 2Byte	Wkid Value(0~0xFFFFFFFF) abcdcda	Data Size(1~256) 3 Byte
Manchester Type '10' is one	Wkid Manchester On	Data Manchester On	Data Buffer On	Data Buffer Size 2-byte	

Figure 16. Packet Configuration GUI

Table 14. Packet Configuration Data Field Description

No.	Configuration Item	Range	Default	Function Description
1	Sync Size	1 - 4 Byte	3 Byte	Sync length.
2	Sync Value	0 - 0xFFFFFFFF	0x1234	Sync value.
3	Wkid	Off / On	On	Wkid enabling.
4	Wkid Size	1 - 4 Byte	1 Byte	Wakeup ID length.
5	Wkid Value	0 ~ 0xFFFFFFFF	0xabcd	Wkid value.
6	Data Size	1 ~ 256 Byte	2	Raw data length after decoding.
7	Manchester Type	"01" is one "10" is one	"10" is one	Manchester encoding type: <i>01 represents 1 in Manchester encoding.</i> <i>10 represents 1 in encoding.</i>
8	Wkid Manchester	Off / On	On	Disable/enable Manchester encoding of Wakup ID.
9	Data Manchester	Off / On	On	Disable/enable Manchester encoding of Data.
10	Data Buffer	Off / On	On	Disable/enable Data buffer.
11	Data Buffer Size	0.5 Byte 1.0 Byte 1.5 Byte 2.0 Byte 4.0 Byte	2 Byte	Data buffer length. The buffer time is calculated through decoding data rate, which is shown as the auto-calculated parameter T_dbuf_mS on RFPDK screen.

6.5.3 Signal_OK Detect Configuration

The figure shows a GUI for Signal_OK Detect Configuration. It includes the following fields and their current values:

- Signal_OK Detect Type:** Carrier Detect (dropdown)
- Signal_OK Auto Clr:** On (dropdown)
- Signal OK Clr Time(0~255):** 15 (text input)
- Signal_OK Auto Clr Type:** Disable after lfrx_wakeu (dropdown)
- Carrier Detect Window:** 906.25uS (dropdown)
- Carrier Detect Margin(0~100):** 10 % (text input)
- SNR Detect Value:** 6dB (dropdown)
- SNR Detect Valid Window:** 2pulse (dropdown)

Figure 17. Signal_OK_Detect Configuration GUI

Table 15. Signal_OK_Detect Configuration Data Field Description

No.	Configuration Item	Range	Default	Function Description
1	Signal_OK Detect Type	Carrier Detect, SNR Detect	Carrier Detect	Valid signal detection type: carrier detection, SNR detection.
2	Signal_OK Auto Clr	On/Off	On	Signal_OK signal auto-clearing enabling.
3	Signal_OK Clr Time	0 ~ 255	30	Signal_OK signal auto-clearing time: When 32KHz RC OSC is selected, Max = 1020 ms with 4 ms/step. When external 32.768KHz LFXO is selected, Max = 996 ms with 3.9 ms/step.
4	Signal_OK Auto Clr Type	Enable all the time, Disable after lfrx_wakup = 1	Disable after lfrx_wakup = 1	Signal_OK signal auto-clearing type selection: 1. Enable all the time. Once it meets Signal_OK Auto Clear Time window, auto-clearing will be performed and it will skip back to the Listen state from the Decode state. 2. Disable after lfrx_wakup = 1. If MCU is woken up, switch off the auto-clearing of Signal_OK immediately and then let the MCU send the manual clearing signal lfrx_manu_clr = 1 at an appropriate time. Otherwise if the MCU is not woken up, enable the auto-clearing function always.
5	Carrier Detect Window	When LFCLK is selected as 32 kHz, the window range is 156.25 - 7906.25 us. When LFCLK is selected as 32.768 kHz, the window range is 156.59 - 7720.95 us.	32 kHz: 906.25 μs 32.768 kHz: 885.01 us	Carrier detection window length configuration.
6	Carrier Detect Margin	0 ~ 100%	10%	Carrier detect margin
7	SNR Detect Value	3 ~ 18 dB	6 dB	SNR detect value
8	SNR Detect Valid Window	1 ~ 8 pulse	2 pulse	The required valid SNR pulse number to determine a valid LFRX_SIGNAL_OK.

6.5.4 System Control Configuration

Figure 18. System Control Configuration GUI

Table 16. System Control Configuration Data Field

No.	Configuration Item	Range	Default	Function Description
1	Antenna Mode	X-only, Scan X+Y, Scan X+Y+Z	Scan X+Y	Antenna mode configuration: X-only, X-axis single antenna mode. Scan X+Y, scanning X-axis and Y-axis antenna mode. Scan X+Y+Z, scanning X-axis, Y-axis, Z-axis antenna mode.
2	MCU Wakeup Mode	signal_ok, sync_pass, wkid_pass	wkid_pass	MCU wakeup mode selection. Wake up the MCU when LFRX_SIGNAL_OK is 1. Wake up the MCU when LFRX_SYNC_PASS is 1. Wake up the MCU when LFRX_WKID_PASS is 1.
3	RX Mode	Listen+Decode, Only Decode	Listen+Decode,	Receiving mode selection. Listen + Decode, apply both the Listen and Decode states during receiving. Only Decode, apply only the Decode state during receiving.
4	RX Duty-Cycle	Off On	On	Duty Cycle receiving mode enabling: Off, Always Rx. On, Duty Cycle Rx.
5	RX Duty-Cycle Method	T1 Extend, T1 T2 Extend	T1 T2 Extend	Duty Cycle method selection. T1 Extend: Rx waits for LFRX_WAKEUP ==1 during T1 time window. If it's satisfied, Rx hands over control to the MCU. Otherwise if it is unsatisfied, it skips to the SLEEP state when T1 ends. T1 T2 Extend: Rx waits for LFRX_SIGNAL_OK==1 during T1 time window. If it is satisfied, extend Rx to T2 time window, and continue to wait for LFRX_WAKEUP ==1 , then if it is satisfied, Rx hands over control to the MCU. If either of above condition is unsatisfied, it skips to the

No.	Configuration Item	Range	Default	Function Description
				SLEEP state when T1 or T2 time window ends.
6	Sleep Time	0~32640 mS	0	LFRX Sleep time configured by users.
7	RX T1 Time	0~3968 mS	0	RX T1 time configured by users.
8	RX T2 Time	0~3968 mS	0	RX T2 time configured by users.

6.5.5 GPIO Output Configuration

The screenshot shows the 'GPIO Output' configuration window. It contains five dropdown menus arranged horizontally:

- MCU Selection:** Inter MCU
- Data_Out_Type:** decode data
- Man Err Flag:** Off
- External_Clear:** Off
- PAD_Output_Sel:** Disable PAD Output

Figure 19. GPIO Output Configuration GUI

Table 17. GPIO Output Configuration Data Field Description

No.	Configuration Item	Range	Default	Function Description
1	MCU Selection	Internal MCU External MCU_1 External MCU_2	Inter MCU	RX MCU wakeup mode selection: Inter MCU, LFRX_WAKEUP is used only for waking up the internal MCU. Exter HP_CLK, LFRX_WAKEUP is used only for the external MCU (configured to map to specified GPIO), and the internal MCU can be used for other functions. Exter No HP_CLK, LFRX_WAKEUP is used only for wake up the external MCU, and the internal MCU is not used.
2	Data_Out_Type	Raw data Cdr data Decode data	Decode data	Output data type: Raw data, modulated data. Cdr data, data after clock synchronization. Decode data: data after decoding.
3	Man Err Flag	Off / On	Off	Disable/enable outputting Manchester code error flag bit to PAD.
4	External Clear	Off / On	Off	Disable/enable external clearing function of LFRX_SIGNAL_OK by inputting positive pulse with the width greater than 100 us.
5	PAD Output Sel	Disable PADOutput, Group 1, Group 2	Disable PADOutput	Data output port selection: Group 1: A4 (Input):External Clear

				A5(Output): LFRX_WAKEUP A6(Output): Data A7(Output): Dclk B5(Output): LFRX_MAN_ERR_FLAG Group 2: A4 (Input): External Clear A1(Output): LFRX_WAKEUP A2(Output): Data A3(Output): Dclk B6(Output): LFRX_MAN_ERR_FLAG
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6.5.6 Output Result Auto-calculation

Figure 20. Output Result GUI

Table 18. Output Result Data Field Description

No.	Configuration Item	Function Description
1	T_sleep_mS	The actual LFRX Sleep time auto-calculated by RFPDK.
2	T_settle_mS	The actual LFRX Sleep time auto-calculated by RFPDK.
3	T1_RX_mS	The actual T1_RX time auto-calculated by RFPDK.
4	T2_RX_mS	The actual T2_RX time auto-calculated by RFPDK.
5	BW_KHz	The current antenna bandwidth auto-calculated by RFPDK.
6	BW_KHz_advice	The recommended antenna bandwidth auto-calculated by RFPDK.
7	T_sync_mS	The sync time auto-calculated by RFPDK.
8	T_wkid_mS	The wkid time auto-calculated by RFPDK.
9	T_data_mS	The data time auto-calculated by RFPDK.
10	T_dbuf_mS	The data buffer time auto-calculated by RFPDK.
11	T_carrier_for_cadet_mS	The maximum carrier length required for carrier frequency detection, which is auto-calculated by RFPDK.

12	T_carrier_for_RX_mS	The maximum carrier length required for always-Rx including the time required for antenna scanning and AGC, which is auto-calculated by RFPDK.
13	T_preamble_for_snrdet_mS	The maximum preamble length required for SNR detection, which is auto-calculated by RFPDK.
14	T_preamble_for_RX_mS	The maximum preamble length required for always-Rx including the time required for antenna scanning and AGC, which is auto-calculated by RFPDK.
15	Signal_ok_autoclr_time	lfrx_signal_ok timeout time. When Signal_OK auto-clearing function is enabled, if it exceeds this time, LFRX_SIGNAL_OK will be cleared automatically.

7. Firmware Upgrading and Downgrading

Users can perform the CMT216xA programmer firmware upgrading or downgrading on CMT216xA RFPDK GUI. Through firmware upgrading, the CMT216xA programmer firmware will be upgraded to the version matched with the latest published CMT216xA RFPDK version. Through firmware downgrading, users can choose to downgrade the CMT216xA programmer firmware back to an appropriate workable lower version.

Before performing upgrading or downgrading, make sure the CMT216xA programmer is well connected with PC via USB cable and the CMT216xA RFPDK software GUI is opened.

7.1 Firmware Upgrading

Upon CMT216xA RFPDK startup, the CMT216xA programmer firmware is checked. If the current firmware version is lower than the CMT216xA RFPDK version, a window will pop up information to notify users of whether to upgrade CMT216xA programmer firmware. Users can click **OK** to perform CMT216xA programmer firmware upgrading as shown in the figure below.

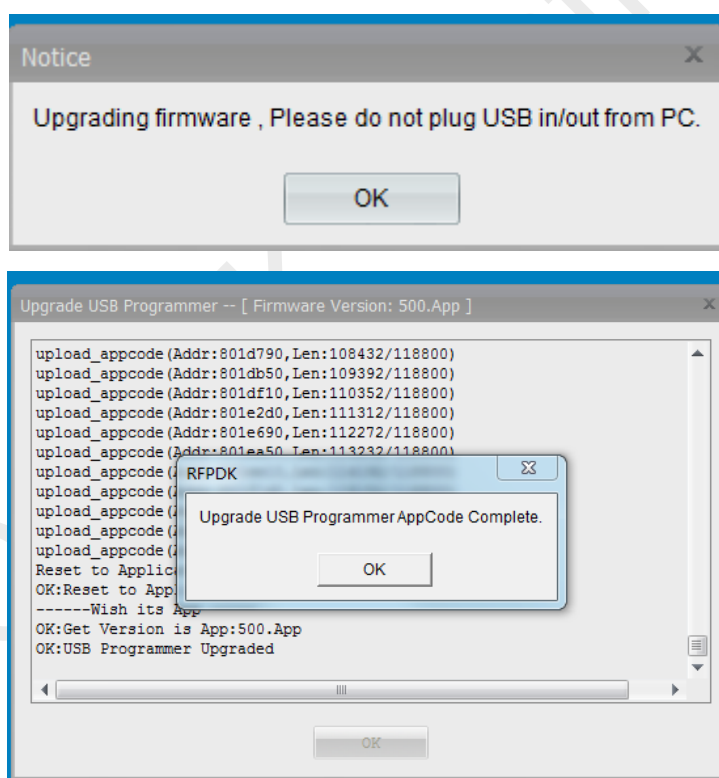


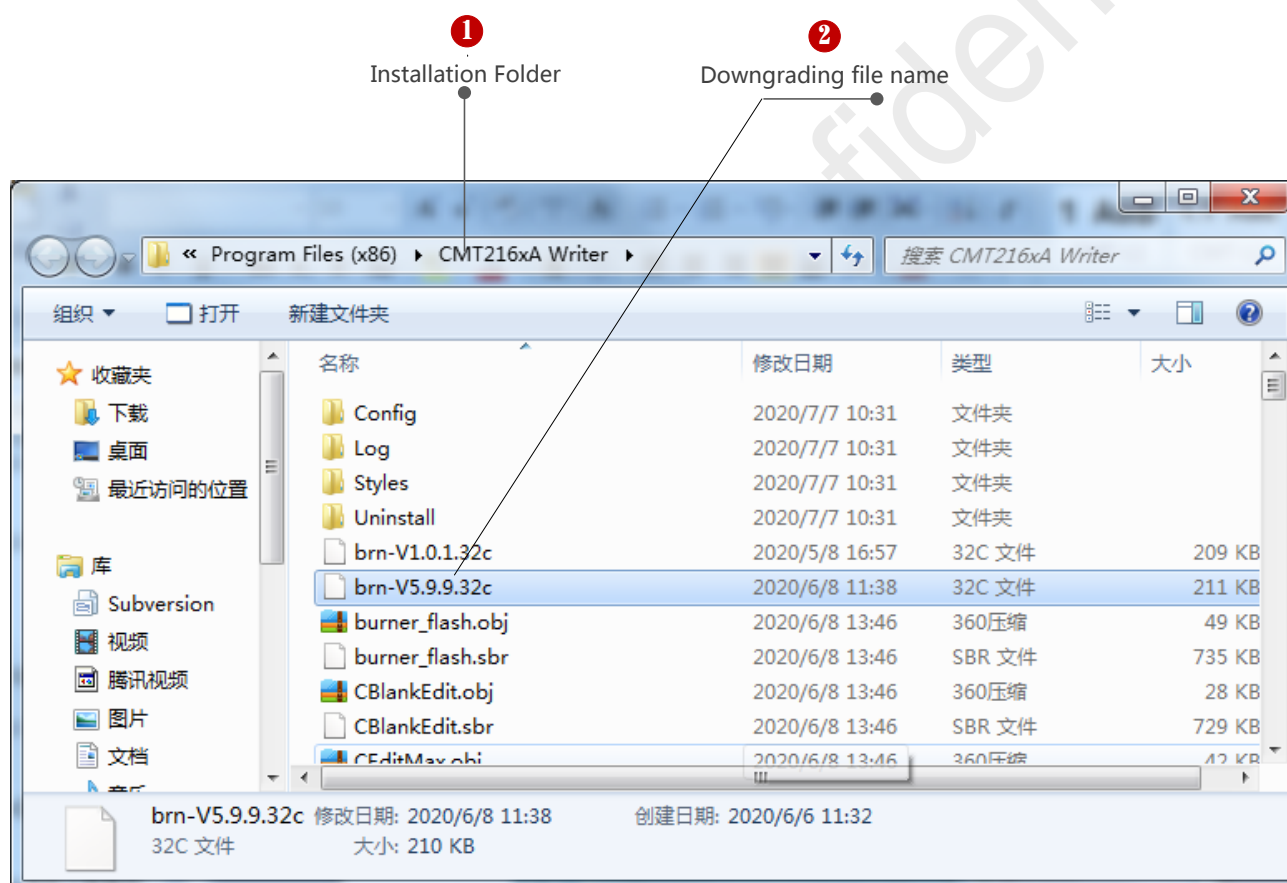
Figure 21. Upgrade CMT216xA Programmer Firmware on CMT216xA RFPDK GUI

7.2 Firmware Downgrading

Before downgrading, users need rename the target firmware file (in the CMT216xA RFPDK installation folder, file name format is brn-Vx.y.z.32c) to brn-V5.9.9.32c. After then, restart CMT216xA RFPDK software, a notification window will pop up with the same information as that in firmware upgrading. Users can click OK to perform CMT216xA programmer firmware downgrading as shown in the figure below.

For the firmware file name format brn-Vx.y.z.32c, x.y.z represents firmware version. For example, for brn-V1.5.1.32c, the firmware version is V1.5.1.

After downgrading, rename the file name brn-V5.9.9.32c back to the original file name to avoid downgrading repeatedly.



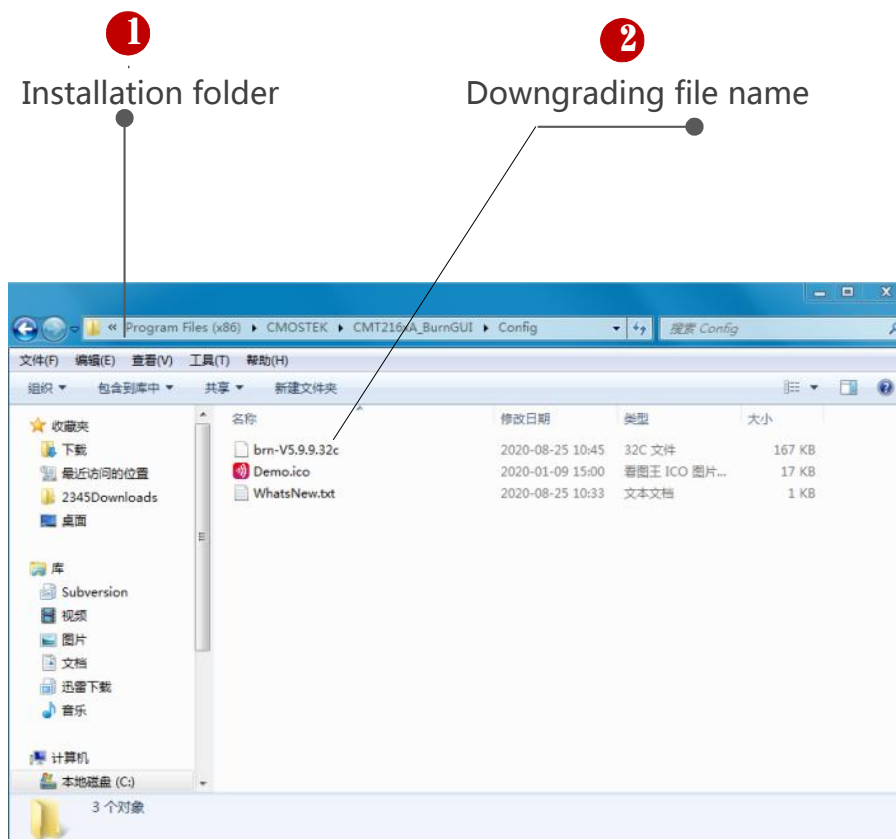


Figure 22. Downgrading CMT216xA Programmer Firmware

7.3 Handling of False Upgrading Across Different RFPDK Types

COMSTEK provides multiple types of RFPDK software and programmer hardware. These different types of RFPDK and programmer have different PC-side software name, firmware name, version number range and target downgrading file name as shown in the table below. When multiple types of RFPDK software entries have been installed on users' PC, users need to ensure opening the correct RFPDK software on PC according to programmer type.

Table 19. Multiple RFPDK and Programmer Types

No.	Programmer Name	PC-side Software Name	PC-side Software Version Range	Target Downgrading File Name	Description
1	CMOSTEK Programmer	CMOSTEK RFPDK	V130 - V499	brn-V4.9.9.32c	Unified CMOSTEK RFPDK and programmer
2	CMT216xA Programmer	CMT216xA RFPDK	V500 - V599	brn-V5.9.9.32c	RFPDK and programmer specific for CMT216xA series chips

When multiple types of RFPDK software entries have been installed on users' PC, it may occur false upgrading across different RFPDK types. For example, a user needs to open CMOSTEK RFPDK, however CMT216xA RFPDK is opened by mistake. If it happens that the CMT216xA programmer firmware version is higher than the CMOSTEK programmer firmware version, the information will pop up indicating users to upgrade firmware. If the user clicks **OK** in this case, a false upgrading will happen, which will impact normal RFPDK operations.

When false upgrading across different RFPDK types occurs, users can follow steps below to restore the RFPDK back to the original normal state before the false upgrading.

1. Power on the correct programmer hardware through USB.
2. Close the wrong PC-side software.
3. Select the target downgrading file and change to downgrading file name. The details are as below.

Select the correct software icon on PC, right click->property->open file location, then it opens the target file folder. In the file folder, among the filenames with a format of brn-Vx.y.z.32c, select the file with the largest xyz value (namely the file with the largest version number). Rename this file name to the downgrading file name (for Unified RFPDK, the downgrading file name is brn-V4.9.9.32c; for CMT216xA RFPDK, it is brn-V5.9.9.32c. Please refer to the above Table 19 for more details).

4. Reopen the correct RFPDK software on PC, the window will pop up to indicate upgrading. Click **OK** and wait for upgrading being done. At this time, the falsely upgraded firmware has been restored to the original normal state.
5. Rename the file name in step 3 back to its original name to avoid the upgrading indication that pops up each time when the RFPDK software is opened.

8. Revision History

Table 20. Revision History Records

Version	Chapter	Description	Date
0.5	All	Initial version	2020-08-27
0.6	Overview 6.1	Modifications according to CMT216x RFPDK V5.01 function update: Overview, add supported chip list. 6.1, add connection status information	2021-05-06
0.7	4.1.1	Update IDC 10P cable schematic diagram	2021-07-27

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