CMT216xA ADC and AFE User Guide

Overview

This document discusses the function and usage of the CMT216x analog front end (AFE) to help users get a quick understanding of the chip series, then to get on with target product design and development efficiently.

The AFE module consists of the below sub-modules.

- 12-bit SAR-ADC
- High-speed and low-power operational amplifiers (HSOAs)
- Micro-power module (including micro-power operational amplifiers and micro-power LDO)
- Constant current source drive module
- LBD voltage detection module

The product models covered in this document are shown in the table below.

Table 1. Product Models Covered in This Document

Product Model	Single-end PA	Differential PA	12-Bit ADC	Operational Amplifier	Low-frequency Wakeup	External 32.768 kHz	Packaging
CMT2160A		●	4-ch				SOP14
CMT2162A	●		8-ch		●		SSOP20
CMT2163A	●	●	9-ch		●	●	TSSOP28
CMT2165A	●		12-ch	●		●	TSSOP28
CMT2168A	●		12-ch	●	●	●	QFN32

Notes:

The performance and parameter details as well as the package size, silk screen and ordering information of each chip model are NOT covered in this document, please refer to the datasheet document of each chip model for details. For specific function details of the CMT216xA series, please refer to *CMT216xA User Guide*.

Reading guidelines:

1. Suggest users read *CMT216xA User Guide* first to get familiar with basic product functions then read this document for more comprehensive understanding on the product.
2. This document has detail description of analog front end sub-modules such as ADC, HSOA and LPOA. Users utilizing these functions should read it carefully.

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1 AFE Function Description

1.1 Overview

The external analog signal needs to be converted into a digital signal for further processing by the MCU. AFE (Analog Front-End) is mainly to complete the conditioning and digitization of the analog signal. The AFE module integrates a band-gap reference, a regulator with adjustable output, an analog signal conditioning circuit, a sensor interface circuit, and a 12-bit high-speed & high-precision successive approximation analog-to-digital converter (SAR-ADC). AFE largely supports the following features and capabilities.

- 2-channel low-power operational amplifiers, HSOA1 and HSOA2
  - Built-in non-inverting amplifier with programmable gain
  - Built-in instrumentation amplifier with programmable gain
  - Built-in buffer operational amplifier HSOA0
- 12-bit high-precision SAR-ADC
  - Built-in buffered operational amplifier HSOA0, and SAR-ADC being able to convert high-impedance input signals
  - Support for SNOOZE operating mode, reducing chip sensor acquisition power effectively
  - 12 external input conversion channels (A1 ~ A7, B5 ~ B7, ASN and PSN)
  - Built-in temperature sensor (T-Cell)
  - Built-in supply battery voltage measurement
- 2-channel micro-power operational amplifiers LPOA0 and LPOA1
- 2-channel constant current source drive output
- Micro-power regulator output
- Rich sensor interfaces
  - Pressure sensor (P-Cell)
  - Acceleration sensor (A-Cell)
  - Shock sensor (S-Cell, piezoelectric type)
  - PIR sensor
  - Smoke sensor (photoelectric)

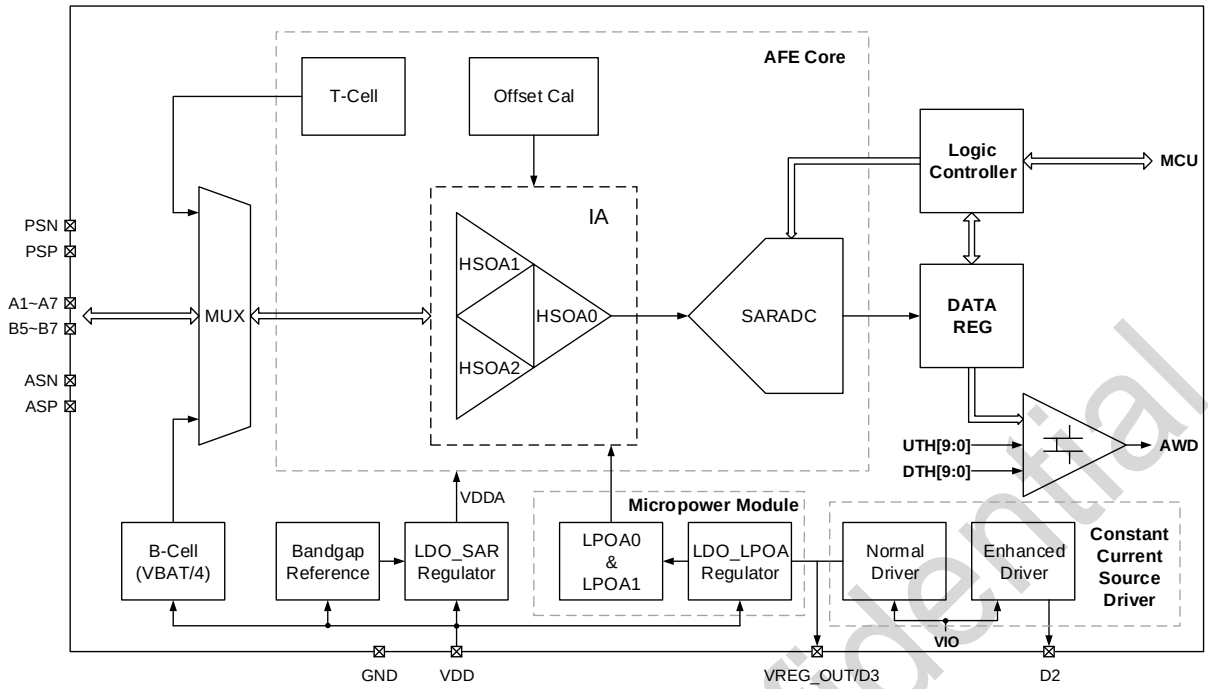

Figure 1. General AFE System Diagram

As shown in above figure, the AFE Core circuits mainly includes low-speed and high-power operation amplifiers HSOA0 / 1/2, SAR-ADC, temperature sensor (T-Cell), and calibration circuits. The LDO_SAR regulator output supplies power for the entire AFE Core module. Power supply (namely VDDA. VDDA output voltage is adjustable).

The micro-power operational amplifiers LPOA0 and LPOA1 are powered by the output VREG_OUT of the micro-power LDO_LPOA regulator. The VREG_OUT output voltage is adjustable and can be output to the VREG_OUT / D3 pin.

As for the constant current drive, it can provide ordinary type and enhanced type of constant current output. The ordinary constant current output port is multiplexed to the VREG_OUT / D3 pin, and the enhanced constant current output is output to the D2 pin.

The other circuits are powered by VDD directly.

1.2 Detailed AFE Block Diagram

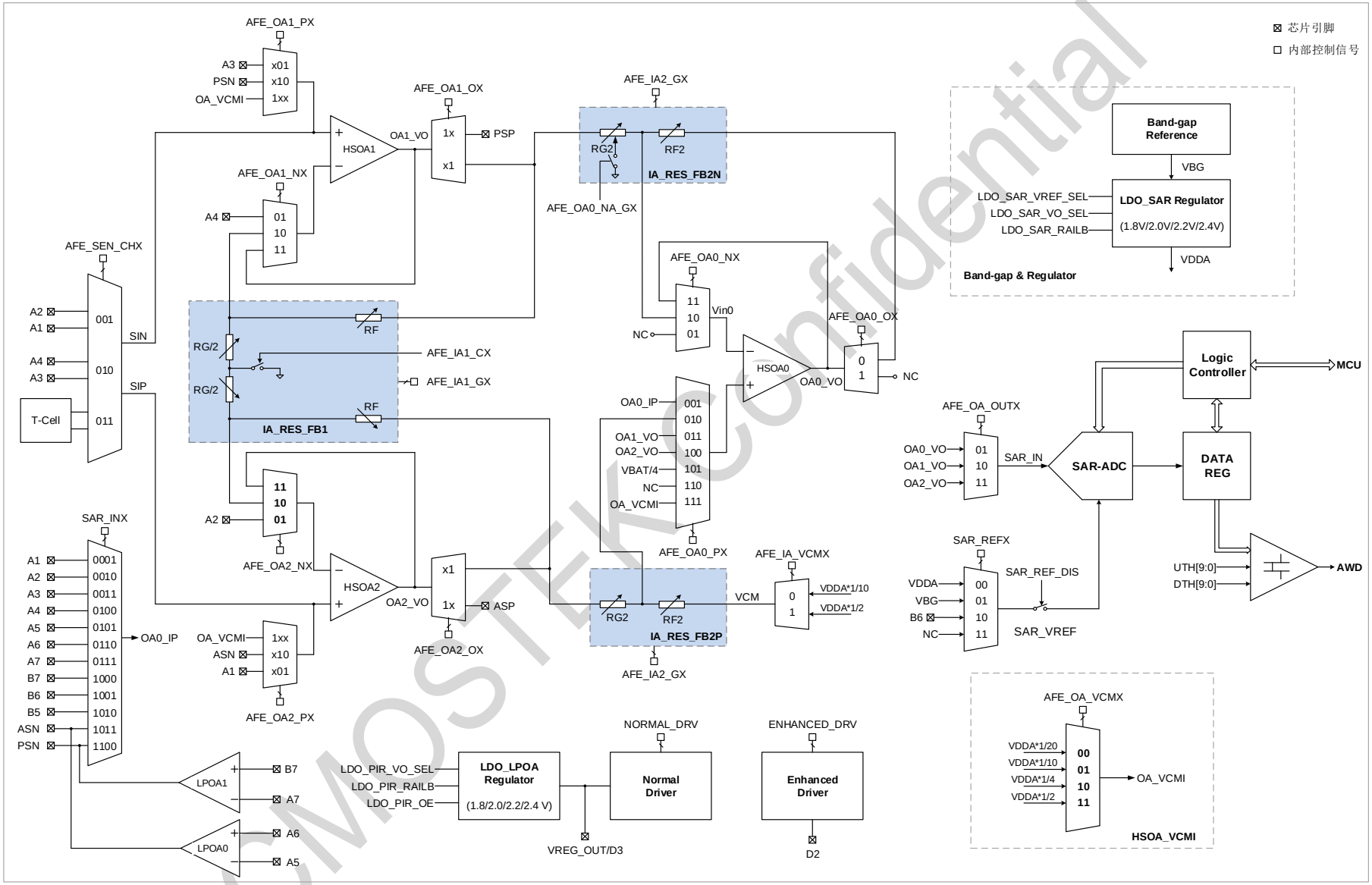

Figure 2. Detailed AFE System Block Diagram

2 Voltage Source

The CMT216xA's analog front-end system has 2 output voltage sources.

- LDO_SAR regulator, providing power supply and reference voltage for SAR-ADC and supply power as well as bias voltage for high-speed and low-power operation amplifier groups (HSOAs).
- LDO_LPOA regulator, providing power supply and bias voltage for micro-power op amps (LPOAs).

2.1 LDO_SAR Regulator

As shown in the detailed AFE block diagram in Section 1.2, in the dotted box *Band-gap & Regulator* is the LDO_SAR regulator module.

- The function of LDO_SAR regulator is to output VDDA, which provides operating voltage for SAR-ADC and HSOAs.
- LDO_SAR_RAILB setting
  - When set as 1, the output voltage of VDDA can be selected by setting LDO_SAR_VO_SEL as shown in the below table. The default output voltage is 2.2 V.
  - When set as 0, the LDO_SAR regulator is bypassed, and VDDA is the same as the chip power supply VDD at this time.

Table 2. Regulator Output Voltage Selection

LDO_SAR_VO_SEL	VDDA (V)
2'b00	1.8
2'b01	2.0
2'b10 (default)	2.2
2'b11	2.4

In above,

- LDO_SAR_RAILB is located at Bit5 of SFR register CUS_AFE15.
- LDO_SAR_VO_SEL is located at Bit7 and Bit6 of CUS_AFE15.

For CUS_AFE15, please refer to Section 8 *Special Function Registers of AFE*" or *AN286 CMT216x Register Guide* for details.

Note: In the detailed block diagram of AFE in Section 1.2, the DO-SAR_VREF_SEL in the Band-gap & Regulator block is the reference voltage selection signal of the LDO_SAR regulator module. This control signal is enabled through the API function afe_front_setup_config. See AN282 CMT216xA API Function Library User Guide for details.

2.2 LDO_LPOA Regulator

As shown in the detailed block diagram of AFE in Section 1.2, in the *LDO_LPOA Regulator* block is this module.

- The LDO_LPOA regulator function is to output the operating voltage of LPOAs, and it can be output to a pin as a specific sensor's power supply (such as PIR sensor).
- LDO_PIR_RAILB setting
  - When set as 1, the LDO_LPOA regulator output voltage VREG can be selected by setting LDO_PIR_VO_SEL as shown in the below table. The default output voltage is 2.2 V.
  - When set as 0, the LDO_LPOA regulator is bypassed, and VREG is the same as the chip power supply VDD.
- When setting LDO_PIR_OE to 1, users can configure the LDO_LPOA regulator to the VREG_OUT / D3 pin for output.

Table 3. LDO_LPOA Regulator Output Voltage Selection

LDO_PIR_VO_SEL	VREG (V)
2'b00	1.8
2'b01	2.0
2'b10 (default)	2.2
2'b11	2.4

In above,

- LDO_PIR_RAILB is located at Bit7 of SFR register CUS_AFE12.
- LDO_PIR_VO_SEL is located at Bit7 and Bit6 of SFR register CUS_AFE13.
- LDO_PIR_OE is located at Bit0 of SFR register CUS_AFE18.

For CUS_AFE12, CUS_AFE13 and CUS_AFE18, see Section 8 *Special Function Registers of AFE* or *AN286 CMT216xA Register Guide* for details.

3 High-Speed Low-Power Op Amps (HSOAs)

As shown in the below figure, the high-speed and low-power operational amplifier group includes HSOA1 as well as HSOA2 for external use, and HSOA0 for internal buffering. Through selection of different channel configurations, it can for a variety of analog signal conditioning architectures to meet different application requirements. Moreover, HSOA0 with built-in buffer can perform high impedance analog input signal conversion for SAR-ADC. In addition, each HSOA can be enabled and controlled by a digital control circuit (not shown in the figure), thus helping users on reducing power consumption.

In summary, the main features of HSOAs are as follows.

- Single power supply, with each HSOA being able to run independently, achieving low power-consumption.
- Rail-to-rail input / output.
- Supporting signal channel selection by for software.
- 2 external analog input channels.
- Built-in buffering amplifier HSOA0 driving SAR-ADC.
- Being able to form an instrumentation amplifier based on three op amps, supporting program-controlled gain.
- Being able to form three non-inverting amplifiers, supporting program-controlled gain.

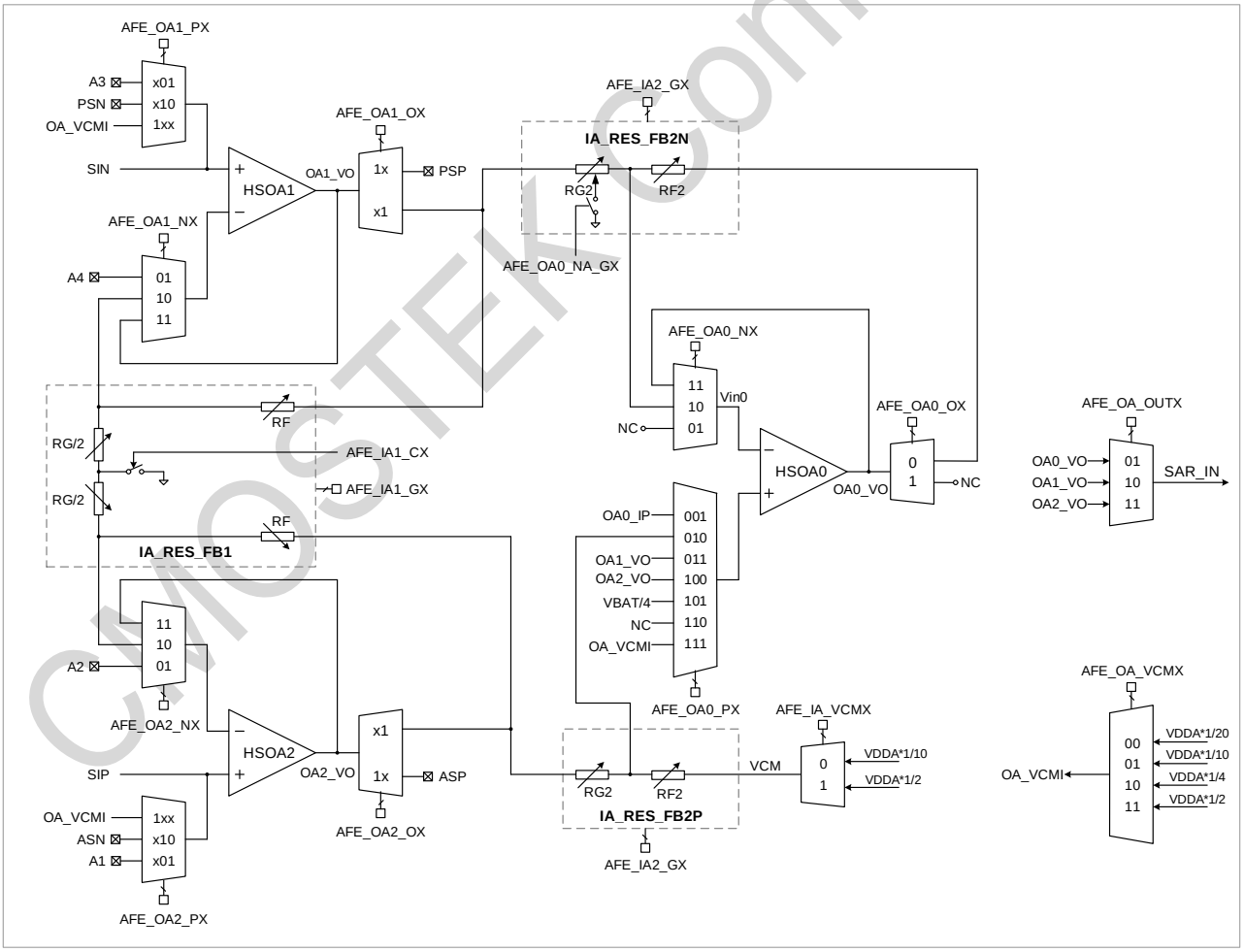

Figure 3. HSOAs Block Diagram

3.1 HSOA1 and HSOA2 as Non-inverting Amplifier

HSOA1 and HSOA2 can be configured by the software to form 2 built-in non-inverting amplifiers, as shown in the below figure. When HSOA1 and HSOA2 are used as built-in non-inverting amplifiers, the key settings are as follows.

1. AFE_IA1_CX must be set to 0, and AFE_OA1_OX or AFE_OA2_OX is set to 2'b01, so that the output of HSOA1 or HSOA2 is input to HSOA1- or HSOA2- input through IA_RES_FB1, thereby forming a non-inverting amplifier.
2. AFE_OA1_NX or AFE_OA2 _NX is selected as the negative input. It must also be configured as 2'b10 to ensure the feedback loop is connected.
3. AFE_OA0_NA_GX must be set to 2'b00, namely, is configured as an inverting amplifier.
4. AFE_OA1_PX and AFE_OA2_PX are used as the positive inputs of HSOA1 and HSOA2. The off-chip input channels can be selected.

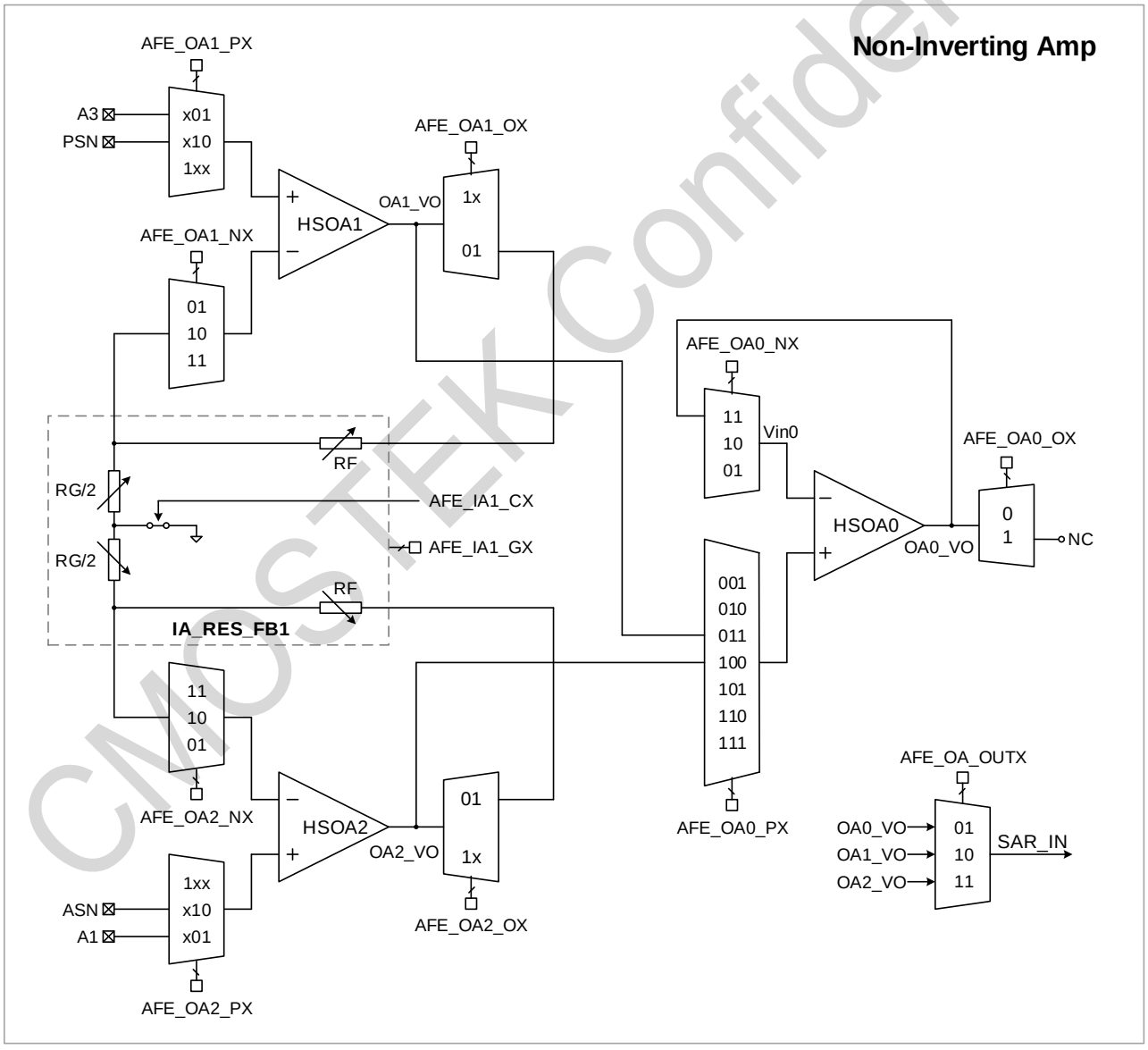

Figure 4. Block Diagram for Non-inverting Amplifier HSOA1 and HSOA2

In addition, the built-in non-inverting amplifier gain can be set by the software configuration AFE_IA1_GX, as shown in the below table.

Table 4. Non-inverting Amplifier Gain Configuration of HSOA1 and HSOA2

AFE_IA1_GX		Gain
Decimal Value	Binary Value	
0	3'b000	invalid
1	3'b001	2
2	3'b010	4
3	3'b011	8
4	3'b100	16
5	3'b101	24
6	3'b110	32
7	3'b111	48

In above,

- AFE_IA1_CX is located at Bit0 of CUS_AFE9 register.
- AFE_OA0_NA_GX is located at Bit1 and Bit0 of the CUS_AFE10 register.
- AFE_1A1_GX is located at Bit5 ～ Bit3 of CUS_AFE6 register.
- AFE_OA1_NX is located at Bit4 and Bit3 of the CUS_AFE11 register.
- AFE_OA1_PX is located at Bit2 ~ Bit0 of CUS_AFE11 register.
- AFE_OA1_OX is located at Bit6 and Bit5 of CUS_AFE11 register.
- AFE_OA2_NX is located at Bit4 and Bit3 of the CUS_AFE12 register.
- AFE_OA2_PX is located at Bit2 ～ Bit0 of CUS_AFE12 register.
- AFE_OA2_OX is located at Bit6 and Bit5 of CUS_AFE12 register.

For details on CUS_AFE6, CUS_AFE9, CUS_AFE10, CUS_AFE11, and CUS_AFE12, see Section 8 *Special Function Registers of AFE* or *AN286 CMT216xA Register Guide*.

3.2 HSOA0 as Non-inverting Amplifier

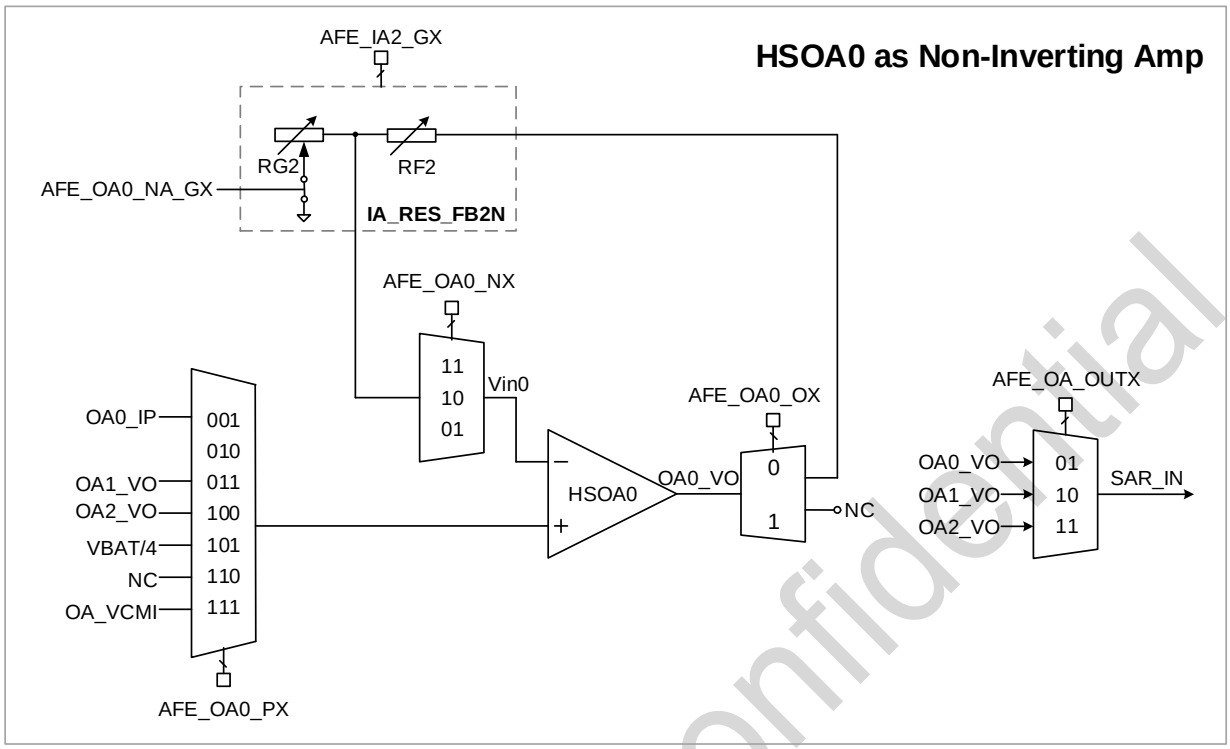

Figure 5. Block Diagram for Non-inverting Amplifier HSOA0

HSOA0 can be configured by the software to form a built-in non-inverting buffer amplifier, as shown in the above figure. When HSOA0 is used as a non-inverting amplifier, the key settings are as follows.

1. AFE_OA0_OX must be set to 0, and AFE_OA0_NX must be set to 2'b10, namely, the HSOA0 output selection channel IA_RES_FB2N is fed back to the HSOA0-input to form a gain-adjustable non-inverting amplifier.
2. By configuring AFE_OA0_NA_GX and AFE_IA2_GX, users can select different gain magnifications, as shown in the below table.
3. Users can select different in-phase input signals by configuring AFE_OA0_PX.

Note:

1. When HSOA0 is used as a non-inverting amplifier, AFE_OA0_NA_GX cannot be set to 2'b00.

Table 5. Non-inverting Amplifier Gain Configuration HSOA0

AFE_IA2_GX	AFE_OA0_NA_GX	Gain
2'b00	2'b01	2
	2'b10	4
	2'b11	7
2'b01	2'b01	2.5
	2'b10	5.5
	2'b11	10

AFE_IA2_GX	AFE_OA0_NA_GX	Gain
2'b10	2'b01	3
	2'b10	7
	2'b11	13
2'b11	2'b01	4
	2'b10	10
	2'b11	19

In above,

- AFE_OA0_OX is located at Bit7 of CUS_AFE10 register;
- AFE_OA0_NX is located at Bit6 and Bit5 of the CUS_AFE10 register;
- AFE_OA0_NA_GX is located at Bit1 and Bit0 of the CUS_AFE10 register;
- AFE_OA0_PX is located at Bit4 ~ Bit2 of CUS_AFE10 register;
- AFE_IA2_GX is located at Bit7 and Bit6 of the CUS_AFE4 register;

For details of CUS_AFE4 and CUS_AFE10, please refer to Section 9 *Special Function Registers of AFE* or *AN286 CMT216xA Register Guide*.

3.3 HSOAs as Instrumentation Amplifier

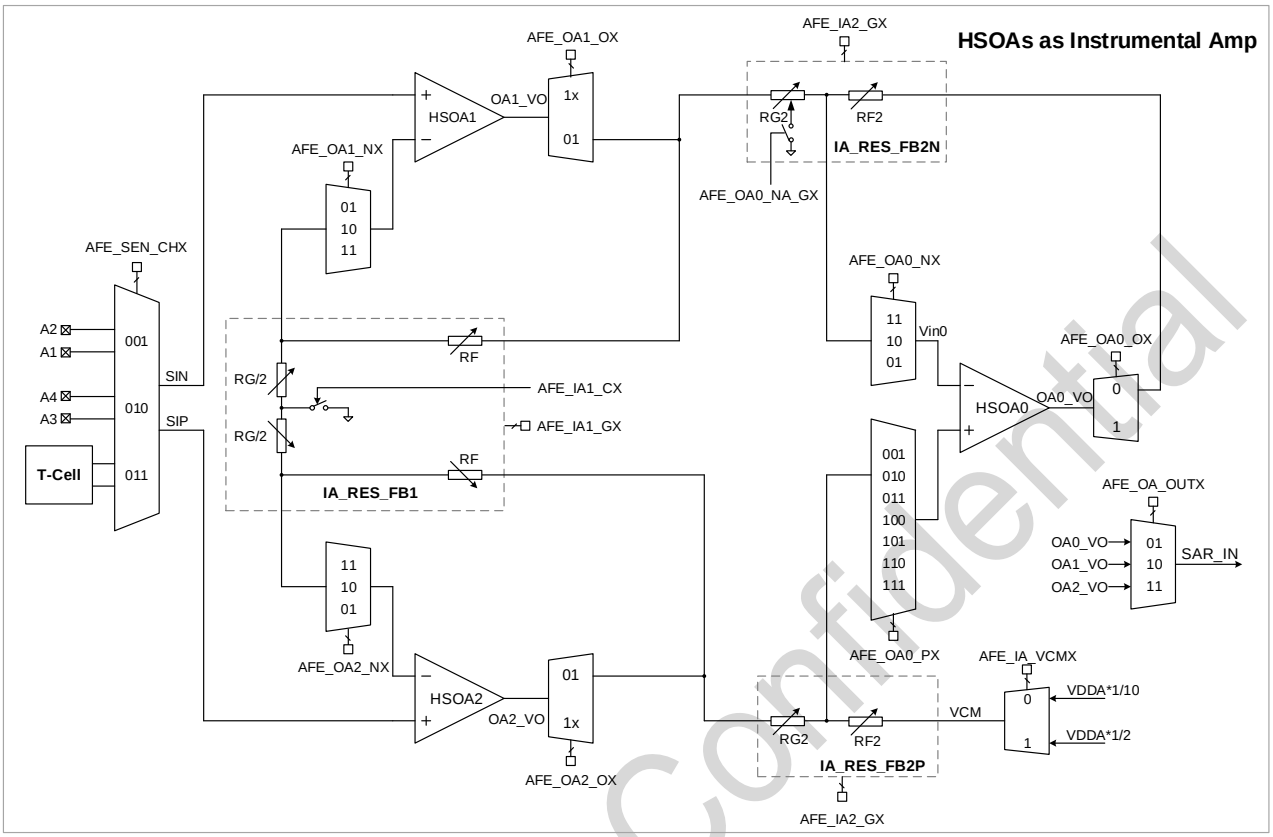

Figure 6. Block Diagram of Instrumentation Amplifier Formed by HSOAs

Through software configuration, HSOA0, HSOA1, and HSOA2 form a built-in instrumentation amplifier, as shown in above figure. The input signal path is set by the software, and the input signal of the instrumentation amplifier can be input from the resistance bridge sensor interface SIP and SIN (internal signal). Through AFE_SEN_CHX, SIP and SIN can select 2 sets of resistance bridge sensor channel interfaces:

- A group of channels are input from the A2 and A1 ports, and the sensor excitation source is provided by the ASP and ASN ports (ASP and ASN are not marked in the figure).
- Another group of channels are input from A4 and A3 ports, and the sensor excitation source is provided by the PSP and PSN ports (the PSP and PSN are not marked in the figure).

The following settings are required when HSOAs are configured for instrumentation amplifier usage.

1. AFE_IA1_CX must be set to 1, namely HSOA1 and HSOA2 as instrumentation amplifiers.

2. AFE_OA0_OX must be set to 0, and AFE_OA0_NX must be set to 2'b10, so that HSOA0 output through IA_RES_FB2N to HSOA0-input, forming a feedback loop.

3. AFE_OA0_NA_GX must be set to 2'b00, so that IA_RES_FB2N and IA_RES_FB1 build a cascade to form the instrument amplification detection loop.

4. AFE_OA0_PX must be set to 3'b010 and select HSOA0 + input to form a detection loop with IA_RES_FB2P and IA_RES_FB1.

5. AFE_OA1_NX and AFE_OA2_NX must be set to 2'b10, and AFE_OA1_OX and AFE_OA1_OX must be set to 2'b01, so that HSOA1 and HSOA2 form the input stage of the pre-stage non-inverting differential-mode instrumentation amplifier.

6. Can select one of the detection channels by configuring AFE_SEN_CHX.

An instrumentation amplifier formed by HSOAs is a 2-stage amplifier. The first stage consists of in-phase differential mode amplifiers formed by HSOA1 and HSOA2, and the second stage uses HSOA0 as the inverting amplifier. At the same time, the gain of the instrumentation amplifier includes 2 stages of gain, each of which can be controlled independently. The first stage gain is selected by the AFE_IA1_GX configuration, and the second one by the AFE_IA2_GX configuration. See the below 2 tables for details.

The output reference voltage VCM of the instrumentation amplifier is controlled by PD_AFE_IACMO. The VCM output can be selected by software setting AFE_IA_VCMX. See

Table 8 for details.

Table 6. Instrumentation Amplifier 1st Stage Gain Configuration

AFE_IA1_GX（Decimal）	AFE_IA1_GX（Binary）	Gain
0	3’b000	invalid
1	3’b001	2
2	3’b010	4
3	3’b011	8
4	3’b100	16
5	3’b101	24
6	3’b110	32
7	3’b111	48

Table 7. Instrumentation Amplifier 2dn Stage Gain Configuration

AFE_IA2_GX（Decimal）	AFE_IA2_GX（Binary）	Gain
0	2’b00	1
1	2’b01	1.5
2	2’b10	2
3	2’b11	3

Table 8. Instrumentation Amplifier Output Reference Voltage Configuration

PD_AFE_IACMO	AFE_IA2_GX	VCM
1	X	AGND
0	0	VDDA / 10
0	1	VDDA / 2

3.4 DC Bias Circuit

The DC bias circuit is built in the AFE module as shown in the below figure.

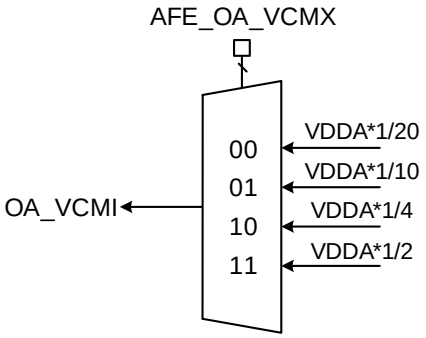

Figure 7. DC Bias Module

This DC bias can be used as the bias voltage of HSOAs. By configuring AFE_OA_VCMX, users can select different levels of DC bias voltages (OA_VCMI), as shown in the below table. When PD_OA_CMI is set to 0, the DC bias circuit is enabled; when set to 1, it's disabled.

Table 9. DC Bias Voltage Output Specifications

PD_OA_CMI	AFE_OA_VCMX	OA_VCMI
1	2'bxx	AGND
0	2'b00	VDDA / 20
0	2'b01	VDDA / 10
0	2'b10	VDDA / 4
0	2'b11	VDDA / 2

4 Constant Current Source Drive Module

The constant current source drive module can provide 2 different levels of adjustable constant current drive.

- Enhanced constant current drive: outputting through D2 pin with a maximum constant current drive of 250 mA.
- Ordinary constant current drive: outputting through D3 pin with a maximum constant current drive of 40 mA.

The drive module consists of the following 4 main parts, as shown in the below figure.

- Current reference (current reference)
- Current driver stage (current driver)
- Normal constant current output stage (normal driver)
- Enhanced constant current output stage (enhanced driver)

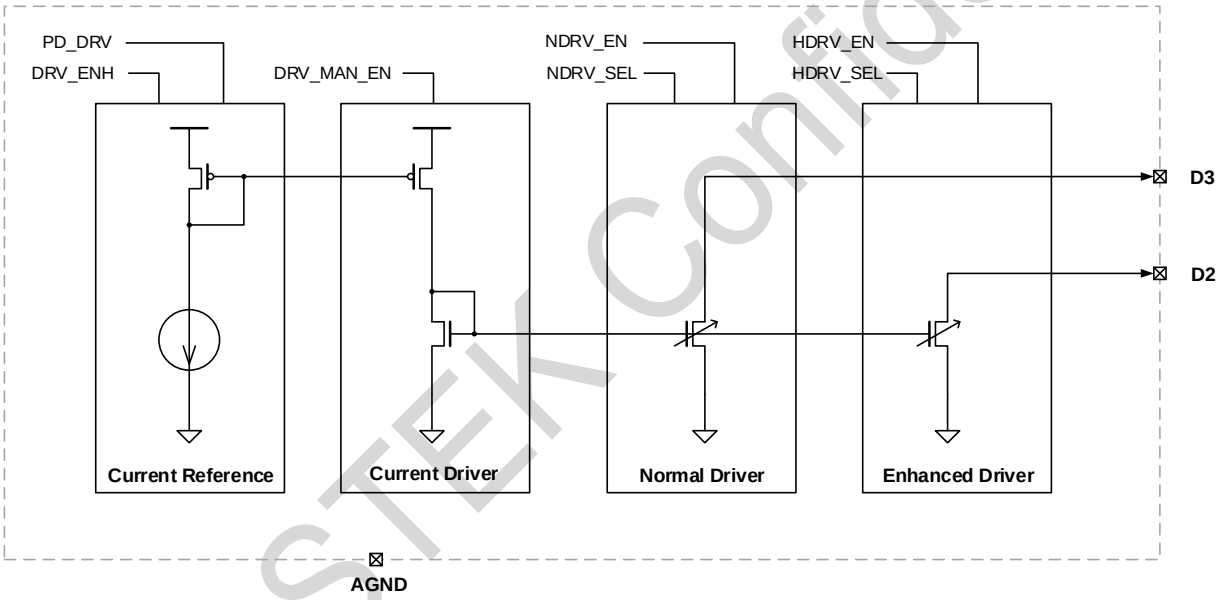

Figure 8. Constant Current Source Drive Sub-modules

Each of the above 4 sub-modules has independent enabling control.

- When PD_DRV is set to 0, the current reference module is enabled.
- When DRV_MAN_EN is set to 1, the current drive stage module is enabled.
- When NDRV_EN is set to 1, the ordinary constant current group is enabled and output through D3 pin.
- When HDRV_EN is set to 1, the enhanced constant current drive is enabled and output through the D2 pin.

For specific register configuration, please refer to Section 8 *AFE Special Function Register*, or *AN286 CMT216xA Register Guide* for details.

5 Micro-power Circuit Module

As shown in the below figure, the micro-power circuit module integrates the following sub-modules.

- 2 micro-power operational amplifiers LPOA0 and LPOA1.
- A micro-power regulator
- A 0.6 V reference voltage source

This module is to meet application scenarios with critical power consumption requirements, such as battery-powered PIR motion detection. Through software configuration, the inputs and outputs of LPOA0 and LPOA1 can be connected to the chip pins. In addition, the built-in 0.6 V reference voltage can be connected to the non-inverting inputs of LPOA0 and LPOA1, much useful in reducing the number of ports when they are used as inverting AC amplifiers.

The main features of micro power modules are as follows.

- Single power supply and low power consumption.
- Rail-to-rail input / output.
- Single operational amplifier consuming a current as low as 0.8 uA.
- 2 sets of external analog input channels.
- Fit for micro-power applications such as PIR motion detection sensors.
- Conditioning of slowly changing signals.

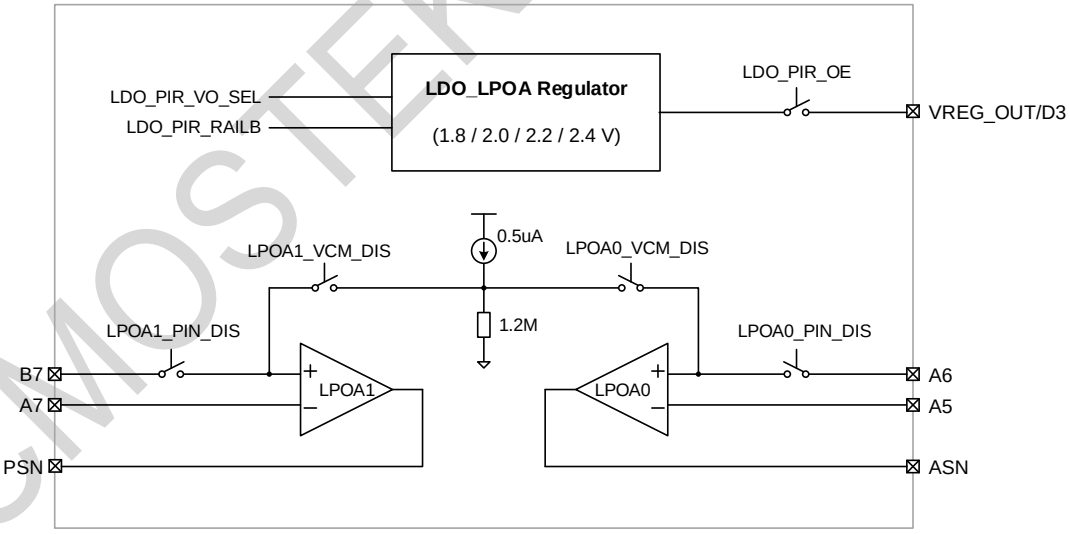

Figure 9. Micro-power Module Block Diagram

In above,

- When LDO_PIR_RAILB is set to 1, the bypass function is disabled, and the LDO_LPOA regulator operates normally; when set to 0, the bypass is enabled and the LDO_LPOA regulator is bypassed.
- By configuring LDO_PIR_VO_SEL, users can select LDO_LPOA Regulator output voltage VREG, providing power to LPOAs. Please refer to Section 2.2 for details.

- When LDO_PIR_OE is set to 1, VREG can be output to VREG_OUT / D3 pin.
- When LPOA0_VCM_DIS or LPOA1_VCM_DIS is set to 0, the internal reference 0.6 V voltage will be output to the non-inverting input terminals of LPOA0 and LPOA1.
- When LPOA0_PIN_DIS or LPOA1_PIN_DIS is set to 0, the non-inverting inputs of LPOA0 and LPOA1 can be connected to the A6 or B7 pins of the chip.

6 ADC

6.1 Basic Function Description

The CMT216xA series integrates a 12-bit successive approximation analog-to-digital converter (SAR-ADC), as shown in the below figure.

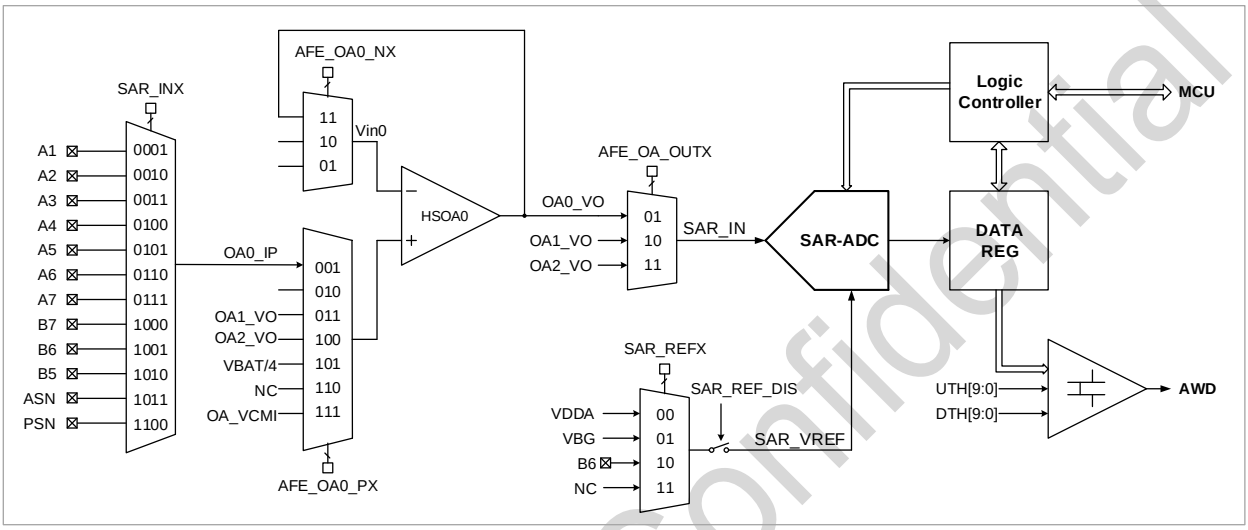

Figure 10. SAR-ADC Block Diagram

The sampling input (SAR_IN) of ADC can select the output from HSOA0, HSOA1, and HSOA2 by setting AFE_OA_OUTX. When HSOA0 is selected, HSOA0 can be used as an internal buffer amplifier, and SAR_INX can be configured to perform direct ADC sampling measurement of 12 analog channels.

The ADC reference voltage can be selected by configuring SAR_REFX.

- VDDA output by the LDO_SAR regulator.
- Built-in 1.2 V band gap reference VBG.
- External reference input voltage (input through pin B6).

Note: When the reference voltage is input from port B6, SAR_REFX must be set to 2'b10, otherwise the ADC may not be driven.

The ADC also supports intermittent low-power operation on hardware level (SNOOZE mode). In the SNOOZE mode, the ADC can be used as an analog watchdog (AWD, short for Analog Watch-Dog). It supports 4 operating modes, in-window interrupt, out-of-window interrupt, upper limit overflow interrupt and lower limit overflow interrupt, to wake up the system while reducing the system power consumption effectively.

Note: Here, window refers to the value range between the upper threshold and the lower threshold during analog acquisition.

6.2 ADC Features

The ADC features are as follows.

- 12-bit high-precision conversion.
- ADC self-calibration.
- Programmable sampling time.
- Programmable ADC clock frequency.
- The highest and second highest conversion times are programmable.
- Programmable conversion time with a typical conversion time of 16 us.
- Supporting being triggered by software or hardware.
- Supporting being awakened regularly with the timing interval programmable.
- Reduce system power consumption effectively by applying SNOOZE operating mode.
- Analog watch dog (AWD) function.
- 4 types of AWD interrupt selection In the SNOOZE mode.
- Supporting continuous conversion (CONT) or single conversion (One-Shot) mode.
- Optional ADC reference voltage.
- ADC input range: 0 ≤ Vin ≤ VDDA.

6.3 Self-calibration of ADC

ADC self-calibration is mainly to eliminate circuit offset voltage and mismatch errors caused by chip manufacturing process. The ADC must perform self-calibration before performing data conversion, otherwise the data conversion result may be inaccurate. In addition, when the power supply voltage and operating temperature change very much, ADC self-calibration can also be performed to eliminate errors caused by power supply voltage and temperature changes. Please refer to the example program for the self-calibration process.

6.4 ADC Operating Flow

In general, the ADC operating flow is as follows.

1. Configure GPIO.

2. Configure the analog signal input channel, set the gain and select the ADC reference (set based on the two structures STRU_AFE_FORNT_SETUP and STRU_AFE_FRONT_POWERUP_SETUP). Please refer to Appendix 9.4.1 and 9.4.3 in Section 9 AN282 *API Function Library Usage Guide* for details.

3. Call the afe_front_setup_config and afe_open_anlaog_front_power API functions. see Section 6.3 in Section 6 or *AN282 API Function Library Usage Guide* for details.

4. Wait for the analog circuit to stabilize, the typical stabilization time (T_{STAB}) is typically 5 us.

5. Enable the ADC clock (SAR_CLK_EN is set).

6. Trigger ADC to start conversion (set SAR_TRIGGER to 1).

7. Wait for the conversion to be completed. When the conversion is complete, the SAR_DATA_UPDATE flag will be set to 1. This flag will be automatically cleared by hardware after lasting 3 ADC clock cycles

8. If requiring to close the related analog modules according to functional requirements, users can call the afe_close_anlaog_front function to close all related circuits.

Notes:

1. *For the related API functions mentioned above, please refer to AN282 API Function Library User Guide for details.*
2. *Please refer to Section 8 or AN286 CMT216xA Register Guide for related register details.*
3. *The SAR_DATA_UPDATE conversion completion signal flag is automatically cleared by hardware. Therefore, it is recommended that users MUST NOT judge the conversion completion of through flag querying, since the software query cycle may possibility miss the ADC conversion completion. Suggest users use a delay wait (with enough time) directly to read the conversion result instead, or use the SAR_DATA_UPDATE interrupt to determine whether the conversion is complete.*

6.5 On-shot Conversion Operating Timing

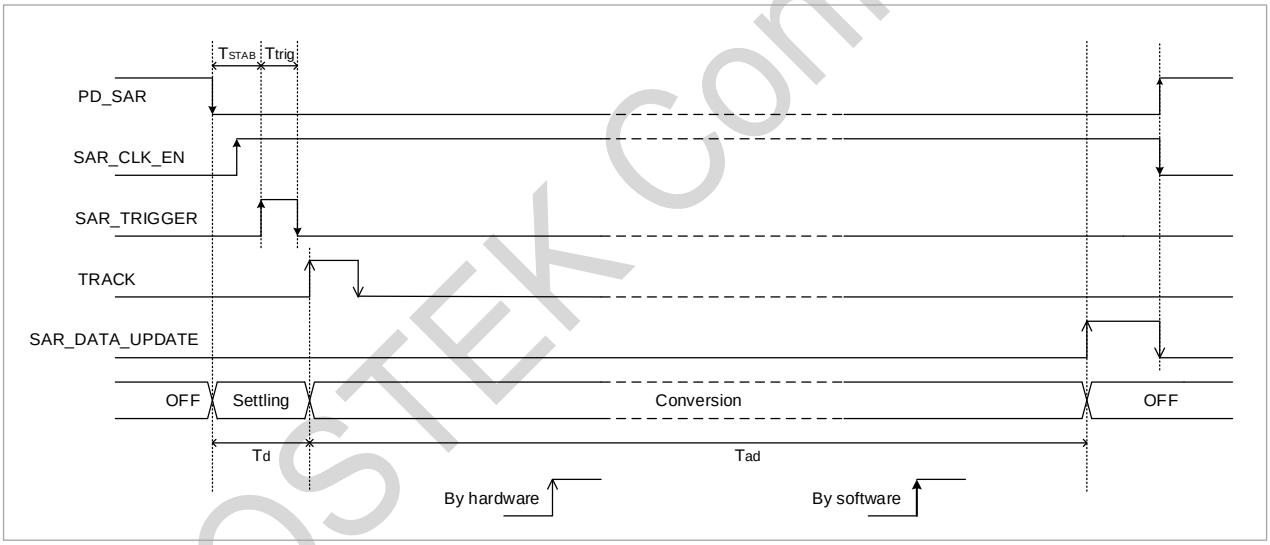

Figure 11. One-Shot Conversion Operation Timing for ADC

By default, the sampling time is 2 ADC clock cycles, the successive approximation conversion time is 13 clock cycles, and the time for conversion result update 1 clock cycle. The sampling time of the ADC, the highest bit conversion time, and the next highest bit conversion time can all be set by the configuration register. The maximum analog circuit setup time T_{STAB} is 5 us. The conversion trigger pulse width T_{trig} is not less than 3 ADC clock cycles.

Thus the total ADC conversion time is calculated as,

$$T_{\mathrm{CONV}} = 5\mathrm{us} + (3 + 16) \times T_{\mathrm{ADC}}$$

In above, T_{ADC} is the time of 1 ADC clock. For instance, if the ADC clock is configured as 1 MHz, the total conversion time is 24 us.

Note: SAR_CLK_EN must be set to 1 before the ADC conversion is triggered, namely the ADC clock is enabled.

6.6 Continuous Conversion (CONT) Operation Timing

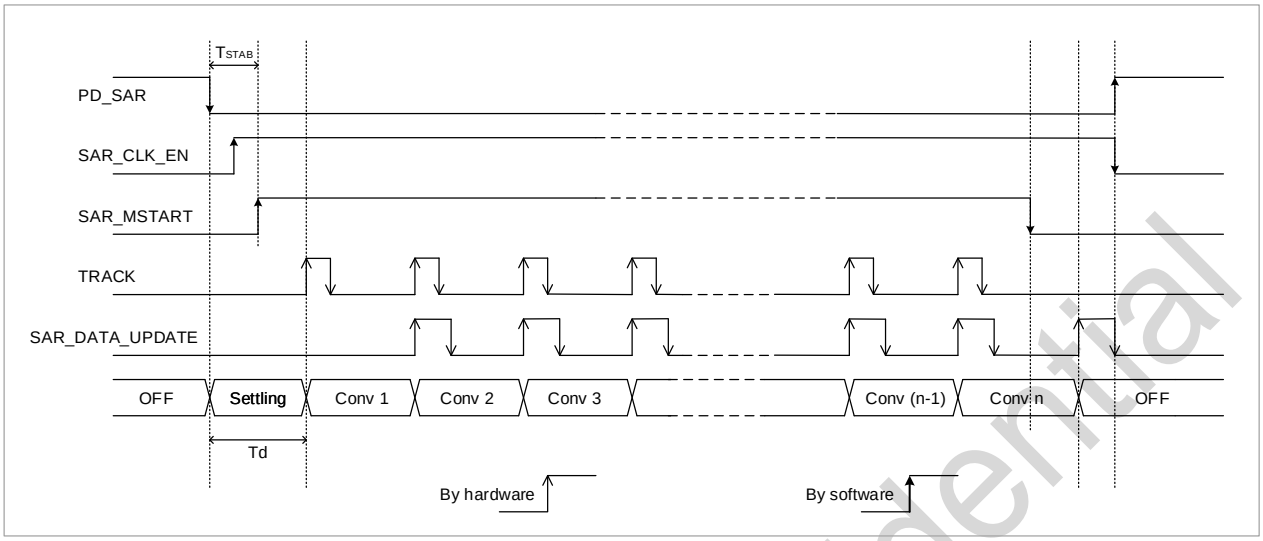

Figure 12. Continuous Conversion (CONT) Operation Timing

To trigger a continuous conversion of the ADC, set SAR_CLK_EN to 1 to turn the clock on first, then set SAR_MSTART to 1. To stop the ADC conversion, users only need to set SAR_MSTART to 0.

6.7 SNOOZE Operating Mode

In the SNOOZE mode, ADC can be used as an analog watchdog (AWD) to wake up the MCU system, which can reduce the system power consumption and extend battery life effectively. The operating timing diagram of SNOOZE is shown in the below figure.

In the SNOOZE mode, ADC will be periodically woken up by the hardware. By detecting the set analog channel signal, the hardware will automatically wake up the MCU when the detected signal meets the set interrupt condition. After the MCU operating completes, ADC re-enters the SNOOZE mode.

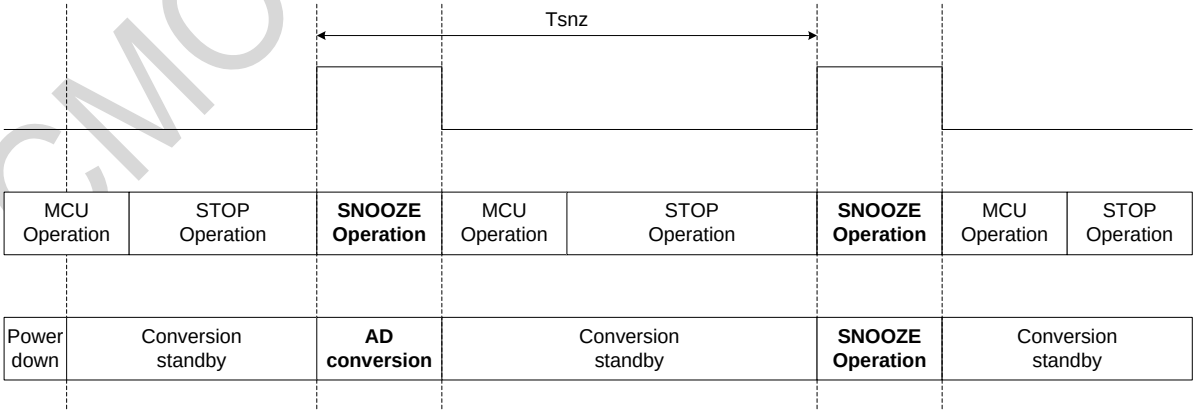

Figure 13. SNOOZE Mode Operating Schematic Diagram

In the SNOOZE mode, the operating flow of the ADC is shown in the below figure. In the SNOOZE mode, the ADC operates in

one-shot mode and can only detect the specified analog channel signals. In addition, the ADC's timer wake-up time can be set by the software configuration register. Section 8 *Special Function Registers of AFE* or *AN286 CMT216xA Register Guide* for more details.

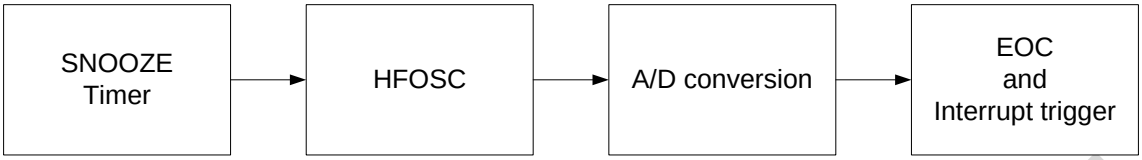

Figure 14. ADC Operating Mode in SNOOZE Mode

The SNOOZE operating mode can only be accessed through software configuration, and it can exit automatically only by the hardware. If a force exit is needed, it can be fulfilled by software reset or power-up again. The entry and exit process of the SNOOZE operating mode is shown in the below figure.

Notes: This flowchart is to present the configuration flow only. Practically, users usually call API to implement the flow. Suggest users take both the example program and the above flowchart as reference for better understanding.

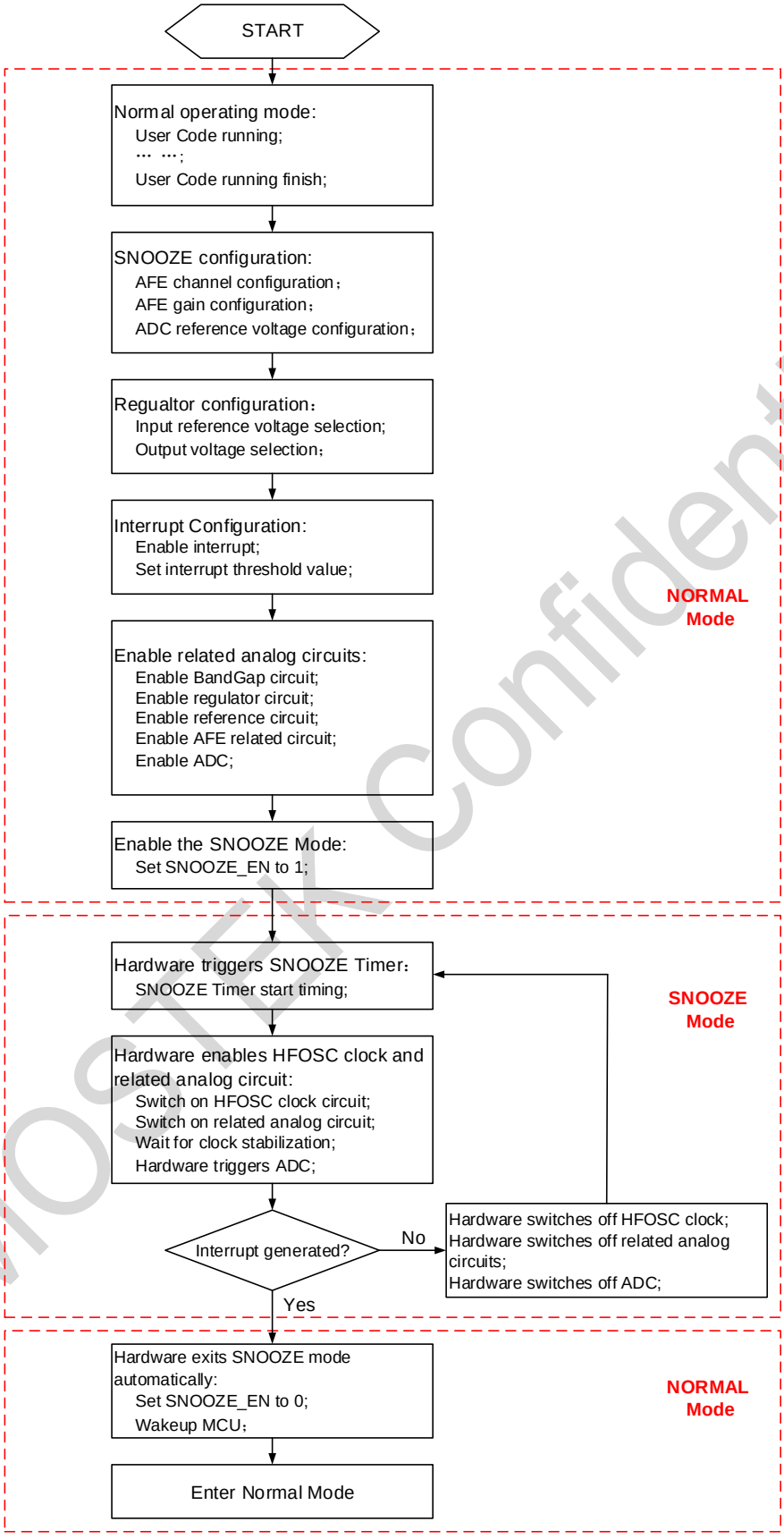

Figure 15. Entry and Exit Process of SNOOZE Operating Mode

7 Sensor Interface Examples

The AFE module integrates a temperature sensor (T-Cell) and a battery sensor (B-Cell). Meanwhile, by configuring HSOAs or LPOAs and the related link registers, it can adapt to a variety of sensor detection interfaces such as pressure sensors and acceleration sensors, and form corresponding signal conditioning circuits to meet various application requirements. The following shows several common sensor measurement methods

7.1 Pressure Sensor Measurement

The measurement circuit of the pressure sensor is shown in the below figure. The pressure sensor P-Cell is a full-bridge piezo-resistive sensor built from MEMS process. The PSP and PSN are used as sensors to provide voltage excitation signals, and the A3 and A4 pins are used as piezo-resistive bridge differential measurement inputs. Then, the signal conditioning of the P-Cell is performed by the internal instrumentation amplifier composed of HSOAs. After then the internal ADC performs conversion measurement.

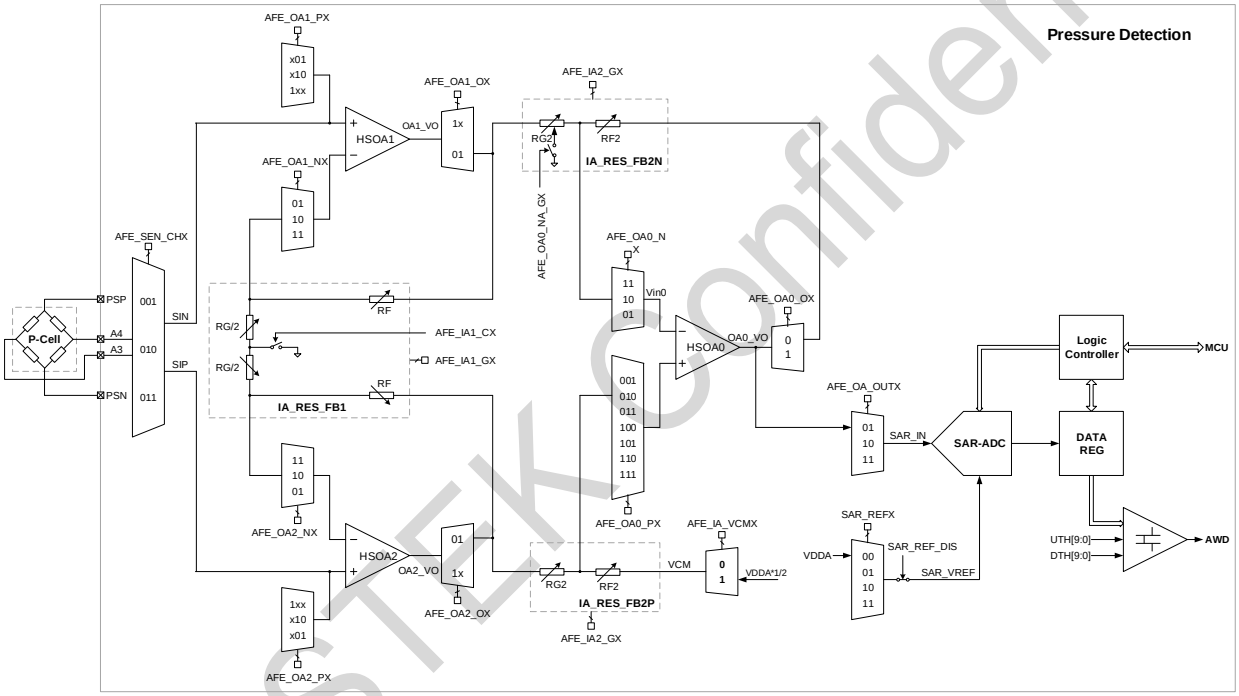

Figure 16. Pressure Sensor Measurement

7.2 Acceleration Sensor Measurement

The measurement circuit of the acceleration sensor is shown in the below figure. The acceleration sensor A-Cell is a full-bridge piezo-resistive sensor built from MEMS process. The ASP and ASN are used as sensors to provide voltage excitation signals, and the A1 and A2 pins are used as piezo-resistive bridge differential measurement inputs. Then the signal conditioning of the A-Cell is performed by the internal instrumentation amplifier composed of HSOAs. After then the internal ADC performs conversion measurement.

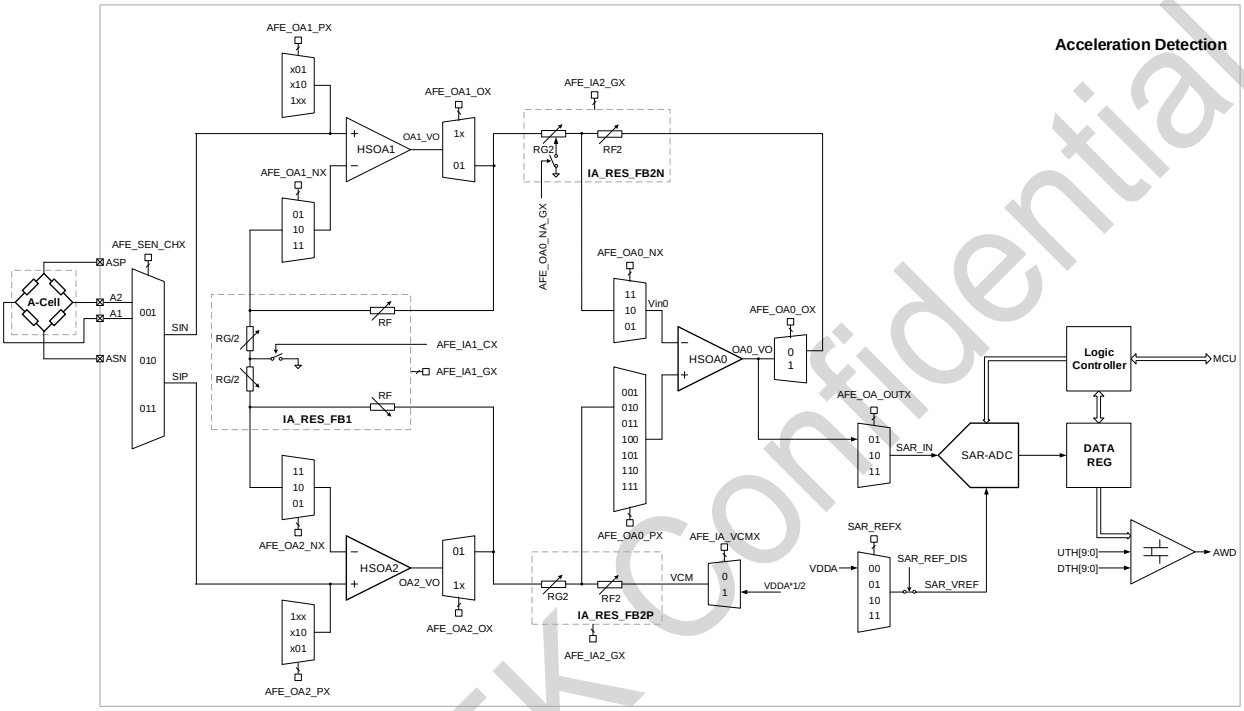

Figure 17. Acceleration Sensor Measurement

7.3 Temperature Sensor Measurement

The measurement circuit of the temperature sensor is shown in the below figure. The temperature sensor T-Cell is a full-bridge temperature-sensitive resistance sensor built in the chip. It is selected by AFE_SEN_CHX. The signal conditioning is performed by the internal instrumentation amplifier composed of HSOAs. Then the ADC performs conversion measurement.

Notes: The T-Cell is used in the system for qualitative calibration. When using the T-Cell for temperature measurement, users need perform calibration before using it for temperature measurement. The T-Cell is not calibrated in factory.

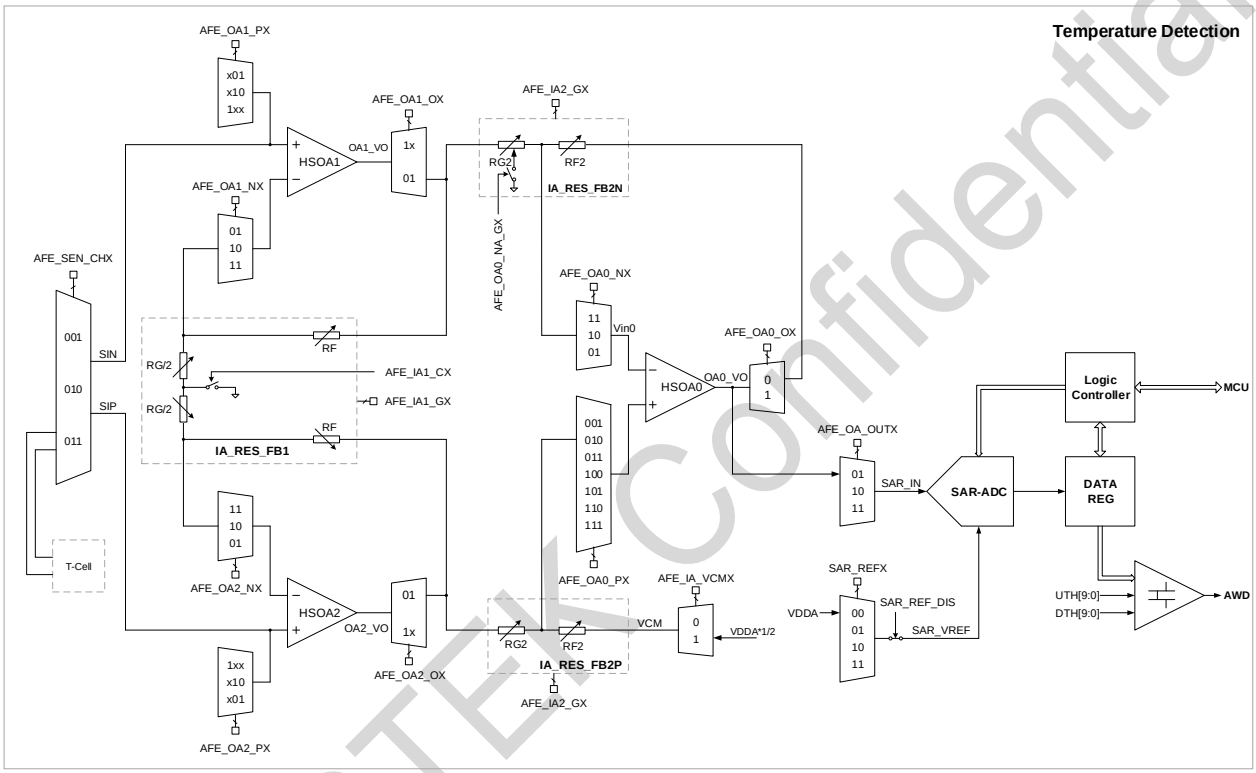

Figure 18. Temperature Sensor Measurement

7.4 Battery Sensor Measurement

The battery sensor outputs a voltage signal VBAT / 4 (VDD/4), which is proportional to the battery voltage change. The battery sensor measurement is shown in the below figure. The output signal of the battery sensor is buffered by HSOA0 internally , then is converted into a digital signal by ADC. ADC adopts a reference voltage of 1.2 V output by the Band-gap Reference (VBG).

Notes: The battery sensor provides an encapsulated API function afe_check_system_voltage, through which it can obtain the current supply voltage. However, it should be noted that after calling this function, the configurations such as the AFE detection channel will be modified. If there exists other analog parameters acquisition in the user system, it needs to reconfigure such configurations as detection channel setting.

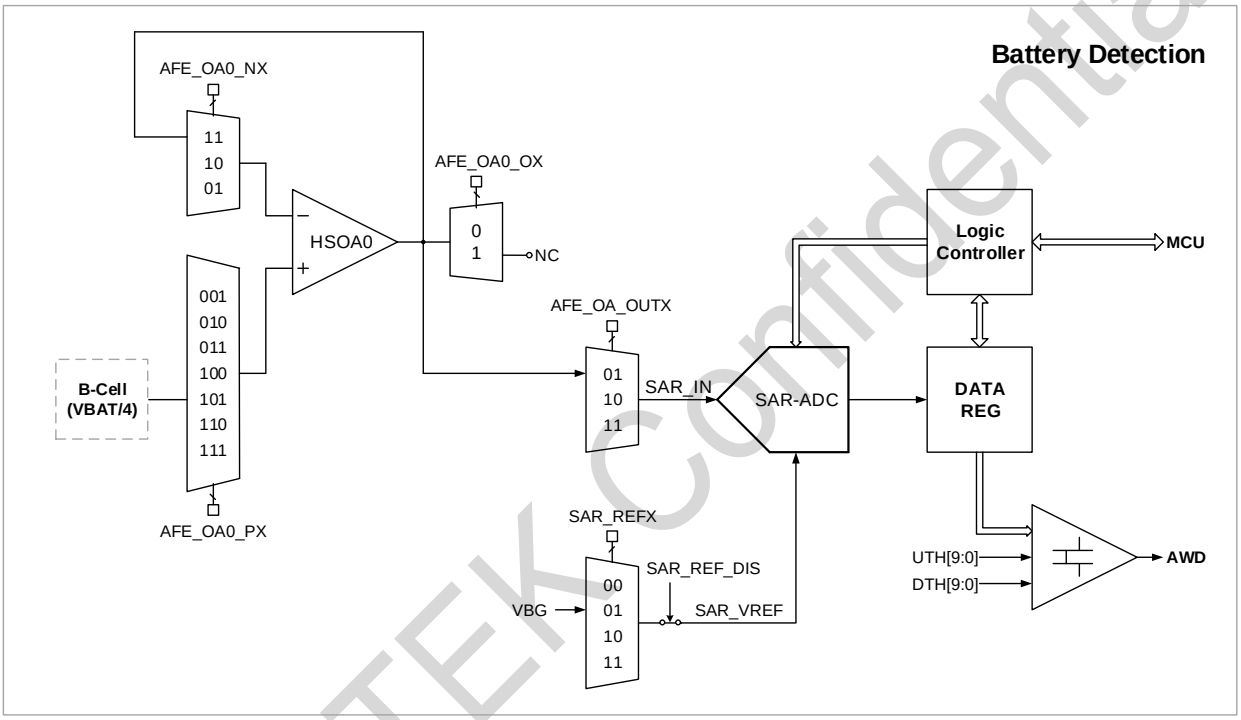

Figure 19. Battery Sensor Measurement

7.5 Shock Sensor Measurement

Shock sensors are usually made of piezoelectric ceramic materials. The measurement circuit of a shock sensor using CMT216xA is shown in the below figure. The shock sensor can be applied to measure acceleration with low-power consumption, which is suitable for qualitative analysis of motion and low-power measurement applications. As shown in the below figure, the signal conditioning is performed by a two-stage cascaded integral amplifier circuit formed by HSOA1 and HSOA2. The DC bias voltage can be selected from either the on-chip OA_VCMI or the external inputting from ports A1 and A4 according to user requirements.

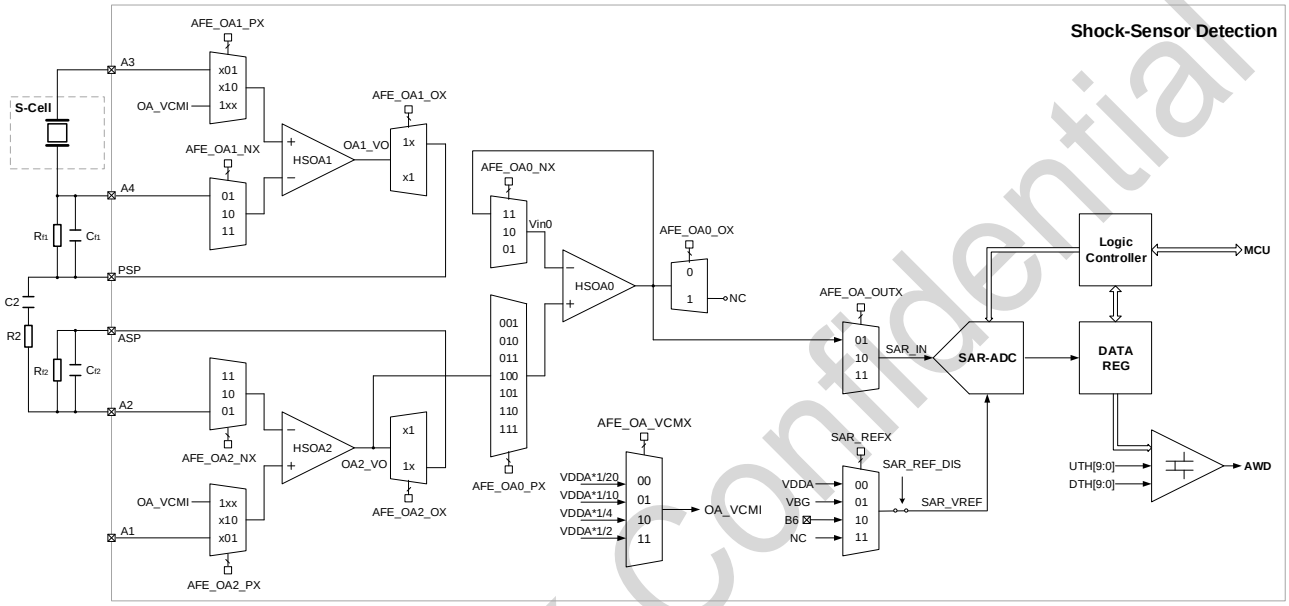

Figure 20. Shock Sensor Measurement

7.6 PIR Motion Detection

Low power consumption is the significant advantage for passive infrared detection (PIR) applied in mobile detection. Thus it is suitable for indoor low-power monitoring applications. The CMT216xA used to process with the PIR sensor is shown in the below figure.

As shown in the below figure, a two-stage cascaded integral amplifier signal conditioning circuit is formed by LPOA1 and LPOA2. The LPOA1's DC bias can select either the internal 0.6 V reference voltage, or the input from the B7 pin directly. The PIR sensor is powered by the VREG output of the micro-power LDO_LPOA regulator (through the VREG_OUT / D3 pin). The signal sensed by the PIR sensor is amplified by a two-stage amplifier circuit, then converted into a digital signal by the ADC, and further processed by the on-chip 8051 system (user software processing). Under normal circumstances, PIR motion detection co-operating with the ADC's SNOOZE operating mode can effectively reduce the overall system power consumption, achieving monitoring power consumption of no more than twenty uA, or even below ten uA.

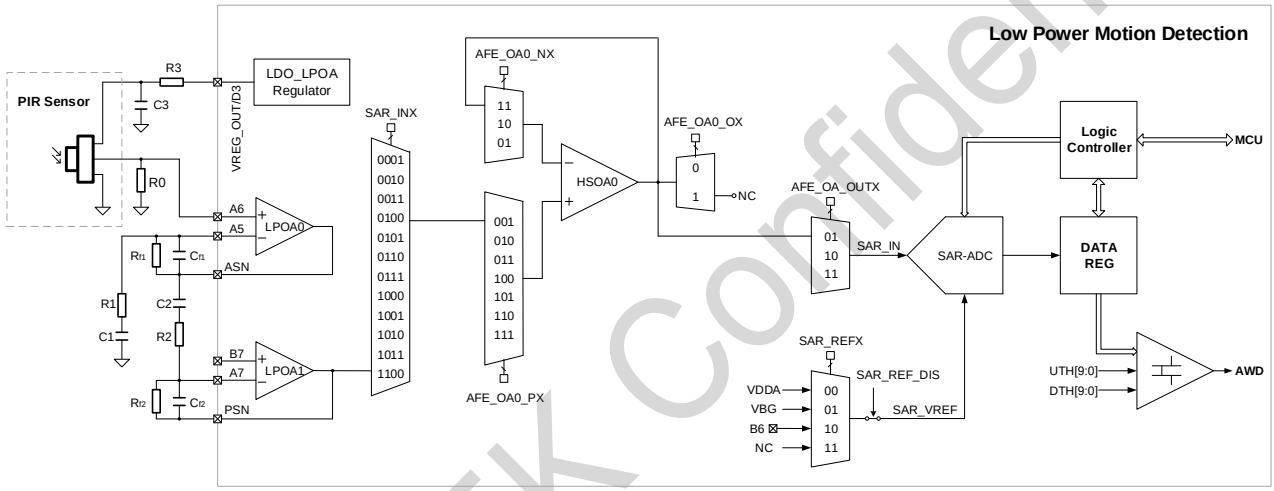

Figure 21. PIR Motion Detection

7.7 Smoke Detection

Photoelectric smoke detector (known as photoelectric maze) is the main component as well as the main technique currently for smoke detection. The mechanism is that, a pair of tubes, a transmission tube (PT tube) and a receiving tube (PD tube) are placed in a dark room (maze cavity). Under normal circumstances, the transmission tube signal cannot reach the receiving tube directly. So there is no signal (only a weak dark current). However, in case of fire, there are smoke particles entering the maze chamber with the air flow. In this case, as the infrared transmission tube is in operating, scattering will occur under the effect of smoke particles. Thus the infrared receiving tube generates a stronger (relative to the dark current signal) signal.

CMT216xA applied for smoke detection is shown in the below figure. The mechanism is that, HSOA1, a trans-impedance amplifier, implements current-to-voltage signal conversion then the signal is provided as the input signal of HSOA2, a non-inverting amplifier. The amplification factor is determined by R2 and R1 as shown in the below figure. Finally, the signal amplified by HSOA2 passes through HSOA0 (as an internal buffer), then is output to the ADC for sampling and conversion. In addition, the DC bias of HSOA1 can select either the internal OA_VCMI, or input from the A3 pin directly. Moreover, the enhanced constant current source output of the CMT216xA chip can be connected to the infrared transmission tube through the D2 pin or used as the constant current drive of the transmission tube.

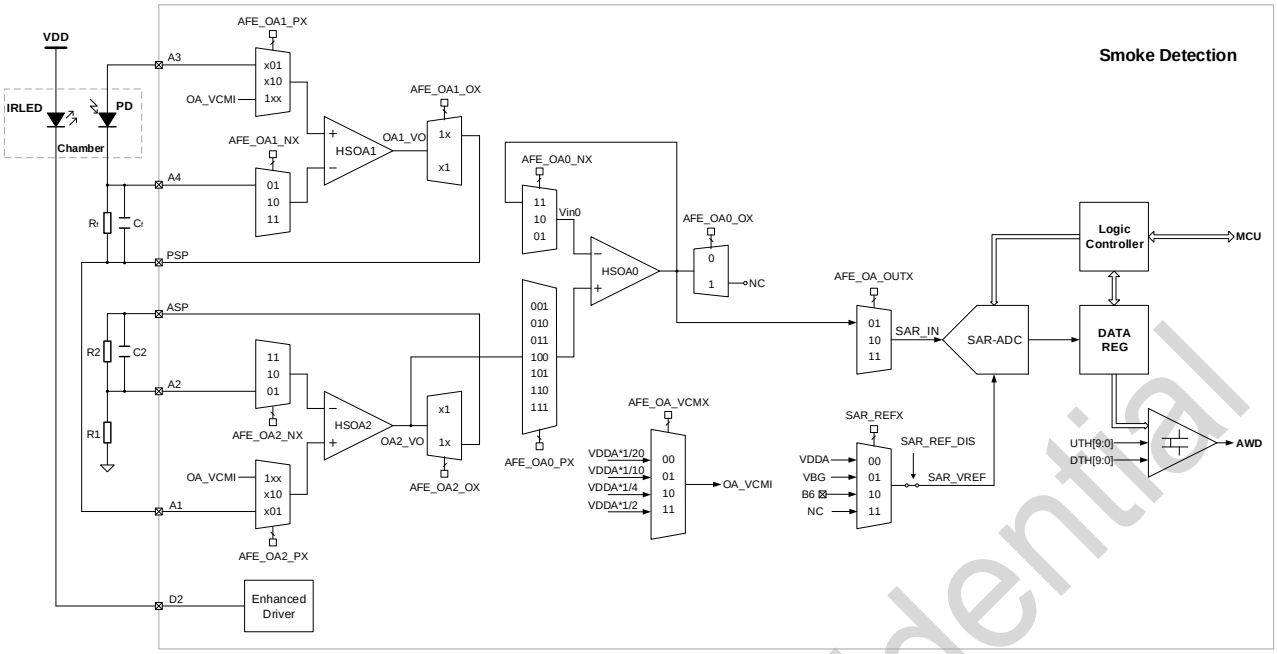

Figure 22. Smoke Detection Block Diagram 1

The above smoke detection solution uses 3 HSOAs to implement sensor detection. This solution features that the analog conditioning is adjustable outside the chip, however it takes up more pins and internal resources. Co-operating with the on-chip AFE function, it can also be adjusted to the solution shown in the below figure. The mechanism is that HSOA1 is the trans-impedance amplifier to achieve current-to-voltage signal conversion, however the HSOA1 output signal goes directly to HSOA0. At this time, HSOA0 is configured as a non-inverting amplifier, and the internal amplification gain is fulfilled by adjusting AFE_IA2_GX. This solution features that the peripheral design is simple and HSOA0 is used as a non-inverting amplifier supporting programmable gain control. At the same time, HSOA2 is saved for other analog sensor usage.

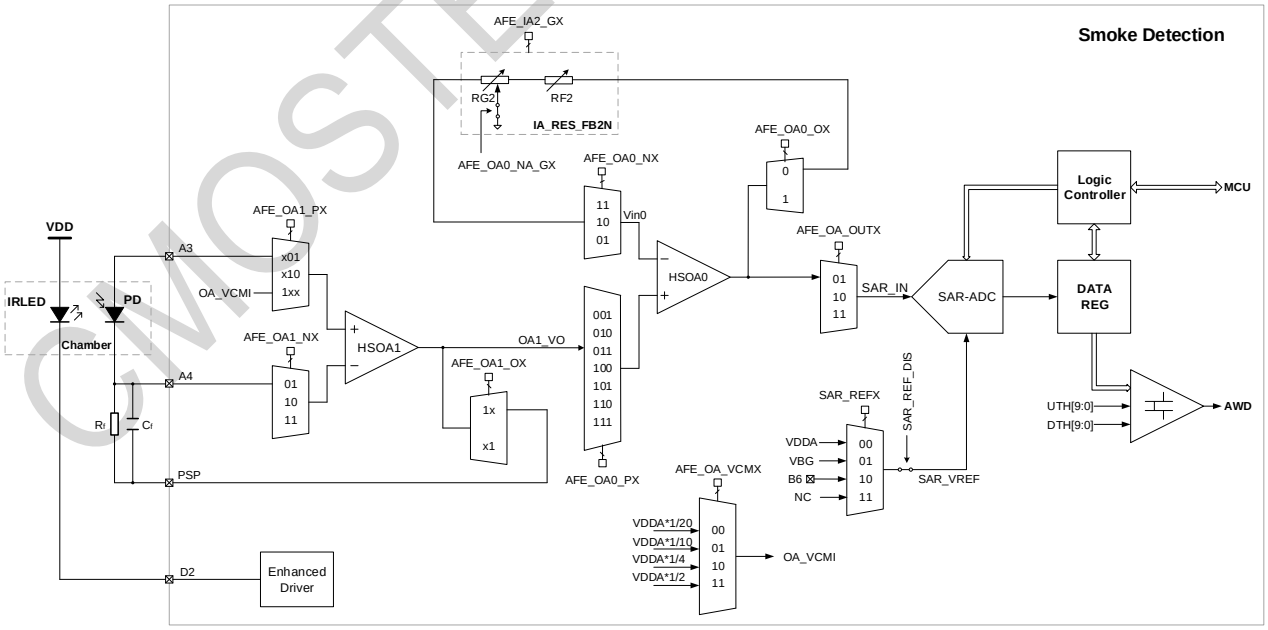

Figure 23. Smoke Detection Block Diagram 2

8 Special Function Register for AFE (SFR)

The AFE Special Function Register (SFR) is mainly used to configure and control AFE. The AFE related registers are shown in the below table. Each register will be described in detail in this section.

Table 10. Special Function Register List for AFE

Register Name	Address	WR	Reset Value	Description
CUS_AFE4	0x03	R/W	0x00	Gain Configuration Register 1
CUS_AFE6	0x05	R/W	0x80	Gain Configuration Register 2
CUS_AFE7	0x06	R/W	0x80	Bridge-type sensor interface configuration register
CUS_AFE9	0x08	R/W	0xC1	DC bias configuration register
CUS_AFE10	0x09	R/W	0x00	HSOA0 configuration register
CUS_AFE11	0x0A	R/W	0x80	HSOA1 configuration register
CUS_AFE12	0x0B	R/W	0x80	HSOA2 configuration register
CUS_AFE13	0x0C	R/W	0x80	Micro-power regulator output and ADC input configuration register
CUS_AFE14	0x0D	R/W	0xBF	AFE control register 1
CUS_AFE15	0x0E	R/W	0xBF	AFE control register 2
CUS_AFE16	0x0F	R/W	0x0F	ADC conversion time configuration and LPOAs control register
CUS_AFE17	0x10	R/W	0x01	Constant current drive control register 1
CUS_AFE18	0x11	R/W	0x00	Constant current drive control register 2
CUS_SNOOZE1	0x1E	R/W	0x00	SNOOZE timer configuration register 1
CUS_SNOOZE2	0x1F	R/W	0x00	SNOOZE timer configuration register 2
CUS_SNOOZE3	0x20	R/W	0x00	SNOOZE interrupt upper threshold register 1
CUS_SNOOZE4	0x21	R/W	0x00	SNOOZE interrupt lower threshold register 2
CUS_SNOOZE5	0x22	R/W	0x00	SNOOZE interrupt enabling and ADC clock frequency selection register.
CUS_SNOOZE6	0x23	R	0x00	SNOOZE interrupt flag mode
CUS_SYSCTL3	0x50	R/W	0x00	SNOOZE mode control register
CUS_SYSCTL12	0x68	R/W	0x80	Interrupt wakeup flag register in SNOOZE mode
CUS_SYSCTL13	0x69	R	0x00	ADC control register
CUS_SYSCTL14	0x6A	R/W	0x00	ADC data register 1
CUS_SYSCTL15	0x6B	R	0x00	ADC data register 2
CUS_SYSCTL16	0x6C	R	0x00	LBD threshold register
CUS_SYSCTL17	0x6D	R/W	0x00	LBD result register
CUS_SYSCTL19	0x6E	R	0x00	Constant current drive pulse output output port control register
CUS_RESV5	0x70	R/W	0x03	LPOAs non-inverting input port configuration register

8.1 Gain Configuration Register

8.1.1 CUS_AFE4: gain configuration register 1

Addr:0x03 Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AFE_IA2_GX		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/W		R/W	R/W	R/W	R/W	R/W	R/W

AFE_IA2_GX: the gain selection of HSOA0, which operates as the 1st or 2nd stage general purpose instrumentation amplifiers or operates as built-in non-inverting amplifiers. When operating as built-in non-inverting amplifiers, it's gain configuration should co-work with AFE_OA0_NA_GX, refer to Table 5 for details.

- 2'b00: the 2nd stage gain of the instrumentation amplifier is 1.0
- 2'b01: the 2nd stage gain of the instrumentation amplifier is 1.5
- 2'b10: the 2nd stage gain of the instrumentation amplifier is 2.0
- 2'b11: the 2nd stage gain of the instrumentation amplifier is 3.0

Note: It is not allowed to modify the default values of other configuration bits, otherwise the chip may not operate properly. Users cannot modify the register field marked as Reserved in the register, otherwise the chip may not work properly. It is recommended that the user follow the "read-modify-write" operation mode or use API library functions to avoid directly operating the register as much as possible. ***This applies to all registers in this document.***

8.1.2 CUS_AFE6: gain configuration register 2

Addr:0x05 Reset value: 0x80

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	AFE_IA1_GX			Reserved	Reserved	Reserved
R/W	R/W	R/W			R/W	R/W	R/W

AFE_IA1_GX: the gain selection of HSOA1 and HSOA2, which operates as the 1st stage general purpose instrumentation amplifiers or operates as built-in non-inverting amplifiers.

- 3'b000: no gain setting. Cannot set to this value when the amplifier is in operating.
- 3'b 001: gain is 2.
- 3'b 010: gain is 4.
- 3'b 011: gain is 8.
- 3'b 100: gain is 16.
- 3'b 101: gain is 24.
- 3'b 110: gain is 32.
- 3'b 111: gain is 48.

8.2 CUA_AFE7: Bridge-type Sensor Interface Configuration Register

Addr:0x06 Reset value: 0x80

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	No Use	Reserved	Reserved	Reserved	AFE_SEN_CHX		
R/W	R/W	R/W	R/W	R/W	R/W		

AFE_SEN_CHX: sensor channel selection

- 3'b000: no channel selection
- 3'b 001: select external sensor channel 1, using HSOAs as instrumentation amplifier, A1 and A2 pins as differential measurement input and ASN and ASP pins as sensor power supply excitation source. It can be used for piezo-resistive bridge acceleration sensor. Refer to Section 7.2 Acceleration Sensor Measurement for details.
- 3'b 010: select external sensor channel 2, using HSOAs as instrumentation amplifier, A3 and A4 pins as differential measurement input and PSN and PSP pins as sensor power supply excitation source. It can be used for piezo-resistive bridge pressure sensor. Refer to Section 7.1 Pressure Sensor Measurement for details.
- 3'b 011: select the built-in temperature sensor channel. Refer to Section 7.3 Temperature Sensor Measurement for details.
- 3'b 100: cannot be used
- 3'b 101: cannot be used
- 3'b 110: cannot be used
- 3'b 111: cannot be used

8.3 CUS_AFE9: DC Bias Configuration Register

Addr:0x08 Reset value: 0xC1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPOA0_VCM_DIS	LPOA1_VCM_DIS	AFE_IA_VCMX	AFE_OA_VCMX		AFE_OA_OUTX		AFE_IA1_CX
R/W	R/W	R/W	R/W		R/W		R/W

LPOA0_OA0_VCM_DIS: LPOA0 internal 0.6 V selection configuration

0: connect the internal 0.6 V reference to the non-inverting input of LPOA0

1: not select

LPOA1_OA1_VCM_DIS: LPOA1 internal 0.6 V selection configuration

0: connect the internal 0.6 V reference to the non-inverting input of LPOA1

1: not select

AFE_IA_VCMX: output reference voltage selection for HSOAs as instrumentation amplifiers

0: VDDA/10

1: VDDA/2

AFE_OA_VCMX: HSOAs non-inverting input DC bias voltage selection

2'b00: VDDA/20

2'b01: VDDA/10

2'b10: VDDA/4

2'b11: VDDA/2

AFE_OA_OUTX: select HSOAs output to drive ADC

2'b 00: no channel selection.

2'b 01: select the output of HSOA0 to drive ADC.

2'b 10: select the output of HSOA1 to drive ADC.

2'b 11: select the output of HSOA2 to drive ADC.

AFE_IA1_CX: select the internal function of HSOA1 and HSOA2

0:built-in non-inverting amplifier function. Refer to Section 3.1 for details.

1:built-in instrumentation amplifier function. Refer to Section 3.1 for details.

8.4 HSOAs Configuration Register

8.4.1 CUS_AFE10: HSOAs Configuration Register 1

Addr:0x09 Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AFE_OA0_OX	AFE_OA0_NX		AFE_OA0_PX			AFE_OA0_NA_GX	
R/W	R/W		R/W			R/W	

AFE_OA0_OX: HSOA0 output channel selection

0: select channel 0 to output. Namely, output to IA_RES_FB2N to have gain adjustment through configuring AFE_IA2_GX and AFE_OA0_NA_GX.

1: select channel 1 to output, namely, no connection for output.

AFE_OA0_NX: HSOA0 inverting input channel selection

- 2'b00: no channel selection.
- 2'b01: channel 1 selection, namely no connection for input.
- 2'b10: channel 2 selection, namely connect to IA_RES_FB2N to have gain adjustment through configuring AFE_IA2_GX and AFE_OA0_NA_GX.
- 2'b11: channel 3 selection, namely connect to HSOA0 for output, forming buffer amplifier.

AFE_OA0_PX: HSOA0 non-inverting input channel selection

- 3'b000: no channel selection.
- 3'b001: channel 1 selection. Connect to OA0_IP and select the 12 analog channel , A1~A7, B5~B7 , ASN and PSN , which are measured directly.
- 3'b010: channel 2 selection. Connect to IA_RES_FB2P to have gain adjustment, applicable to HSOAs forming instrument amplifier.
- 3'b011: channel 3 selection. Connect to OA1_VO, namely the output of HSOA1.
- 3'b100: channel 4 selection. Connect to OA2_VO, namely the output of HSOA2.
- 3'b101: channel 5 selection. Connect to supply battery sensor V_{BAT}/4, namely VDD/4.
- 3'b110: channel 6 selection. cannot be used.
- 3'b111: channel 7 selection. Connect to OA_VCMI, namely HSOAs DC bias voltage.

AFE_OA0_NA_GX: HSOA0 non-inverting amplification gain selection, co-working with AFE_IA2_GX, see Table 5 for details.

- 2'b 00: inverting amplification.
- 2'b 01: non-inverting amplification with small gain.
- 2'b 10: non-inverting amplification with medium gain.
- 2'b 11: non-inverting amplification with high gain.

Notes: The above configuration can be either modified by the registers directly or by calling the afe_front_setup_config function. For the API function, see AN282 CMT216xA API Function Library User Guide for more details..

8.4.2 CUS_AFE11: HSOAs Configuration Register 2

Addr:0x0A Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SAR_DIRECT_DIS	AFE_OA1_OX		AFE_OA1_NX		AFE_OA1_PX		
R/W	R/W		R/W		R/W		

SAR_DIRECT_DIS: ADC internal test control bit. Must be set to 1 in the normal use of ADC.

0: Internal test mode, for internal test use only. Prohibit users from using this option.

1: ADC in normal use

AFE_OA1_OX: HSOA1 output channel selection

- 2'b00: no channel selection.
- 2'b01: channel 1 selection. Connect to IA_RES_FB2N and IA_RES_FB1 for gain adjustment. It can form instrument amplifier or non-inverting amplifier.
- 2'b10: channel 2 selection. Connect to the PSP pin of the chip.
- 2'b11: channel 1 and channel 2 selection at the same time.

AFE_OA1_NX: HSOA1 inverting input channel selection

- 2'b00: no channel selection.
- 2'b01: channel 1 selection. Connect to the A4 pin of the chip.
- 2'b10: channel 2 selection. Connect to the IA_RES_FB1 for gain adjustment. It can form instrument amplifier or non-inverting amplifier.
- 2'b11: channel 3 selection. Connect to OA1_VO, the output of HSOA1. It can form buffer amplifier.

AFE_OA1_PX: HSOA1 non-inverting input channel selection

- 3'b000: no channel selection
- 3'b001: channel 1 selection. Connect to the A3 pin of the chip.
- 3'b010: channel 2 selection. Connect to the PSN pin of the chip.
- 3'b011: cannot be used.
- 3'b100: channel 3 selection. Connect to OA_VCMI, namely the internal DC bias voltage.
- 3'b101: channel 1 and channel 2 selection at the same time.
- 3'b110: channel 2 and channel 3 selection at the same time.
- 3'b111: cannot be used.

8.4.3 CUS_AFE12: HSOAs Configuration Register 3

Addr:0x0B Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDO_PIR_RALIB	AFE_OA2_OX		AFE_OA2_NX		AFE_OA2_PX		
R/W	R/W		R/W		R/W		

LDO_PIR_RALIB: the bypass selection of the micro-power LDO_LPOA regulator.

0: enable bypass.

1: disable bypass.

AFE_OA2_OX: HSOA2 output channel selection

- 2'b00: no channel selection
- 2'b01: channel 1 selection. Connect to IA_RES_FB2P and IA_RES_FB1 for gain adjustment. It can form instrument amplifier or non-inverting amplifier.
- 2'b10: channel 2 selection. Connect to the ASP pin of the chip.
- 2'b11: channel 1 and channel 2 selection at the same time.

AFE_OA2_NX: HSOA2 inverting input channel selection

- 2'b00: no channel selection.
- 2'b01: channel 1 selection. Connect to the ASP pin of the chip.
- 2'b10: channel 2 selection. Connect to IA_RES_FB1 for gain adjustment. It can form instrument amplifier or non-inverting amplifier.
- 2'b11: channel 3 selection. Connect to OA2_VO, the output of HSOA2. It can form buffer amplifier.

AFE_OA2_PX: HSOA2 non-inverting input channel selection

- 3'b000: no channel selection
- 3'b001: channel 1 selection. Connect to the A1 pin of the chip.
- 3'b010: channel 2 selection. Connect to the ASP pin of the chip.
- 3'b011: cannot be used.
- 3'b100: channel 3 selection. Connect to OA_VCMI, the internal DC bias voltage.
- 3'b101: channel 1 and channel 3 selection at the same time.
- 3'b110: channel 2 and channel 3 selection at the same time.
- 3'b111: cannot be used.

8.5 CUS_AFE13: Micro-power Regulator Output and ADC Input Configuration Register

Addr:0x0C Reset value: 0x80

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDO_PIR_VO_SEL		SAR_INX				SAR_REFX	
R/W		R/W				R/W	

LDO_PIR_VO_SEL: the output voltage VREG selection of the micro-power LDO_LPOA regulator.

- 2'b00: 1.8 V
- 2'b01: 2.0 V
- 2'b10: 2.2 V
- 2'b11: 2.4 V

SAR_INX: OA0_IP channel selection, namely HSOA0 non-inverting amplifier channel selection.

- 4'b0000: no channel selection .
- 4'b0001: channel A1 selection.
- 4'b0010: channel A2 selection.
- 4'b0011: channel A3 selection.
- 4'b0100: channel A4 selection.
- 4'b0101: channel A5 selection.
- 4'b0110: channel A6 selection.
- 4'b0111: channel A7 selection.
- 4'b1000: channel B7 selection.
- 4'b1001: channel B6 selection.
- 4'b1010: channel B5 selection.
- 4'b1011: the input of the ASN pin, namely LPOA0 output channel selection.
- 4'b1100: the input of the PSN pin,namely LPOA1 output channel selection.
- 4'b1101: cannot be used.
- 4'b1110: cannot be used.
- 4'b1111: cannot be used.

SAR_REFX: ADC reference voltage selection

- 2b'00: select VDDA, namely the output of the LDO_SAR regulator.
- 2b'01: select 1.2 V band-gap reference. Drive ADC by the internal buffer.
- 2b'10: select the external reference voltage from the B6 port. Drive ADC by the internal buffer.
- 2b'11: cannot be used.

8.6 AFE Control Register

8.6.1 CUS_AFE14: AFE Control Register 1

Addr：0x0D Reset value: 0xBF

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PD_AFE_OACMI	PIR_ST	PD_AFE_OSADJ	PD_AFE_IACMO	PD_SAR	PD_AFE_OA2	PD_AFE_OA1	PD_AFE_OA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PD_AFE_OACMI: HSOAs non-inverting input DC bias voltage enabling

0: enable DC bias voltage.

1: disable it.

PIR_ST: micro-power regulator DC bias circuit enabling bit.

0: default

1: disable

PD_AFE_OSADJ: instrumentation amplifier calibration enabling.

0: enable

1: Disable

PD_AFE_IACMO: the enabling of the output voltage of the instrumentation amplifier.

0: enable reference voltage.

1: disable.

PD_SAR: ADC enabling.

0: enable ADC

1: disable ADC

PD_AFE_OA2: HSOA2 amplifier enabling.

0: enable HSOA2 amplifier.

1: disable it.

PD_AFE_OA1: HSOA1 amplifier is enabled

0: enable HSOA1 amplifier.

1: disable

PD_AFE_OA0: HSOA0 amplifier enabling.

0: enable HSOA0 amplifier.

1: disable it.

8.6.2 CUS_AFE15: AFE Control Register 2

Addr: 0x0E Reset value: 0xBF

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDO_SAR_VO_SEL		LDO_SAR_RAILB	PD_BG	SAR_LBD_DIS	SAR_REF_DIS	PD_LDO_SAR	PD_AFE_VTR
R/W		R/W	R/W	R/W	R/W	R/W	R/W

LDO_SAR_VO_SEL: LDO_SAR regulator output voltage (VDDA) selection

- 2'b00: 1.8 V
- 2'b01: 2.0 V
- 2'b10: 2.2 V
- 2'b11: 2.4 V

LDO_SAR_RAILB: LDO_SAR regulator output bypass selection

0: bypass the LDO_SAR regulator. At this time, VDDA is the chip supply voltage, namely VDD.
1: Do not bypass LDO_SAR Regulator.

PD_BG: built-in band-gap reference source (namely VBG) enabling control

0: enable. VBG is 1.2 V.
1: disable.

SAR_LBD_DIS: power supply voltage detection enabling.

0: enable.
1: disable.

SAR_REF_DIS: ADC reference voltage enabling.

0: enable.
1: disable.

PD_LDO_SAR: LDO_SAR regulator enabling control.

0: enable.
1: disable.

PD_AFE_VTR: AFE DC bias enabling. When HSOAs or ADC is operating, this bit must be set to 0 to enable VTR.

0: enable
1: disable

Notes: The above HSOAs settings can be configured by calling API functions such as sys_set_afe_sensor_channel and afe_front_setup_config, with no need for to operate each register one by one. For details about these API functions, please refer to AN282 CMT216xA API Function Library Usage Guide.

8.7 CUS_AFE16 : ADC Conversion Time Configuration and Micro-power Circuit Control Register

Addr：0x0F Reset value: 0x0F

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SAR_MBC0	SAR_MBC1	SAR_STM		PD_LDO_PIR	PD_PIR_VTR	PD_LPOA1	PD_LPOA0
R/W	R/W	R/W		R/W	R/W	R/W	R/W

SAR_MBC0: ADC second-highest bit conversion time selection.

0: 1 ADC clock.

1: 2 ADC clocks.

SAR_MBC1: ADC highest bit conversion time selection.

0: 2 ADC clocks.

1: 4 ADC clocks.

SAR_STM: ADC sampling time selection.

- 2'b00: 2 ADC clocks.
- 2'b01: 4 ADC clocks.
- 2'b10: 6 ADC clocks.
- 2'b11: 8 ADC clocks.

PD_LDO_PIR: micro-power LDO_LPOA Regulator enabling.

0: enable.

1: disable.

PD_PIR_VTR: micro-power circuit bias current enabling control.

0: enable. When LDO_LPOA regulator or LPOAs operate, PD_PIR_VTR must be set to 0.

1: disable.

PD_LPOA1: LPOA1 enabling control.

0: enable.

1: disable.

PD_LPOA0: LPOA0 enabling control.

0: enable.

1: disable.

8.8 Constant Current Source Drive Control Register

8.8.1 CUS_AFE17: Constant Current Source Drive Control Register 1

Addr：0x10 Reset value: 0x01

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HDRV_SEL					DRV_ENH	DRV_MAN_EN	PD_DRV
R/W					R/W	R/W	R/W

HDRV_SEL: enhanced constant current source drive selection. It is valid when HDRV_EN is 1.

HDRV_SEL	Output Current (mA)	HDRV_SEL	Output Current (mA)
5'b00000	0.0	5'b10000	138.5
5'b00001	8.5	5'b10001	146.7
5'b00010	17.0	5'b10010	155.0
5'b00011	25.4	5'b10011	163.0
5'b00100	34.5	5'b10100	171.8
5'b00101	42.9	5'b10101	179.8
5'b00110	51.2	5'b10110	187.8
5'b00111	59.2	5'b10111	195.6
5'b01000	69.5	5'b11000	207.3
5'b01001	77.8	5'b11001	215.4
5'b01010	86.2	5'b11010	223.6
5'b01011	94.3	5'b11011	231.4
5'b01100	103.2	5'b11100	240.3
5'b01101	111.3	5'b11101	248.1
5'b01110	120.0	5'b11110	256
5'b01111	128.2	5'b11111	263.7

DRV_ENH: enhanced constant current source current reference enhancing enabling (enhance by 10%)

0: disable.

1: enable.

DRV_MAN_EN: constant current source current drive stage enabling.

0: disable.

1: enable.

PD_DRV: constant current source current reference circuit enabling.

0: enable.

1: disable.

8.8.2 CUS_AFE18: Constant Current Source Drive Control Register 2

Addr：0x11 Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	NDRV_SEL				NDRV_EN	HDRV_EN	LDO_PIR_OE
R/W	R/W				R/W	R/W	R/W

NDRV_SEL: normal constant current source drive selection. It is valid when NDRV_EN is 1.

NDRV_SEL	Output Current (mA)	NDRV_SEL	Output Current (mA)
4'b0000	0.0	4'b1000	22.0
4'b0001	2.8	4'b1001	24.8

NDRV_SEL	Output Current (mA)	NDRV_SEL	Output Current (mA)
4'b0010	5.6	4'b1010	27.6
4'b0011	8.4	4'b1011	30.4
4'b0100	11.3	4'b1100	33.3
4'b0101	14.1	4'b1101	36.0
4'b0110	17.0	4'b1110	38.8
4'b0111	19.7	4'b1111	41.5

NDRV_EN: normal constant current source drive selection.

0: disable.

1: enable.

HDRV_EN: enhanced constant current source drive selection.

0: disable.

1: enable.

LDO_PIR_OE: micro-power LDO_LPOA regulator output enabling control

0: disable. Disconnect the micro-power LDO_LPOA regulator output from the VREG_OUT/D3 pin.

1: enable. The micro-power LDO_LPOA regulator outputs voltage through the REG_OUT/D3 pin.

Notes:

1. *To use the VREG_OUT / D3 pin as an ordinary constant current source source driver output (ie D3 function), LDO_PIR_OE must be set to 0 and NDRV_EN is set to 1*
2. *To use VREG_OUT / D3 pin as VREG_OUT output (that is, LDO_LPOA regulator output), LDO_PIR_OE must be set to 1, and NDRV_EN must be set to 0.*

8.9 SNOOZE Configuration Register

8.9.1 CUS_SNOOZE1: SNOOZE Timer Configuration Register 1

Addr：0x1E Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SNOOZE_TIMER_M_SLEEP[7:0]							
R/W							

8.9.2 CUS_SNOOZE2: SNOOZE Timer Configuration Register 2

Addr：0x1F Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SNOOZE_UTH[9:8]		SNOOZE_DTH[9:8]		SNOOZE_TIMER_R_SLEEP[3:0]			
R/W		R/W		R/W			

SNOOZE_TIMER_M_SLEEP [7: 0], M value of sleep timing in SNOOZE mode, which meets the below calculation formula.

SNOOZE_TIMER_R_SLEEP [3: 0], R value of sleep timing in SNOOZE mode, which meets the below calculation formula.

In SNOOZE mode, the sleep time T_{SNOOZE} of the ADC meets the below calculation formula.

$$T_{\mathrm{SNOOZE}} = \mathrm{M} \times 2^{(R+1)} \times T_{CLK}$$

In above, T_{CLK} is provided by the system LFOSC module. By default, the LFOSC clock source comes from the internal LPOSC, namely, a 32 kHz low-power RC clock with T_{CLK} = 31.25 us. When the LFOSC module selects the external 32.768 kHz crystal oscillator, T_{CLK} is 30.5176us.

SNOOZE_UTH [9: 8]: the higher 2 bits of the 10-bit upper-limit interrupt threshold.

SNOOZE_DTH [9: 8]: the higher 2 bits of the 10-bit lower-limit interrupt threshold;

8.9.3 CUS_SNOOZE3: SNOOZE Upper-limit Threshold Register

Addr：0x20 Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SNOOZE_UTH[7:0]							
R/W							

SNOOZE_UTH[7:0]: the lower 8 bits of the 10-bit upper-limit interrupt threshold.

Note: In the SNOOZE mode, SNOOZE_UTH [9: 0] is both the threshold of the upper-limit interrupt and the upper-limit threshold of the window interrupt.

8.9.4 CUS_SNOOZE4: SNOOZE Lower-limit Threshold Register SNOOZE

Addr：0x21 Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SNOOZE_DTH[7:0]							
R/W							

SNOOZE_DTH [7:0]: the lower 8 bits of the 10-bit upper-limit interrupt threshold.

Note: In SNOOZE mode, SNOOZE_DTH [9: 0] is both the threshold of the lower-limit interrupt and the threshold of the window interrupt.

8.9.5 CUS_SNOOZE5: SNOOZE Interrupt Enabling and ADC Clock Frequency Selection Register

Addr：0x22　　Reset value: 0x40

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SAR_CKX		Reserved	Reserved	DWTH_WK_EN	UPTH_WK_EN	WOUT_WK_EN	WIN_WK_EN
R/W		--	--	R/W	R/W	R/W	R/W

SAR_CKX: ADC clock frequency selection.

- 2'b00: 0.5 MHz.
- 2'b01: 1.0 MHz.
- 2'b10: 1.5 MHz.
- 2'b11: 2.0 MHz.

DWTH_WK_EN: lower limit interrupt enable.

0: disabled.

1: enable, interrupt when SAR_DATA [11: 2] <SNOOZE_DTH.

UPTH_WK_EN: upper-limit interrupt enabling.

0: disable.

1: enable, interrupt when SAR_DATA [11: 2]> SNOOZE_UTH.

WOUT_WK_EN: enable out-of-window interrupts.

0: disabled.

1: enable, interrupt when SAR_DATA [11: 2]> SNOOZE_UTH [9: 0] or SAR_DATA [11: 2] <SNOOZE_DTH [9: 0].

WIN_WK_EN: enable in-window interrupts.

0: disable.

1: enable, generate an interrupt when SNOOZE_DTH [9: 0] <SAR_DATA [11: 2] <SNOOZE_UTH [9: 0].

8.9.6 CUS_SNOOZE6: SNOOZE Interrupt Flag Register

Addr：0x23　　Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GPIO_HOLD	Reserved			DWTH_WK_INT	UPTH_WK_INT	WOUT_WK_INT	WIN_WK_INT
R/W	R/W			R	R	R	R

DWTH_WK_INT: lower-limit interrupt flag.

0: no interrupt occurred.

1: generate an interrupt when SAR_DATA [11: 2] <SNOOZE_DTH [9: 0].

UPTH_WK_INT: upper-limit interrupt flag.

0: no interrupt occurred.

1: interrupt is generated when SAR_DATA [11: 2]> SNOOZE_UTH [9: 0].

WOUT_WK_INT: ou-of-window interrupt flag.

0: no interrupt occurred.

1: interrupt is generated when SAR_DATA [11: 2]> SNOOZE_UTH [9: 0] or SAR_DATA [11: 2] <SNOOZE_DTH [9: 0].

WIN_WK_INT: in-window interrupt flag.

0: no interrupt occurred.

1: generate an interrupt, that is, SNOOZE_DTH [9: 0] <SAR_DATA [11: 2] <SNOOZE_UTH [9: 0].

Note: The above settings of SNOOZE in ADC can be configured by calling the afe_snooze_setup_config function, with no need for operating each register one by one. For details of this API function, please refer to AN282 CMT216xA API Function Library User Guide.

8.10 CUS_SYSCTL3 : SNOOZE Mode Control Register

Addr：0x50　　Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LED_INV	AFE_IR_EN	SNOOZE_EN	SNOOZE_ DEBUG_EN	LFRX_DEBUG _EN	LFRX_EN	SLPT_WAKEUP _MODE	SLEEP_ TIME_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

AFE_IR_EN: in the SNOOZE mode, the constant current source drive synchronous pulse output is enabled
0: disable.
1: enable.

SNOOZE_EN: SAR-ADC SNOOZE operating mode enabling bit.
0: disable.
1: enable.

SNOOZE_DEBUG_EN: SAR-ADC SNOOZE simulation debug mode enable control bit
0: disable.
1: enable.

Notes:

1. *The function of AFE_IR_EN is to synchronize the constant current source drive pulse with the ADC sampling operating time window in SNOOZE mode, that is, in SNOOZE mode, when the ADC sampling operating window is valid, the constant current source drive operates accordingly. When the ADC sleeps, the constant current source drive stops accordingly.*
2. *SNOOZE_DEBUG_EN is used in 1-Wire simulation debugging mode. The method is, set this bit to 1 after the SNOOZE configurations are complete. Setting this bit to 1 will have no impact in normal operating mode.*

8.11 SNOOZE Interrupt Flag and Software Clearing Register

8.11.1 CUS_SYSCTL11: SNOOZE Interrupt Flag and Software Clearing Register

Addr：0x68　　Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SLPT_MAN U_RSTN	Reserved	Reserved	SNOOZE_M ANU_CLR	LBD_MANU_ CLR	LFRX_MANU_ CLR	SLPT_MANU_ CLR	BUT_MANU _CLR
R/W	R/W	R/W	W	W	W	W	W

SNOOZE_MANU_CLR:　SNOOZE interrupt waking-up flag clearing.
0: set to 0, invalid.
1: set to 1, clear the flag.

LBD_MANU_CLR:　LBD flag clearing.
0: set to 0, invalid.
1: set to 1, clear the flag.

8.11.2 CUS_SYSCTL12: SNOOZE Interrupt Waking-up Flag Register

Addr：0x69　　Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	SNOOZE_WAKEUP	Reserved	WKID_PASS	SYNC_PASS	LFRX_SIGNAL_OK	SLEEP_TIMESUP	KEY_LAUNCH
R	R	R	R	R	R	R	R

SNOOZE_WAKEUP: SNOOZE interrupt waking-up flag.

0: no interrupt

1: woken up by transmission interrupt.

8.12 ADC and LBD Register

8.12.1 CUS_SYSCTL13: ADC and LBD Control Register

Addr：0x6A　　Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LBD_STATUS	LBD_FINISH	LBD_AVG_SEL	LBD_ENABLE	SAR_DATA_UPDATE	SAR_MSTART	SAR_TRIGGER	SAR_CLK_EN
R	R	R/W	R/W	R	R/W	R/W	R/W

LBD_STATUS: low-voltage detection status flag

0: the power supply voltage is normal.

1: supply voltage is low.

LBD_FINISH: low-voltage detection or ADC calibration ending flag

0: not end.

1: end.

LBD_AVG_SEL: low-voltage detection or ADC calibration average selection.

0: average value of 8 successive voltage measurements or average value of 4 successive ADC calibrations.

1: once measurement.

LBD_ENABLE: low-voltage detection or ADC calibration enabling.

0: disable.

1: enable.

SAR_DATA_UPDATE: ADC conversion ending flag.

0: ADC conversion does not end.

1: ADC conversion ends. Note that this flag is automatically cleared by hardware after 3 ADC clock cycles have passed since it was generated.

SAR_MSTART: ADC continuous conversion software trigger.

0: no conversion is performed

1: continuous conversion is valid, ADC enters continuous conversion operating mode.

SAR_TRIGGER: ADC one-shot conversion software trigger

0: not perform conversion.

1: trigger ADC to perform a conversion.

SAR_CLK_EN: ADC clock enabling.

0: disable.

1: enable.

Notes:

1. The SAR_DATA_UPDATE bit has the same effect as the Bit7 of SAR_DATA_UPDATE of in the LED_CTL register in Bank0, Block1 area.

2. SAR_TRIGGER and SAR_MSTART cannot be set to 1 at the same time, as the one-shot operating mode and continuous conversion mode cannot be enabled at the same time.

8.12.2 CUS_SYSCTL14: ADC Data Register 1

Addr：0x6B Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SAR_DATA[11:4]							
R							

8.12.3 CUS_SYSCTL15: ADC Data Register 2

Addr：0x6C Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	Reserved	SAR_DATA[3:0]			
--	--	--	--	R			

SAR_DATA: 12-bit ADC conversion result

Notes: The ADC conversion result can be read either from the above 2 registers or by calling the API afe_read_sar_adc_data. For the API function, see AN282 CMT216xA API Function Library User Guide for more details.

8.12.4 CUS_SYSCTL16: LBD Threshold Register

Addr：0x6D Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LBD_TH[7:0]							
R/W							

8.12.5 CUS_SYSCTL17: LBD Result Register

Addr：0x6D Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LBD_RESULT[7:0]							
R							

In above, the low battery detection module uses VBG(1.2 V) as reference voltage. When setting LBD_TH or reading LBD_RESULT, it follows the below formulas.

$$\text{LBD\_TH} = \frac{V_{\text{LBD}_{TH}}}{4.8} \times 255$$

$$V_{BAT} = \frac{LBD\_RESULT}{255} \times 4.8V$$

8.13 CUS_SYSCTL19: Constant Current Source Drive Pulse Output Port Control Register

Addr：0x70　　Reset value: 0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LFRX_OSC_OUT_EN	IRLED_DOUT_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRLED_DOUT_EN: in the SNOOZE mode, the constant current source drive pulse (namely the ADC sampling operating window) output port enabling.

0: disable

1: enable. The synchronous pulse generated by hardware is output through the B5 port.

8.14 CUS_RESV5: LPOAs Non-inverting Input Port Configuration Register

Addr：0x7A Reset value: 0xC1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPOA0_PIN_DIS	LPOA1_PIN_DIS	WDT_REFRESH	WDT_START	WDT_RESET_TH[2:0]			WDT_DIS
R/W	R/W	R/W	R/W	R/W			R/W

LPOA0_PIN_DIS: LPOA0 non-inverting input port control.

0: LPOA0 non-inverting input port connects A6 port.

1: LPOA0 non-inverting input port disconnects with A6 port.

LPOA1_PIN_DIS: LPOA1 non-inverting input port control.

0: LPOA1 non-inverting input port connects B7 port.

1: LPOA1 non-inverting input port disconnects with B7 port.

9 Revise History

Table 11. Revise History Records

Version No.	Chapter	Description	Date
0.5	All	Initial version	2018/03/19
0.5B	All	Revision	2019/07/26

10 Contacts

CMOSTEK Microelectronics Co., Ltd. Shenzhen Branch
Address: 2/F Building 3, Pingshan Private Enterprise S.T. Park, Xili, Nanshan District, Shenzhen, Guangdong, China

Tel: +86-755-83231427
Post Code: 518057
Sales: sales@cmostek.com
Supports: support@cmostek.com
Website: www.cmostek.com