CMT83085 High Reliability Isolated Half- Duplex RS-485 Transceivers

1 Features

- Safety-related certifications
  - DIN VDE V 0884-11: 2017-01
  - UL recognition: up to 5000Vrms for 1 minute per UL1577
  - CSA component notice 5A
  - CQC approval per GB4943.1-2011
- Up to 5000Vrms Insulation voltage
- Bus side power supply voltage: 3.0V to 5.5V
- VDD1 supply voltage: 2.5 to 5.5 V
- High CMTI: ±200Kv/us
- High system level EMC performance:
- Bus Pins meet IEC61000-4-2±12 kV ESD
  - Other Pins meet ±7 kV contact ESD
  - Operation temperature: -40°C to 125°C
- Fail-safe protection receiver
- Slew rate limitation
- Robust isolation barrier life:
  - More than 40-year projected lifetime
- Up to 256 transceivers on the bus
- RoHS-compliant packages: SOIC 16 (wide body)

2 Applications

- Industrial automatic control
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

3 Description

CMT83085 is a high reliability isolated half duplex RS-485 transceiver based on CMOSTEK digital isolation technology. It is safety certified by UL1577 support 5kVrms insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption.

The Bus pins of CMT83085 is protected from ±12kV system level ESD to GND2 on Bus side. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

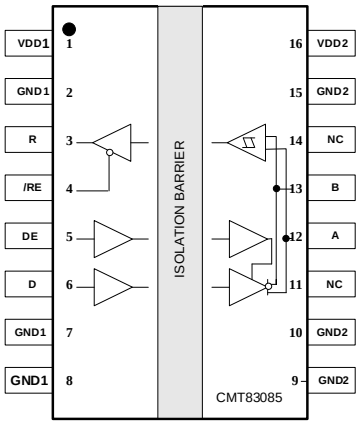
The data rate of CMT83085 is 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line.

The CMT83085 is available in wide-body (WB) 16-pin SOIC packages.

Device Information

Part No.	Package	Body Size (mm x mm)
CMT83085	WB(W) SOIC-16	10.4 x 7.5
Refer to section 12 for ordering information.		

Functional Block Diagram



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4 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameters	Symbol	Condition	Min.	Max.	Unit
Power supply voltage[2]	VDD_1, VDD_2		-0.5	6	V
Maximum input voltage	/RE, DE, TxD		-0.4	VDD+0.4	V
Common-mode transients	CMTI		200		kV/us
Driver Output/Receiver Input Voltage	VA, VB, VY, VZ		-7	12	V
Voltage input, transient pulses, A,B,Y and Z (through 100 Ω resistors)	V_{IT}		-50	50	V
Receiver output current	IO		-15	15	mA
Maximum surge isolation voltage	VIOSM			8	kV
Operating temperature	Topr		-40	125	℃
Storage temperature	T_{STG}		-40	150	℃
Electrostatic discharge	HBM (Bus pins and GND)			±8000	V
	HBM (All pins)			±6000	V
	CDM			±2000	V

5 Pin Description

The pin list is shown as below.

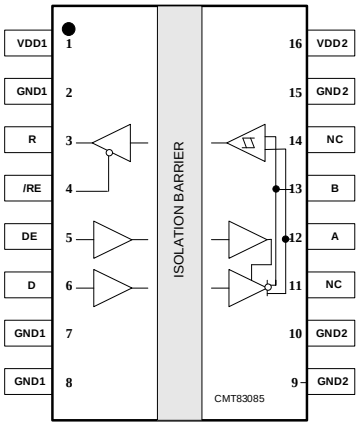


Figure 1. CMT83085 Pin List

Table 2. CMT83085 Pin Description

Symbol	Pin No. CMT83085	Description
VDD1	1	Power Supply for Isolator Side 1
GND1	2	Ground reference for Isolator Side 1
R	3	Receive output
/RE	4	Receive enable input. It is low level input.
DE	5	Driver enabled input. It is high level input
D	6	Driver transmitting data input.
GND1	7,8	Ground reference for Isolator Side 1
GND2	9,10,15	Ground reference for Isolator Side 2
NC	11,14	No Connection.
A	12	Non-inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD1 or VDD2 is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
B	13	Inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD1 or VDD2 is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
VDD2	16	Power Supply for Isolator Side 2

6 Typical Application

6.1 Typical Application Schematic

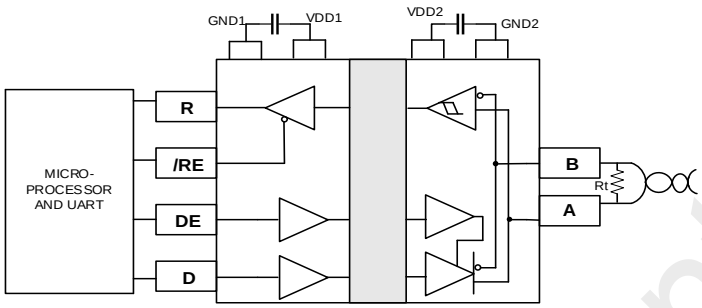
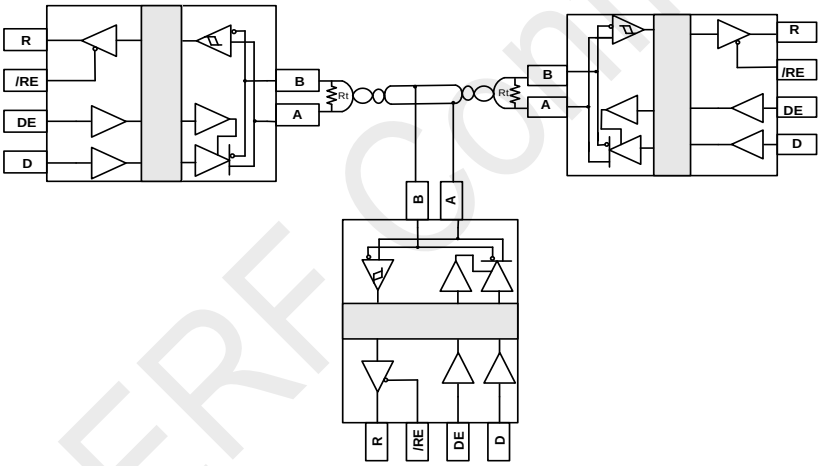


Figure 2. Typical Application Circuit



Note: Rt is a special matching impedance with typical value of 120 Ω.

Figure 3. Typical Isolated Half-duplex RS-485 Application

6.2 PCB Layout Guidelines

The CMT83085 requires a 0.1 μF bypass capacitor between VDD1 and GND1, 10uF bypass capacitor between VDD2 and GND2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

6.3 ESD Protecion

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handing and assembly. The Bus pins have extra protection against static electricity to both the logic side (VDD1 side) and bus side (VDD2 side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices. Bus pins:

- ± 8 kV HBM.
- ±12 kV using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±6 kV HBM.
- ±7 kV using the Contact Discharge method specified in IEC 61000-4-2

6.4 256 Transceivers on the Bus

The devices have a 1/8 unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

7 Parameter Measurement Circuit Setup

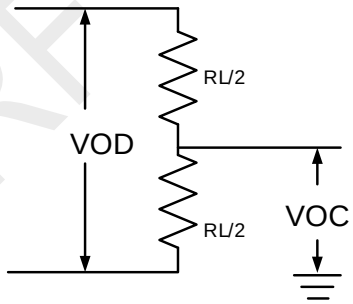


Figure 4. Driver DC Test Load

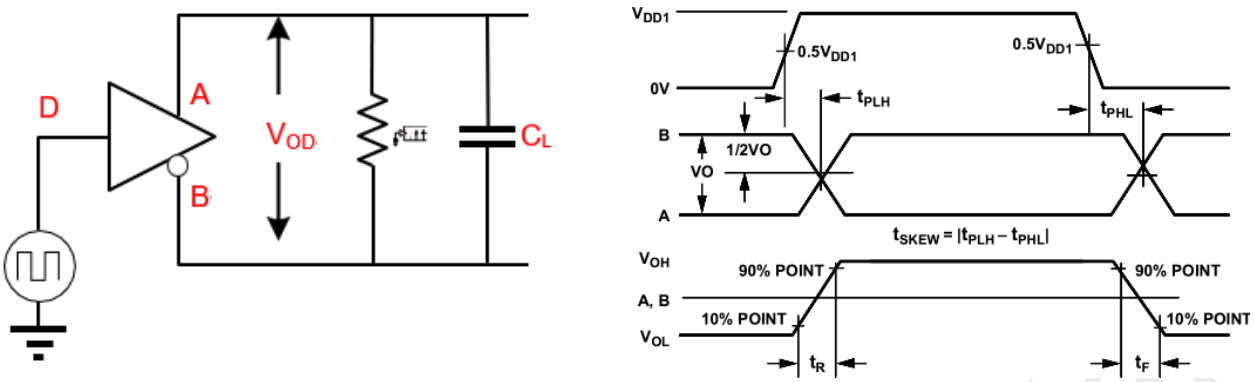


Figure 5. Driver Timing Test Circuit and Waveform

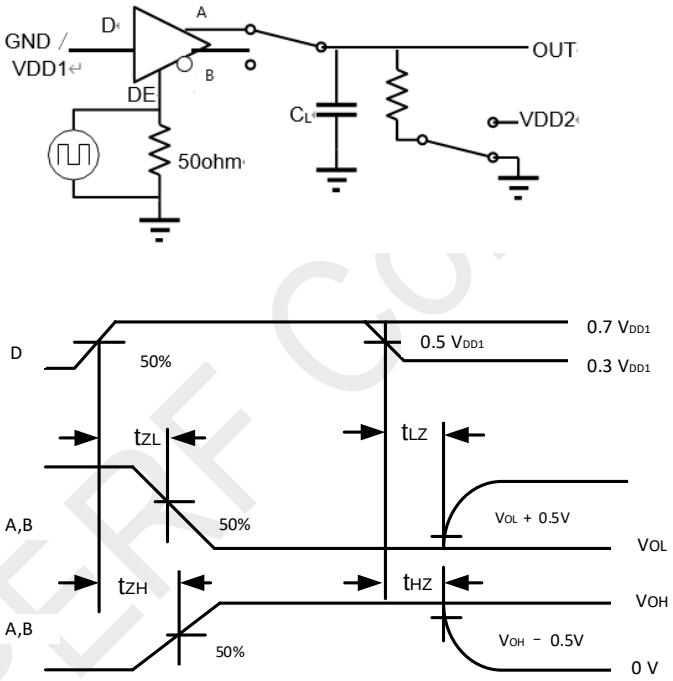


Figure 6. Driver Enable Disable Timing Test Circuit and Waveform

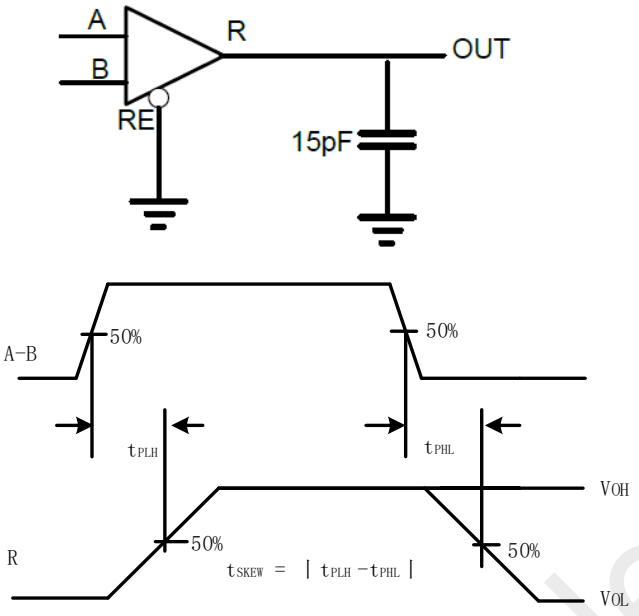


Figure 7. Receiver Propagation Delay Test Circuit and Waveform

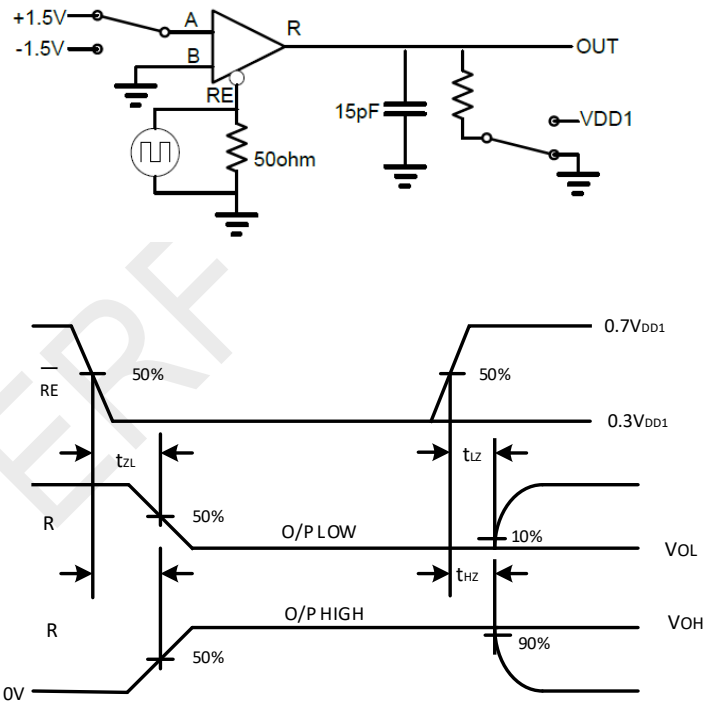


Figure 8. Receiver Enable Disable Timing Test Circuit and Waveform

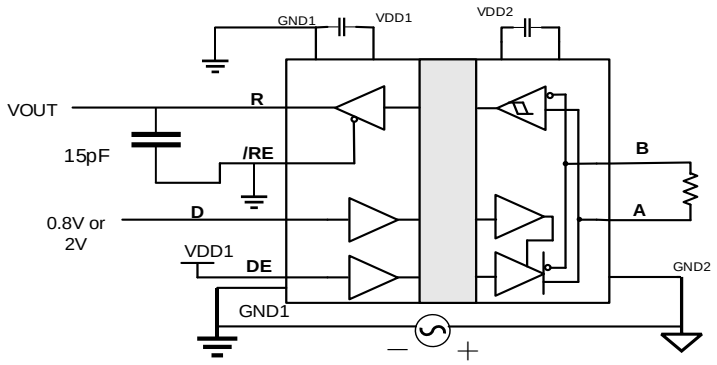


Figure 9. Common-Mode Transient Immunity Test Circuit

8 Specifications

8.1 DC Electrical Characteristics

VDD1 =2.5V~5.5V, VDD2= 3.0V~5.5V, T_A= -40 to 125 ℃. Unless otherwise noted, typical values are at VDD1=5V, VDD2=5V, T_A=25 ℃.

Table 3. Electrical Characteristics

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD1}		2.5		5.5	V
	V_{DD2}		3.0		5.5	V
Logic side supply current	I_{DD1}	VDD_1 = 5 V, DE = high, /RE = D = low, no load		2.85	5.2	mA
		VDD_1 = 3 V, DE = high, /RE = D = low, no load		2.81	5	
Bus side supply current	I_{DD2}	VDD_1 = 5 V, DE = high, /RE = D = low, no load		2.1	5	mA
		VDD_1 = 5 V, DE = high, /RE = D = low, no load		2.12	4.5	
Thermal-shutdown Threshold	T_{TS}			145		℃
Thermal-shutdown Hysteresis	T_{TSH}			15		℃
Common Mode Transient Immunity	CMTI			±200		kV/us
Logic Side						
High level input voltage	V_{IH}	DE, D		1.65		V
		/RE		0.8		
Low level input voltage	V_{IL}	DE, D, /RE		1.65		V
		/RE		0.8		
Input threshold	V_{IT}	Input Threshold at rising edge		1.65		V
	V_{IT_HYS}	Input Threshold Hysteresis		0.2		
Input Pull up Current	I_{PU}	DI/RE			10	uA

Input Pull down Current	I_{PD}	DE	-10			uA
Output Voltage High	V_{OH}	I_{OH} = -4mA	V_{DD1}- 0.3			V
Output Voltage Low	V_{OL}	I_{OL} = 4mA			0.3	V
Output Short-Circuit Current	I_{OSR}	0 ≤ V_R ≤VDD_1			109	mA
Three-State Output Current	I_{OZ}	0 ≤ V_R ≤ VDD_1, /RE = high	-15			uA
Input Capacitance	C_{IN}	DE, D, /RE		2		pF
Driver						
Differential output voltage	| V_{OD} |	VDD=5V, TXD=0, R_{load} = 60Ω	2.4		VDD2	V
		R_L=100Ω (RS-422)	3		VDD2	
		R_L=54Ω (RS- 485)	2.2		VDD2	
Change in magnitude of the differential output voltage	Δ|V_{OD} |	R_L=100Ω or R_L=54Ω			0.2	
Common-Mode Output Voltage	| V_{OC} |	R_L=100Ω or R_L=54Ω		VDD_2/2	2.8	
Change in Magnitude of Common-Mode Voltage	Δ|V_{OC} |	R_L=100Ω or R_L=54Ω			0.2	V
Driver Short-Circuit Output Current	I_{OSD}	0 ≤ V_{OUT} ≤ +12 V			100	mA
		−7V ≤ V_{OUT} ≤ VDD_2	-100			
Receiver						
Input Current (A and B)	I_A , I_B	DE=GND, VDD_2=GND or VDD_2, V_{IN}=12V			80	uA
		DE=GND, VDD_2=GND or VDD_2, V_{IN}=-7V	-60			
Receiver Differential Threshold Voltage	V_{TH}	−7V ≤ V_{CM} ≤ 12V	-200	-125	-50	mV
Receiver Input Hysteresis	$ΔV_{TH}$	V_A+V_B=0		40		mV
Receiver Input Resistance	R_{IN}	−7V ≤ V_{CM} ≤ 12V, DE=low	96kΩ			

8.2 Switching Electrical Characteristics

VDD1 = 2.5V ~ 5V, VDD2 = 2.5V~5.5V, TA= -40 to 85℃. Unless otherwise noted, Typical values are at VDD1= 5V，VDD2 = 5V，TA = 25℃）

Table 4. Switching Electrical Characteristics

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Driver						
Maximum Data Rate	f_{MAX}				12	Mbps
Driver Propagation Delay	t_{PLH}			11.5	50	ns
	t_{PHL}			13.2	50	ns
Driver Pulse Width Distortion, |t_{PHL}– t_{PLH} |	PWD			1	10	ns

Driver Output Falling Time or Rising time	t_F			1.7	16	ns
	t_R			1.8	16	
Driver Enable to Output High	t_{ZH}			30	60	ns
Driver Enable to Output Low	t_{ZL}			30	60	ns
Driver Output High to Disable	t_{HZ}			18	60	ns
Driver Output Low to Disable	t_{LZ}			12	60	ns
Receiver						
Maximum Data Rate	f_{MAX}				12	Mbps
Receiver Propagation Delay	t_{PLH}	C_L=15pF		90	200	ns
	t_{PHL}	C_L=15pF		75	200	
Receiver Pulse Width Distortion	PWD	C_L=15pF		3	20	ns
Receiver Output Falling Time or Rising time	t_F	C_L=15pF		4.5	6	ns
	t_R	C_L=15pF		4.5	6	
Receiver Enable to Output High	t_{ZH}	R_L=1kΩ，C_L=15pF		30	80	ns
Receiver Enable to Output Low	t_{ZL}	R_L=1kΩ，C_L=15pF		30	80	ns
Receiver Disable to Output High	t_{HZ}	R_L=1kΩ，C_L=15pF		18	60	ns
Receiver Disable to Output Low	t_{LZ}	R_L=1kΩ，C_L=15pF		12	60	ns

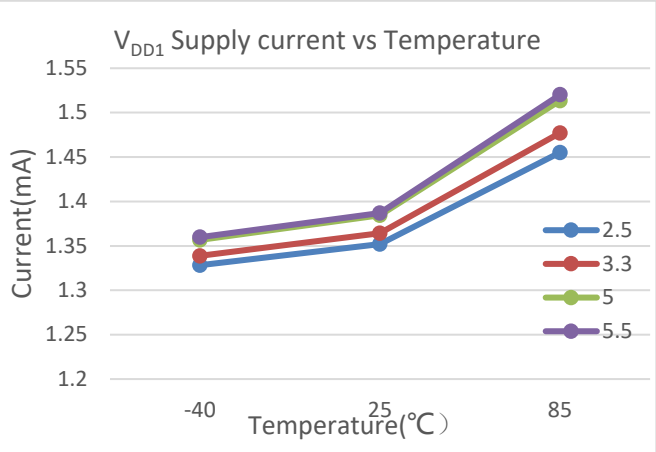
8.3 Insulation Specifications

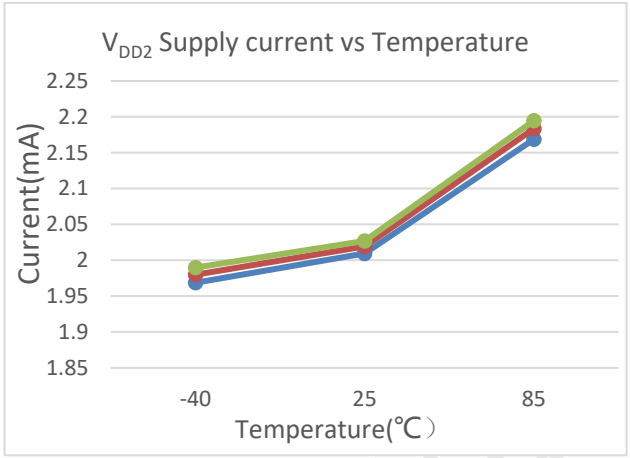
Table 5. Insulation Specifications

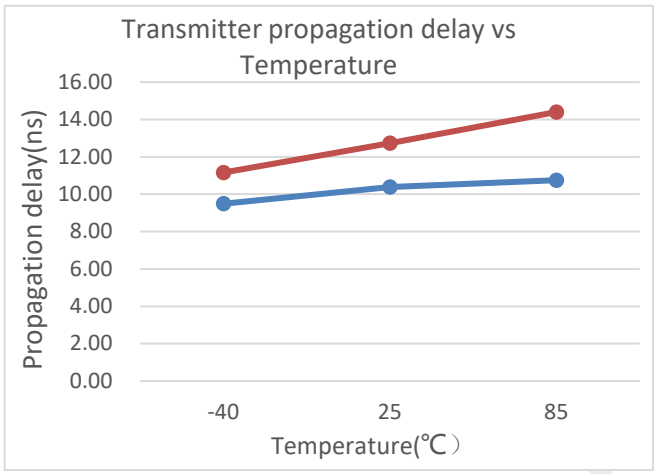
Parameters	Sym.	Condition	Value	Unit
External clearance[1]	CLR	The shortest terminal-to-terminal distance through air	8.0	mm
External creepage[1]	CRP	The shortest terminal-to-terminal distance across the package surface	8.0	mm
Distance through insulation	DTI	Minimum internal gap	26	um
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	V
Material group	-		II	-
DIN VDE V 0884-11:2017-01[2]				
Voltage Classification as standard of IEC 60664-1		For Rated Mains Voltage ≤ 150Vrms	Ⅰ to Ⅳ	
		For Rated Mains Voltage ≤ 300Vrms	Ⅰ to Ⅳ	

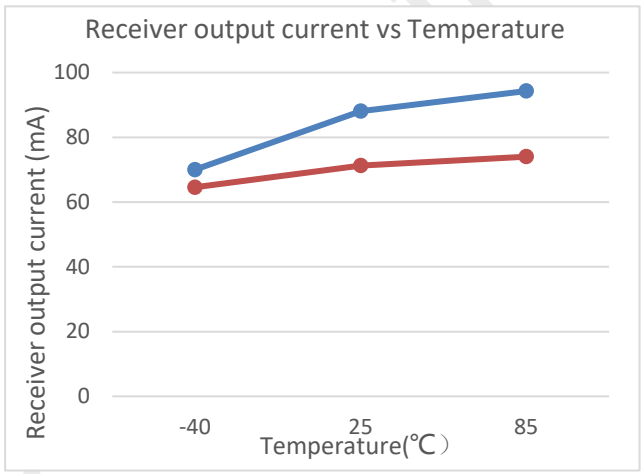
		For Rated Mains Voltage ≤ 300Vrms	Ⅰ to Ⅳ	
Pollution Degree per DIN VDE 0110			2	
Maximum repetitive isolation voltage	V_{IORM}		1414	V_{pk}
Maximum working insulation voltage	V_{IOWM}	AC voltage (sine wave); Dielectric layer breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{pk}
Maximum transient isolation voltage	V_{IOTM}	VTEST = VIOTM, t = 60 s (certified); t = 1 s (100% production)	7000	V_{pk}
Maximum surge isolation withstand voltage [3]	V_{IOSM}	According to the IEC60065 test, 1.2/50 us waveform, VTEST = 1.6 x VIOSM (certified)	7000	V_{pk}
Apparent electric charge [4]	q_{pd}	Method a：after the security test subgroup, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.2 × VIORM, tm = 10 s	<5	pC
		Method a：after the environmental test subgroup1, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.6 × VIORM, tm = 10 s	<5	
		Method b1：General test (100% production) and preconditioning (test style) Vini = VIOTM, tini = 1 s; Vpd(m) = 1.875 × VIORM, tm = 1 s	<5	
Insulation capacitance, from input to output [5]	C_{IO}	f = 1 MHz	0.8	pF
Isolation resistor, from input to output[5]	R_{IO}	V_{IO} = 500 V	$>10^9$	Ω
Input capacitance	C_I		2	pF
Total power consumption at 25 ° C	Ps		1499	mW
Secure input, output, or supply current	I_S	θ_{JA} = 140 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C		mA
Isolation resistance, from input to output [5]	R_{IO}	θ_{JA} = 84 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	237	Ω
Temperature	Ts		150	℃

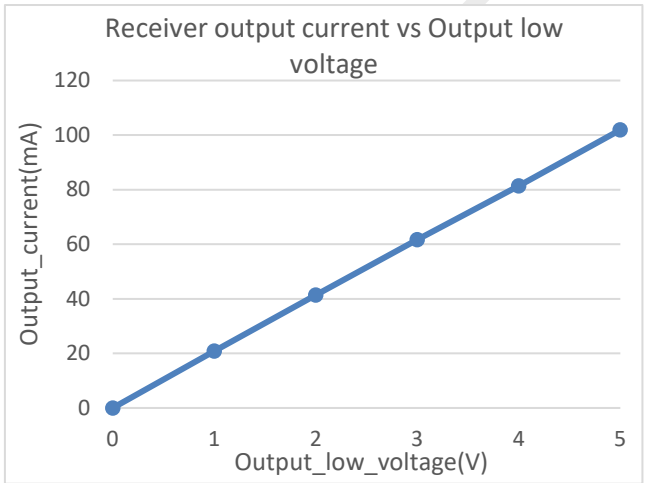
8.4 Typical Performance

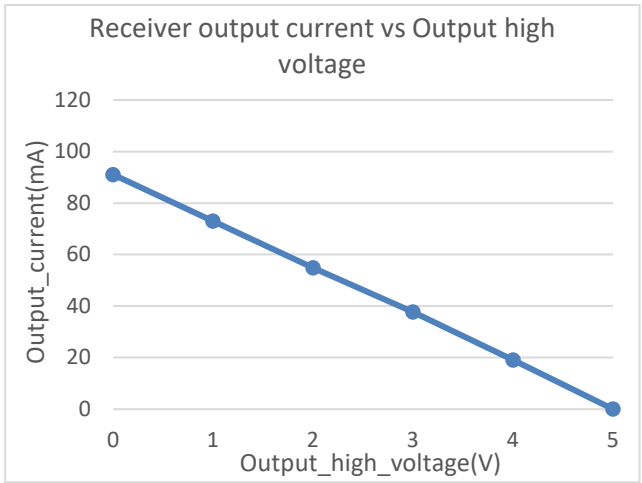

V_{DD1} Supply current vs Temperature
Current(mA)
1.55
1.5
1.45
1.4
1.35
1.3
1.25
1.2
-40
25
85
Temperature(℃)
2.5
3.3
5
5.5


V_{DD2} Supply current vs Temperature
Current(mA)
2.25
2.2
2.15
2.1
2.05
2
1.95
1.9
1.85
-40
25
85
Temperature(℃)


Transmitter propagation delay vs Temperature
Propagation delay(ns)
16.00
14.00
12.00
10.00
8.00
6.00
4.00
2.00
0.00
-40
25
85
Temperature(℃)


Receiver output current vs Temperature
Receiver output current (mA)
100
80
60
40
20
0
-40
25
85
Temperature(℃)


Receiver output current vs Output low voltage
Output_current(mA)
120
100
80
60
40
20
0
0
1
2
3
4
5
Output_low_voltage(V)


Receiver output current vs Output high voltage
Output_current(mA)
120
100
80
60
40
20
0
0
1
2
3
4
5
Output_high_voltage(V)

9 Safety-related Certifications

Table 6. Safety-related Certifications

VDE	UL		CQC
DIN VDE V0884-11:2017-01	UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	GB 4943.1-2011
Certificate number: pending	Certificate number: UL-US-2439077-1	Certificate number: UL-CA-2429797-0	Certificate number: pending

10 Function Description

10.1 Function Overview

CMT83085 is a high reliability isolated half duplex RS-485 transceiver. Data isolation is achieved using Cmostek integrated capacitive isolation that allows data transmission between the logic side and the Bus side. CMT83085 is safety certified by UL1577 support 5kVRMS insulation withstand voltages.

10.2 Data Rate

The data rate of CMT83085 is 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line.

10.3 True Fail-safe Receiver Inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -50mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage (VA-VB) is greater than or equal to -50mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

10.4 Truth Tables

Table 7. Driver Function Table[1]

V_{DD1}	V_{DD2}	Input (D)	Enable Input (DE)	Output (OUTx)	
				A	B
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

Table 8. Reciever Function Table

V_{DD1}	V_{DD2}	Differential Input (V_A-V_B)	Enable Input (/RE)	Output(R)
PU	PU	⩾-50mV	L/Open	H
PU	PU	⩽-200mV	L/Open	L
PU	PU	OPEN/SHORT	L/Open	H
PU	PU	X	H	Z

PU	PU	IDLE	L	H
PD	PU	X	X	Z
PU	PD	X	X	H
PD	PD	X	X	Z
1. PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.				

10.5 Thermal Shutdown

The device is protected from over temperature damage by integrated thermal shutdown circuitry. When the junction temperature (TJ) exceeds +165°C (typ), the driver outputs go high-impedance. The device resumes normal operation when TJ falls below +145°C (typ).

11 Packaging Information

The packaging information of the CMT83085 SOIC16 is shown in the figures below.

11.1 CMT83085 Wide Body SOIC-16 Packaging

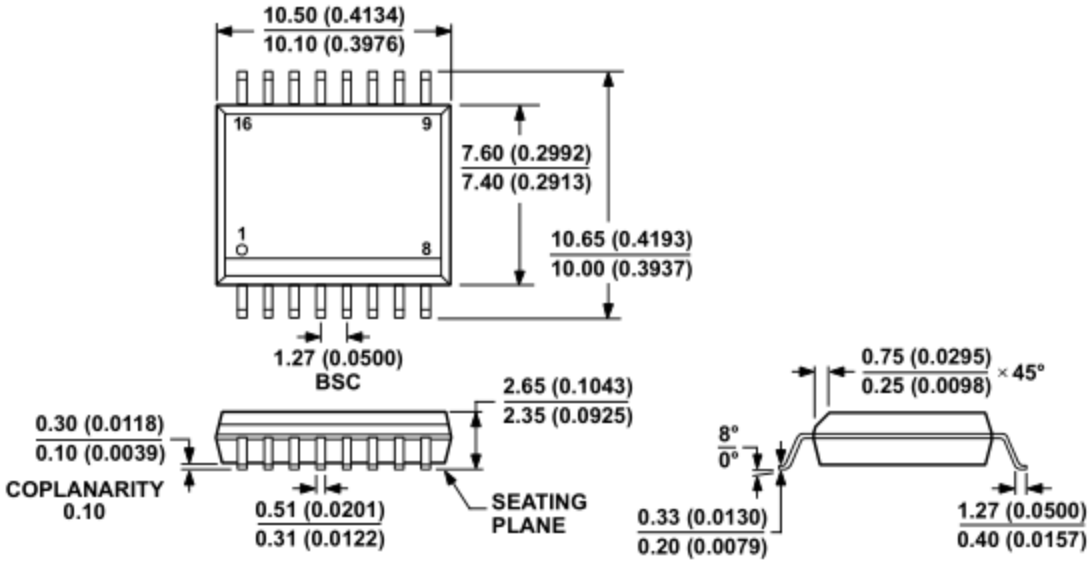


Figure 10. Wide Body SOIC-16 Packaging

Table 9. Wide Body SOIC-16 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	0.20	0.30
A2	2.25	2.30	2.35

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A3	1.00	1.05	1.10
b	0.35	0.37	0.43
c	0.15	0.20	0.30
D	10.30	10.40	10.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.14	1.27	1.40
L	0.65	0.70	0.85
L1		1.40	
θ	0	-	8°

12 Ordering Information

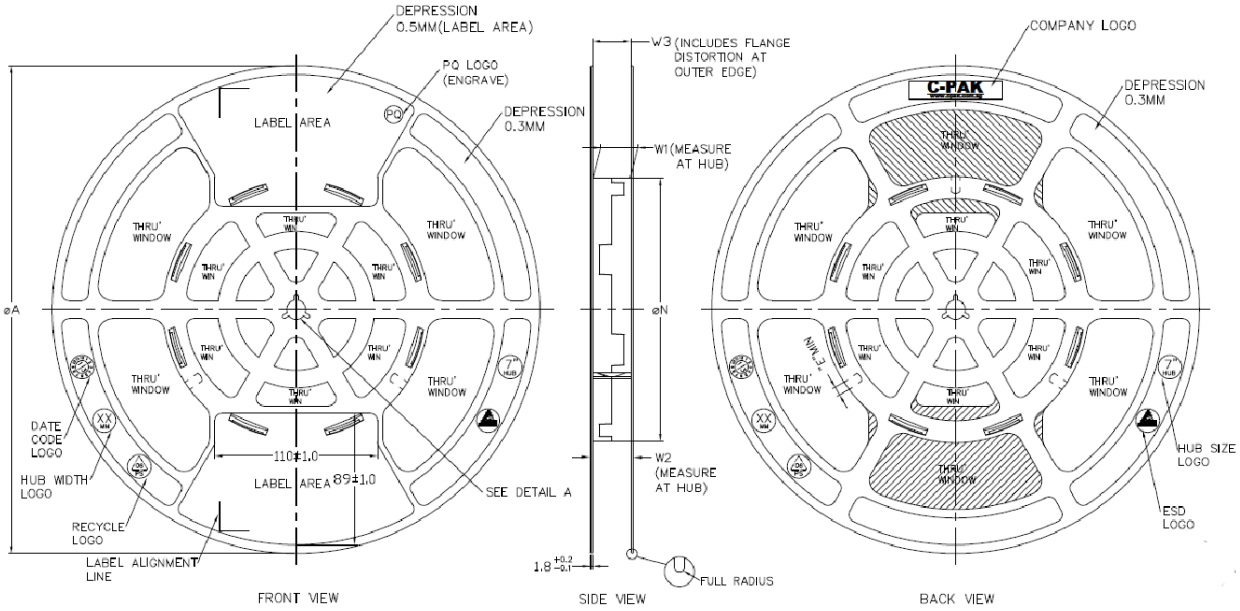
Table 10. Part Number List

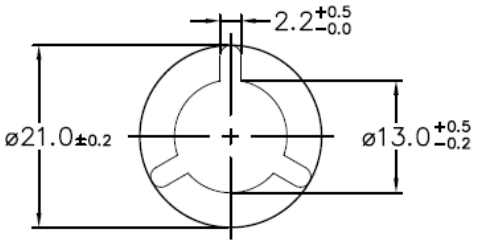
Part Number	MOQ	Isolation Rating (kV)	Duplex	Number of nodes	Max Data Rate (Mbps)	Temperature Range	Package	MSL
CMT83085	1000	5	Half	256	12	-40 to 125℃	WB SOIC-16	3

Please visit www.hoperf.com for more product/product line information.

Please contact sales@hoperf.com or your local sales representative for sales or pricing requirements.

13 Tape and Reel Information

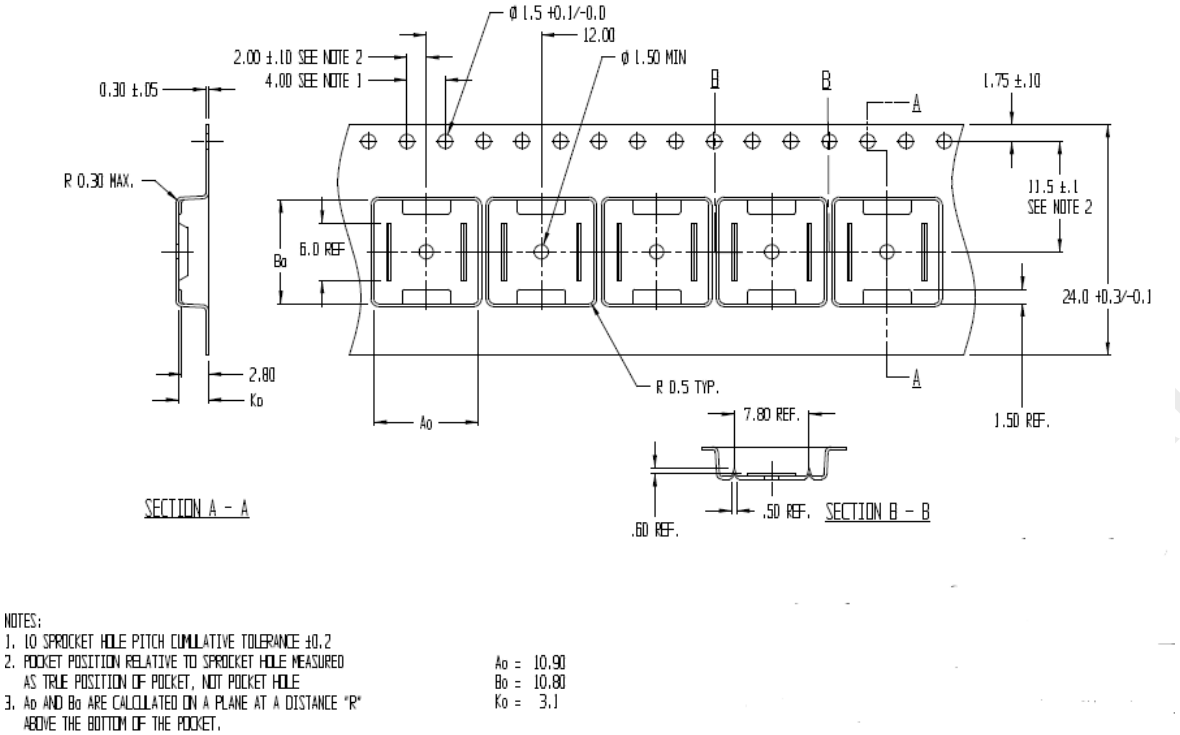




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Ao = 10.90
Bo = 10.80
Ko = 3.1

Figure 11. CMT83085 WB SOIC-16 Tape and Reel Information

14 Revise History

Table 11. Revise Records

Version No.	Chapter	Description	Date
0.1	All	Initial version	2023/11/14
0.2	7	Update Figure 6/7/8 in chapter 7	2023/12/12
0.3	All	Update circuit specification	2024/1/28
0.4	All	Update current of V_{DD1}	2024/3/21
0.5	All	Add MSL in order information	2024/12/3

15 Contacts

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