CMT2189B User Guideline

Summary

CMT2189B is a low power, high performance, Flash-based, OOK RF transmitter chip.It covers the 240MHz - 960MHz wireless communication band. This chip is embedded with RISC Flash type MCU. It belongs to the CMOSTEK NextGenRF™ series product.The product series includes the short range wireless communication chips, such as transmitter, receiver, transceiver, SoC and so on.

The part numbers covered by this document are as shown below.

Table1. Part Numbers Covered by This Document

Part No.	Frequency	Modem	Tx Power	Tx Current	Configuration	Package
CMT2189B	240 - 960MHz	OOK	+13dBm	17.5mA	Embedded MCU	SOP14

Note: The test condition for the Tx power and Tx current is at 433.92MHz. CW mode is always in the Tx carrier mode. The Tx current is about 8.5mA according to the Tx mode of Duty 50%.

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1 Chip Architecture Introduction

1.1 Overall Operation Principle

CMT2189B is a digital and analog integrated RF transmiter chip. It is applied with the crystal oscillator to provide the reference frequency and digital clock for PLL, supports the OOK modulation that the data rate is from 1Kbps to 40Kbps, and supports the status control based on the MCU programming. It is suitable for all kinds of low power transmission applications.

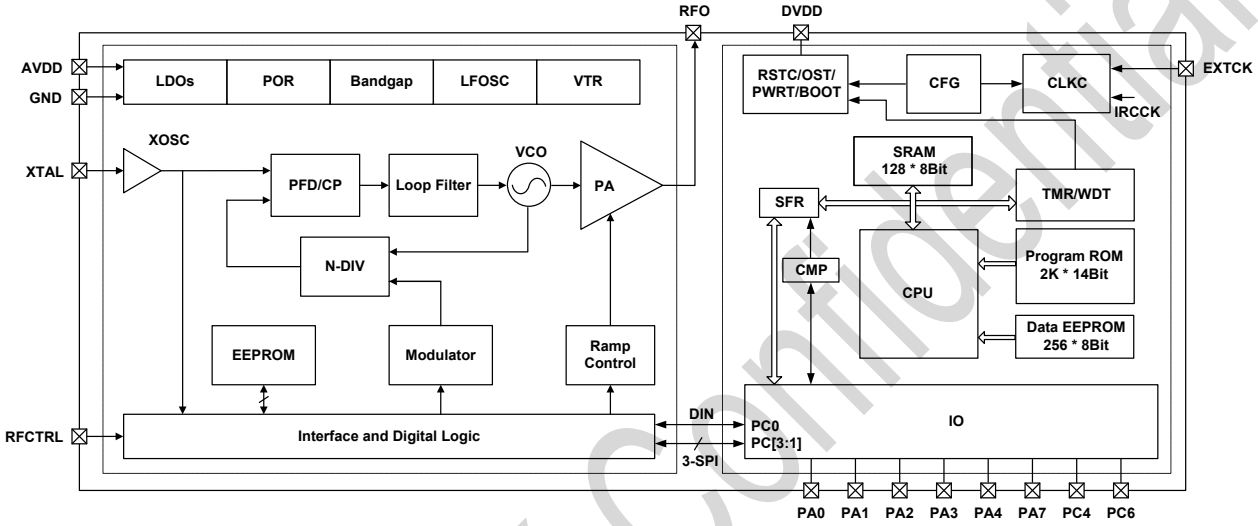


Figure 1-1. CMT2189B System Architecture

The chip adopts the PLL+PA architecture to achieve the Sub-GHz wireless transmission function. It supports the packet FIFO mode and Direct mode (The embedded encoder in the Packet FIFO mode can select the appropriate encoding format). The processed data is sent to the modulator (For the Direct mode, they are not processed by the encoder, and directly deburred, and then sent to the modulator), the modulator controls PLL and PA, and the data is modulated by OOK and transmitted out.

The MCU of the chip controls the RF part by the 3-wire SPI interface, and achieves various status switching, mode selection and low power control.

1.2 IO Pin Description

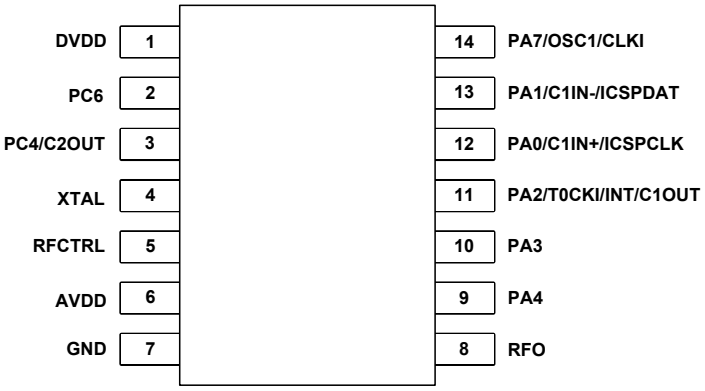


Figure 1-2. CMT2189B Pin Top View

Table 1-2. CMT2189B SOP14 Package Pin Description

Pin No.	Name	Type	I/O	Function Description	
1	DVDD	Digital	I	Chip power supply positive pole	
2	PC6	Digital	IO	General IO	
3	PC4/C2OUT	Digital	IO	PC4	General IO
				C2OUT	Comparator2 output
4	XTAL	Analog	I	RF part crystal oscillator input	
5	RFCTRL	Digital	I	RF part SPI interface enable control bit, active low, internal pull-up	
6	AVDD	Analog	I	RF part power supply positive pole	
7	GND	Digital	--	Chip power supply ground	
8	RF0	Analog	O	RF part PA output	
9	PA4	Digital	IO	General IO, support IOC, can be configured as pull-up	
10	PA3	Digital	IO	General IO, support IOC, can be configured as pull-up	
11	PA2/T0CKI/INT/C1OUT	Digital	IO	PA2	General IO, support IOC, can be configured as pull-up
				T0CKI	Timer0 clock source input (Max=4MHz)
				INT	External interrupt input
				C1OUT	Comparator1 output
12	PA0/C1IN+/ICSPCLK	Digital	IO	PA0	General IO, support IOC, can be configured as pull-up
				C1IN+	Comparator1 input+
				ICSPCLK	Debug/ burning mode serial port Clock signal
13	PA1/C1IN-/ICSPDAT	Digital	IO	PA1	General IO, support IOC, can be configured as pull-up
				C1IN-	Comparator1 input -

Pin No.	Name	Type	I/O	Function Description	
				ICSPDAT	Debug/ burning mode serial port Data signal
14	PA7/OSC1/CLKI	Digital	IO	PA7	General IO, support IOC, can be configured as pull-up
				OSC1	MCU Crystal pin
				CLKI	External clock input pin
Internal pin	PC0/C2IN+/RFDIN	Digital	IO	PC0	General IO
				C2IN+	Comparator2 input +
				RFDIN	Data input pin in the RF direct mode
Internal pin	PC1/C2IN-/SDIO	Digital	IO	PC1	General IO，it is connected to the RF part inside the chip.
				C2IN-	Comparator2 output -
				SDIO	RF Part 3-wire SPI serial bus data SDIO, SDIO itself has no pull-up or pull-down resistance, it is a bi-directional port.
Internal pin	PC2/SCLK	Digital	IO	PC2	General IO，it is connected to the RF part inside the chip.
				SCLK	RF Part 3-wire SPI serial bus clock SCLK
Internal pin	PC3/CSB	Digital	IO	PC3	General IO，it is connected to the RF part inside the chip.
				CSB	RF 3-wire SPI serial bus chip selection bar CSB, with internal pull-up resistor.

Note:

1. The two comparators are integrated within the MCU, but the internal comparator can not be used because they have the package terminals and some of them are reused to the RF part at the same time.However, in the initialization process, MCU needs to turn off the comparator function and set its corresponding pin as the digital IO, to avoid affecting the work of other functions.

2. The clock source system of MCU supports the internal oscillation and the external oscillation. The external oscillation supports the dual-end crystal and the single-end clock source input. However, due to the limitation of the package pin, the PA6 has no the package terminal, so the external oscillation mode of the dual-end crystal is not supported, which only supports the external oscillation mode of the single-end clock source.

3. PC<3:0> is the internal control pin of the chip and not the package terminal, but it is used as a bus to control the RF.

2 RF Configuration and Control Mechanism

2.1 Work Mode

There are two working modes for the OOK Tx function of CMT2189B.

- Simple work mode: the default entry mode on Power-up, that is, the non configuration mode, only supports the Direct Tx mode in this mode.
- Advanced configuration mode: the mode of configuring registers and controlling the working state through the SPI bus, which supports the FIFO and the Direct mode.

Note: the direct Tx input source in the two work modes is different, and the following is described in detail.

2.2 Simple Work Mode

In the simple work mode, the peripheral only needs to match a crystal oscillator. After power-up, the chip controls the transmitted data through the internal PC1 (SDIO), and then to realize the transmission of the corresponding frequency. In this mode, the frequency doubling coefficient is fixed to 16.5, which is the following formula:

$$F_{XTAL} = \frac{F_{RF}}{16.5},\ 314\ MHz \le F_{RF} \le 480\ MHz$$

Among them, FXTAL is the crystal frequency and FRF is the target frequency, and the frequency range is 314MHz ~ 480MHz.

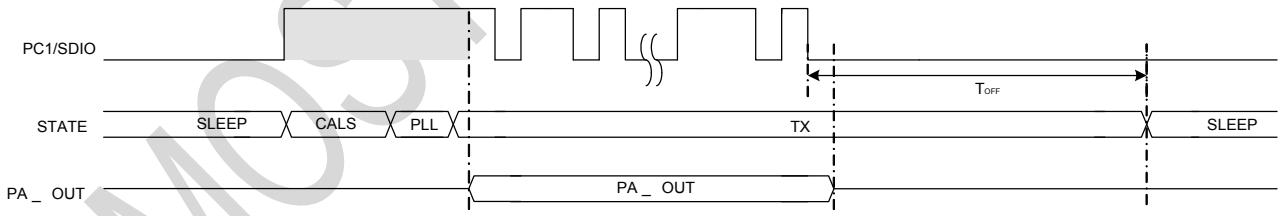


Figure 2-1. Tx Timing Diagram in the Simple Work Mode

Note:

1. This mode supports the rate of 1Kbps to 20Kbps.
2. The maximum power output is fixed to +13dBm. When the user needs to reduce the Tx power, he can only connect the current limiting resistor before the Chock inductor.
3. The internal SPI bus does not need to send any control commands and only needs to hold PC<3:0> in a high resistance input status (except PC1).
4. The RFCTRL pin can be suspended in this mode.
5. In this mode, the transmitted data pin is PC1(SDIO), which is set to 0 in the low power consumption

status(that is normal). When the transmission is needed, the rising edge is triggered to enter the transmission status. After transmitting, PC1 is set to 0 and lasts more than 20ms (T_{OFF} time), and RF automatically exit from the Tx mode to enter the low power consumption status.

6. In this mode, the low power internal pin processing, PC1/SDIO is set to 0 output, PC2/SCLK, PC3/CSB, and PC0/RFDIN are set to high resistance input.

2.3 Advanced Configuration Mode

When users need to achieve more functions and higher performance, such as: the target working frequency is 868MHz, the chip automatically sends packets in the transmission process, and so on, and they need to use the advanced configuration mode. In this mode:

- Select more frequency multiplication ratio coefficients to achieve the frequency range coverage of 240MHz ~ 960MHz.
- Release the MCU to do more work (In the Direct mode, this process takes up the MCU resource) by filling the FIFO and automatically sending the message (repeatedly, multiply and periodically).
- Support the more accurate Tx rate, and the accuracy is determined by the crystal. It is quite accurate (in the Direct mode, the speed is controlled by the MCU software, and the accuracy depends on the software and internal RC).
- Support the voltage detection function inside the RF, and realize the simple power supply voltage detection and analysis judgment processing.
- Adjust the Tx power dynamically according to the power supply voltage, so as to save the power and prolong the battery life.

In this mode, the internal MCU of the chip can control the mode of RF part operation register through 3-wire SPI (PC3/CSB, PC2/SCLK, PC1/SDIO), and to achieve the two Tx modes.

1. Hardware packet Tx mode that fill FIFO through SPI (see Section 2.9 in detail)

The contents that need to be transmitted are filled into the specified registers, which are automatically transmitted according to the speed, coding mode, number of packets and packet interval, etc. (The data package format and other relevant information are detailed in Section 2.7 of this chapter).

2. Direct Tx mode that PC0/RFDIN is as the data pin(see Section 2.10 in detail)

That is, the 1-Pin Tx mode, the data stream is generated by the MCU, and the output is carried out by the specified pin to achieve the most basic work mode of "data entry and antenna out".

Note:

1. The two Tx modes mentioned above are all under the advanced configuration mode, that is, configuring and operating the chip through SPI.
2. In the advanced configuration mode, RFCTRL needs to be controlled, that is to say, the RFCTRL needs to be controlled by other pins, so the RFCTRL can not be suspended.
3. The Direct mode which is supported by the advanced configuration mode is similar to the Direct mode of the simple work mode, by which is controlled by one data pin, but the data input source is different. In the

simple work mode, the Tx input pin is PC1/SDIO, while in the advanced configuration mode, it is changed to PC0/RFDIN because PC1/SDIO is the serial data line of SPI. Of course, the Direct mode in the advanced configuration mode can support more frequency selection and power selection than in the simple mode.

2.4 SPI Interface Timing

The RF function inside the chip is controlled by the 3-wire SPI, and the corresponding relationship to the IO of the MCU part is as follows:

Table 2-1. The Relationship between SPI Bus and Control Port

3-wire SPI	MCU Control Port	Function
CSB	PC3	Bus chip selection bar, enabled low, built-in pull-up.
SCLK	PC2	Bus clock line, rising edge trigger
SDIO	PC1	Bus bi-directional data

Note: SDIO, a bi-directional port, used for input and output data. Both the address and the data section are transmitted from the MSB.

When the RF part is accessed, RFCTRL is pulled down [*], the SPI serial port function is enabled, then the chip selection bar (PC3/CSB) is pulled down, a R/W bit is sent, and followed by a 7-bit register address. After the chip selection bar (PC3/CSB) is pulled down, it is necessary to wait for at least half a PC2 (SCLK) cycle to start sending R/W bit.After sending the falling edge of the last PC2 (SCLK), the chip must wait for at least half a SCLK cycle, and then pull the PC3 (CSB) high.

In the SPI read operation below, pay special attention to PC1/SDIO, because SDIO is a bi-directional port.SDIO will switch from the input state to output state on the eighth clock falling edge (middle dotted line in the figure below), and SDIO needs to switch from the output state to input state before the eighth clock falling edge.

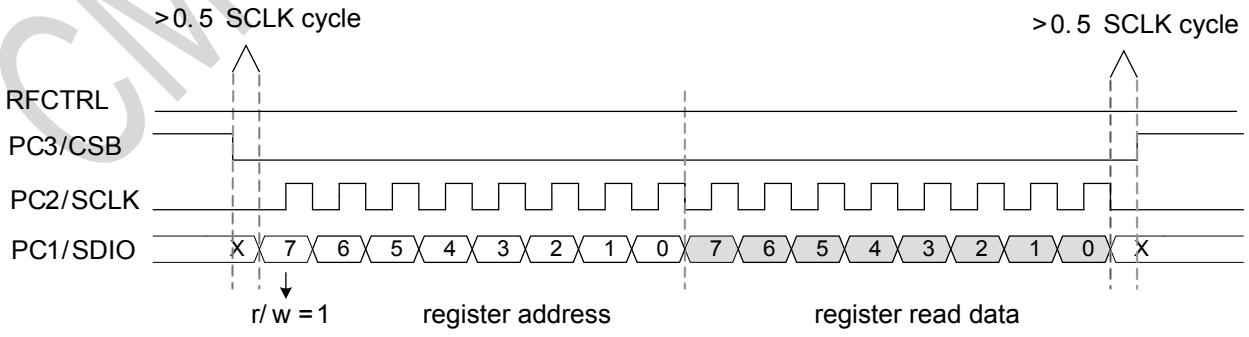


Figure 2-2. SPI Read Register Timing

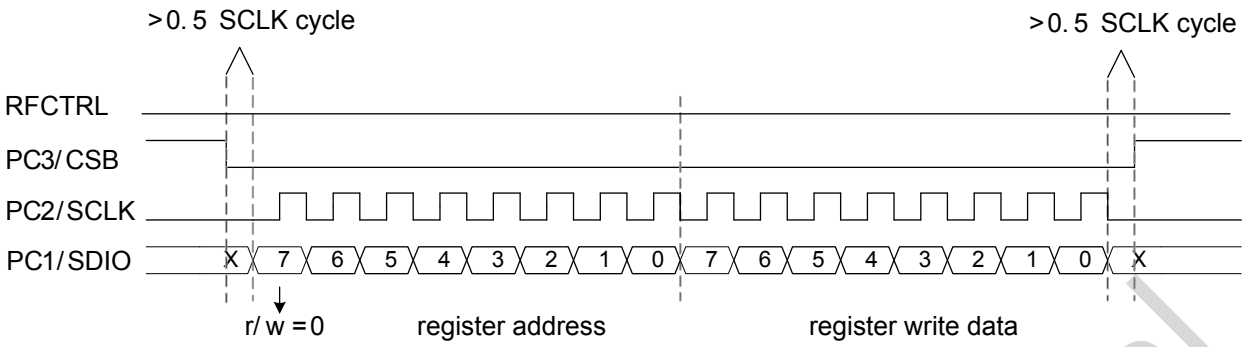


Figure 2-3. SPI Write Register Timing

Note: RFCTRL is the input port and needs the external control. It is recommended that users control it by any function port in CMT2189B, and pull it down to enable the SPI interface function. In the whole process, RFCTRL can hold low, but in the low power sleep mode, need to set the RFCTRL pin of MCU to a high impedance input, because RFCTRL internal pull-up can pull the level high. Do not set the MCU pin to low output, because the pull-down can generate the power consumption.

2.5 RF Configuration Parameter

CMT2189B operates in the advanced configuration mode, which can achieve more wide working frequency, packet format, and other functions. These functions need corresponding configuration parameters, which can be exported by RFPDK software. The specific approach is to open the RFPDK software and select the CMT2157B model (the same specifications and performance as the CMT2189B built-in RF), as shown in the following figure.

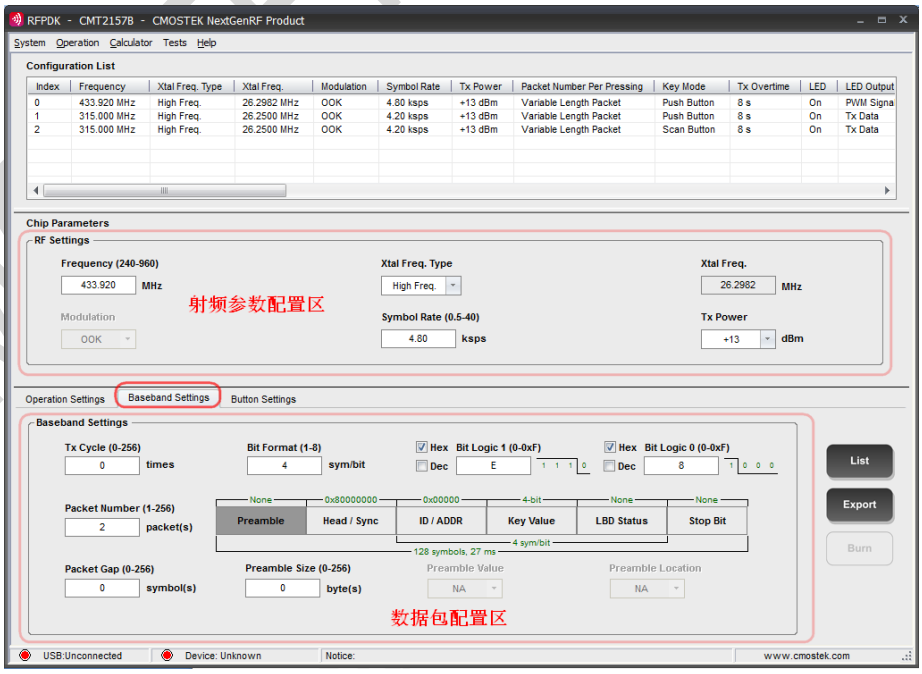


Figure 2-4. RFPDK CMT2157B Interface

On the interface, there are mainly two zones: RF parameter settings zone and data packet settings zone. Users configuration are based on the requirements according to the relevant registers below, and then click Export to generate an exp file, which is as follows:

```
;---------------------------------------
;   CMT2157B Configuration File
;   Generated by CMOSTEK RFPDK 1.46
;   2017.11.14 13:47
;---------------------------------------
;   (The annotation with ";" in the middle is omitted.)
;---------------------------------------
;   The following are the EEPROM contents
;---------------------------------------
0x7E4F
0x2134
0x017F
0x8015
0x0018
0x7F00
0x0000
0x8000
0x0000
0x0000
0xA073
0xE080
0x2010
0x8040
0x5030
0x6090
0xC0A0
0x0000
0x0100
0x027C
0x957B
0x70F0
0x0083
0x0000
;---------------------------------------
;   The following is the CRC result for
;   the above EEPROM contents
;---------------------------------------
0xEDFA
;---------------------------------------
```

; The following are for CMOSTEK
; use, customers can ignore them
;----------
0x0000
0x0018

Among them, the red font part is the specific configuration content, they are all 16-bit word, a total of 24 words, so users need to convert the 16-bit word to the 8-bit register content. The method of conversion is that the higher 8-bit of each 16-bit word is an odd number address, and the lower 8-bit is an even address. The 24 words conversion gets 48 register configuration values, and the address range is 0x00 to 0x2E (the last 8-bit is invalid). According to the above file, the contents of the register are as follows:

Table 2-2. Conversion Table from 16-bit EEPROM Word to 8-bit Register Content

16-bit Word	Register Address	8-bit Register Configuration Value
0x7E4F	0x00	0x4F
	0x01	0x7E
0x2134	0x02	0x34
	0x03	0x21
0x017F	0x04	0x7F
	0x05	0x01
0x8015	0x06	0x15
	0x07	0x80
0x0018	0x08	0x18
	0x09	0x00
0x7F00	0x0A	0x00
	0x0B	0x7F
0x0000	0x0C	0x00
	0x0D	0x00
0x8000	0x0E	0x00
	0x0F	0x80
0x0000	0x10	0x00
	0x11	0x00
0x0000	0x12	0x00
	0x13	0x00
0xA073	0x14	0x73
	0x15	0xA0
0xE080	0x16	0x80
	0x17	0xE0
0x2010	0x18	0x10

16-bit Word	Register Address	8-bit Register Configuration Value
	0x19	0x20
0x8040	0x1A	0x40
	0x1B	0x80
0x5030	0x1C	0x30
	0x1D	0x50
0x6090	0x1E	0x90
	0x1F	0x60
0xC0A0	0x20	0xA0
	0x21	0xC0
0x0000	0x22	0x00
	0x23	0x00
0x0100	0x24	0x00
	0x25	0x01
0x027C	0x26	0x7C
	0x27	0x02
0x957B	0x28	0x7B
	0x29	0x95
0x70F0	0x2A	0xF0
	0x2B	0x70
0x0083	0x2C	0x83
	0x2D	0x00
0x0000	0x2E	0x00

The user only needs to write the above contents to the 0x01～0x2E register address through SPI write timing.

2.6 Configuration Register

The above exported configuration parameter address from 0x01 to 0x2E can be divided into three banks according to the functions, which are as follows:

Table 2-3. Configuration Register Bank Partition Table

Bank	Address	Involved Content
Tx Bank	0x00 – 0x03	Tx frequency,Tx power
Packet Bank	0x04 – 0x27	Tx rate, packet format (only for hardware packet Tx mode）
System Bank	0x28 – 0x2E	System working parameters

- **Tx Bank**

The register address range associated with the Tx bank parameter is 0x00~0x03. These parameters are mainly about Tx central frequency and Tx power. Therefore, when users need to transmit multiple frequencies in the application, such as frequency hopping, or adjusting the Tx power according to the voltage value, they can export different parameter tables by setting in the RFPDK, and only need to take 0x00~0x03 segment. So there is no detailed description about each register meaning in this part.

- **Packet Bank**

The register address range associated with the packet bank parameters is 0x04~0x27. These parameters are mainly setting items of the hardware packet format, and also applicable to the hardware packet Tx mode. For the meaning of the specific registers, please read Section 2.7 in this chapter.

- **System Bank**

The register address range associated with the system bank parameters is 0x28~0x2E. These parameters are the specific parametersof RF, and are not related to user applications. Users need not pay attention to them, only need to configure them according to the parameters exported from RFPDK, so they are also not discussed in detail here.

2.7 Packet Bank Register

The overview of the packet bank register is shown below.

Table 2-4. Packet Bank Register Overview Table

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	CUS_DIG1	SYMBOL_TIME<7:0>							
0x05	CUS_DIG2	SYMBOL_TIME<15:8>							
0x06	CUS_DIG3			LBD_TH<3:0>				LBD_OUT_EN	LBD_ON
0x07	CUS_DIG4					DEGLITCH_EN	TX_OVERTIMES<2:0>		
0x08	CUS_PKT1	TCYCLE_EN	INTERVAL_EN	STOP_EN	KEY_EN	SYNC_EN	PREAMBLE_LOCATION	PREAMBLE_SEL	PREAMBLE_EN
0x09	CUS_PKT2	TXCYCLE<7:0>							
0x0A	CUS_PKT3	PREAMBLE_LENGTH<7:0>							
0x0B	CUS_PKT4	KEY_LENGTH<2:0>				SYNC_LENGTH<4:0>			
0x0C	CUS_PKT5	SYNC_HEADER<7:0>							
0x0D	CUS_PKT6	SYNC_HEADER<15:8>							
0x0E	CUS_PKT7	SYNC_HEADER<23:16>							
0x0F	CUS_PKT8	SYNC_HEADER<31:24>							
0x10	CUS_PKT9	ADDR_ID<7:0>							
0x11	CUS_PKT10	ADDR_ID<15:8>							
0x12	CUS_PKT11	ADDR_ID<23:16>							
0x13	CUS_PKT12	ADDR_ID<31:24>							
0x14	CUS_PKT13	BIT_FORMAT<2:0>				ADDR_LENGTH<4:0>			
0x15	CUS_PKT14					STOP_LENGTH<3:0>			

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x16	CUS_PKT15	BIT_LOGIC_L<7:0>							
0x17	CUS_PKT16	BIT_LOGIC_H<7:0>							
0x18	CUS_PKT17	KEY<7:0>							
0x19 ~ 0x21	CUS_PKT18 ~ CUS_PKT26								
0x22	CUS_PKT27	STOP_BIT_L<7:0>							
0x23	CUS_PKT28	STOP_BIT_H<15:8>							
0x24	CUS_PKT29	INTERVAL_LENGTH<7:0>							
0x25	CUS_PKT30	PKT_NUM<7:0>							
0x26	CUS_RESV1								
0x27	CUS_RESV2							INTERVAL_STBY_DIS	STBY_PLLOFF_DIS

Note:

1. The gray area indicates that users do not need to understand, and is not without content. Users only need to configure them according to the parameters exported from RFPDK, and users can set the individual bit to 1 or 0 by the "read-modify-write" process.
2. The blue area indicates that users need to know, and the following will explain them one by one.
3. The CMT2189B built-in packet structure pattern is the same as CMT2157B.The user can select the packet structure in the CMT2157B configuration interface through RFPDK, and generate the “exp” parameter and configure them in the order of parameters.In the software implementation process, the user only needs to fill the specific data content.

2.7.1 Tx Rate

The Tx rate is determined by SYMBOL_TIME<15:0> and can be generated by RFPDK.

Register Name	Bits	R/W	Bit Name	Function description
CUS_DIG1 (0x04)	7:0	RW	SYMBOL_TIME<7:0>	Packet format Tx data rate
CUS_DIG2 (0x05)	7:0	RW	SYMBOL_TIME<15:8>	

2.7.2 Hardware Packet Format

The interior of the CMT2189B supports the hardware packet structure, and its data frame structure is as follows:

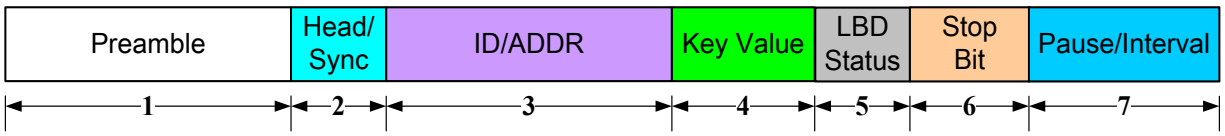


Figure 2-5. Packet Structure

In the packet structure figure above, there are 7 main parts:

1. Preamble： Preamble code, optional, the value can be selected as 0x55 or 0xAA[1], range from 0~256 Bytes, arbitrary selection;
2. Head/Sync： Synchronous word, optional, range from 0~32 bits[2], arbitrary selection;
3. ID/ADDR： Sequence number, must be selected, range from 1~32 logic bits[3], arbitrary selection;
4. Key Value： Key value, optional, range from 0~8 logic bits[3], arbitrary selection;
5. LBD Status： Low battery detection status bit, optional, onlyone logic bit [3];
6. Stop Bit： Stop bit, optional, range from 0~16 bits[2], arbitrary selection;
7. Pause/Interval： Packet interval, fixed to send"0", range from 0~256 bits[2];

Note:

[1]. The preamble code does not need to be encoded, that is, using the NRZ format, such as the selection of 0x55, the data flow is 0b01010101 according to the setting rate (0 represents low level, 1 represents high level).

[2]. Head/Sync, Stop Bit and Pause/Interval all do not need to be encoded and output according to the setting rate, just like the preamble code.

[3]. The logic bit represents the encoded bit, which is described in detail below; the number 3~5 of the message structure above all support the internal encoder for coding.

For example, the coding rules choose one symbol as one logical bit at least, that is, 0b0 is logic 0, and 0b1 is logic 1 (NRZ encoding), sets as following:

Preamble： Set to open, the value is 0xAA, the length is 5 Bytes;
Head/Sync： Set to open, the value is 0x2DD4, the length is 2 Bytes;
ID/ADDR： The value is 0x12345678, the length is 4 Bytes;
Key Value： The value is 0x9A;
LBD Status： Set to close
Stop Bit： Set to open, the value is 0xBCDE, the length is 16 bits (2 Bytes);
Pause/Interval： Pause/Interval: set to open, the length is 32 bits (4 Bytes);
Then the data flow is as follows:
0xAA AA AA AA AA 2D D4 12 34 56 78 9A BC DE 00 00 00 00 AA AA AA AA AA 2D D4 12 34 56 78 9A BC DE 00…

2.7.3 Preamble

Table 2-5. Preamble Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	2	RW	PREAMBLE_LOCATION	When enabling Tcycle, it represents the Preamble location in the packet structure: 0：In one cycle, each packet contains 1

Register Name	Bits	R/W	Bit Name	Function Description
				Preamble, i.e. there are N packets in the 1 cycle, which contain N Preambles. 1：In one cycle, only contains 1 Preamble, and it is only in the first packet. Note: The concept of Tcycle is described in detail later.
	1	RW	PREAMBLE_SEL	Preamble Select bit: 0：0x55 1：0xAA
	0	RW	PREAMBLE_EN	Preamble Enable bit: 0：Disable 1：Enable
CUS_PKT3 (0x0A)	7:0	RW	PREAMBLE_LENGTH<7:0>	The length of Preamble can be configured to be 0~255, and 0 represents that sending 1 Byte of Preamble, and so on, and 255 represents that sending 256 Bytes of Preamble.

For the user, if the PREAMBLE_EN is 0, the Preamble is not sent, and if the configuration is 1, the Preamble of 1-256 Bytes is sent.

2.7.4 Head/Sync

Table 2-6. Head/Sync Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	3	RW	SYNC_EN	Sync Enable bit： 0：Disable 1：Enable
CUS_PKT4 (0x0B)	4:0	RW	SYNC_LENGTH<4:0>	The Sync length can be configured to 0~31, 0 represents that sending 1 Symbol of Sync, and so on, 31 represents that sending 32 Symbols of Sync, and the Symbol is random in length.
CUS_PKT5 (0x0C)	7:0	RW	SYNC_HEADER<7:0]>	The value of the Sync can be filled in different registersaccording to the different SYNC_LENGTH settings, please look at the next table.
CUS_PKT6 (0x0D)	7:0	RW	SYNC_HEADER<15:8>	
CUS_PKT7 (0x0E)	7:0	RW	SYNC_HEADER<23:16>	
CUS_PKT8 (0x0F)	7:0	RW	SYNC_HEADER<31:24>	

Table 2-7. The Relationship Between Head/Sync Length Selection and Register

	SYNC/HEADER			
SYNC_LENGTH	<31:24>	<23:16>	<15:8>	<7:0>
0~7	√			
8~15	√	√		
16~23	√	√	√	
24~31	√	√	√	√

The position of the tick in the table indicates the register to be filled. For example, if SYNC_LENGTH is set to 15, that is, the length is 16 Symbols, Sync value is 0x5678, then the user will fill the value into SYNC_HEADER<31:24> and SYNC_HEADER<23:16> registers, MSB is corresponds to the thirty-first bit, LSB is corresponding to the sixteenth bit, that is, 0x56 is filled into SYNC_HEADER<31:24> and 0x78 is filled into SYNC_ HEADER<23:16>. For the user, if the Sync Enable bit is 0, the Sync is not sent, and if the Sync Enable bit is 1, the Sync of 1-32 Symbols is sent.

2.7.5 Addr/ID

Table 2-8. Addr/ID Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT13 (0x14)	4:0	RW	ADDR_LENGTH<4:0>	The Addr ID length can be configured to 0~31, and 0 represents that sending the Addr of 1 Logic bit, and so on, 31 represents that sending the Addr of 32 Logic bits, and the Logic bit length is random.
	7:5	RW	BIT_FORMAT<2:0>	The number of Symbol that is contained by 1 Logic bit can be configured to 0~7, 0 represents 1 Symbol, and so on, and 7 represents 8 Symbols.
CUS_PKT15 (0x16)	7:0	RW	BIT_LOGIC_L<7:0>	Logic 0 definition
CUS_PKT16 (0x17)	7:0	RW	BIT_LOGIC_H<7:0>	Logic 1definition
CUS_PKT9 (0x10)	7:0	RW	ADDR_ID<7:0>	Addr ID value
CUS_PKT10 (0x11)	7:0	RW	ADDR_ID<15:8>	
CUS_PKT11 (0x12)	7:0	RW	ADDR_ID<23:16>	
CUS_PKT12 (0x13)	7:0	RW	ADDR_ID<31:24>	

Table 2-9. The Relationship Between Addr/ID Length Selection and Register

	ADDR_ID			
ADDR_LENGTH	[31:24]	[23:16]	[15:8]	[7:0]
0~7	√			
8~15	√	√		
16~23	√	√	√	
24~31	√	√	√	√

The position of the tick in the table indicates the register to be filled. For example, If ADDR_LENGTH is set to 15, the length is 16 Logic bits, the value is 0x5678, then the user will fill the value into ADDR_ID<31:24> and ADDR_ID<23:16> registers, MSB is corresponding to the thirty-first bit, LSB is corresponding to the sixteenth bit, that is , 0x56 is filled into ADDR_ID<31:24>, 0x78 is filled into ADDR_ID<23:16>.

Table 2-10. The Corresponding Relationship Between the Encoding Length Selection and the Bit Enabling

	BIT_LOGIC_L/ BIT_LOGIC_H							
BIT_FORMAT	7	6	5	4	3	2	1	0
0	√							
1	√	√						
2	√	√	√					
3	√	√	√	√				
4	√	√	√	√	√			
5	√	√	√	√	√	√		
6	√	√	√	√	√	√	√	
7	√	√	√	√	√	√	√	√

The location of the tick in the table indicates the corresponding value of register to be filled. For example, if BIT_FORMAT is set to 3, i.e. 1 Logic bit contains 4 Symbols, if Logic 0= 0b'1000', then the user will fill the value into BIT_LOGIC_L<7:4>, if Logic 1= 0b'1110', then the user will fill the value into BIT_LOGIC_H<7:4>, MSB is corresponding to the seventh bit, LSB is corresponding to the fourth bit.

The above examples are combined. If ADDR_LENGTH is set to 20, ADDR_ID<31:12> is 0x56789, BIT_FORMAT is set to 4, BIT_LOGIC_L<7:4> is 0b '1000', BIT_LOGIC_H<7:4> is 0b '1110', ADDR_ID is expanded to Symbol, then the Tx data is as follows:

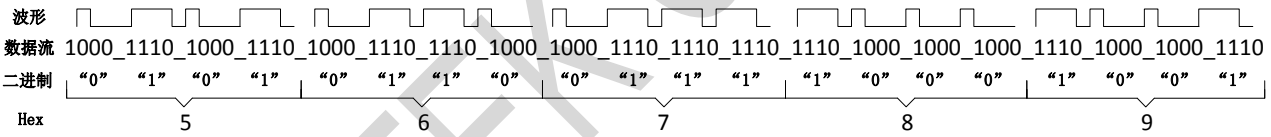


Figure 2-6. ADDR ID Example Diagram

That is, ID/ADDR = 0h '8E8E_8EE8_8EEE_E888_E88E', a total of 80 Symbols, transmitting from the high bit.

2.7.6 Key Value

Table 2-11. Key Value Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	4	RW	KEY_EN	Key Enable bit 0：Disable 1：Enable
CUS_PKT4 (0x0B)	7:5	RW	KEY_LENGTH<2:0>	The Key Value length can be configured to 0~7, and 0 represents sending the Key of 1 Logic bit, and so on, 7represents sending the Key of 8 Logic bits, and the Logic bit length is random.

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT17 (0x18)	7:0	RW	KEY<7:0>	Key Value

The maximum length of the corresponding Key Value in the packet structure can be configured to 8, and the location of the tick in the table indicates the corresponding value of register to be filled. For example, if the KEY_LENGTH is set to 3, that is, the length is four Logic bits and the value is 0x5, the user will fill the value into KEY0<7:4>. As for configuring Logic bit as Symbol, please refer to the description of Addr ID.

Table 2-12. The Corresponding Relationship Between the Key Value Length Selection

	KEY Value							
KEY_LENGTH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	√							
1	√	√						
2	√	√	√					
3	√	√	√	√				
4	√	√	√	√	√			
5	√	√	√	√	√	√		
6	√	√	√	√	√	√	√	
7	√	√	√	√	√	√	√	√

For the user, if the KEY_EN is 0, the Key Value is not sent, and if the configuration is 1, the Key Value of the 1-8 Logic bits is sent.

2.7.7 LBD Status Configuration

Table 2-13. LBD Status Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_DIG3 (0x06)	0	RW	LBD_ON	LBD（Low Battery Detection）Enable bit： 0：Disable 1：Enable
	1	RW	LBD_OUT_EN	LBD Output Enable bit（Whether or not it is added to the message） 0：Disable 1：Enable
	5:2	RW	LBD_TH<3:0>	The voltage comparison threshold of the LBD, if the actual voltage is greater than the threshold, the LBD result is 1 (logic 1), and conversely, it is 0 (logic 0).
CUS_LBD_RESULT (0x4B)	3:0	R	LBD_RESULT<3:0>	Voltage measurement value

Note: CUS_LBD_RESULT register is a function register, not the parameter register exported through the RFPDK, see the Section 2.8 in details.

The working principle of LBD is that the voltage value LBD_TH set by the user is the threshold of LBD, then comparing the actual value LBD_RESULT got by the test with LBD_TH, if it is smaller than LBD_TH, then the low voltage has occurred, on the contrary, the voltage is normal. According to the comparison result, the LBD indicating signal will be output internally. If configuring LBD_OUT_EN as 1, then the LBD result will be sent out as part of the packet, and see the Section 2.7.1" Packet Structure" in details.

In the chip, the voltage value is converted by 4bits's ADC. The LBD_RESULT is obtained by each step of 0.2V, and the relationship between the voltage value and LBD_RESULT is as follows:

Table 2-14. LBD_TH Configuration Register

NUM	LBD_TH	LBD_TH<3:0> or LBD_RESULT<3:0>
1	<1.45v	4'b0000
2	1.45~1.65v	4'b0001
3	1.65~1.85v	4'b0010
4	1.85~2.05v	4'b0011
5	2.05~2.25v	4'b0100
6	2.25~2.45v	4'b0101
7	2.45~2.65v	4'b0110
8	2.65~2.85v	4'b0111
9	2.85~3.05v	4'b1000
10	3.05~3.25v	4'b1001
11	3.25~3.45v	4'b1010
12	3.45~3.65v	4'b1011
13	3.65~3.85v	4'b1100
⩾14	>3.85	4'b1101

Note:

1. LBD is not tested in real time, it is tested once after PLL frequency calibration. So users need to switch to STBY status first and then switch to Tx status to trigger the measurement process.
2. LBD_RESULT can be used as a condition for judgment, so users can use LBD_RESULT as a quantitative analysis after triggering the LBD condition.

2.7.8 Stop Bit Configuration

Table 2-15. Stop Bit Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	5	RW	STOP_EN	Stop Bit Enable bit： 0：Disable 1：Enable
CUS_PKT14 (0x15)	3:0	RW	STOP_LENGTH<3:0>	The Stop Bit length can be configured to 0~15, and 0 represents sending the Stop of 1 Symbol, and so on, 15 represents sending the Stop of16 Symbols, and the Symbol length is random.
CUS_PKT27 (0x22)	7:0	RW	STOP_BIT<7:0>	STOP_BIT Value
CUS_PKT28 (0x23)	7:0	RW	STOP_BIT<15:8>	

Table 2-16. The Corresponding Relationship Between the Stop Bit Length Selection

	STOP_BIT	
STOP_LENGTH	<15:8>	<7:0>
0~7	√	
8~15	√	√

The location of the tick in the table indicates the corresponding value of register to be filled. For example, if STOP_LENGTH is set to 7, that is, the length is 8 Symbols, and the value is 0x56, then the user will fill this value into STOP_BIT[15:8], MSB is corresponds to the fifteenth bit, and LSB is corresponds to the eighth bit.

For users, if the STOP_EN is configured to 0, the Stop Bit is not sent, and if it is configured to 1, the Stop Bit of 1-8 Symbols is sent.

2.7.9 Pause/Interval Configuration

Table 2-17. Pause/Interval Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	6	RW	INTERVAL_EN	Interval Enable bit: 0：Disable 1：Enable
CUS_PKT29 (0x24)	7:0	RW	INTERVAL_LENGTH<7:0>	The Interval length can be configured to 0~255, 0 represents sending 0 of 1 Symbol, and so on, 255 represents sending 0 of 256 Symbols, and the Symbol length is random. Note: Interval is fixed to send 0.

Note: In a strict sense, Pause/Interval is a packet interval, only a number of 0 of the Symbol, which is not an effective part of the packet structure.

For the user, if INTERVAL_EN is configured to 0, the Pause/Interval is not sent, and if it is configured to 1, the Pause/Interval of 1-256 Symbols is sent.

2.7.10 Tcycle Configuration

Tcycle is one transmission cycle (the transmission process) in the hardware packet Tx mode.The transmission cycle contains several transmitting packet ways, such as: N data packets are transmitted repeatedly and there are Pause/Interval between the packets,or N data packets compose one group and one transmission cycle contains M groups. These ways are shown in the following figure.

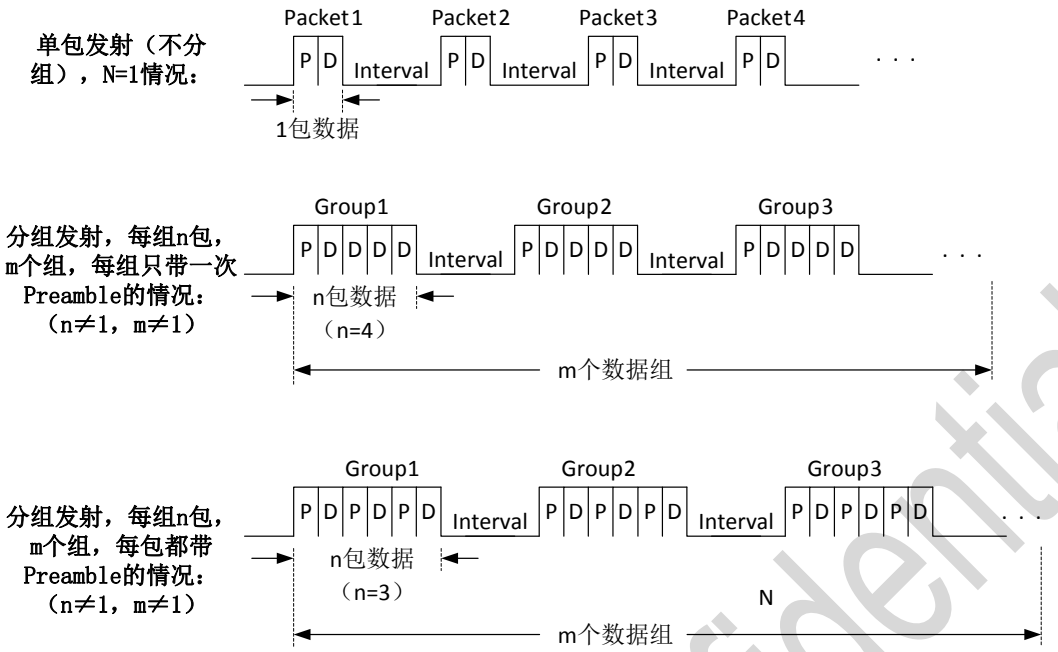


Figure 2-7. Transmitting Packet Way Diagram

- If Tcycle is disabled, then the way is the above first case.If Preamble is enabled, then the Preamble is fixed at the beginning of each packet.
- If Tcycle is enabled, Preamble is enabled, and PREAMBLE_LOCATION = 1, then the way is the above second case. That is, Preamble appears once in a group and appears at the beginning of each group, and there are M times (M = TXCYCLE) within onetransmission cycle.
- If Tcycle is enabled, Preamble is enabled, and PREAMBLE_LOCATION = 0, then the way is the above third case. That is, Preamble appears at the beginning of each packet, there are n times (n = PKT_NUM) within one group, and there are m*n times (TXCYCLE * PKT_NUM) within one transmission cycle.

Note:

1. In the above figure, P = Preamble，D = Sync/Head + Addr/ID + Key Value + LBD Status + Stop Bit
2. If Preamble is disabled, Preamble is not sent.
3. If Interval is disabled, Interval is not sent.
4. If Tcycle is disabled, preamble_location is configured to 0.
5. If Tcycle is disabled, Tcycle is configured to 0.

Table 2-18. Tcycle Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	2	RW	PREAMBLE_LOCATION	When Tcycle is enabled, it is the location of Preamble in the packet structure. 0: In one cycle, each Packet contains 1 Preamble, i.e. in one cycle, N Packets contain N Preambles. 1: In one cycle, only 1 Preamble is included,

Register Name	Bits	R/W	Bit Name	Function Description
				which is only in the first Packet.
	7	RW	TCYCLE_EN	Tcycle Enable bit: 0：Disable 1：Enable
CUS_PKT2 (0x09)	7:0	RW	TXCYCLE[7:0]	The number of Tcycle inone transmission cycle: 0-255 means sending 1-256 Tcycles.
CUS_PKT30 (0x25)	7:0	RW	PKT_NUM[7:0]	The number of Packet in one cycle: 0-255 means sending 1-256 Packets

2.8 Status and Function Register

Table 2-19. Status and Function Register Overview Table

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2F	CUS_SOFTRST	0xFF							
0x33	CUS_MODE					STBY		TX	SLEEP
0x34	CUS_DATA					DATAIN_EN			
0x4B	CUS_LBD_RESULT					LBD_RESULT			
0x4D	CUS_STATUS					MAIN_STATUS			

The above status and function registers cannot be exported in RFPDK, but users need to use them in the advanced configuration mode, which involves the chip status switching, status reading and reset etc..

2.8.1 Soft Reset

Through the SPI bus, the 0xFF is written to the CUS_SOFTRST (0x2F), and the reset process of the RF part can be realized.

Table 2-20. Soft Reset Register

Control Register	Command Type	Command	Writing Value	Function Description
CUS_SOFTRST（0x2F）	Soft reset	soft_rst	0xFF	Reset the chip and allow the chip to initialize again and return to the SLEEP status.

Note:

1. After executing the soft_rst, the chip is reset again, and the user needs to update the configuration register according to the requirement.
2. After power-up, the configuration register is based on the internal default value (that is, the EERPOM value burned by the factory) before the configuration register (CFG) is configured.

2.8.2 Working Status and Status Switching

CMT2189B RF has three main working statuses. In the advanced configuration mode, the status and the status switching are shown in the following diagram:

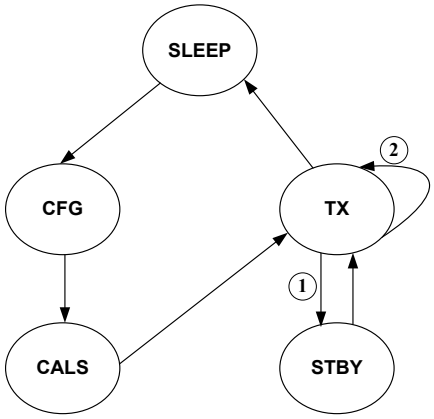


Figure 2-8. RF Working Status and Status Switching

Table 2-21. Every Status Description

Status/Process	Description
SLEEP	Low power mode, close all modules.
CFG	Configure the register process.
CALS	Calculate the analog module.
TX	Transmit packets; all modules on the transmitter will be opened.
STBY	Transmit the interval in the power saving mode, turn off PA. PLL can be opened according to the configuration.The oscillator keeps working.

Note:

1. CFG is the process of configuring the chip working parameters for the MCU through SPI;
2. CALS is the process of calibrating the analog module in the RF internal. After starting, it is automatically executed and processed to switch to the TX status in the RF internal.

Table 2-22. Status Switching Command and Reset Command

Control Register	Command Type	Command	Writing Value	Function Description
CUS_MODE（0x33）	Status-jump	go_sleep	0x01	Return SLEEP status
		go_tx	0x02	Enter TX status
		go_stby	0x08	Enter STBY status

2.8.3 Work Status Query

The user needs to query the current work status by reading the CUS_STATUS (0x4D) status register, of

which the lower 4-bit represents the current work status. Specifics see the table below.

Table 2-23. Status Switching Command and Reset Command

Status Register	Status Coding	Description
CUS_STATUS（0x4D<3:0>）	0b0000	SLEEP
	0b1010	TX
	0b1101	STBY

2.9 Hardware Packet TxMode

2.9.1 Power-up Initialization

1. Power up for the chip, initialize the port, and wait for 20ms to stabilize.
2. Control RFCTRL=1.
3. Configure PC3/CSB, PC2/SCLK and PC0/RFDIN as the high resistance input, configure PC1/SDIO as the output 0.
4. After initialization, the chip can enter the sleep low power status, or do the other processing.

2.9.2 Tx Process

To implement the hardware packet mode, users need to follow the following process:

1. Control RFCTRL = 0, enable the SPI interface of the RF part, and immediately send the soft_rst command, wait for the 20ms stability time to ensure that the soft reset is completed.
2. Send the go_stby command through SPI, and confirm that RF is in the Standby state (it is recommended to wait for 2ms after sending the command).
3. Configure the related registers according to user requirements (Tx bank, packet format, etc., configuration range 0x00~0x2E)
   a) All the parameters exported by RFPDK are configured in order.
   b) If necessary, modify the individual registers that need to be modified (such as filling the FIFO content, etc.);
4. Set the register 0x34<5> to 0, and then set the register 0x2A<1:0> to 0b00.
5. Send the go_tx command through SPI, and start the chip hardware packet transmissionaccording to the above configuration.
6. Read the status through SPI (read according to a certain interval) to determine whether the chip transmissionis completed (the transmission is completed when it returns to the Sleep state).
7. After the transmission is completed, users need to set RFCTRL high, switch SPI and RFDIN to high resistance input (SPI and RFDIN have the internal pull-up). MCU will also enter the SLEEP mode after that, that is, the whole device will enter the low-power state.

Note:

1. When the transmission is started up again, the transmission process will be re executed.
2. In the fourth step, users need to use "read-modify-write" to avoidmodifying thevalue of other bits by

mistake.

3. The Standby can not be judged by the completion of the transmission because the data packet interval may be in a Standby state.
4. The internal pin status processing after the end of the transmissionis different from the processing after the power-up initialization. This needs to be paid attention to.

2.10 Direct Tx Mode(Advanced Configuration Mode)

2.10.1 Power-up Initialization

1. Power up for the chip, initialize the port, and wait for 20ms to stabilize.
2. Control RFCTRL = 1.
3. Configure PC3/CSB, PC2/SCLK and PC0/RFDIN as the high resistance input, configure PC1/SDIO as the output 0.
4. After initialization, the chip can enter the sleep low power state, or do the other processing.

2.10.2 Tx Process

To implement the Direct transmission in the configuration mode, users need to follow the following process:

1. Set PC0/RFDIN to 0 output.
2. Control RFCTRL = 0, enable the SPI interface of RF part, immediately send the soft_rst command and wait for 20ms to stabilize.
3. Set the register 0x34<3> to 1 and confirm the success of the modification.
4. Send the go_stby command through SPI to confirm that RF is in the Standby state (it is recommended to wait for 2ms after sending the command).
5. Configure the related registers as the user needs (configuration range is 0x00~0x03)
6. Set the register 0x34<5> to 0, and then set the register 0x2A<1:0> to 0b01.
7. Send the go_tx command through SPI, and start the chip transmission according to the above configuration (it is recommended to wait for 1ms after sending the command).
8. Control the data stream required by PC0/RFDIN.
9. After sending, hold PC0/RFDIN to 0 output.
10. Set the register 0x02<6:0> to 0 and then set the register 0x4E<7> to 1.
11. Set the register 0x34<3> to 0 and confirm the success of the modification.
12. Send the go_sleep command through SPI and enter the Sleep state.
13. Set the MCU pin that controls the RFCTRL to high resistance input, switch PC3/CSB, PC2/SCLK and PC0/RFDIN to high resistance input (internal pull-up), switch PC1/SDIO to output 0, then MCU will also enter the SLEEP mode after that, that is, the whole device will enter the low-power state.

Note:

1. In the fifth step, the configuration register only needs to be configured as 0x00~0x03, which can adjust the Tx frequency and Tx power, and the others can be ignored.
2. When the transmission is started up again, execute the Tx process once again.

3. In the third, sixth, tenth and eleventh step, users need to use "read-modify-write" to avoidmodifying thevalue of other bits by mistake.

2.10.3 Related Register

Table 2-24. Direct Mode Related Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_DIG4 (0x07)	2:0	RW	TX_OVERTIMES[2:0]	The overtime of ending Tx can be configured to be 0~7. The calculation formula for the overtime is: T = 20ms + TX_OVERTIMES * 10ms That is: the overtime range is from 20ms to 90 ms.
CUS_DATA (0x34)	3	RW	DATAIN_EN	RFDIN Tx mode Data Input Enable bit: 0：Disable 1：Enable

In the Direct mode, the data rate of the Tx data is controlled by RFDIN (PC0). When the time that PC0 holds the output 0 is greater than the time that TX_OVERTIMES sets, it will automatically enter the OvertimeExit mechanism and stop the current transmission until triggering on the rising edge of PC0 next time. So users need to think according to the encoding format. TX_OVERTIMES is 20ms by default, and can be added to 90ms that the stepping is 10ms.

3 Program Memory

The program address register is 13-bit.Maximum supports for access to 8K Bytes space(0x0000~0x1FFF). But the actual chip memory is 2K Words, plus 4 additional user configuration banks (UCFGx) and factory configuration banks (FCFGx), the total is 64 Words.They are made up of EEPROM. Among them, the 0~0x7FF is the main program bank, the 0x800~0x1FFF is unimplemented bank which isreserved.The user and factory configuration information bank is 0x2000~0x203F.

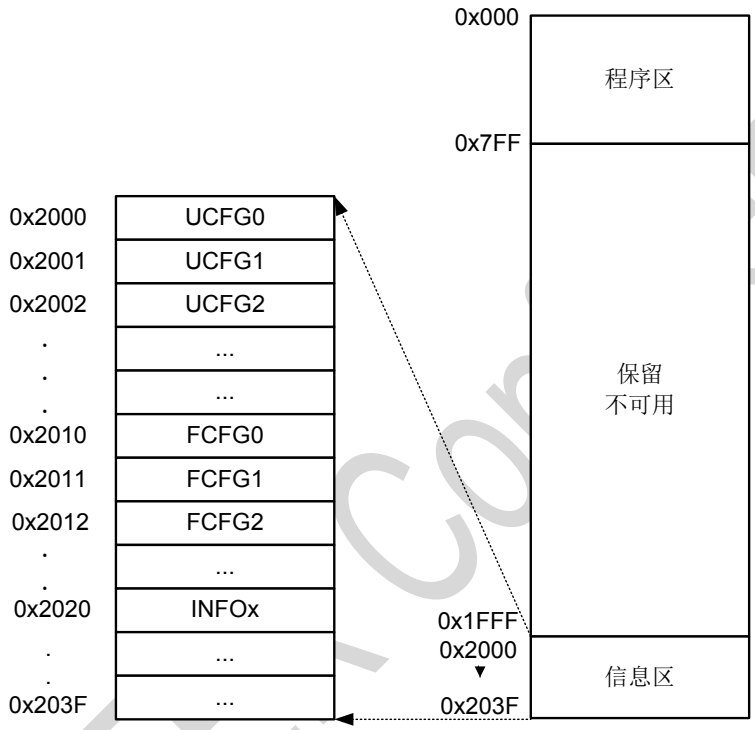


Figure 3-1. Program Space Address Mapping

4 Special Function Register(SFR)

4.1 Address Mapping

4.1.1 Bank0 SFR

Table 4-1. Bank0 Register List

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
0	INDF	Access the data memory by using the content of FSR(non physical registers)								xxxx xxxx
1	TMR0	Timer0<7:0>								xxxx xxxx
2	PCL	Program Counter<7:0>								0000 0000
3	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
4	FSR	Indirect Data Memory Address Pointer								
5	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00x0 0000
6										---- ----
7	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	0000 0000
8										---- ----
9										---- ----
A	PCLATH	-	-	-	Program Counter<13:8>					---0 0000
B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-	00-0 000-
D										---- ----
E										---- ----
F										---- ----
10										---- ----
11	TMR2	Timer2<7:0>								0000 0000
12	T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000
13										---- ----
14										---- ----
15										---- ----
16										---- ----
17										---- ----
18	WDTCON	-	-	-	WDTPS<3:0>				SWDTEN	---0 1000
19	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>			0000 0000
1A	PR0	PR0<7:0>								1111 1111
1B	MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-	---0 -00-
1C	SOSCPPRL	SOSCPR<7:0>								1111 1111
1D	SOSCPRH	-	-	-	-	SOSCPR<11:8>				---- 1111
1E										---- ----
1F										---- ----
20-7F		Bank0's SRAM, which is the general RAM of 96Bytes.								xxxx xxxx

4.1.2 BANK1 SFR

Table 4-2. Bank1 Register List

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
80	INDF	Access the data memory by using the content of FSR (non physical registers)								xxxx xxxx
81	OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL	Program Counter<7:0>								0000 0000
83	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
84	FSR	Indirect Data Memory Address Pointer								
85	TRISA	TRISA<7:6>		PA5	TRISA<4:0>					11x1 1111
86										---- ----
87	TRISC	TRISC<7:0>								1111 1111
88										---- ----
89										---- ----
8A	PCLATH	-	-	-	Program Counter<13:8>					---0 0000
8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
8C	PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-	00-0 000-
8D										---- ----
8E	PCON							/POR	/BOR	---- --qq
8F	OSCCON	LFMOD	IRCF<2:0>			OSTS	HTS	LTS	SCS	0101 x000
90										---- ----
91										0000 0000
92	PR2	PR2<7:0>, Timer2 period register								1111 1111
93										---- ----
94										---- ----
95	WPUA	WPUA<7:6>		-	WPUA<4:0>					11-1 1111
96	IOCA	IOCA<7:0>								---- ----
97										---- ----
98										---- ----
99	VRCON	VREN	-	VRR	-	VR<3:0>				0-0- 0000
9A	EEDAT	EEDAT<7:0>								0000 0000
9B	EEADR	EEADR<7:0>								0000 0000
9C	EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD	--00 x0-0
9D	EECON2	-	-	-	-	-	-	-	WR	---- ---0
9E										---- ----
9F										---- ----
A0-BF		Bank1's SRAM, which is the general RAM of32Bytes.								xxxx xxxx
C0-EF										---- ----
F0-FF		SRAM, Access Bank0's 0x70 ~ 0x7F.								xxxx xxxx

Note:

1. INDF is not a physical register.
2. The gray part is unimplemented, please do not access.

3. "-" indicates that it is unimplemented; the unimplemented register bits can not beused or written as 1. It is used for subsequent chip upgrading.

4.1.3 TMR0（Addr:0x01）

Table 4-3. TMR0 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR0	Timer0<7:0>，Count result register							
Reset	X	X	X	X	X	X	X	X
Type	RW							

4.1.4 STATUS（Addr:0x03）

Table 4-4. STATUS Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	-	-	PAGE	/TF	/PF	Z	HC	C
Reset	-	-	0	1	1	X	X	X
Type	-	-	RW	R	R	RW	RW	RW

Table 4-5. STATUS Bit Function Description

Bit	Name	Function
7:6	-	No function, read as “0”
5	PAGE	Register Bank Select bit: 0 = BANK0（00h-7Fh） 1 = BANK1（80h-FFh）
4	/TF	Time Out Bit 1 = After power-up, CLRWDT instruction or SLEEP instruction 0 = A WDT time-out occured.
3	/PF	Power Down Bit 1 = After power-up or by the CLRWDT instruction 0 = By executation of the SLEEP instruction
2	Z	Zero Bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
1	HC	Half-carry/$\overline{\text{borrow}}$ bit(ADDWF、ADDLW、SUBLW、SUBWF instructions) 1 = A carry/$\overline{\text{borrow}}$ from the 4th low-order bit of the result occurred 0 = No carry/$\overline{\text{borrow}}$ from the 4th low-order bit of the result occurred
0	C	Carry/$\overline{\text{borrow}}$ bit(ADDWF、ADDLW、SUBLW、SUBWF instructions) 1 = A carry/$\overline{\text{borrow}}$ from the Most Significant bit of the result occurred 0 = No carry/$\overline{\text{borrow}}$ from the Most Significant bit of the result occurred

Table 4-6. Flag Situation in Each Reset Status

/TF	/PF	Condition
1	1	Power on or low voltage reset
0	u	WDT reset
0	0	WDT wake-up
u	u	MCLR reset under the normal operation
1	0	MCLR reset in the sleep status

Note:

1. The Status register can also be the destination for any instruction, like any other register.If the Status register is the destination for an instruction that affects the Z, HC, or C bits, then the write to these three bits isdisabled. These bits are set to 1 or cleared according to the device logic.Therefore, the result of an instruction with the Status register as destination may be different than intended.
2. It is suggested that only using the BCR, BSR, SWAPR and STR instructions change the status register.

4.1.5 PORTA（Addr:0x05）

Table 4-7. PORTA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset	X	X	X	X	X	X	X	X
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 4-8. PORTA Bit Function Description

Bit	Name	Function
7	PA7	PORTA7 data
6	PA6	PORTA6 data
5	PA5	PORTA5 has only the input function.There is no corresponding output data register.
4	PA4	PORTA4 data
3	PA3	PORTA3 data
2	PA2	PORTA2 data
1	PA1	PORTA1 data
0	PA0	PORTA0 data

4.1.6 PORTC（Addr:0x07）

Table 4-9. PORTC Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Reset	X	X	X	X	X	X	X	X
Type	RW	RW	RW	RW	RW	RW	RW	RW

Table 4-10. PORTC Bit Function Description

Bit	Name	Function
7	PC7	PORTC7 data
6	PC6	PORTC6 data
5	PC5	PORTC5 data
4	PC4	PORTC4 data
3	PC3	PORTC3 data
2	PC2	PORTC2 data
1	PC1	PORTC1 data
0	PC0	PORTC0 data

4.1.7 INTCON（Addr:0x0B）

Table 4-11. INTCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Table 4-12. INTCON Bit Function Description

Bit	Name	Function
7	GIE	Global Interrupt Enable bit 1 = Enable all unmasked interrupts 0 = Disable all interrupts
6	PEIE	Peripheral Interrupt Enable bit 1 = Enable all unmasked peripheral interrupts 0 = Disable allperipheral interrupts
5	T0IE	Timer0 Overflow Interrupt Enable bit 1 = Enable 0 = Disable

4	INTE	PA2/INT External InterruptEnable bit 1 = Enable 0 = Disable
3	PAIE	PORTA Change Interrupt Enable bit 1 = Enable the PORTA<7:0> change interrupt 0 = Disable the PORTA<7:0> change interrupt
2	T0IF	Timer0 Overflow Interrupt Flag bit 1 = Timer0 register has overflowed (must be cleared in software) 0 = Timer0 register does not overflow
1	INTF	PA2/INT External Interrupt Flag bit 1 = PA2/INT external interrupt occurred (must be cleared in software) 0 = PA2/INT external interrupt does not occur
0	PAIF	PORTA Change Interrupt Flag bit 1 = Any one or more ports of PORTA<7:0>have changed state (must be cleared in software) 0 = None of the PORTA<7:0> have changed state

4.1.8 PIR1（Addr:0x0C）

Table 4-13. PIR1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-
Reset	0	0	-	0	0	0	0	-
Type	RW	RW	-	RW	RW	RW	RW	-

Table 4-14. PIR1 Bit Function Description

Bit	Name	Function
7	EEIF	EEPROM Write Operation Interrupt Flag bit 1 = The write operation completed(must be cleared in software) 0 = The write operation has not completed
6	CKMEAIF	Fast clock measuring slow clock operation Interrupt Flag bit 1 = Fast clock measuring slow clock operation completed (must be cleared in software.) 0 = Fast clock measuring slow clock operation has not completed
5	-	Reserved-bit, can not be written as 1
4	C2IF	Comparator2 Interrupt Flag bit 1 = Comparator2 output has changed 0 = Comparator2 output has not changed
3	C1IF	Comparator1 Interrupt Flag bit 1 = Comparator1 output has changed 0 = Comparator1 output has not changed

2	OSFIF	Oscillator Fail Interrupt Flag bit 1 = System oscillator failed, clock input has changed to INTOSC(must be cleared in software) 0 = System clock runs normally
1	TMR2IF	Timer2 to PR2 Match Interrupt Fag bit 1 =Timer2 to PR2 match occurred(must be cleared in software) 0 = Timer2 to PR2 match has not occurred
0	-	Reserved-bit, can not be written as 1

4.1.9 TMR2（Addr:0x11）

Table 4-15. TMR2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR2	TMR2<7:0>							
Reset	0000 0000							
Type	RW							

4.1.10 T2CON（Addr:0x12）

Table 4-16. T2CON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>	
Reset	-	0000				0	00	
Type	-	RW				RW	RW	

Table 4-17. T2CON Bit Function Description

Bit	Name	Function
7	-	Reserved-bit, read as 0
6:3	TOUTPS<3:0>	Timer2 Output Postscale Select bits 0000 = 1:1 postscale 0001 = 1:2 postscale 0010 = 1:3 postscale 0011 = 1:4 postscale 0100 = 1:5 postscale 0101 = 1:6 postscale 0110 = 1:7 postscale 0111 = 1:8 postscale 1000 = 1:9 postscale 1001 = 1:10 postscale 1010 = 1:11 postscale 1011 = 1:12 postscale

		1100 = 1:13 postscale 1101 = 1:14 postscale 1110 = 1:15 postscale 1111 = 1:16 postscale
2	TMR2ON	Timer2 On bit 1 = Timer2 is on 0 = Timer2 is off
1:0	T2CKPS<1:0>	Timer2 Clock Prescale Select bits 00 = 1:1 Prescaler is 1 01 = 1:4 Prescaler is 4 1x = 1:16 Prescaler is 16

4.1.11 WDTCON（Addr:0x18）

Table 4-18. WDTCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	-	-	-	WDTPS<3:0>				SWDTEN
Reset	-	-	-	0	1	0	0	0
Type	-	-	-	RW	RW	RW	RW	RW

Table 4-19. WDTCON Bit Function Description

Bit	Name	Function
7:5	-	Reserved-bits, read as 0
4:1	WDTPS<3:0>	Watchdog Timer Period Select Bits 0000 = 1:32 0001 = 1:64 0010 = 1:128 0011 = 1:256 0100 = 1:512 (Reset value) 0101 = 1:1024 0110 = 1:2048 0111 = 1:4096 1000 = 1:8192 1001 = 1:16384 1010 = 1:32768 1011 = 1:65536 11xx = 1:65536
0	SWDTEN	Software Enable or Disable the watchdog timer 1 = WDT is turned on 0 = WDT is turned off

4.1.12 CMCON0（Addr:0x19）

Table 4-20. CMCON0 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>		
Reset	0	0	0	0	1	0	0	0
Type	R	R	RW	RW	RW	RW	RW	RW

Table 4-21. CMCON0 Bit Function Description

Bit	Name	Function
7	C2OUT	Comparator2 Output bit When C2INV=0, 1：C2VIN+ ＞ C2VIN- 0：C2V IN+ ＜ C2VIN- When C2INV=1, 1：C2VIN+ ＜ C2VIN- 0：C2V IN+ ＞ C2VIN-
6	C1OUT	Comparator1 Output bit When C1INV=0, 1：C1VIN+ ＞ C1VIN- 0：C1V IN+ ＜ C1VIN- When C1INV=1, 1：C1VIN+ ＜ C1VIN- 0：C1V IN+ ＞ C1VIN-
5	C2INV	Comparator2 Output Inversion bit 0 = C2 output not inverted 1 = C2 output inverted
4	C1INV	Comparator1 Output Inversion bit 0 = C1 output not inverted 1 = C1 output inverted
3	CIS	Comparator Input Switch bit When CM[2:0]=010, 1 = C1IN+ connects to C1VIN+, C2IN+ connects to C2VIN+ 0 = C1IN- connects to C1VIN-，C2IN- connects to C2VIN- When CM[2:0]=001, 1 = C1IN+ connects to C1VIN+ 0 = C1IN- connects to C1VIN-

2:0	CM<2:0>	Comparator Mode Select bits 000 = The comparator is turned off, and the CxIN pin is the analog IO pin. 001 = Three inputs multiplexed to two comparators 010 = Four inputs multiplexed to two comparators 011 = Two common reference comparators 100 = Two independent comparators 101 = One independent comparator 110 = Two common reference comparators with outputs 111 = The comparator is turned off, and the CxIN pin is the digital IO pin.

4.1.13PR0（Addr:0x1A）

Table 4-22. PRO Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PR0	PR0<7:0>							
Reset	0xFF							
Type	RW							

Table 4-23. PR0 Function Description

Bit	Name	Function
7:0	PR0<7:0>	Timer0 period (comparison) register

4.1.14 MSCKCON（Addr:0x1B）

Table 4-24. MSCKCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-
Reset	-	-	-	0	-	0	0	-
Type	-	-	-	RW	-	RW	RW	-

Table 4-25. MSCKCON Bit Function Description

Bit	Name	Function
7:5	-	Reserved-bits, can not be written as 1.
4	SLVREN	Software Control LVR Enable bit 1 = When UCFG<1:0> is 00, enable LVR. 0 = No matter what value of UCFG<1:0> is, disable LVR.
3	-	Reserved-bit, can not be written as 1.

2	CKMAVG	Measurement average mode of fast clock measuring slow clock period 1 = Open the average mode.(Automatically measure and accumulate four times) 0 = Close the average mode.
1	CKCNTI	Fast clock measuring slow clock period Enable bit 1 = Enable fast clock measuring slow clock period. 0 = Disable fast clock measuring slow clock period. Note: The bit will automatically return to zero after the measurement is completed.
0	-	Reserved-bit, can not be written as 1.

4.1.15 SOSCPR（Addr:0x1C/0x1D）

Table 4-26. SOSCPRL Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOSCPRL	SOSCPR<7:0>							
Reset	0xFF							
Type	RW							

Table 4-27. SOSCPRH Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOSCPRH	-				SOSCPR<11:8>			
Reset	-				1111			
Type	-				RW			

Table 4-28. SOSCPR Function Description

Bit	Name	Function
11:0	SOSCPR<11:0>	Low-frequency oscillator period (unit: fast clock period number) is used for slow clock measurement.

4.1.16 OPTION（Addr:0x81）

Table 4-29. OPTION Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS<2:0>		
Reset	1	1	1	1	1	111		
Type	RW	RW	RW	RW	RW	RW		

Table 4-30. OPTION Bit Function Description

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>7</td><td>/PAPU</td><td>PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual port latch values</td></tr>
<tr><td>6</td><td>INTEDG</td><td>Interrupt Edge Select bit
1 = Interrupt on rising edge of PA2/INT pin
0 = Interrupt on falling edge of PA2/INT pin</td></tr>
<tr><td>5</td><td>T0CS</td><td>Timer0 Clock Source Select bit
1 = Transition on PA2/T0CKI bit
0 = Internal instruction cycle clock (FOSC/2)</td></tr>
<tr><td>4</td><td>T0SE</td><td>Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on PA2/T0CKI pin
0 = Increment on low-to-high transition on PA2/T0CKI pin</td></tr>
<tr><td>3</td><td>PSA</td><td>Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module</td></tr>
<tr><td>2:0</td><td>PS<2:0></td><td>Prescaler Rate Select bits
<table>
<tr><th>Value</th><th>Timer0</th><th>WDT</th></tr>
<tr><td>000</td><td>1:2</td><td>1:1</td></tr>
<tr><td>001</td><td>1:4</td><td>1:2</td></tr>
<tr><td>010</td><td>1:8</td><td>1:4</td></tr>
<tr><td>011</td><td>1:16</td><td>1:8</td></tr>
<tr><td>100</td><td>1:32</td><td>1:16</td></tr>
<tr><td>101</td><td>1:64</td><td>1:32</td></tr>
<tr><td>110</td><td>1:128</td><td>1:64</td></tr>
<tr><td>111</td><td>1:256</td><td>1:128</td></tr>
</table></td></tr>
</table>

4.1.17 TRISA（Addr:0x85）

Table 4-31. TRISA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 4-32. TRISA Bit Function Description

Bit	Name	Function
7:6	TRISA<7:6>	PORTA<7:6> port direction Control bits 1 = Input 0 = Output

5	TRISA<5>	PORTA5 port direction Control bit Only as input, fixed to 1
4:0	TRISA<4:0>	PORTA<4:0> port direction Control bits 1 = Input 0 = Output

4.1.18 TRISC（Addr:0x87）

Table 4-33 TRISC Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 4-34. TRISC Bit Function Description

Bit	Name	Function
7:0	TRISC<7:0>	PORTC<7:0> port direction Control bits 1 = Input 0 = Output

4.1.19 PIE1（Addr:0x8C）

Table 4-35. PIE1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-
Reset	0	0	-	0	0	0	0	-
Type	RW	RW	-	RW	RW	RW	RW	-

Table 4-36. PIE1 Bit Function Description

Bit	Name	Function
7	EEIE	EEPROM Write Complete Interrupt Enable bit 1 = Enable the EEPROM write complete interrupt 0 = Disable the EEPROM write complete interrupt
6	CKMEAIE	Fast clock measuring slow clock operation Interrupt Enable bit 1 = Enable fast clock measuring slow clock operation interrupt 0 = Disable fast clock measuring slow clock operation interrupt
4	C2IE	Comparator2 Interrupt Enable bit 1 = Enable the comparator2 interrupt 0 = Disable the comparator2 interrupt

3	C1IE	Comparator1 Interrupt Enable bit 1 = Enable the comparator1 interrupt 0 = Disable the comparator1 interrupt
2	OSFIE	Oscillator Fail Interrupt Enable bit 1 = Enable the oscillator fail interrupt 0 = Disable the oscillator fail interrupt
1	TMR2IE	Timer2 to PR2 Match Interrupt Enable bit 1 = Enable 0 = Disable

4.1.20 PCON（Addr:0x8E）

Table 4-37. PCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	-	-	-	-	-	-	/POR	/BOR
Reset	-	-	-	-	-	-	q	q
Type	-	-	-	-	-	-	RW	RW

Table 4-38. PCON Bit Function Description

Bit	Name	Function
1	/POR	Power-on Reset Status bit, active low 0 = A Power-on Reset occured 1 = No Power-on Reset occured or software set it to 1. /POR is set to 0 after a Power-on Reset occurs. After that, the software should set it to 1.
0	/BOR	Brown-out Reset Status bit, active low 0 = A Brown-out Reset occured 1 = No Brown-out Reset occurred or software set it to 1.

4.1.21 OSCCON（Addr:0x8F）

Table 4-39. OSCCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OSCCON	LFMOD	IRCF<2:0>			OSTS	HTS	LTS	SCS
Reset	0	101			1	0	0	0
Type	RW	RW			R	R	R	RW

Table 4-40. OSCCON Bit Function Description

Bit	Name	Function
7	LFMOD	Internal Low Frequency Oscillation Mode: 1 = 256K oscillation frequency mode 0 = 32K oscillation frequency mode
6:4	IRCF<2:0>	Internal Oscillator Frequency Select bits 111 = 16MHz 110 = 8MHz 101 = 4MHz(default) 100 = 2MHz 011 = 1MHz 010 = 500KHz 001 = 250KHz 000 = 32KHz（LFINTOSC）
3	OSTS	Oscillator Start-up Timeout Status bit 1 = Device is running from the external system clock defined by the FOSC<2:0>. 0 = Device is running from the internal system clock
2	HTS	Internal High FrequencyClock Status bit 1 = HFINTOSC is stable 0 = HFINTOSC is not stable
1	LTS	Internal Low Frequency Clock Status bit 1 = LFINTOSC is stable 0 = LFINTOSC is not stable
0	SCS	System Clock Select bit 1 = Internal oscillator is used for system clock 0 = Clock source is defined by FOSC<2:0>

4.1.22 PR2（Addr:0x92）

Table 4-41. PR2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PR2	PR2<7:0>							
Reset	0xFF							
Type	RW							

Table 4-42. PR2 Bit Function Description

Bit	Name	Function
7:0	PR2<7:0>	Timer2 period (comparison) register (See the Timer2 description chapter in details.)

4.1.23 WPUA（Addr:0x95）

Table 4-43. WPUA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
Reset	1	1	-	1	1	1	1	1
Type	RW	RW	-	RW	RW	RW	RW	RW

Table 4-44. WPUA Bit Function Description

Bit	Name	Function
7:6	WPUA<7:6>	PORTA Weak Pull-up Enable bit 1 = Enable 0 = Disable
4:0	WPUA<4:0>	PORTA Weak Pull-up Enable bit 1 = Enable 0 = Disable

4.1.24 IOCA（Addr:0x96）

Table 4-45. IOCA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IOCA	IOCA<7:0>							
Reset	0x00							
Type	RW							

Table 4-46. IOCA Bit Function Description

Bit	Name	Function
7:0	IOCA<7:0>	Interrupt-on-change PORTA Control bit 1 = Interrupt-on-change enabled 0 = Interrupt-on-change disabled

4.1.25 VRCON（Addr:0x99）

Table 4-47. VRCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VRCON	VREN	-	VRR	-	VR<3:0>			
Reset	0	-	0	-	0			
Type	RW	-	RW	-	RW			

Table 4-48. VRCON Bit Function Description

Bit	Name	Function
7	VREN	CVref Enable bit 1 = CVref circuit powered on 0 = CVref circuit powered down, no I_{DD} drain
5	VRR	CVref Range Select bit 1 = Low level range 0 = High level range
3:0	VR<4:0>	CVref Value Select Control bit When VRR = 1，CVref = （VR<4:0>÷24）×VDD When VRR = 0，CVref = （VDD÷4）+（VR<4:0>÷32）×VDD

4.1.26 EEDAT（Addr:0x9A）

Table 4-49. EEDAT Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EEDAT	EEDAT<7:0>							
Reset	0x00							
Type	RW							

4.1.27 EEADR（Addr:0x9B）

Table 4-50. EEADR Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EEADR	EEADR<7:0>							
Reset	0x00							
Type	RW							

4.1.28 EECON1（Addr:0x9C）

Table 4-51. EECON1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD
Reset	-	-	0	0	X	0	-	0
Type	-	-	RW	RW	RW	RW	-	W

Table 4-52. EECON1 Bit Function Description

Bit	Name	Function
5,4,2	WREN<2:0>	EEPROM Write Enable bit 111 = Allow write to the data EEPROM. After the program is completed, each bit will automatically return to 0. Other values=Inhibit write to the data EEPROM
3	WRERR	EEPROM Write Error Flag bit 1 = A write operation is prematurely terminated (any /MCLR Reset, any WDT Reset during EEPROM programming period) 0 = The write operation completed during EEPROM programming period.
0	RD	EEPROM Read Control bit. This bit is written only, reading will return to 0 forever. 1 = Initiate an EEPROM read 0 = Does not initiate an EEPROM read

4.1.29 EECON2（Addr:0x9D）

Table 4-53. EECON2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON2	-	-	-	-	-	-	-	WR
Reset	-	-	-	-	-	-	-	0
Type	-	-	-	-	-	-	-	RW

Table 4-54. EECON2 Bit Function Description

Bit	Name	Function
0	WR	EEPROM Write Control bit Read operation, 1= Data EEPROM is in the programming period. 0= Data EEPROM is not in the programming period Write operation, 1= Initiates a data EEPROM programming cycle 0= No function

4.1.30 Configuration Register UCFGx

The software does not access UCFG0, UCFG1 and UCFG2.They are only written by the hardware (burning) in the power-up process.

- **UCFG0 address is 0x2000 in PROM**

Table 4-55. UCFG0 Configuration Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG0	-	CPB	MCLRE	PWRTEB	WDTE	FOSC<2:0>		

Table 4-56. UCFG0 Bit Function Description

Bit	Name	Function
6	CPB	1 = Flash content is not protected 0 = Intiate the Flash content protection, MCU can read it, the serial port can not read it. Note: The bit can only be rewritten from 1 to 0, but it can not be rewritten from 0 to 1.The only way to rewrite from 0 to 1 is to erase the register including USER_OPT, and the CPB becomes 1 after power-up again.
5	MCLRE	1 = The PA5/MCLR pin executes the MCLR function, which is the reset pin. 0 = The PA5/MCLR pinexecutes the PA5 function, which is the digital input pin.
4	PWRTEB	1 = Disable PWRT 0 = Enable PWRT
3	WDTE	1 = Enable WDT, the program cannot disable it. 0 = Disable WDT, but the program can enable WDT by setting the SWDTEN bit of the WDTCON
2:0	FOSC<2:0>	000 = 32K crystal oscillator mode, PA6/PA7 connects the low frequencycrystal oscillator. 001 = 20MHz crystal oscillator mode, PA6/PA7 connects the high speed crystal oscillator. 010 = External clock mode, PA6 is the IO pin, PA7 is connected to the clock input. 011 = INTOSC mode, PA6 output the 2 frequency division of the system clock, PA7 is the IO pin; 1xx = INTOSCIO mode, both PA6 and PA7 are the IO pins

- **UCFG1address is 0x2001 in PROM**

Table 4-57. UCFG1 Configuration Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG1	-	-	TSEL	FCMEN	IESO	RD_CTRL	LVDEN<1:0>	

Table 4-58. UCFG1 Bit Function Description

Bit	Name	Function
5	TSEL	Instruction Period Select bit 1 = The instruction period is 2T. 0 = The instruction period is 4T.
4	FCMEN	Clock Fault Monitoring Enable bit 1 = Enable the clock fault monitoring 0 = Disable the clock fault monitoring
3	IESO	Two Speed Clock Enable bit 1 = Enable 0 = Disable
2	RD_CTRL	Read Port Control bit in output mode 1 = Read the value of the PAD returned from the data port. 0 = Read the value of the Latch returned from the data port.
1:0	LVDEN<1:0>	Low Voltage Reset Select bit 00 = Enable the low voltage reset. Others = Disable the low voltage reset.

- **UCFG2address is 0x2002 in PROM**

Table 4-59. UCFG2 Configuration Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG2	-	-	-	-	LVDS<3:0>			

Table 4-60. UCFG2 Bit Function Description

Bit	Name	Function
7:4	-	Reserved-bit
3:0	LVDS[3:0]	Low voltage reset threshold selection

Value	Voltage
0010	1.8V
0011	2.0V
0100	2.2V
0110	2.8V
Others	Reserved

4.1.31 PCL and PCLATH

The program counter (PC) is 11-bit.The lower 8-bit is from the PCL register, which is a readable and writable register. The higher 3-bit (PC<10:8>) is not directly readable and writable and comes from PCLATH. On any reset, PC will be cleared.The following figure shows the two situations for the loading of PC.Notice the LCALL and LJUMP instructions on the right side of the figure. Because the operating code in the instruction

is 11-bit, and the PC of the chip is just 11-bit, so PCLATH is not needed.

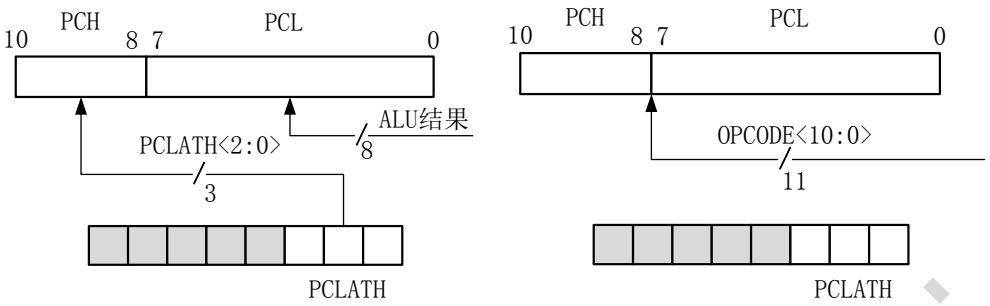


Figure 4-1. PC Loading Diagram in Different Situations

Modify PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<10:8> bits to be replaced by the content of the PCLATH register.This allows the entire contents of the program counter to be changed by writing the desired high 3-bit to the PCLATH register.

A computed LJUMP instruction is accomplished by adding an offset to the program counter (ADDWR PCL). Care should be exercised when jumping into the look-up table or the program branch table (computed LJUMP) by modifying the PCL register. Assuming that PCLATH is set as the table start address, if the table length is greater than 255 instruction, or if the lower 8-bit of memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and target location within the table.

4.1.32 INDF and FSR Register

INDF is not a physical register, and addressing the INDF will generate an indirect addressing, and the addressable range is 0~255.Any instruction that uses the INDF register is actually access to the unit that the file selection register FSR points to.Reading the INDF indirectly will return 0. Writing the INDF indirectly will cause the control operation. (It may affect the status flag bit.)

5 System Clock Source

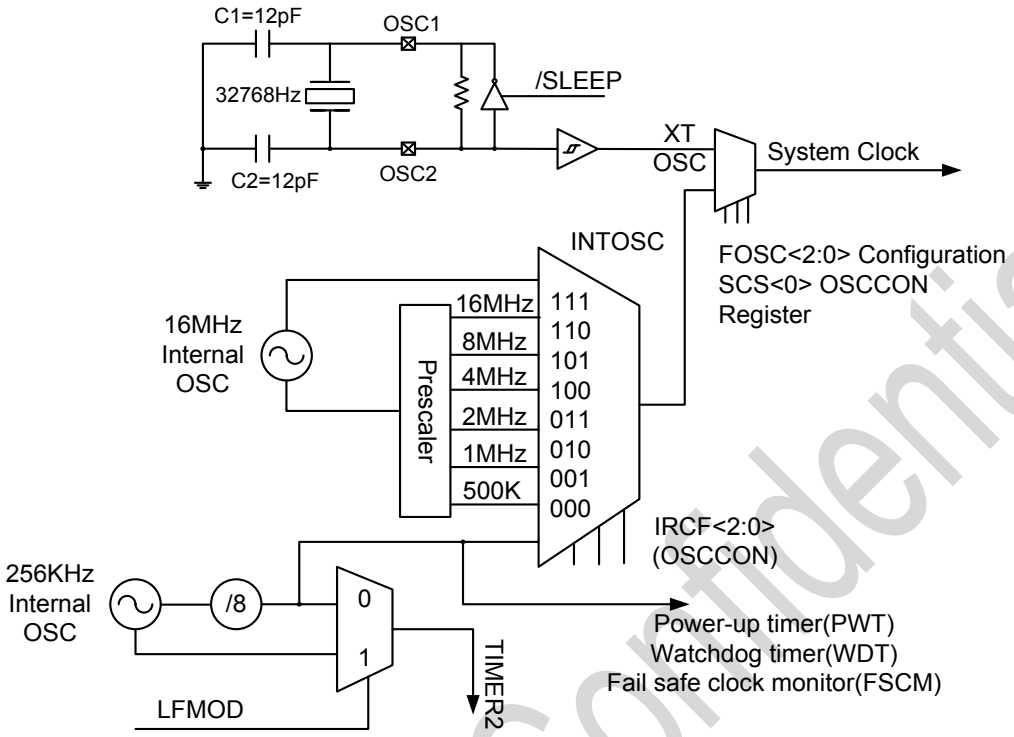


Figure 5-1. System Clock Source Diagram

The chip contains three clock sources: two built-in oscillators as variousclock sources, and one external clock input source.The built-in oscillator includes one internal 16M high-frequency precise oscillator (HFINTOSC), and one internal 32K/256Klow-frequency and low-power oscillator(LFINTOSC).These clocks or oscillators, combined with prescaler, can provide the system with a variety of frequency clock sources. The prescaler ratio of the system clock source can be controlled by the IRCF<2:0> bit in the OPTION register.

Note:
The watchdog, the system clock source (IRCF=000) and the PWRT use the output uniformlyafter 8 frequency division, that is32KHz, regardless of the value of the LFMOD.

5.1 Clock Source Mode

The clock source mode includes the external mode and the internal mode.

- The external clock mode relies on the external circuit forthe clock source, such as the external clock EC mode, the crystal resonator XT and LP mode.
- The internal clock mode is built in the oscillator module. The oscillator module has a 16MHz high frequency oscillator and a 32KHz low frequency oscillator.

The internal or external clock source can be selected by the system clock selection bit(SCS) of the OSCCON register.

5.2 External Clock Mode

5.2.1 EC Mode

The external clock mode allows the external logic level as the system clock source. When working in this mode, the external clock source is connected to the OSC1 input.

When the EC mode is selected, the oscillator start-up timer (OST) is prohibited. Therefore, there is no delay in the operation after Power-on Reset (POR) or wake-up from Sleep. When MCU is awakened, the external clock is restarted, and the device is restored to work as if it has not stopped.

5.2.2 LP and XT Modes

The LP and XT modes support the use of quartz crystal resonators or ceramic resonators connected to the OSC1 and OSC2 pins. The mode selects a low or high gain settings of the internal inverter-amplifier to support various resonator types and speeds.

LP oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least in the two modes. The mode design is only suited to drive the 32.768KHz tuning fork type crystals (clock crystal oscillator).

XT oscillator mode selects the high gain setting of the internal inverter-amplifier.

5.3 Internal Clock Mode

The oscillator mode has two independent internal oscillators, which can be configured or selected as the system clock source.

1. The high frequency internal oscillator(HFINTOSC) has been calibrated when out of the factory, and the operating frequency is 16MHz.

2. The low frequency internal oscillator(LFINTOSC) is uncalibrated and operates at 32KHz. The Internal Oscillator Frequency Select bitI RCF<2:0> can be operated to select the system clock speed via software.

The system clock can be selected between the external or internal clock source via System Clock Select bit (SCS) of the OSCCON register.

Note:
The LFMOD of the OSCCON register can select LFINTOSC as 32KHz or 256KHz, but the watchdog is fixed with 32KHz, regardless of the LFMOD value.

5.3.1 Frequency Selection Bit（IRCF）

The output of 16MHz HFINTOSC and 32KHz LFINTOSC is connected to the prescaler and multiplexer (see Figure 5-1).The OSCCON register's internal oscillator frequency selection bit IRCF<2:0> is used to select the frequency output of the internal oscillator. Select one of the following eight frequencies via the software:

- 16MHz
- 8MHz
- 4MHz (Default value after reset)
- 2MHz
- 1MHz
- 500KHz
- 250KHz
- 32KHz

5.3.2 Clock Switch Timing of HFINTOSC and LFINTOSC

When switching between LFINTOSC and HFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-2).In this case, there is a delay after the IRCF bit of the OSCCON register is modified before the frequency selection takes place.The LTS and HTS bits of the OSCCON register will reflect the current active status of the LFINTOSC and HFINTOSC oscillators. The frequency selection timing is as follows:

1. The IRCF<2:0> bit of the OSCCON register is modified.
2. If the new clock is shut down, start a clock start-up delay.
3. The clock switch circuit waits for the arrival of the falling edge of the current clock.
4. Hold CLKOUT to low, the clock switch circuit waits for the arrival of the falling edge oftwo new clocks.
5. CLKOUT is now connected with the new clock, and the HTS and LTS bits of the OSCCON register are updated as required.
6. Clock switch is completed.

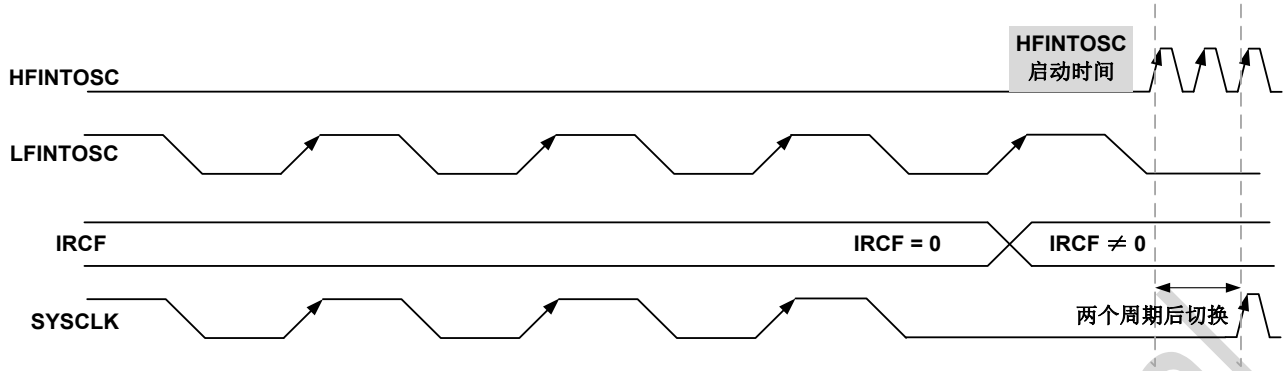


Figure 5-2. Switch from Slow Clock to Fast Clock Diagram

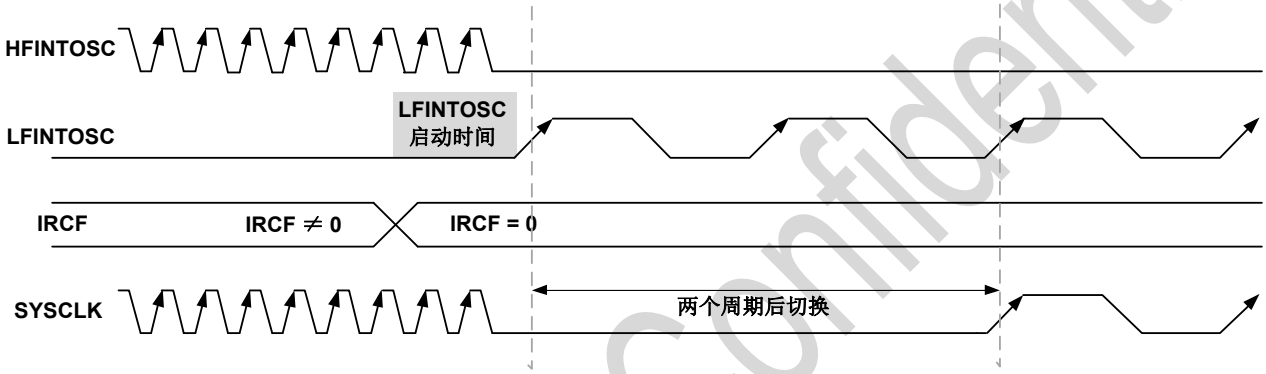


Figure 5-3. Switch from Fast Clock to Slow Clock Diagram

5.4 Clock Switching

The System Clock Select bit (SCS) of the OSCCON register is operated via software, and the system clock source can be switched between the external and internal clock sources.

5.4.1 System Clock Select Bit (SCS)

The System Clock Select bit (SCS)of the OSCCON register selectsthe system clock sourcethat is used for the CPU and peripherals.

- When the System Clock Select bit (SCS)of the OSCCON register is 0, the system clock source is determined by configuration of the FOSC<2:0> bit in the Configuration Word register (UCFG0).
- When the System Clock Select bit (SCS)of the OSCCON register is 1, the system clock source is selected according to the internal oscillator frequency selected by the IRCF<2:0> bit of the OSCCON register.After aReset, SCS is always cleared.

Note:
Any clock switching caused by the hardware (possibly from Two-Speed Start-up or Fail-Safe Clock Monitor) will not update the SCS bit of the OSCCON register.The user should monitor the OSTS bit of the OSCCON register to determine the current system clock source.

5.4.2 Oscillator Start-up Timeout Status(OSTS) Bit

The Oscillator Start-up Timeout Status (OSTS) bit of the OSCCON register is used to indicate whether the system clock is from the external clock source or from the internal clock source.The external clock source is defined by the FOSC<2:0> bit in the Configuration Word register (UCFG0). OSTS also indicates whether the Oscillator Start-up Timer (OST) is timeout in the LP or XT mode.

5.5 Two-Speed Clock Start-up Mode

Two-Speed Start-upMode reduces the power consumption further by minimizing the latency between the external oscillator and the code execution.For using the sleep mode frequently, Two-Speed Start-upMode will removethe external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.This mode allows the application to wake-up from Sleep, use INTOSC as a clock source to execute several instructions, and then go back to the Sleep status without waiting for the stability of primary oscillator.

Note:
Executing a SLEEP instruction will abort the oscillator start-up time and clear the OSTS bit of the OSCCON register.

When the oscillator module is configured as LP mode or XT mode, enable the Oscillator Start-up Timer (OST). (See the section 5.4.2 “Oscillator Start-up Timeout Status”).OST will suspend the program execution until the 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as OST is counting.When OST count reaches 1024 and the OSTS bit of the OSCCON register is set to 1, the program will switch to the external oscillator.

5.5.1 Two-Speed Start-up Mode Configuration

Two-Speed Start-up Mode is configured by the following settings:

- Configure the IESObit in the Configuration Word register UCFG1 as 1, Internal/External Switch Over bit. (Enable the Two-Speed Start-up Mode.)
- Configure the SCS bit of the OSCCON register as 0.
- Configure the F_{OSC}<2:0> in the Configuration Word register CONFIG as the LP or XT mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after PWRT has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured as any mode except the LP or XT mode, the Two-Speed Start-up will be disabled.This is because the external clock oscillation does not require any stablilization time after POR or an exit from Sleep.

5.5.2 Two-Speed Start-up Sequence

1. Wake-up from Power-on Reset or Sleep.
2. Start executing the instructions by the internal oscillator at the frequency set in the IRCF<2:0> bit of the OSCCON register.
3. OST is enabled to count 1024 clock cycles.
4. OST is timeout and waiting for the falling edge of the internal oscillator.
5. OSTS is set to 1.
6. The system clock is held low until the arrival of the next falling edge of the new clock (LP or XT mode).
7. System clock is switched to the external clock source.

5.6 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate in the event of an oscillator failure.FSCM can detect the oscillator failure at any time after the Oscillator Start-up Timer (OST) has expired. FSCM can be enabled by setting the FCMEN bit in the Configuration Word register（UCFG1）to 1. FSCM can be used for all external oscillator modes (LP, XT and EC).

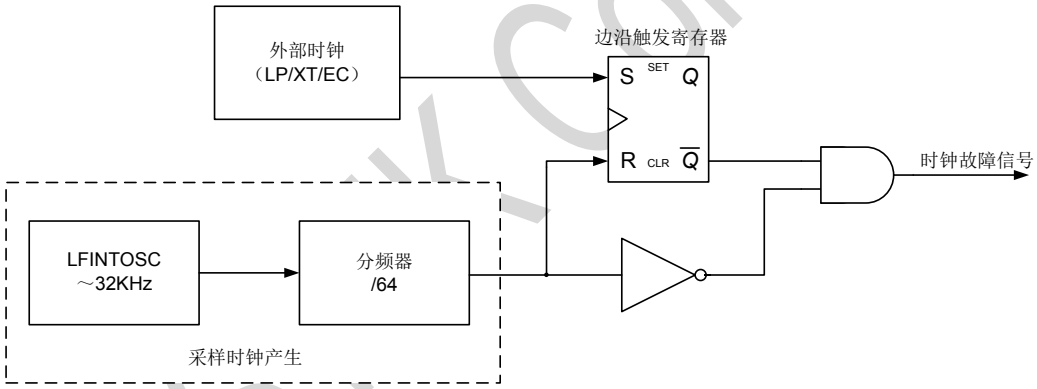


Figure 5-4. FSCM Schematic Block Diagram

5.6.1 Fail-Safe Detection

The FSCM module detects the oscillator fault by comparing the external oscillator with the FSCM sampling clock.LFINTOSC divided by 64 is the sampling clock. Please see the Figure 5-4. There is a latch inside the fault detector. On each falling edge of the external clock, the latch is set to 1. On each rising edge of the sampling clock, the latch is cleared. If the entire half cycle of the sampling clock has passed and the main clock is still not in the low level, the fault is detected.

5.6.2 Fail-Safe Operation

When the external clock fault occurs, the FSCM switches the device clock to the internal clock source, and the OSFIF flag bit of the PIR1 register is set to 1.If setting the OSFIF flag bit to 1while setting the OSFIE bit of the

PIR1 register to 1, the interrupt will be generated. The device firmware will take the measure to alleviate the problem caused by the fault clock.The system clock will continue to come from the internal clock source until the device firmware restarts the external oscillator successfully and switches back to the external operation. The internal clock source selected by FSCM is determined by the IRCF<2:0>bit of the OSCCON register. It can be configured before the fault occurs.

5.6.3 Fail-Safe Condition Being Cleared

The Fail-Safe condition is cleared after a reset, the execution of a SLEEP instruction or a flipping of the SCS bit of the OSCCON register. After the SCS bit of the OSCCON register is modified, the OST will be restarted. When OST runs, the device continues to operate with the INTOSC selected by the OSCCON. After the OST is timeout, the Fail-Safe condition is cleared and the device will operate with the external clock source.The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

5.6.4 Reset or Wake-up from Sleep

FSCM is designed to detect the oscillator fault at any time after the Oscillator Start-upTimer (OST) has expired. OST is suitable for Wake-up from Sleep or any type of Reset. OST can't be used in the EC clock mode, so once the Reset or Wake-up is done, FSCM is in the active status.When FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, when OST runs, the program is always in the operation.

Note:
Because the range of oscillator start-up time varies greatly, the Fail-Safe circuit is not active during the oscillation start-up period (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit of the OSCCON register to verify whether the oscillator has successfully started and whether the system clock has been switched successfully.

6 Reset Timing

CMT2189B has several different resets:

1. Power-on Reset(POR)
2. WDT Reset during normal operation
3. WDT Wake-up during Sleep
4. /MCLR Reset during normal operation
5. /MCLR Reset during Sleep
6. Brown-out Reset（BOR/LVR）
7. Error instruction Reset (Disable)

Some registers are not affected in any Reset condition.The status of these registers is unknown on POR, and is not affected by the Reset event.Most of the other registers are restored to their "reset status" at the time of the following reset event.

- Power-on Reset(POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- /MCLR Resetduring normal operation
- Brown-out Reset（BOR）
- Error instruction Reset

WDT (watchdog) Sleep Wake-up will not cause the reset caused by the timeout of the WDT (watchdog) during normal operation. Because WDT Sleep Wake-up itself means that MCU continues to run rather than clear the settings of the /TO and /PD bits.The reset action under different conditions is different. See Table 6-1 and Table 6-2 in details.

The /MCLRB pin corresponding circuit has the anti shake function. It can filter the sharp pulse signal caused by the interference. The following figure is the overall block diagram of the reset circuit:

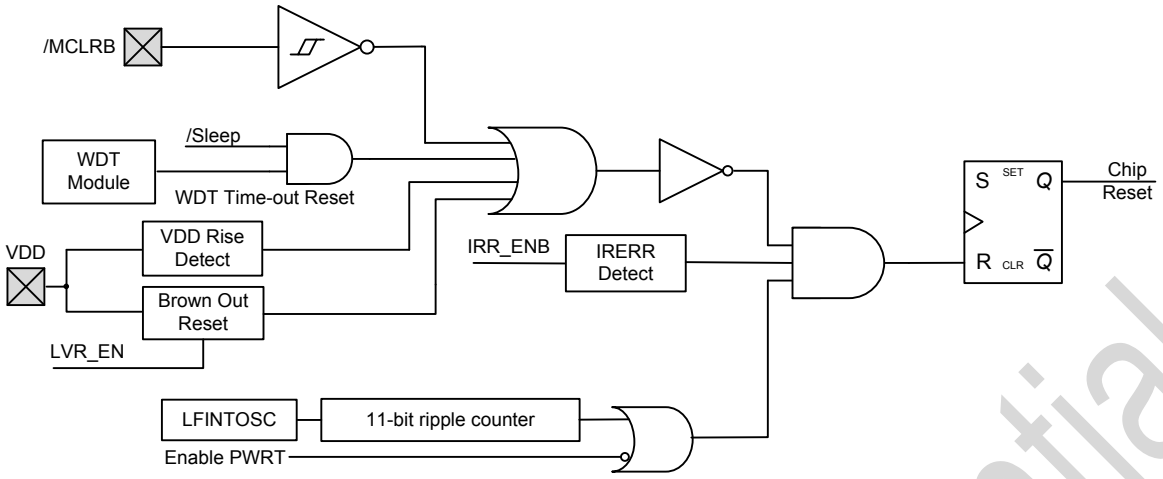


Figure6-1. Reset Function Block Diagram

6.1 Power-on Reset (POR)

The on-chip POR circuit will hold the chip in the Reset status until the VDD has reached a high enough level. In order to take advantage of the POR, the user can simply connect the /MCLR pin through a resistor to VDD. This will eliminate the external RC Reset circuit, but a maximum rise time for VDD is required. After the power-up is done, the system reset will not be released immediately, and a delay of about 8ms is needed, while the digital circuit is held in the reset status.

6.2 External Reset (MCLR)

It should be noted that a WDT Reset does not pull the /MCLRB pin down. Voltages applied to the pin that exceed its specification (such as ESD event) can result in both /MCLRB Reset and excessive current beyond the device specification. Therefore, we recommend that users no longer connect /MCLRB to VDD directly with one resistor but use the following circuit.

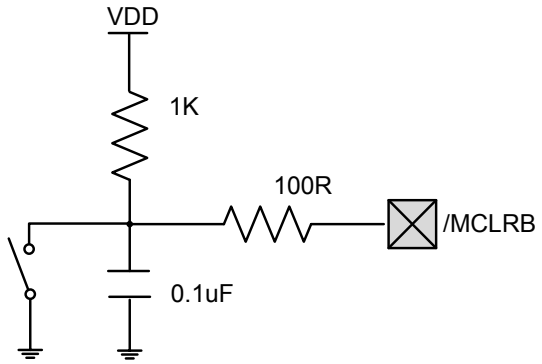


Figure 6-2. External Reset Reference Circuit Diagram

The chip's CONFIG OPTION register (UCFG0) has a MCLRE Enable bit. When this bit is 0, the reset signal is generated inside the chip. When this bit is 1, the PA5/MCLR pin of the chip becomes the external reset pin.In this mode, the /MCLR pin has a Weak-Pull on the VDD.

6.3 Power-up Timer (PWRT)

PWRT provides a fixed 64ms timing(normal) for Power-on Reset and Brown-out Reset.This timer is driven by an internal slow clock.The chip is held in a reset status before the timeout of the timer.This time ensures that the VDD will rise to a sufficiently high voltage to make the system work properly.PWRT can also be enabled by the system CONFIG register (UCFG0).When the low voltage reset function is opened, the user should also open the PWRT.The PWRT timing is triggered by the VDD voltage exceeding the VBOR threshold. It is also important to note that the actual time varies with the conditions of temperature and voltage due to the internal slow clock drive. This time is not a precise parameter.

6.4 Brown-out Reset (BOR（LVR）)

Low Voltage Reset is controlled by UCFG1<1:0> bit.Low voltage reset refers to the reset that the power supply voltage is lower than the VBOR threshold voltage. However, low voltage reset may not occur when the VDD voltage is lower than VBOR and the time does not exceed TBOR.The VBOR voltage needs to be calibrated before the chip is shipped.The calibration can be completed by writing the internal calibration register through the serial port.If the BOR (Brown-out Reset) is enabled (UCFG1<1:0>=00), the requirement for the maximum VDD voltage rising time will not exist.The BOR circuit will control the chip in the reset status until the VDD voltage exceeds the VBOR threshold voltage. It is important to note that the POR circuit does not generate a reset signal when the VDD is lower than the threshold of the system that can work normally.If the reset signal is generated by the BOR circuit, the VDD voltage must hold for more than 100us at the VSS level.

6.5 Error Instruction Reset

When the instruction register of CPU obtains the undefined instruction, the system will be reset. Using this function can increase the anti-interference ability of the system.

6.6 Timeout Action

During the power up process, the timeout action sequence inside the chip is executed according to the following process: Start the PWRT timing after POR. Because the timing is started at the end of the POR pulse, if the /MCLR holds long enough in the low level status, the timeout event will take place. If the /MCLR is pulled up, the CPU will start immediately. This will be useful when testing or requiring multiple MCU synchronization.

PCON（Power Control Register）

There are two status bits in the PCON register to indicate what type of Reset has occurred. Bit0 is the /BOR bit, which is an unknown status on Power-on Reset, and the software must set it to 1 and check if it is 0. Bit1 is the /POR bit, which is 0 on Power-on Reset, and the software must set it to 1.

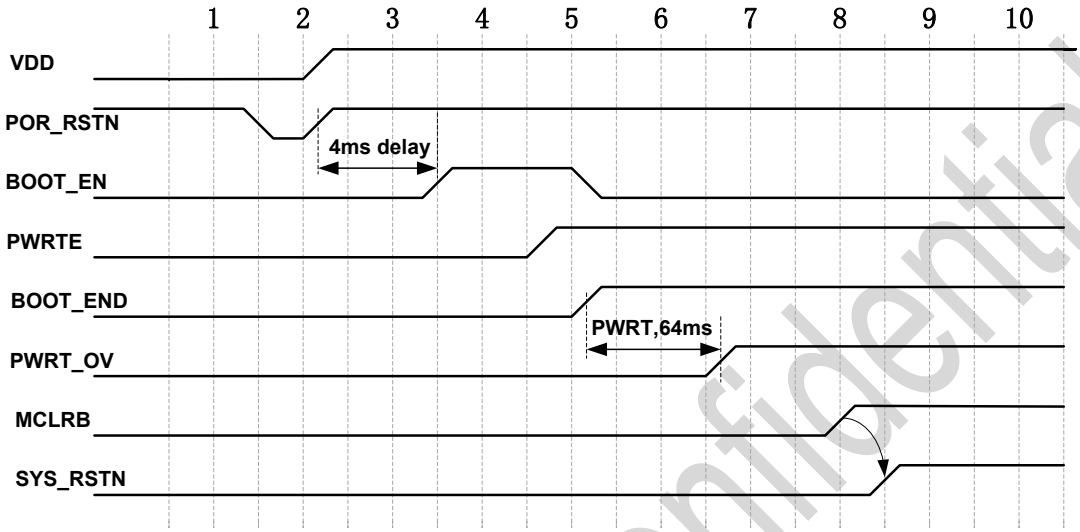


Figure 6-3. Power-on Reset with MCLRB

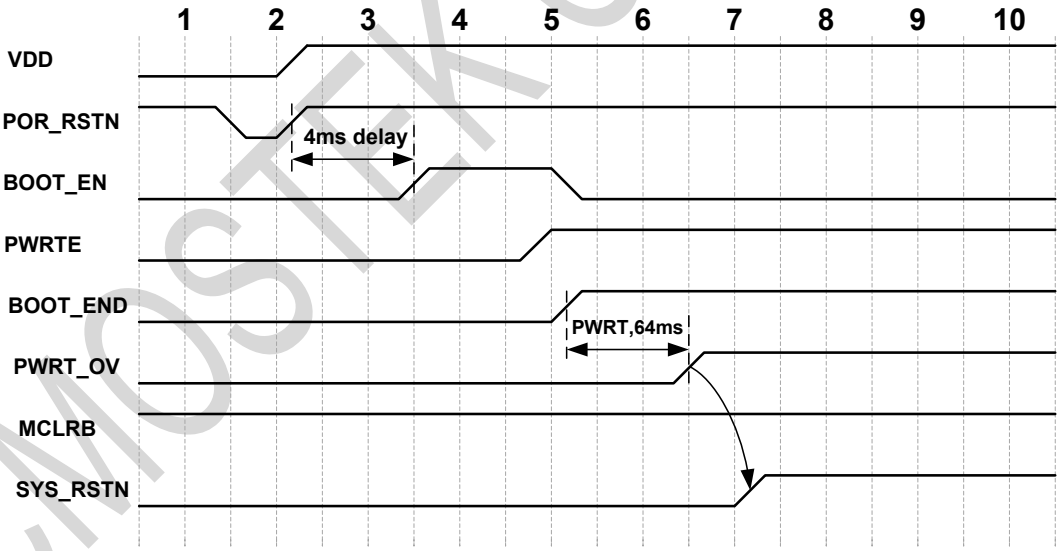


Figure 6-4. Power-on Reset without MCLRB

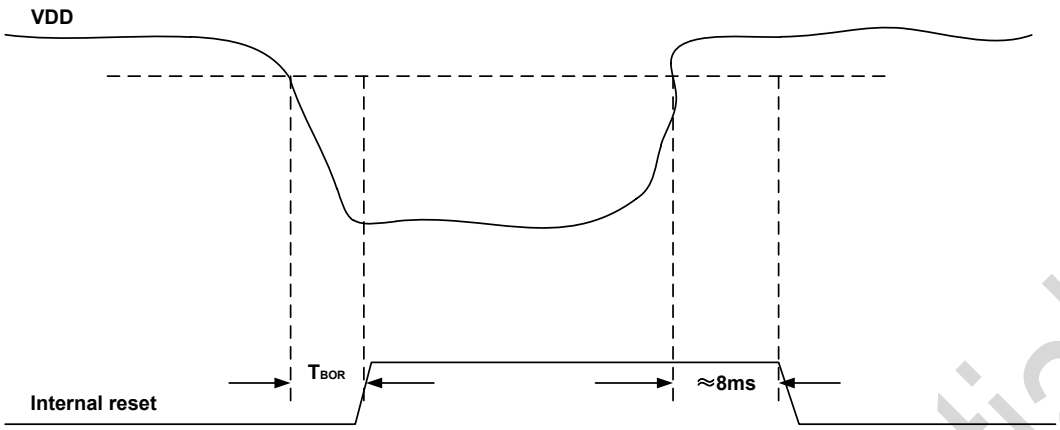


Figure 6-5. BOR Reset

Note:

1. After POR or BOR, and when PWRTEB (UCFG0.4) is low, PWRT is active. It is 2048 internal slow clock cycles, about 64ms.
2. The TBOR time is about 157us.
3. After the voltage is restored to normal, the internal reset will not be released immediately, but wait for about 8ms.

Table 6-1. Timeout in a Variety of Cases

Oscillator configuration	Power-on Reset		Brown-out Reset		Sleep Wake-up
	/PWRTEB=0	/PWRTEB=1	/PWRTEB=0	/PWRTEB=1	
INTOSC	TPWRT	-	TPWRT	-	-

Table 6-2. STATUS/PCON Bit and Significance（U-No change，X-Unknown）

/POR	/BOR	/TO	/PD	Condition
0	X	1	1	POR
U	0	1	1	BOR
U	U	0	U	WDT Reset
U	U	0	0	WDT Wake-up
U	U	U	U	/MCLR Reset during normal operation
U	U	1	0	/MCLR Reset during Sleep

7 BOOT

After POR or BOR, inserting a status, the unit of EEPROM is mapped into a configuration register.The address of EEPROM starts from 2000H. The system reset is released until the end of the BOOT, as shown in Figure 6-3 and Figure 6-4.The process needs about 14us.

8 Watchdog Timer

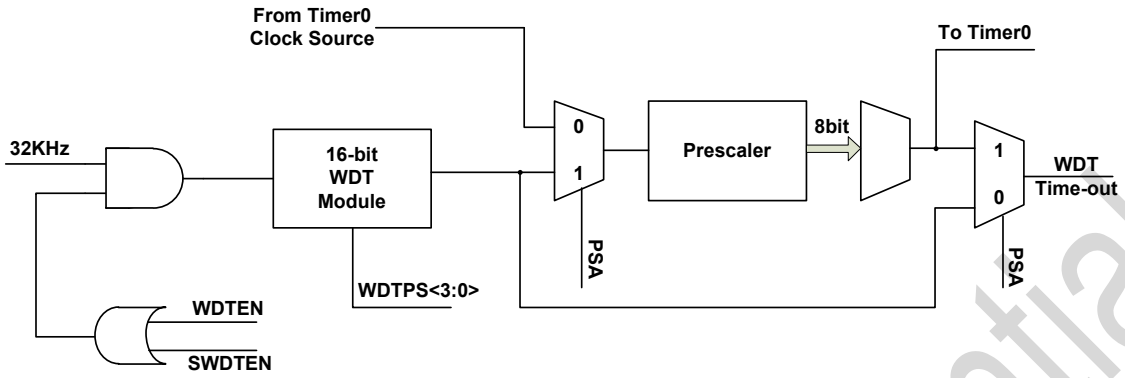


Figure 8-1. Watchdog and Timer0 Diagram

The watchdog's clock source is the internal slow clock (32KHz), which is a 16-bit counter.It shares a 8-bit prescaler with the timer0. The enabled bit WDTEN is the third bit of the configuration register UCFG0. When WDTEN is 1, enable the watchdog. When it is 0, disable the watchdog. It is determined by the BOOT during the power start-up process, or it can be written through the external serial port.Clearing the watchdog instruction CLRWDT and SLEEP will clear the watchdog counter. In the case of enabling the watchdog, the watchdog overflowing can be used as a wake-up source when the MCU is in sleep, and the watchdog can be used as a reset source when the MCU works well.

Table 8-1. Watchdog Status

Condition	Watchdog Status
WDTEN and SWDTEN are 0 at the same time	Clear
CLRWDT instruction	
Enter the SLEEP, exit the SLEEP	

Note:
If the internal slow clock switches from 32K to 256K mode (or vice versa from 256K to 32K mode), it doesn't affect the watchdog timing, because WDT is fixed to use the 32K clock source.

9 Timer0

9.1 Timer0 Introduction

The timer0 is 8-bit and can be configured as the counter or the timer.When it is the external event (T0CKI) counter, it can count on the rising edge or the falling edge. When it is the timer, the counting clock is 2 frequency division of the system clock, that is, it increases once in each instruction cycle.There is an 8-bit prescaler shared with WDT. When the PSA bit is 0, the prescaler is assigned to the timer0.
Note: When the value of PSA is changed, the hardware will automatically clear the prescaler.

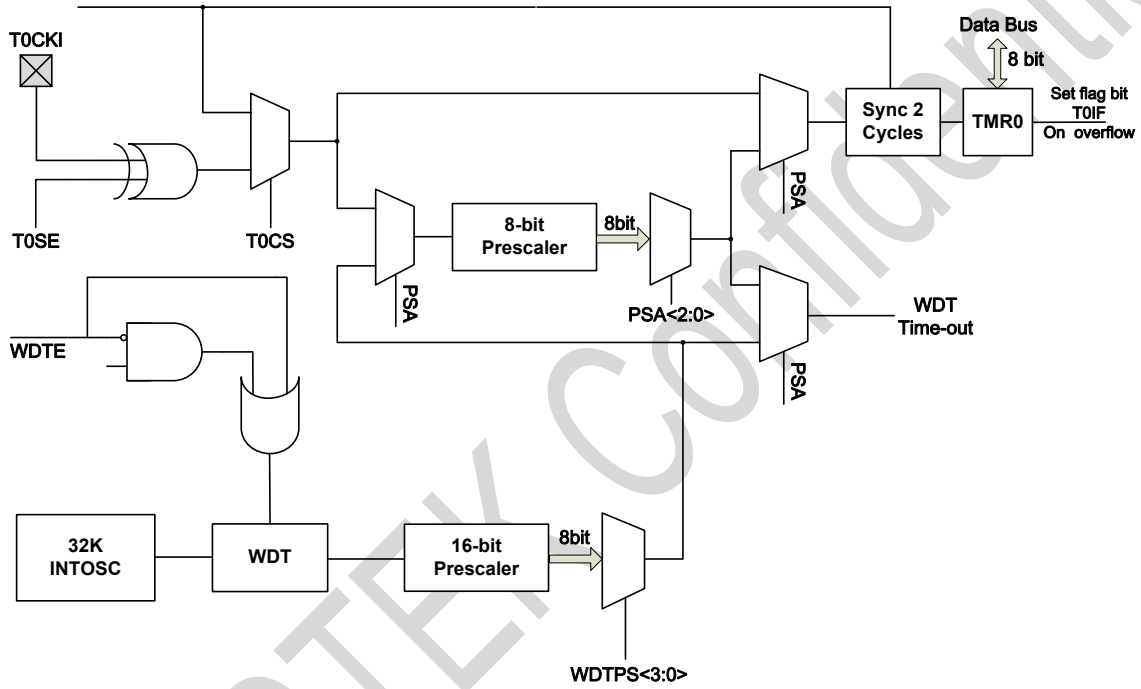


Figure 9-1. Watchdog and Timer0 Diagram

9.2 Timer0 Timer Mode

In this mode, the timer0 adds 1 (without prescaler) in each instruction cycle.The software can clear the T0CS bit of the OPTION register to enter the timer mode.When the software writes to TMR0, the timer does not increase progressively in the following 2 cycles.

9.3 Timer0 Counter Mode

In this mode, the timer0 adds 1 when it is triggered by the rising or falling edge of each T0CKI pin (without prescaler). The T0SE bit of the OPTION register determines which edge to be triggered. The software can set the T0CS bit of OPTION register to 1 to enter the counter mode.

9.3.1 Software Configuring Prescaler Circuit

The chip has a prescaler circuit in front of the Timer0 and WDT timer, which can be assigned to Timer0 or WDT timer, but the two can not use the prescaler at the same time. Specifically assigning to Timer0 or WDT is determined by the PSA bit of the OPTION register. When the PSA is 0, the prescaler is assigned to Timer0. In the Timer0 prescaler mode, there are 8 prescale rate (1:2 to 1:256). It can be set by the PS<2:0> bit of the OPTION register.

Note:

1. The prescaler circuit is neither readable nor writable. Any write operation to the TMR0 register will clear the prescaler circuit.
2. When the prescaler circuit is assigned to WDT, one CLRWDT instruction can clear the prescaler circuit.
3. The prescaler circuit can be assigned to Timer0 or WDT timer, the switching of the prescaler between the timer0 and the WDT may result in a false reset.

When the prescaler assignment is switched from TMR0 to WDT, please execute the following instruction sequence.

```
BANKSEL   TMR0
CLRWDT                          ；Clear WDT
CLRR      TMR0                  ；Clear TMR0 and prescaler
BANKSEL   OPTION_REG
BSR       OPTION_REG,  PSA      ；Select WDT
CLRWDT

LDWI      b'11111000'；Mask prescaler bits
ANDWR     OPTION_REG,  W
IORWI     b'00000101'；Set WDT prescaler to 1:32
LDWI      OPTION_REG
```

When the prescalerassignment is switched from WDT to TMR0, please execute the following instruction sequence.

```
CLRWDT                          ；Clear WDT and prescaler
BANKSEL   OPTION_REG
LDWI      b'11110000'；Mask TMR0 select and prescaler bits
ANDWR     OPTION_REG,  W
IORWI     b'00000011'；Set prescaler to 1:16
STR       OPTION_REG
```

9.3.2 Timer0 Interrupt

An interrupt is generated (if enabling the interrupt) and the T0IF bit is set when the TMR0 timer overflows from

0xFF to 0x00.

Note:
Timer0 interrupt cannot wake up the CPU from Sleep since the timer is shut off during Sleep.

9.3.3 Drive Timer0 with the External Clock

In the counter mode, the synchronization between T0CKI pin input and Timer0 register is accomplished by sampling the output on the Q1 and Q2 cycles of the internal clock phase, so the high level time and low level time of the external clock source cycle must meet the relevant timing requirement.

10 Timer2

The timer2 is the 8-bit timer, which contains the following functions:

- 8-bit timer register
- 8-bit period register
- Interrupt on TMR2 match with PR2
- Software programmable prescaler(1:1，1:4，1:16)
- Software programmable postscaler(1:1 to 1:16)

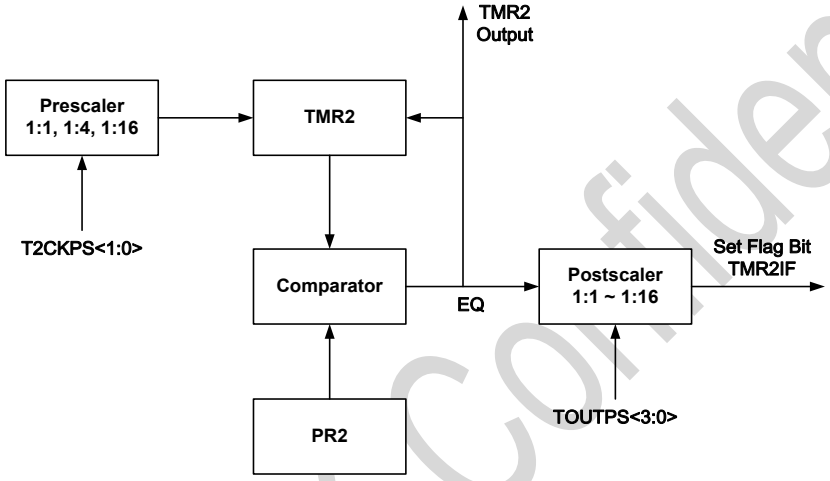


Figure 10-1. Timer2 Diagram

Timer2 Operation Principle

The clock input of the Timer2 module is the system instruction clock (FOSC/2).The clock is sent to the Timer2 prescaler, and its prescale rate has three options of 1:1, 1:4 and 1:16. The output of the prescaler is used to increase the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when to match.TMR2 will increase from 00h until it matches PR2. The following two cases will occur when matching:

- TMR2 is reset to 0x00 on the next incrementcycle
- Timer2 postscale rate increases progressively.

The matching output of comparing Timer2andPR2 is sent to the Timer2 postscaler.The option range of the postscaler is from 1:1 to 1:16. The output of the Timer2 postscaler is used to set the interrupt flag bit TMR2IF of the PIR1 register to 1.

Note:

1. Both TMR2 and PR2 are read-write registers. Their values are initialized to 0 and 0xFF respectively upon

Reset.

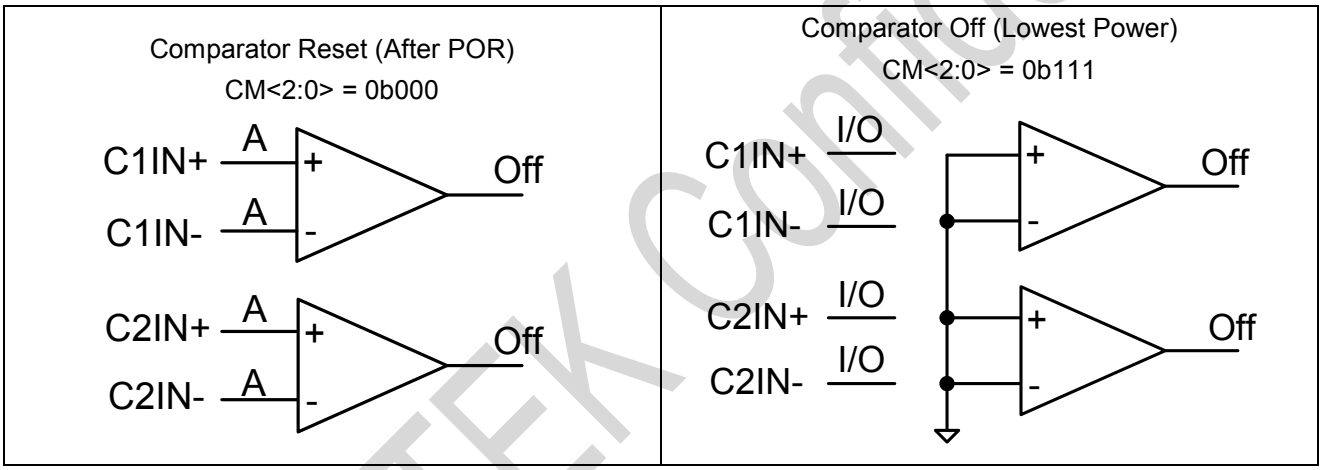
2. Setting the TMR2ON bit of the T2CON register to 1 can open Timer2, and conversely clearing the TMR2ON bit can close the Timer2.
3. The Timer2 prescaler is controlled by the T2CKPS bit of the T2CON register.
4. The Timer2 postscaler is controlled by the TOUTPS bit of the T2CON register.
5. The prescalercounter and postscaler counter will be cleared when the following register is written:
   - Write TMR2
   - Write T2CON
   - Any Reset action
6. Writing T2CON does not clear the TMR2 register.

11 Comparator

The chip is integrated with two analog comparators. Since the function pins of the comparator2 are used for the RF serial control bus at the same time, the two comparators can not be used.

It should be noted that when reading a port register, the value that the software read is 0 if the pin is configured as an analog signal pin.When the pin is set to the digital input pin, the comparator will still think that the pin will input an analog signal and output the corresponding result.If a pin is set to the digital input, and the actual voltage on this pin is still an analog voltage, it may cause the input buffer circuit to consume more current than that in the specifications.

The analog comparator has eight configuration modes. They are selected by the CM<2:0> bit of the CMCON0 register. Because the functional pins are used in the RF serial control bus, there are only two statuses as follows:



- Analog function (A): The digital input cache is shielded.
- Digital function (D): The comparator digital output will cover the other functions in the pin
- Normal port function (I/O): Be independent of the comparator.

When the word "A" is marked on the port, the status of the current pin or the statusof the TRIS bit of the I/O control register will return to 0 when reading.The user should set the TRIS bit corresponding to the the analog input pin to 1 to close its digital output drive circuit.

When the word "D" is marked on the port, the user should set the corresponding TRIS bit to 0 to open the digital output driver circuit.

In addition, the comparator configuration switching should mask the comparator interrupt to avoid unnecessary mistrigger events.

12 Data EEPROM

The chip is integrated with 256 Bytes of EEPROM, which is accessed through the EEADR. The software can program EEPROM through EECON1 and EECON2. The hardware implements its own timing function of erasing and programming without software query, and saves the limited code space.At the same time, using this feature, after starting the programming cycle, the chip can enter the sleep mode to reduce the power consumption.

The following initialization operations must be performed before the data EEPROM is used(either read or write):Two times 0xAA is written for a certain unit of EEPROM that is not used, and the subsequent program no longer operates on this unit. Such as:

```
SYSTEM_INIT
……
……
LDWI      0x55
STR       EEROM_ADDR
LDWI      0xAA
STR       EEPROM_DATA
LCALL     EEPROM_WRITE
LCALL     EEPROM_WRITE
```

Programming data EEPROM steps

In order to read the data memory unit, the user must write the address into the EEADR register, and then set the control bit RD of the EECON1 register to 1. In the next cycle that follows, the user can write the EEPROM data into the EEDAT register.This data can therefore be read by the next instruction. EEDAT will keep this value until the user reads or writes data to the unit next time (during the write operation).

```
BANKSEL   EEADR
LDWI      dest_addr
STR       EEADR
BSR       EECON1,   RD
LDR       EEDAT,    W
```

13 Clock Measurement

This function can accurately measure the internal slow clock period.

In this mode, the prescaler and postscaler configuration of TIMER2 is automatically changed to 1:1. They make up a 12-bit timer. The TIMER2 count clock is the system clock Fosc, not the instruction clock Fosc/2 under the ordinary mode.After the end of the count, the result is automatically stored in the SOSCPR register. The unit is the number of the system clock Fosc.

Operation steps:

1. In order to improve the measurement accuracy, it is suggested that IRCF is set to 111 and SCS is set to 1, and the system clock of 16M is selected.
2. Set T2CON.2 to 1, enable TIMER2.
3. If selecting the average of the four times, set MSCKCON.2 to 1, and otherwise clear it.
4. Set MSCKCON.1, start measuring.
5. After the end of the measurement, MSCKCON.1 is automatically cleared, and the interrupt flag is set to 1.
6. The user can end the measurement in a query or interrupt manner.
7. When the interrupt flag is checked to be 1, the read SOSCPR is the final result.

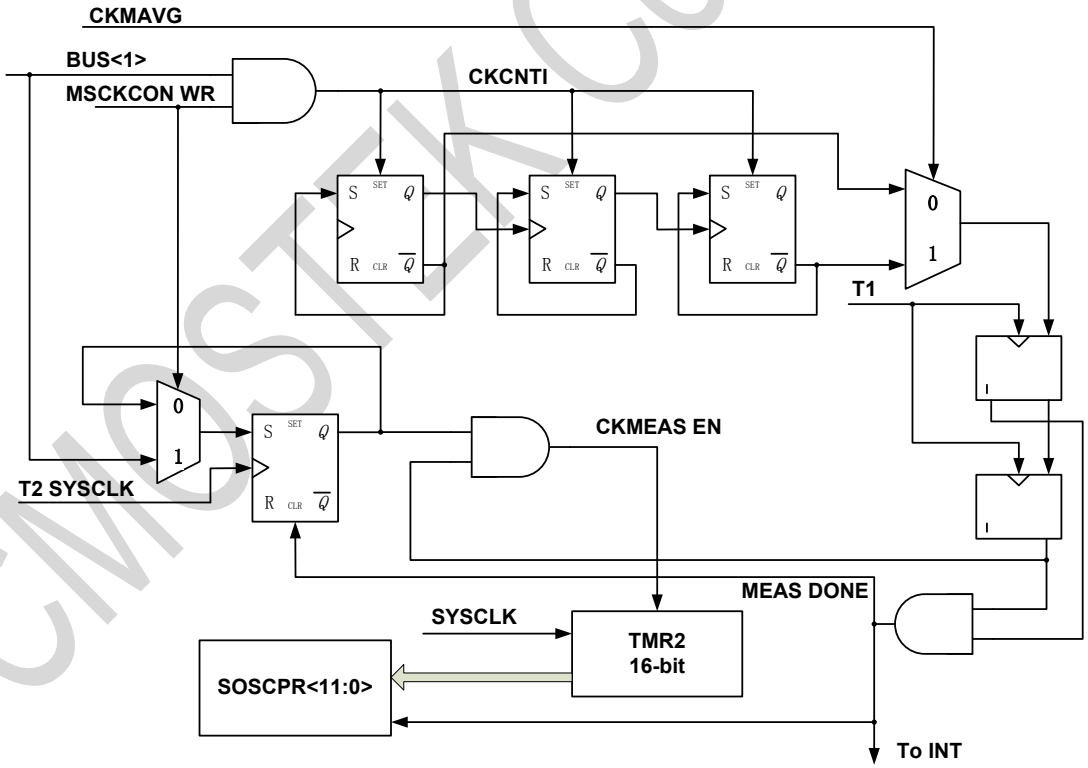


Figure 13-1. Slow Clock Measurement Mode Block Diagram

14 Interrupt Mode

CMT2189B has the following interrupt sources:

- External Interrupt PA2/INT
- Timer0 Overflow Interrupt
- PORTA Change Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- Comparator Interrupt

The Interrupt Control Register (INTCON) and the Peripheral Interrupt Request Register (PIR1) record the interrupt flag bit. INTCON also contains the Global Interrupt Enable bit GIE.

When the interrupt is served, the following action occurs automatically:

- GIE is cleared to close the interrupt.
- The return address is pushed onto the stack.
- The program pointer is loaded to the 0004h address.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enable unmasked interrupt.

The INTCON register contains the following interrupt flag bit:

- INT pin interrupt
- PORTA change interrupt
- Timer0 overflow interrupt

PIR1 includes the peripheral interrupt flag bit. PIE1 includes its corresponding interrupt enable bit.

14.1 INT Interrupt

The external interrupt of the INT pin is triggered by the edge. When the INTEDG bit of the OPTION register is set to 1, it is triggered on the rising edge. And when the INTEDG bit is cleared, it is triggered on the falling edge. When an effective edge occurs on the INT pin, the INTF bit of the INTCON register is set to 1. The interrupt can be disabled by clearing the INTE control bit of the INTCON register. Before the interrupt is reallowed, the INTF bit must be cleared by the software in the interrupt service program. If the INTE bit is set to 1 before entering the sleep status, the INT interrupt can wake up the MCU from the sleep status.

Note:
When INT interrupt is used, the ANSEL and CM2CON0 registers must be initialized so that the analog

channel is configured as a digital input.The pin configured as an analog input is always read to 0.

14.2 PORTA Level Change Interrupt

The input change on PORTA can set the PAIF bit of the INTCON register. The interrupt can be enabled or disabled by setting/clearing the PAIE bit. In addition, each pin of the port can be configured through the IOCA register.

Note:

1. When using the PORTA level changeinterrupt, the ANSEL and CM2CON0 registers must be initialized so that the analog channel is configured as a digital input.The pin configured as an analog input is always read to 0.
2. When initializing the level change interrupt, first configure it as a digital input IO, and set the corresponding IOCA to 1, and then read the PORTA.
3. When the IO level changes, the PAIF bit is set to 1.
4. Read the PORTA before clearing the interrupt flag, and then clear the PAIF.

14.3 Interrupt Response

The external interrupt includes the interrupt from the INT pin or the PORTA change interrupt, and the interrupt delay is usually 1 to 2 instruction cycles. It depends on the actual situation of the interrupt.

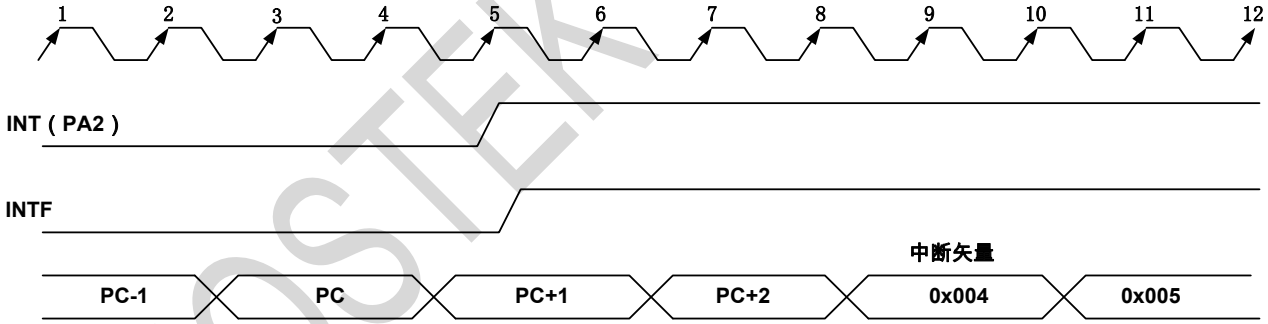


Figure 14-1. Interrupt Response Timing Diagram

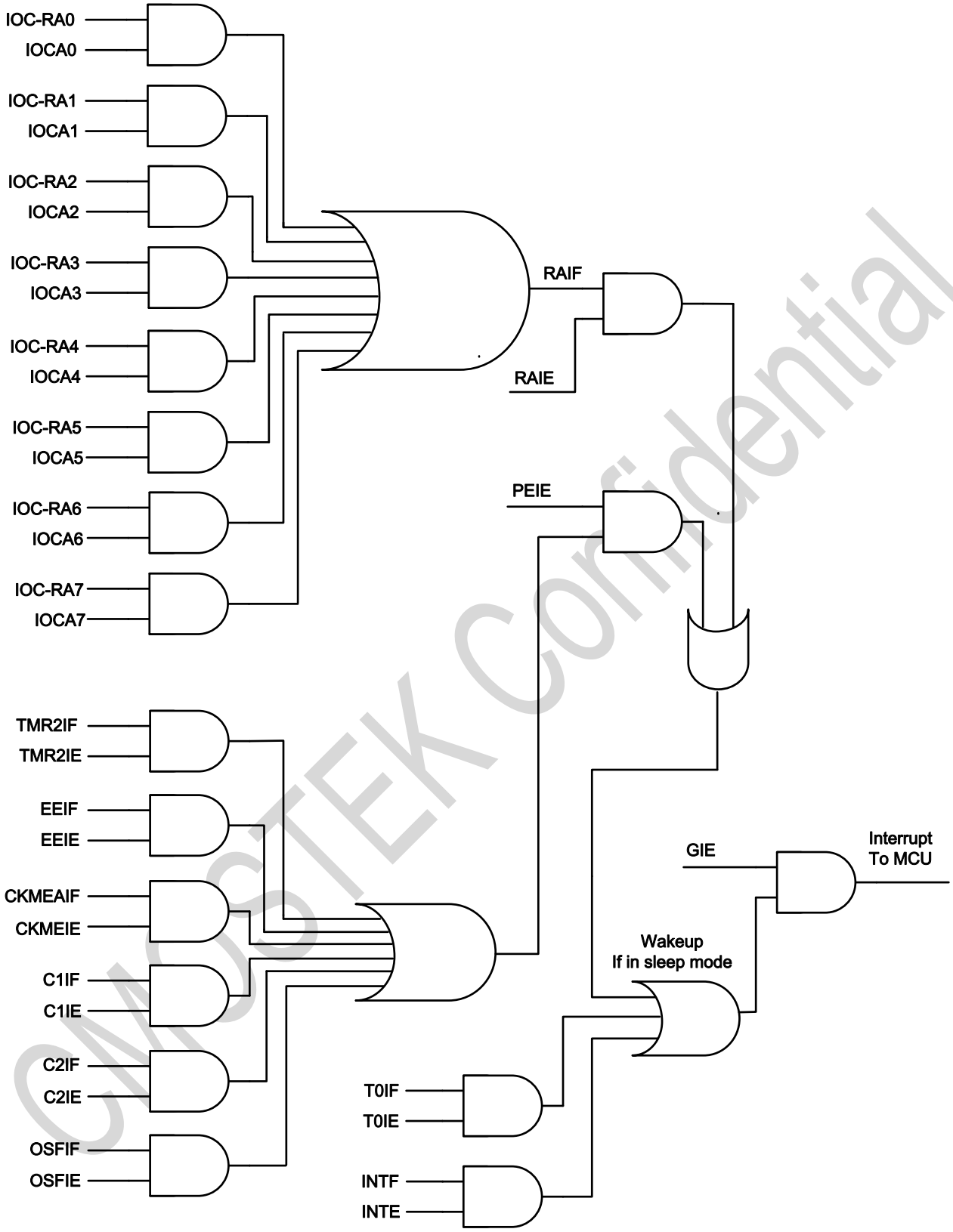


Figure 14-2. Interrupt Generation Circuit Block Diagram

14.4 Context Saving During Interrupts

During an interrupt, only the return PC is automatically saved on the stack.In general, users may wish to save the key register value on the stack, such as W, STATUS register, and so on. These must be implemented in software. The temporary registers W_TEMP and STATUS_TEMP should be placed in the last 16 Bytes of the GPR.The 16 Bytes of GPR cross two pages, so users can save a little bit of code space.

15 MCU Sleep Saving Mode

The chip enters the sleep status after the execution of the SLEEP instruction.

In order to achieve the lowest sleep power consumption, the software should set all IO to high or low, and there is no the external circuitconsumption from the IO pin. I/O is the input pin, and the external circuit should pull it high or low to avoid flipping the level and increasing the power consumption. /MCLR should be set to high level.

In order to achieve the lowest power consumption, it is recommended that when the configuration is the crystal mode or external clock mode, the clock loss detection is turned off, that is, the FCMEN bit of UCFG1 is cleared. Meanwhile, the configuration bit CM<2:0> of the comparator is written as 0b111, and the comparator module is closed.

15.1 Wake-up Mode

The following events can wake up the chip:

- There is an external reset on the /MCLR pin.
- WDT is timeout
- There is the interrupt on the PA2/INT pin. There is the PORTA change interrupt or other peripheral interrupt.

Clearing watchdog (CLRWDT), entering the sleep mode (SLEEP) or waking up the sleep mode will clear the watchdog counter.

15.2 Watchdog Wake-up

The watchdog works in the internal slow clock (32KHz). It is a 16-bit counter, and shares an 8-bit prescaler with the timer0. Enable bit is the third bit WDTEN of the configuration register UCFG0. When it is 1, enable the watchdog; when it is 0, whether or not to enablethe watchdog is determined by the SWDTEN bit. SWDTEN is located in the WDTCON register.

Clearing watchdog (CLRWDT) and SLEEP instruction will clear the watchdog counter.

When enabling the watchdog, the watchdog overflowing event can be used as a wake-up source when MCU is in Sleep, while it can be used as a reset source when MCU works normally.

16 I/O Port

There are 16 GPIO portsin the chip. But limited to the packagesize, only 6 IO ports of PORTA<7:0>have the package terminals (except for PA6 and PA5), PC4 and PC6 of PORTC have the package terminals, and the others inside the chip have no the package terminals. In addition to being an ordinary input / output port, these IO ports usually have some functions to communicate with the kernel peripheral circuits, see the following in details.

16.1 PORTA Port and TRISA Register

PORTA is a 8-bit bi-directional port.The corresponding data direction register is TRISA. However, it is important to note that the fifth bit is not used here because PORTA<5> is a single input directional port.Setting a certain bit to "1" in the TRISA register will set the corresponding PORTA port as the input port (at this time, the output driver will be turned off). Conversely, setting a certain bit to "0" will set the corresponding PORTA port as the output port.When configurated as the output port, the output drive circuit is opened and the data in the output register will be sent to the output port.When reading the PORTA, the PORTA content will reflectthe status of the input port.When writing the PORTA, the PORTA content will be written to the output register.All operations follow the "read-modify-write" micro process, namely the data is read, and then is modified, and then is written to the output register.When MCLRE is 1, the value read from PORTA<5> is 0, which is as the external reset pin at this time.

16.2 Other Functions of the Port

Each port of the PORTA has a status change interrupt option and a weak pull-up option.

16.2.1 Weak Pull-Up

Each port of the PORTA (except for PORTA<5>) has an internal weak pull-up function that can be set individually. Controlling the bit of the WPUAx register can enable or turn off the weak pull-up circuit.When the GPIO is set as output, these weak pull-up circuits are automatically turned off.The weak pull-up circuit can be turned off during the power-upreset period.This is determined by the /PAPU bit of the OPTION register.There is also a weak pull-up function inside PORTA<5>. The weak pull-up function will be automatically enabled when the PORTA<5> is set as /MCLR.When the PORTA<5> is set as GPIO, the weak pull-up circuit will be automatically turned off.

16.2.2 Interrupt-On-Change

Each port of the PORTA can be separately set as an interrupt source (interrupt-on-change). Controlling the bitof the IOCAx register can enable or turn off the interrupts of these ports. The interrupt-on-change is invalid on Power-on Reset.

When enabling the interrupt-on-change function, the current port level value is compared to the old value of the data register read by the last reading action.All error matching results will be OR to form an interrupt flag bit. The PAIF flag bit of the INTCON register can wake the chip from the sleep status. The user needs to execute the following program to clear the flag bit:

1. A read or write operation to the PORTA will end any mismatched status;
2. Clear the PAIF flag bit.

The error matching result will always set the PAIF bit. Reading the PORTA once can end any status of error matching and clear the PAIF bit. The last read value kept in the data register will not be affected by /MCLR or BOR. As long as the error matching status exists, the PAIF bit is set to 1.

16.3 Port Description

Each port of PORTA and PORTC contains different reuse functions. Its specific functions and controls are described in this section.

16.3.1 PORTA<2:0>

The following figure describes the internal circuit architecture of the port, and PA<2:0> can be configured as the following functional port:

- GPIO
- Debug serial clock (PA0)
- Debug serial data (PA1)
- External interrupt input (PA2)
- Timer0 external clock source (PA2)

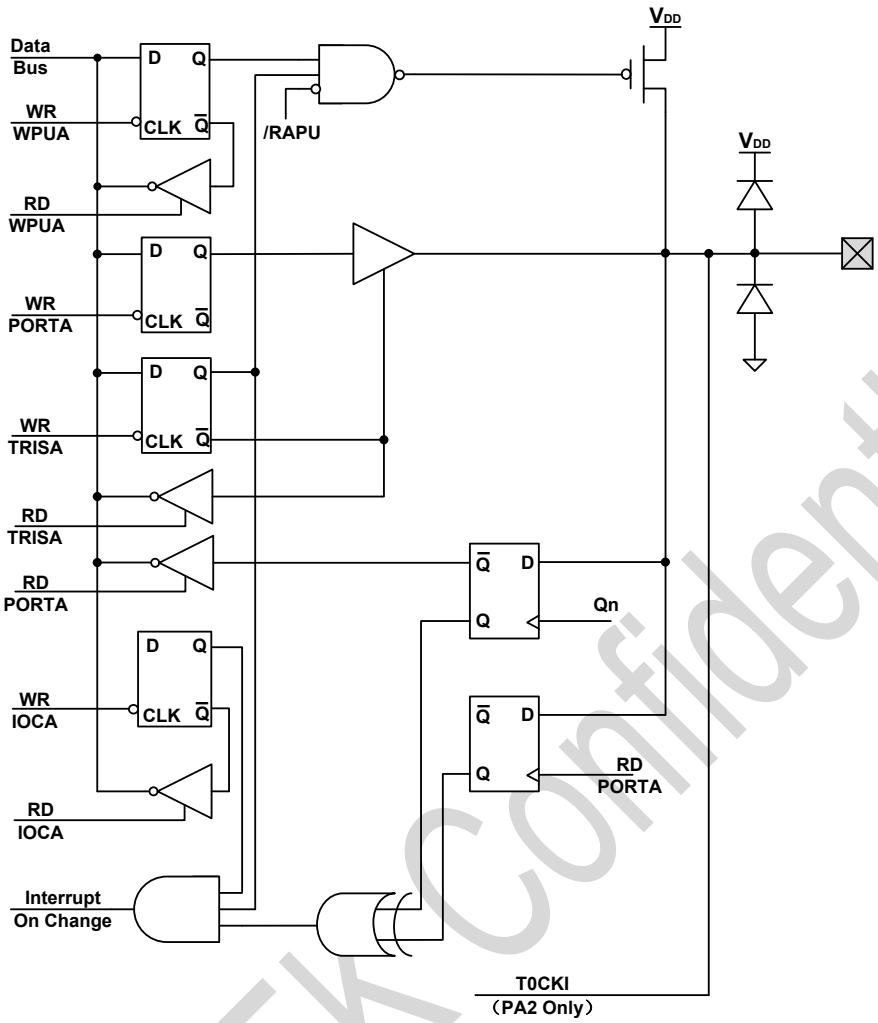


Figure 16-1. PA<2:0> Architecture Block Diagram

16.3.2 PORTA3/PA3

The following figure describes the internal circuit architecture of the port, and PA3 can be configured as the following functional port:

- GPIO

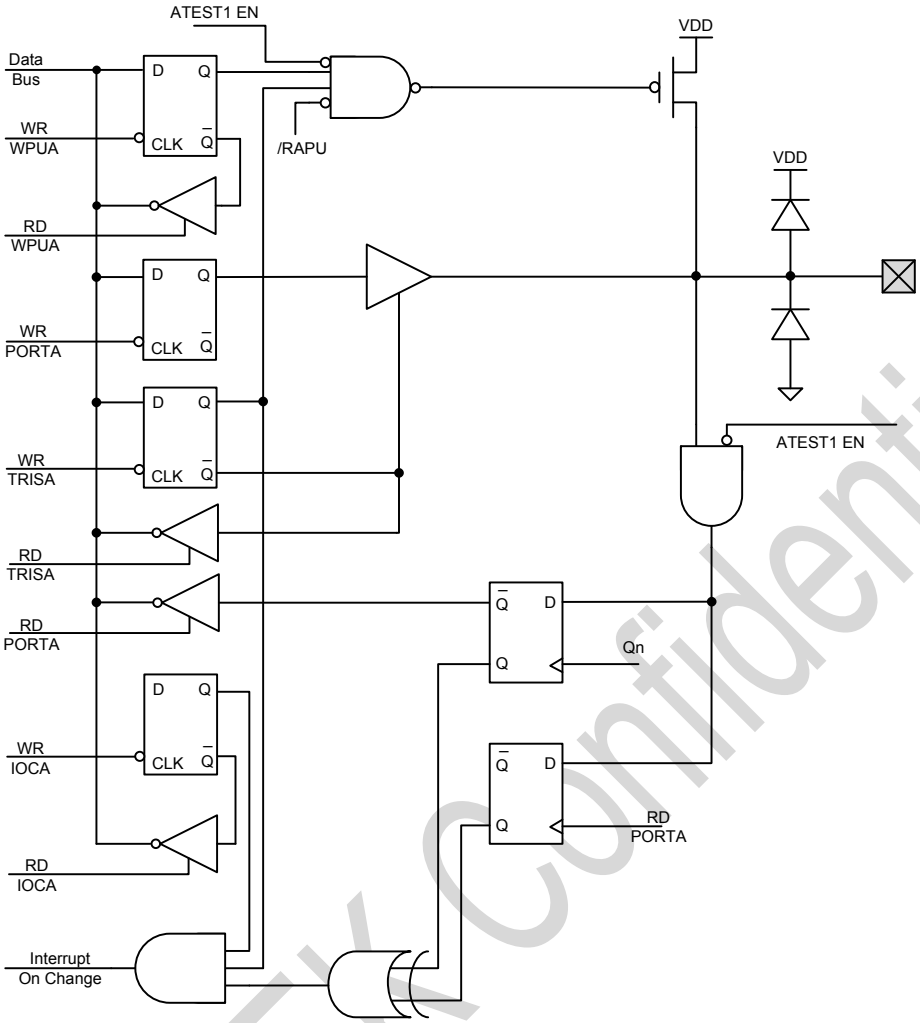


Figure 16-2. PA3 Architecture Block Diagram

Note: ATEST1 is used for the internal test, not open to users, and users can ignore it.

16.3.3 PORTA4/PA4

The following figure describes the internal circuit architecture of the port, PA4 can be configured as the following functional ports

- GPIO

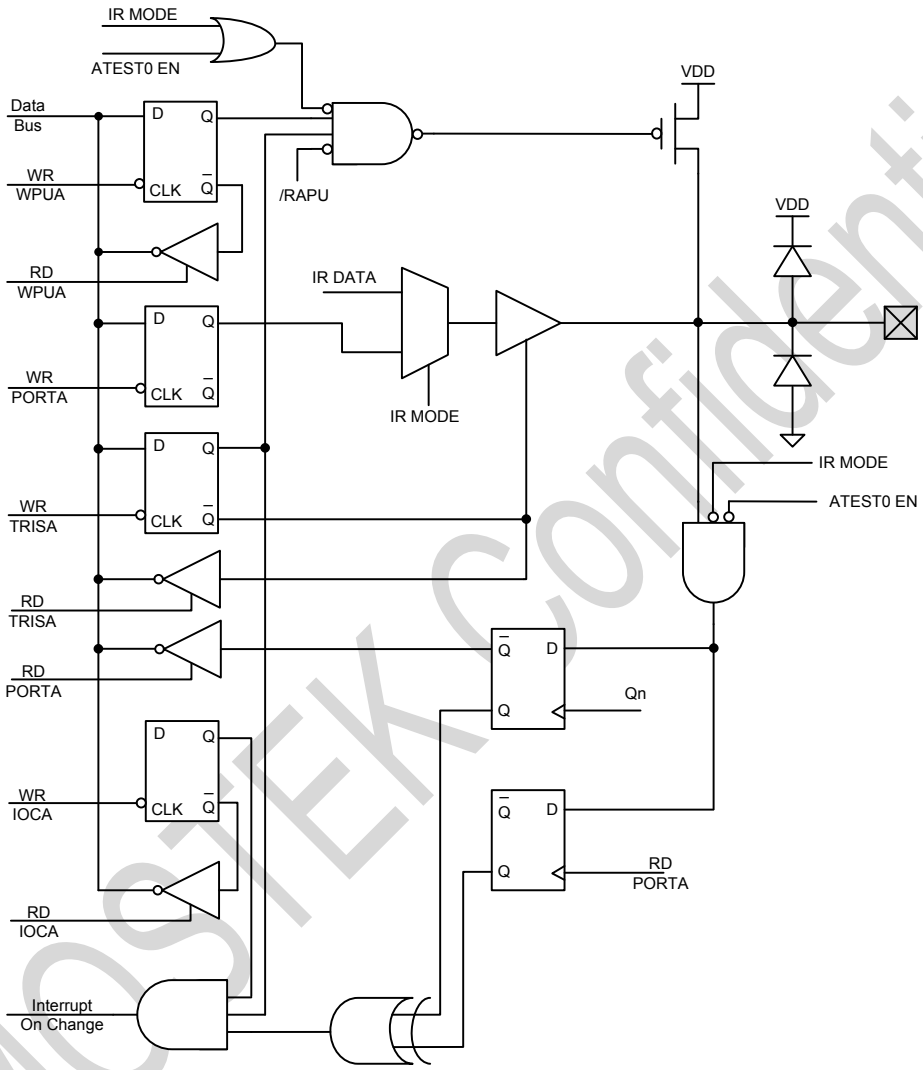


Figure 16-3. PA4 Architecture Block Diagram

Note: ATEST0 and IR are used for the internal test, not open to users, and users can ignore them.

16.3.4 PORTA5/PA5

PA5 has no the package terminal because of package size, so the user can only configure it as the internal Reset through the UCFG configuration, and it is not recommended to be configured as an external Reset.

16.3.5 PORTA7/PA7

The following figure describes the internal circuit architecture of the port; PA7 can be configured as the following functional ports:

- GPIO
- Crystal oscillator and resonator connection
- Clock input

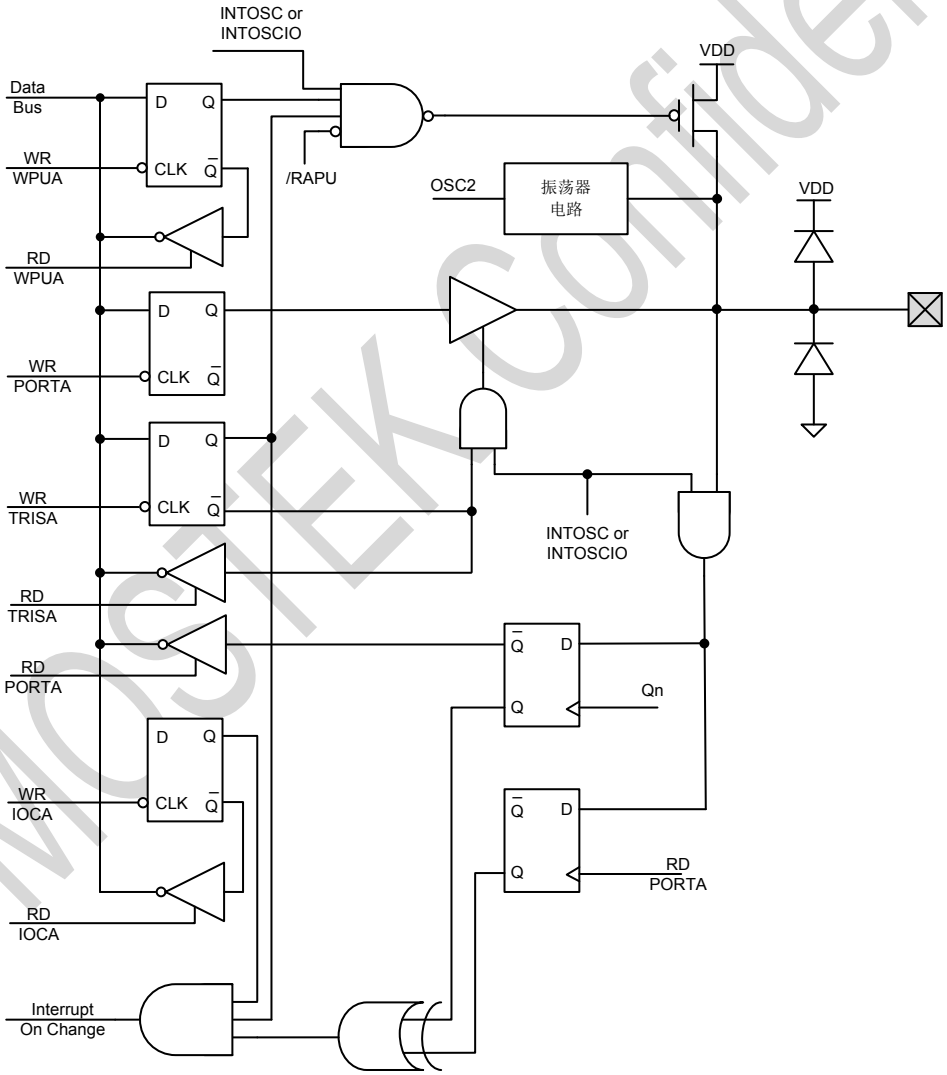


Figure 16-4. PA7 Architecture Block Diagram

16.3.6 PORTC<7:0>

The following figure describes the internal circuit architecture of the port;PC7~PC0 can be configured as the following functional ports:

- GPIO
- RFDIN, that is the RF direct mode data input (only PC0)
- SCLK, that is the serial clock of the RF part SPI(only PC2)
- CSB, that is the chip selection bar of RF part SPI (only PC3)
- SDIO, that is the serial data of RF part SPI (only PC4)
- Comparator input (only PC0 and PC1, but not available, because it is used to control the RF part)
- Comparator output (only PC4, but not available, because it is used to control the RF part)

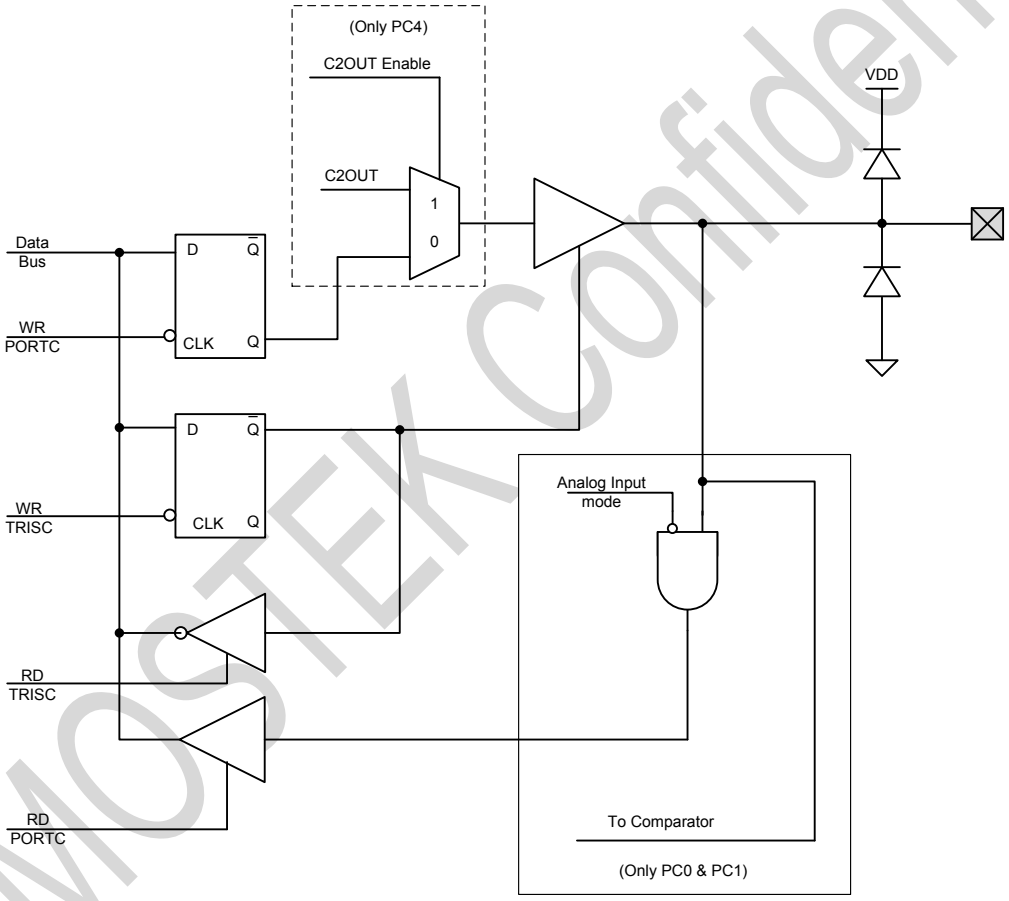


Figure 16-5. PC7~PC0 Architecture Block Diagram

17 Instruction Set List

CMT2189B uses the reduced instruction set architecture with a total of 37 instructions, and the following is the description of the instructions.

Table 17-1. Instruction Set Table

CMT	Instruction Period	Function	Operation	Status
BCR R, b	1	Bit clear	0-> R(b)	NONE
BSR R, b	1	Bit set	1-> R(b)	NONE
BTSC R, b	1（2）	Bit test, skip if 0	Skip if R(b)=0	NONE
BTSS R, b	1（2）	Bit test, skip if 1	Skip if R(b)=1	NONE
NOP	1	No operation	None	NONE
CLRWDT	1	Clear WDT	0-> WDT	/PF, /TF
SLEEP	1	ENTER SLEEPMODE	0-> WDT, STOP OSC	/PF, /TF
STTMD	1	Store W TO TMODE	W-> TMODE	NONE
CTLIO R	1	Control IO direction reg	W-> IODIRr	NONE
STR R	1	Store W to reg	W-> R	NONE
LDR R, d	1	Load reg to d	R-> d	Z
SWAPR R,d	1	Swap halves reg	[R(0-3)R(4-7)]-> d	NONE
INCR R, d	1	Increment reg	R+ 1-> d	Z
INCRSZ R, d	1（2）	Increment reg, skip if 0	R+ 1-> d	NONE
ADDWR R, d	1	Add W and reg	W+ R-> d	C, HC, Z
SUBWR R, d	1	Sub W from reg	R- W-> d R+ /W+ 1-> d	C, HC, Z
DECR R, d	1	Decrement reg	R- 1-> d	Z
DECRSZ R, d	1（2）	Decrement reg, skip if 0	R- 1-> d	NONE
ANDWR R, d	1	AND W and reg	R& W-> d	Z
IORWR R, d	1	Inclu.OR W and reg	W| R-> d	Z
XORWR R, d	1	Exclu.OR W and reg	W^ R-> d	Z
COMR R, d	1	Complement reg	/R-> d	Z
RRR R, d	1	Rotate right reg	R(n)-> R(n-1), C-> R(7), R(0)-> C	C
RLR R, d	1	Rotate left reg	R(n)-> R(n+1), C-> R(0), R(7)-> C	C
CLRW	1	Clear working reg	0-> W	Z
CLRR R	1	Clear reg	0-> R	Z
RETI	2	Return from interrupt	Stack-> PC,1-> GIE	NONE
RET	2	Return from subroutine	Stack-> PC	NONE
LCALL N	2	Long CALL subroutine	N-> PC, PC+1-> Stack	NONE
LJUMP N	2	Long JUMP address	N-> PC	NONE
LDWI I	1	Load immediate to W	I-> W	NONE
ANDWI I	1	AND W and imm	W& I-> W	Z
IORWI I	1	Inclu.OR W and imm	W| I-> W	Z
XORWI I	1	Exclu.OR W and imm	W^ I-> W	Z

CMT	Instruction Period	Function	Operation	Status
RETW I	2	Return, place imm to W	Stack-> PC, I-> W	NONE
ADDWII	1	Add imm to W	W+I-> W	C, HC, Z
SUBWI I	1	Subtract W from imm	I-W-> W	C, HC, Z

Note:
The TMODE register of the chip refers to the OPTION, that is, the operation of the STTMD instruction is to save the W to OPTION.

18 Document Modification Record

Table 18-1. Document Modification Record Sheet

Version	Chapter	Modification descriptions	Date
1.0	All	Initial release	2017-11-23
1.1	2	Increase the Section 2.7.1 “Tx rate description”	2017-11-29
1.2	All	“PC4/RFDIN” is modified as “PC0/RFDIN”	2018-01-09

19 Contact Information

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