CMT2189C User Guideline

Summary

CMT2189C is a low power, high performance, Flash-based, (G) FSK / OOK RF transmitterchip.It can cover the 240MHz ~ 960MHz wireless communication band. This chip is embedded with RISC Flash type MCU. It belongs to the CMOSTEK NextGenRF™ series product. The product series include the short range wireless communication chips, such as transmitter, receiver, transceiver, SoC and so on.

The part numbers covered by this document are as shown below.

Table1. Part Number Covered by This Document

Part No.	Frequency	Modem	Tx Power	Tx Current	Configuration	Package
CMT2189C	240 - 960MHz	OOK/(G)FSK	+13dBm	32.5mA	Embedded MCU	SOP14

Note:
The test conditions for the Tx power and Tx current are at 433.92MHz and FSK mode.

Contents

1 Chip Architecture Introduction

1.1 Overall Operation Principle

CMT2189C is a MCU integrated with RF transmiterchip. It uses the crystal oscillator to provide the reference frequency and digital clock for PLL, supports the OOK modulation which data rate is from 1Kbps to 30Kbps and the (G) FSK modulationwhich data rate is from 1Kbps to 100Kbps, and supports the status control based on the MCU program. It is suitable for all kinds of low power transmitting applications.

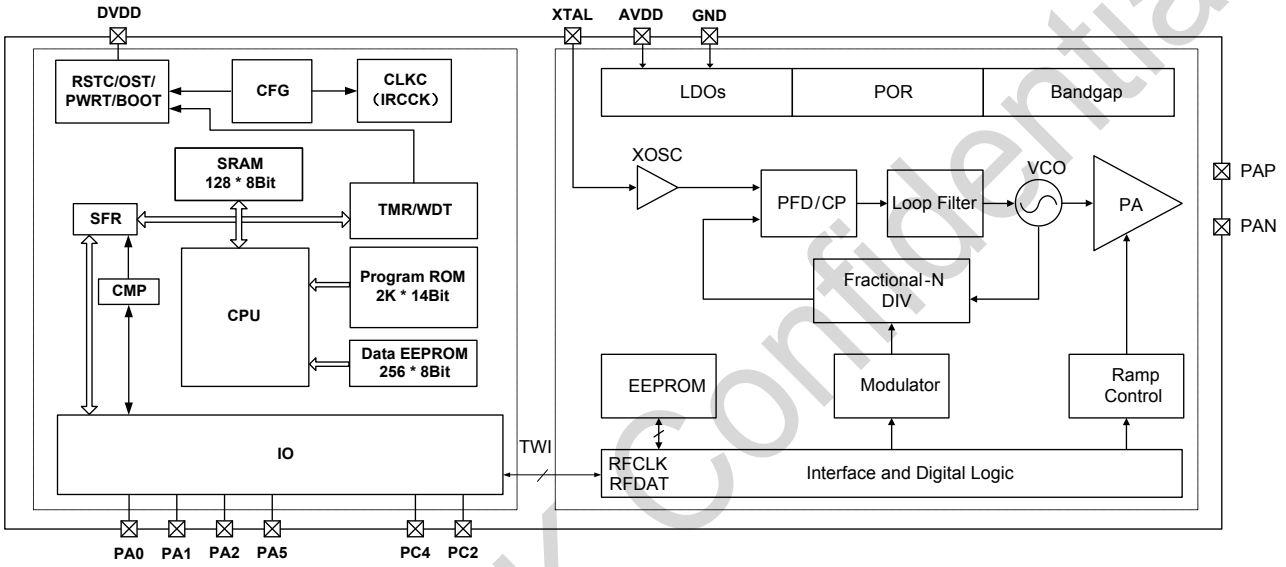


Figure 1-1. CMT2189C System Architecture

The chip uses the PLL+PA architecture to achieve the Sub-GHz wireless transmitting function. It supports the direct mode that the data inputs and transmits from the antenna. The processed data is sent to the modulator, the modulator controls PLL and PA, and the data is modulated by OOK/ (G) FSK and transmitted out.

The MCU of the chip controls the RF part by the Two-wire interface, and can achieve various status switching, mode selection and low power control.

1.2 IO Pin Description

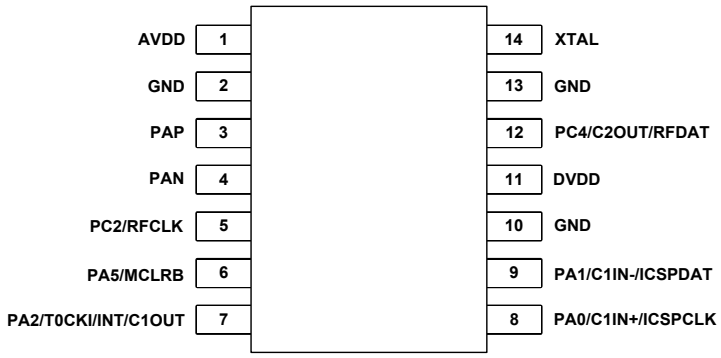


Figure 1-2. CMT2189C Pin Top View

Table 1-2. CMT2189C SOP14 Package Pin Description

Pin No.	Name	Type	I/O	Function Description	
1	AVDD	Analog	I	Chip RF power supply positive pole	
2	GND	Digital	I	Chip power supply ground	
3	PAP	Analog	O	Chip PA output +	
4	PAN	Analog	O	Chip PA output -	
5	PC2/RFCLK	Digital	IO	PC2	General IO
				RFCLK	RF communication TWI bus clock line,CLK,internal pull-up
6	PA5/MCLRB	Digital	I	PA5	Only as input, support IOC
				MCLRB	External reset input, can be configured aspull-up
7	PA2/T0CKI/INT/C1OUT	Digital	IO	PA2	General IO, support IOC, can be configured aspull-up
				T0CKI	Timer0 clock source input（Max=4MHz）
				INT	External interrupt input
				C1OUT	Comparator1 output
8	PA0/C1IN+/ICSPCLK	Digital	IO	PA0	General IO, support IOC, can be configured as pull-up
				C1IN+	Comparator 1 input +
				ICSPCLK	Debug/ burning mode, serial port clock signal
9	PA1/C1IN-/ICSPDAT	Digital	O	PA1	General IO, support IOC, can be configured as pull-up

Pin No.	Name	Type	I/O	Function Description	
				C1IN-	Comparator1 input -
				ICSPDAT	Debug/ burning mode, serial port data signal
10	GND	Digital	I	Chip power supply ground	
11	DVDD	Digital	I	Chip digital power supply positive pole	
12	PC4/C2OUT/RFDAT	Digital	IO	PC4	General IO
				C2OUT	Comparator2 output
				RFDAT	RF communication TWI bus data line, DAT, and also data transmitting pin, internal pull-down
13	GND	Digital	I	Chip power supply ground	
14	XTAL	Analog	I	RF part crystal oscillator input	

Note:

The two comparators are integrated within the MCU, but the internal comparator can not be used because they have the package terminals and some of them are reused to the RF part at the same time. However, in the initialization process, MCU needs to turn off the comparator function and set its corresponding pin as the digital IO to avoid affecting the work of other functions.

2 RF Configuration and Control Mechanism

2.1 Operation Status

The RF part of CMT2189C has four main operation statuses: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

- SLEEP

In this status, the whole module of RF is in a low power status, and the internal related circuits are closed, and the consumption is only 20nA (only for the RF part).

- XO-STARTUP

In the sleep status, the RF part will start up the oscillator when it is triggered by the RFDAT edge (rising edge).

- TUNE

This status is that the frequency synthesizer tunes the oscillation frequency to the desired value.

- TRANSMIT

After the frequency synthesizer tuned the frequency to the desired value, the transmitted data is input through RFDAT to control the PA transmitting.In the transmitting process, if the time RFDAT holds a low level is longer than t_{STOP} setting time (T_{STOP} is not unique, and can be selected. the specifics refer to RFPDK and the following chapters), the RF part will automatically stop the transmitting and enter the SLEEP status.

Table 2-1.Status Switching Time

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	tXTAL		400		us
Time to Tune to Desired Frequency	tTUNE		370		us
Hold Time After Rising Edge	tHOLD	10			ns
Time to Stop the Transmission[2]	tSTOP	2		90	ms
Notes: This parameter mainly depends on the crystal itself. The range is from 2 ms to 9ms (step unit is 1ms, only for FSK), and from 20ms to 90ms (step unit is 10ms).					

2.2 Transmitting Control Timing

The RF transmitting of CMT2189C is mainly controlled by setting RFDAT (RFCLK holds the high level in the process of transmitting), and the specific timing diagram is as follows:

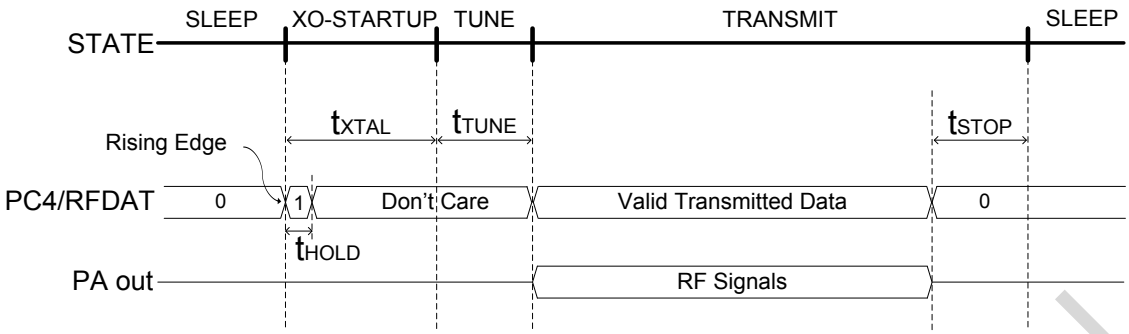


Figure 2-1. Transmitting Timing Diagram

2.3 TWI Configuration Bus（Two-wire Interface）

CMT2189C's internal integrated transmitting circuit is the same as CMT2119A. It supports any frequency of Sub-G ranging from 240MHz ~ 960MHz, and it also uses the TWI bus configuration interface.Through the TWI interface, users can allow CMT2189C to change the frequency(frequency hopping), transmitting power (amplitude), modulation mode (OOK, FSK, GFSK) by programming.

The specific operation steps are: Select CMT2119A at the RFPDK interface at first; set the required frequency, modulation mode and other parameters; click Export to generate the configuration parameters, as shown below:

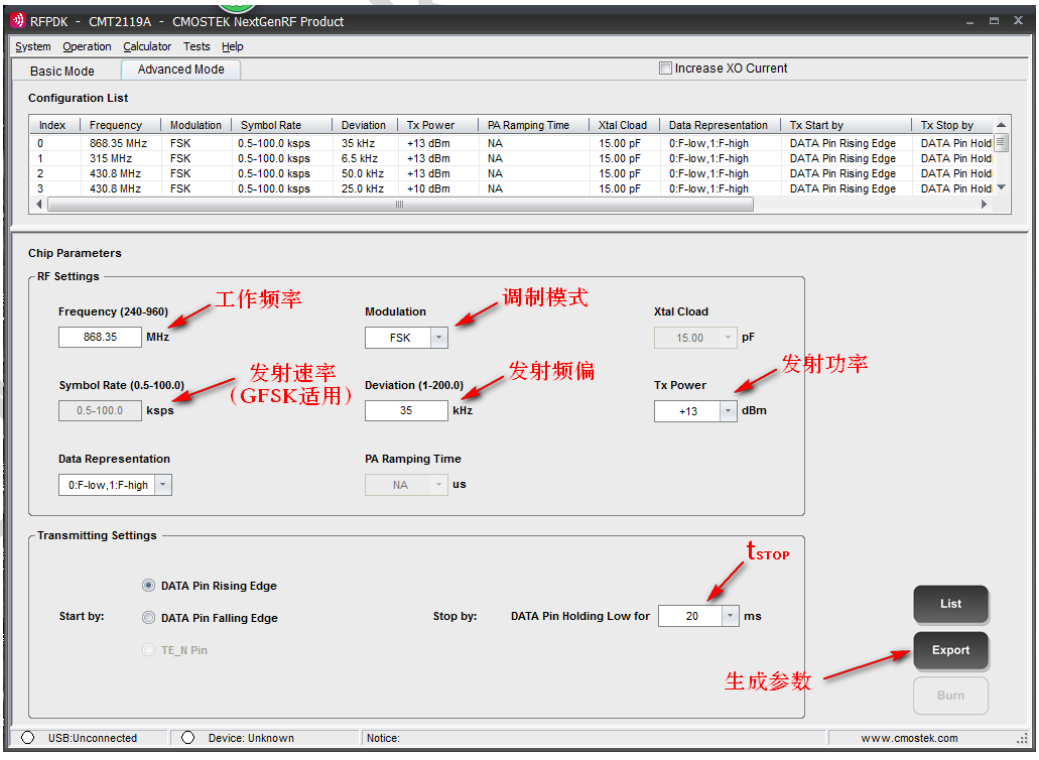


Figure2-2. RFPDK Setting Interface

Open the exp file, as shown below:

```
;---------------------------------------
;  CMT2119A Configuration File
;  Generated by CMOSTEK RFPDK 1.46 Beta
;  2017.11.12 17:02
;---------------------------------------
;  Mode                 = Advanced
;  Part Number          = CMT2119A
;  Frequency            = 868.35 MHz
;  Modulation           = GFSK
;  Symbol Rate          = 2.4 ksps
;  Tx Power             = +13 dBm
;  Deviation            = 35.0 kHz
;  PA Ramping Time      = NA
;  Xtal Cload           = 15.00 pF
;  Data Representation  = 0:F-low,1:F-high
;  Tx Start by          = DATA Pin Rising Edge
;  Tx Stop by           = DATA Pin Holding Low For 20 ms
;  Increase XO Current  = No
;  FILE CRC             = 22F9

;---------------------------------------
;  The following are the EEPROM contents
;---------------------------------------
0x007F
0x5000
0x0000
0x0000
0x0000
0xF000
0x0000
0xCBCE
0x4208
0x00B0
0xA401
0x11A0
0x8000
0x0000
0xFFFF
0x0020
0x5F1E
0xA2D6
0x0E13
0x0019
0x0000
;---------------------------------------
;  The following is the CRC result for
;  the above EEPROM contents
;---------------------------------------
0x22F9
;---------------------------------------
;  The following are for CMOSTEK
;  use, customers can ignore them
;---------------------------------------
0x000F
```

配置参数，地址按顺序从0x00～0x14

Figure 2-3. Export the parameter file

Configure the generation parameters to the RF of CMT2189C according to the software lookup mode, and then control the transmission according to the controlling sequence (see Section2.2).

2.4 TWI timing Requirement

Table 2-2. TWI timing Requirement

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	VIH		0.8			VDD
Digital Input Level Low	VIL				0.2	VDD
CLK Frequency	FCLK		10		1,000	kHz
CLK High Time	t_{CH}		500			ns
CLK Low Time	t_{CL}		500			ns
CLK Delay Time	t_{CD}	CLK delay time for the first falling edge of the TWI_RST command, see Figure 2-6	20		15,000	ns
DATA Delay Time	t_{DD}	The data delay time from the last CLK rising edge of the TWI command to the time DATA return to default status			15,000	ns
DATA Setup Time	t_{DS}	From DATA change to CLK falling edge	20			ns
DATA Hold Time	t_{DH}	From CLK falling edge to DATA change	200			ns

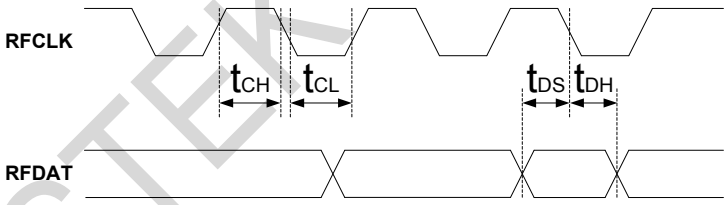


Figure 2-4. TWI Timing Diagram

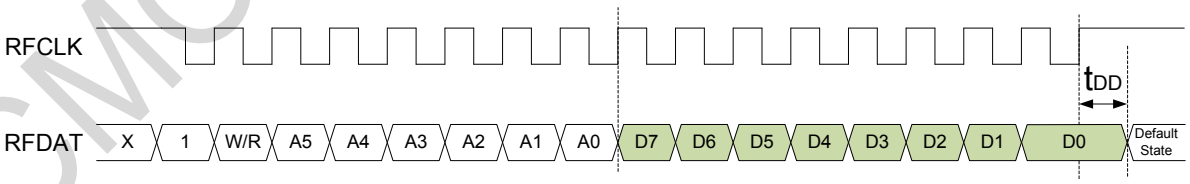


Figure 2-5. TWI 16-bit Command Timing Diagram

A group of TWI commands are composed of 16-bit data sent by RFCLK and RFDAT. The above diagram is a set of standard command timing format. In the high 8-bit data, the first bit is fixed to 1. Bit6 is a read/write distinction bit, "0" represents the write operation. "1" represents the read operation. The latter 6-bit is the register address of the operation. The low 8-bit data is the writing value or reading value of the operation register.

Among them, TWI_WRREG represents the write operation of the register; TWI_RDREG represents the read operation of the register, detailed as follows:

Table 2-3. TWI_WRREG and TWI_RDREG

Command	Description
TWI_WRREG	TWI write operation, Pseudo instruction format: TWI_WRREG(XX，YY) represents a set of 16 clock data streams，0b'10xx xxxx yyyy yyyy，where 0b 'XX XXXX is the address of the target operation register, the range is from 0x00 to 0x3F; 0b 'yyyy yyyy is the value that needs to be written to the target register, and the range is from 0x00 to 0xFF. For example, TWI_WRREG (0x12, 0xAA), the data stream is 0x92AA.
TWI_RDREG	TWI read operation, Pseudo instruction format: TWI_RDREG(XX, ZZ) represents a set of 16 clock data streams，0b'11xx xxxx zzzz zzzz，where 0b 'XX XXXX is the address of the target operation register, and the range is from 0x00 to 0x3F; 0b 'Zzzz Zzzz is the read value of the target register, and the range is from 0x00 to 0xFF. For example: TWI_RDREG (0x2A, DAT), the high 8-bit data stream is 0xEA, and the low 8-bit data stream is the actual read value.

2.5 TWI Timing Enter and Exit

In the TWI bus, RFDAT is the data line of the TWI, and it is also the data line of Tx. When the RFDAT edge changes, in order to distinguish between entering the Tx status or the TWI configuration mode, users need to access to the TWI configuration mode by a specific operation.

Here are three sets of special commands:

- SOFT_RST：Reset command of RF part circuit
- TWI_RST：TWI bus reset timing. Enter the TWI configuration mode after operation.
- TWI_OFF：TWI bus closing timing. Exit the TWI configuration mode after operation.

Table 2-4. TWI Command Description

Command	Descriptions
TWI_RST	Hold RFDAT continuously to low level (Not allowed to be pulled up in the middle). RFCLK sends 32 clock signals continuously, which is 4 bytes of 0x00, and then sends a set of 0x8D00 command. Thereafter RF enters the TWI configuration mode, the RFDAT change will no longer trigger the Tx status.
TWI_OFF	In the TWI configuration mode, send a set of 0x8D02 command. Thereafter exit the TWI configuration mode, the RFDAT change will trigger the Tx status.
SOFT_RST	At any time, when sending a set of 0xBD01 command, RF part executes reset. After reset, RF part enters the SLEEP mode directly to wait for the RFDAT edge to trigger the Tx status.

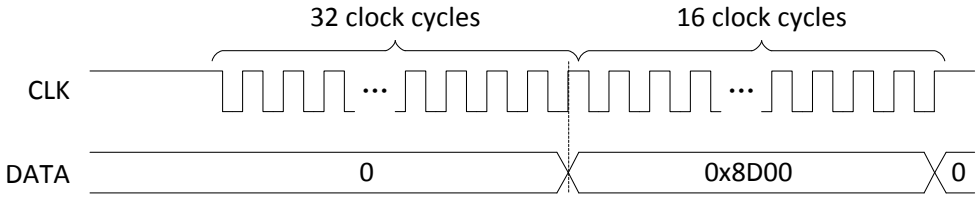


Figure 2-6. TWI_RST Command Timing Diagram

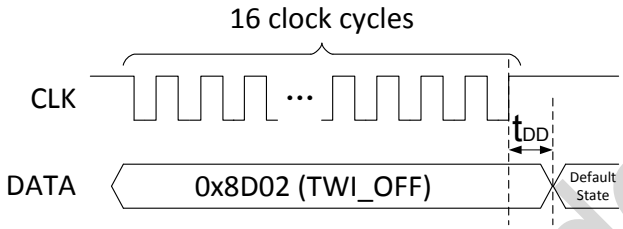


Figure 2-7. TWI_OFF Command Timing Diagram

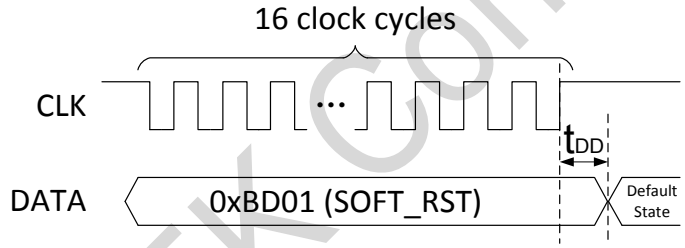


Figure 2-8. SOFT_RST Command Timing Diagram

2.6 TWI Configuration Process

TWI configuration process is as follows:

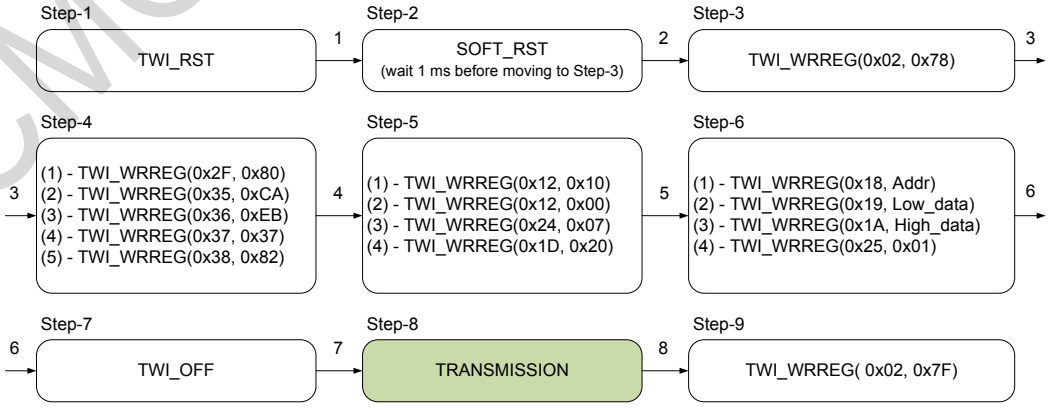


Figure 2-9. TWI Configuration Process Diagram

Note:

1. After completing the SOFT_RST at the Step2, it needs to wait for 1ms before the Step3 operation.
2. Step6 is a configuration register operation, which is not a direct write operation, but an indirect operation through internal circuit. So writing a register must repeat the process of Step6:
3. Write the target register address to 0x18.
4. The low 8-bit of the 16-bit data is written to 0x19.
5. The high 8-bit of the 16-bitdata is written to 0x1A.
6. Write 0x01 to the register 0x25, triggering the operation will take effect.

For example: The value to be written is 0xC3F6. The target address is 0x02. According to Step6, the process is as follows:

```
TWI_WRREG(0x18, 0x02);      // Write the Addr 0x02 to register 0x18
TWI_WRREG(0x19, 0xF6);      // Write the Low_data 0xF6 to register 0x19
TWI_WRREG(0x1A, 0xC3);      // Write the High_data 0xC3 to register 0x1A
TWI_WRREG(0x25, 0x01);      //Trigger the overwriting to the feature register, the writing process completes
```

In the configuration above, you can repeat the Step6 process in the Step6 stage, and configure all the registers that need to be. When the user needs to do a read operation to confirm whether the write operation is correct, the read operation is also indirect, similar to the Step6 process.

For example: The read address is 0x02, the process is as follows:

```
TWI_WRREG(0x18, 0x02);      // Write the Addr 0x02 to register 0x18
TWI_RDREG(0x1B, DATAL);     // Read theLow_data from 0x1B and store it in the DATAL variable
TWI_RDREG(0x1C, DATAH);     // Read the High_data from 0x1C and store it in the DATAH variable
```

But users need to notice that the read operation is the same as the write operation. The front Step1 to Step5 still needs to be executed, and reading and writing can be done in the Step6 stage.

2.7 Complete Transmission Process

A complete transmission process includes the parameter configuration, transmission, resetting TWI bus and RF part, as shown in the following figure:

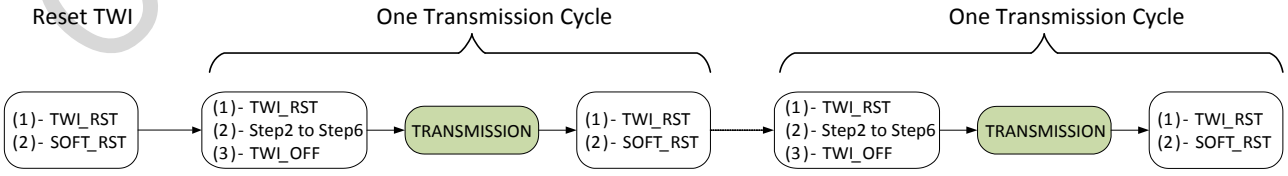


Figure 2-10. Configure Parameters for Each Transmission

The advantage of configuring parameters for each transmission is reliable. At the same time, after completing

the transmission, resetting the TWI bus and RF part to allow RF part to enter the low power status of sleep. The disadvantage is that users have to do a cumbersome configuration process every time.

Note:
Users may ask if they can only execute configuration parameters once after power-up. This method is to hold the RFDAT to low and continue until the end of the t_{STOP} time, as shown in the following figure:

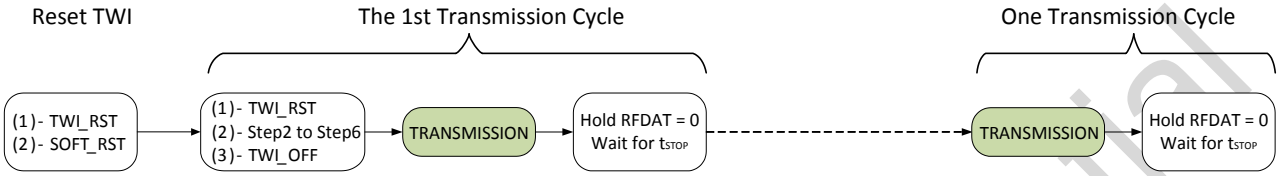


Figure 2-11. Only Execute Configuration Parameters Once

But this method is unable to achieve the low power consumption, because users trigger the RF internal register to save temporarily the configuration content, these temporary storage functions need to consume a certain amount of power (100uA or so); unless users do not execute the configuration mechanism, or do not use temporarily saving register (i.e. there is nothe process from Step2 to Step6, shown as below). Users only rely on the RF internal burning parameters as theconfiguration parameters.

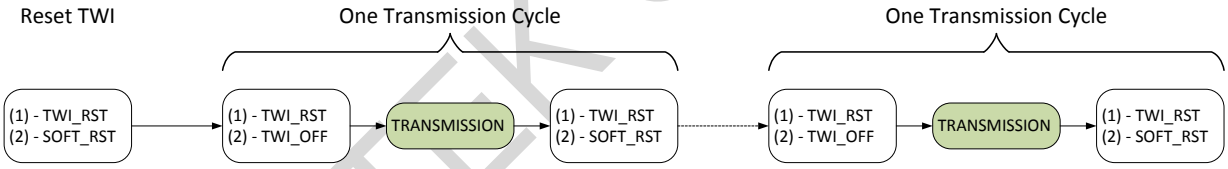


Figure 2-12. Burning Way Transmission Process (Not configuring the register)

3 Program Memory

The program address register is 13-bit, supports for access to 8K Bytes space (0x0000~ 0x1FFF) in maximum. But the actual chip memory is 2K Words, plus 4 additional user configuration banks (UCFGx) and factory configuration banks (FCFGx), the total is 64 Words.They are made up of EEPROM. Among them, the 0~0x7FF is the main program bank, the 0x800~0x1FFF is unimplemented bank which isreserved.The user and factory configuration information bank is 0x2000~0x203F.

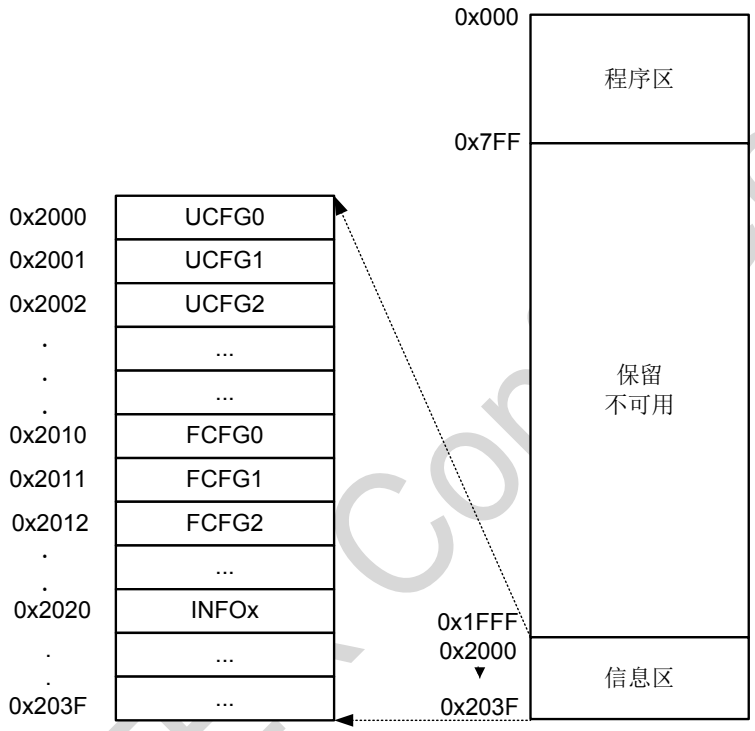


Figure 3-1. Program Space Address Mapping

4 Special Function Register(SFR)

4.1 Address Mapping

4.1.1 Bank0 SFR

Table 4-1. Bank0 Register List

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
0	INDF	Access the data memory by using the content of FSR(non physical registers)								xxxx xxxx
1	TMR0	Timer0<7:0>								xxxx xxxx
2	PCL	Program Counter<7:0>								0000 0000
3	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
4	FSR	Indirect Data Memory Address Pointer								
5	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00x0 0000
6										---- ----
7	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	0000 0000
8										---- ----
9										---- ----
A	PCLATH	-	-	-	Program Counter<13:8>					---0 0000
B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-	00-0 000-
D										---- ----
E										---- ----
F										---- ----
10										---- ----
11	TMR2	Timer2<7:0>								0000 0000
12	T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000
13										---- ----
14										---- ----
15										---- ----
16										---- ----
17										---- ----
18	WDTCON	-	-	-	WDTPS<3:0>				SWDTEN	---0 1000
19	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>			0000 0000
1A	PR0	PR0<7:0>								1111 1111
1B	MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-	---0 -00-
1C	SOSCPPRL	SOSCPR<7:0>								1111 1111
1D	SOSCPRH	-	-	-	-	SOSCPR<11:8>				---- 1111
1E										---- ----
1F										---- ----
20-7F		Bank0's SRAM, which is the general RAM of 96Byte.								xxxx xxxx

4.1.2 Bank1 SFR

Table 4-2. Bank1 Register List

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
80	INDF	Access the data memory by using the content of FSR (non physical registers)								xxxx xxxx
81	OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL	Program Counter<7:0>								0000 0000
83	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
84	FSR	Indirect Data Memory Address Pointer								
85	TRISA	TRISA<7:6>		--	TRISA<4:0>					11x1 1111
86										---- ----
87	TRISC	TRISC<7:0>								1111 1111
88										---- ----
89										---- ----
8A	PCLATH	-	-	-	Program Counter<13:8>					---0 0000
8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
8C	PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-	00-0 000-
8D										---- ----
8E	PCON							/POR	/BOR	---- --qq
8F	OSCCON	LFMOD	IRCF[2:0]			OSTS	HTS	LTS	SCS	0101 x000
90										---- ----
91										0000 0000
92	PR2	PR2[7:0], Timer2 period register								1111 1111
93										---- ----
94										---- ----
95	WPUA	WPUA<7:6>		-	WPUA<4:0>					11-1 1111
96	IOCA	IOCA<7:0>								---- ----
97										---- ----
98										---- ----
99	VRCON	VREN	-	VRR	-	VR<3:0>				0-0- 0000
9A	EEDAT	EEDAT<7:0>								0000 0000
9B	EEADR	EEADR<7:0>								0000 0000
9C	EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD	--00 x0-0
9D	EECON2	-	-	-	-	-	-	-	WR	---- ---0
9E										---- ----
9F										---- ----
A0-BF		Bank1's SRAM, which is the general RAM of 32Bytes.								xxxx xxxx
C0-EF										---- ----
F0-FF		SRAM. Access Bank0's 0x70 ~ 0x7F.								xxxx xxxx

Note:

1. INDF is not a physical register.
2. The gray part is unimplemented, please do not access.
3. "-" indicates that it is unimplemented; the unimplemented register bits can not be used or written as1. It is

used for subsequent chip upgrading.

4.1.3 TMR0（Addr:0x01）

Table 4-3. TMR0 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR0	Timer0<7:0>，Count result register							
Reset	X	X	X	X	X	X	X	X
Type	RW							

4.1.4 STATUS（Addr:0x03）

Table 4-4. STATUS Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	-	-	PAGE	/TF	/PF	Z	HC	C
Reset	-	-	0	1	1	X	X	X
Type	-	-	RW	R	R	RW	RW	RW

Table 4-5. STATUS Bit Function Description

Bit	Name	Function
7:6	-	No function, read as “0”
5	PAGE	Register Bank Select bit: 0 = BANK0（00h-7Fh） 1 = BANK1（80h-FFh）
4	/TF	Time-out bit 1 = After power-up, CLRWDT instruction or SLEEP instruction 0 = A WDT time-out occured.
3	/PF	Power-down bit 1 = After power-up or by the CLRWDT instruction 0 = By executation of the SLEEP instruction
2	Z	Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
1	HC	Half-carry/$\overline{\text{borrow}}$ bit(ADDWF、ADDLW、SUBLW、SUBWF instructions) 1 = A carry/$\overline{\text{borrow}}$ from the 4th low-order bit of the result occurred 0 = No carry/$\overline{\text{borrow}}$ from the 4th low-order bit of the result occurred
0	C	Carry/$\overline{\text{borrow}}$ bit(ADDWF、ADDLW、SUBLW、SUBWF instructions) 1 = A carry/$\overline{\text{borrow}}$ from the Most Significant bit of the result occurred 0 = No carry/$\overline{\text{borrow}}$ from the Most Significant bit of the result occurred

Table 4-6. FlagSituation in Each ResetStatus

/TF	/PF	Condition
1	1	Power on or low voltage reset
0	u	WDT reset
0	0	WDT wake-up
u	u	MCLR reset under the normal operation
1	0	MCLR reset in the sleep status

Note:

1. The Status register can also be the destination register for any instruction, like any other register. If the Status register is the destination register for an instruction that affects the Z, HC, or C bit, then the “write” to these three bits is disabled. These bits are set to 1 or cleaned according to the device logic.Therefore, the result of an instruction with the Status register as destination may be different than intended.
2. It is suggested that only using the BCR, BSR, SWAPR and STR instructions to change the status register.

4.1.5 PORTA（Addr:0x05）

Table 4-7. PORTA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset	X	X	X	X	X	X	X	X
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 4-8. PORTA Bit Function Description

Bit	Name	Function
7	PA7	PORTA7 data
6	PA6	PORTA6 data
5	PA5	PORTA5 only acts as the input.There is no corresponding output data register.
4	PA4	PORTA4 data
3	PA3	PORTA3 data
2	PA2	PORTA2 data
1	PA1	PORTA1 data
0	PA0	PORTA0 data

4.1.6 PORTC（Addr:0x07）

Table 4-9. PORTC Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Reset	X	X	X	X	X	X	X	X
Type	RW	RW	RW	RW	RW	RW	RW	RW

Table 4-10. PORTC Bit Function Description

Bit	Name	Function
7	PC7	PORTC7 data
6	PC6	PORTC6 data
5	PC5	PORTC5 data
4	PC4	PORTC4 data
3	PC3	PORTC3 data
2	PC2	PORTC2 data
1	PC1	PORTC1 data
0	PC0	PORTC0 data

4.1.7 INTCON（Addr:0x0B）

Table 4-11. INTCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Table 4-12. INTCON Bit Function Description

Bit	Name	Function
7	GIE	GlobalInterrupt Enable bit 1 = Enable all unmasked interrupts 0 = Disable all interrupts
6	PEIE	PeripheralInterrupt Enable bit 1 = Enable all unmasked peripheral interrupts 0 = Disable allperipheral interrupts
5	T0IE	Timer0 Overflow Interrupt Enable bit 1 = Enable 0 = Disable
4	INTE	PA2/INT External InterruptEnable bit 1 = Enable 0 = Disable

3	PAIE	PORTA Change Interrupt Enable bit 1 = Enable the PORTA<7:0> change interrupt 0 = Disable the PORTA<7:0> change interrupt
2	T0IF	Timer0 Overflow Interrupt Flag bit 1 = Timer0register has overflowed (must be cleared in software) 0 = Timer0 register has not overflowed
1	INTF	PA2/INT External Interrupt Flag bit 1 = PA2/INT external interrupt has occurred (must be cleared in software) 0 = PA2/INT external interrupt has not occurred
0	PAIF	PORTA Change Interrupt Flag bit 1 = Any one or more ports of PORTA<7:0>have changed state (must be cleared in software) 0 = None of the PORTA<7:0> have changed state

4.1.8 PIR1（Addr:0x0C）

Table 4-13. PIR1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-
Reset	0	0	-	0	0	0	0	-
Type	RW	RW	-	RW	RW	RW	RW	-

Table 4-14. PIR1 Bit Function Description

Bit	Name	Function
7	EEIF	EEPROM Write OperationInterrupt Flag bit 1 = The EE write operation completed(must be cleared in software) 0 = The EE write operation has not completed
6	CKMEAIF	Fast clock measuringslow clock operationInterruptFlag bit 1 = Fast clock measuringslow clock operation completed (must be cleaned in software.) 0 = Fast clock measuringslow clock operation has not completed
5	-	Reserved-bit, can not be written as“1”
4	C2IF	Comparator2 Interrupt Flag bit 1 = Comparator2 output has changed 0 = Comparator2 output has not changed
3	C1IF	Comparator1 Interrupt Flag bit 1 = Comparator1 output has changed 0 = Comparator1 output has not changed
2	OSFIF	Oscillator FailInterrupt Flag bit 1 = System oscillator failed, clock input has changed to INTOSC(must be cleared in software) 0 = System clock runs normally

1	TMR2IF	Timer2 to PR2 Match Interrupt Fag bit 1 = Timer2 to PR2 match occurred(must be cleared in software) 0 = Timer2 to PR2 match has not occurred
0	-	Reserved-bit, can not be written as 1

4.1.9 TMR2（Addr:0x11）

Table 4-15. TMR2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR2	TMR2<7:0>							
Reset	0000 0000							
Type	RW							

4.1.10 T2CON（Addr:0x12）

Table 4-16. T2CONRegister

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>	
Reset	-	0000				0	00	
Type	-	RW				RW	RW	

Table 4-17. T2CON Bit Function Description

Bit	Name	Function
7	-	Reserved-bit, read as 0
6:3	TOUTPS<3:0>	Timer2 OutputPostscale Select bits 0000 = 1:1 postscale 0001 = 1:2 postscale 0010 = 1:3 postscale 0011 = 1:4 postscale 0100 = 1:5 postscale 0101 = 1:6 postscale 0110 = 1:7 postscale 0111 = 1:8 postscale 1000 = 1:9 postscale 1001 = 1:10 postscale 1010 = 1:11 postscale 1011 = 1:12 postscale 1100 = 1:13 postscale 1101 = 1:14 postscale 1110 = 1:15 postscale 1111 = 1:16 postscale

2	TMR2ON	Timer2 On bit 1 = Timer2 is on 0 = Timer2 is off
1:0	T2CKPS<1:0>	Timer2 Clock Prescale Select bits 00 = 1:1 Prescaler is 1 01 = 1:4 Prescaler is 4 1x = 1:16 Prescaler is 16

4.1.11 WDTCON（Addr:0x18）

Table 4-18. WDTCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	-	-	-	WDTPS<3:0>				SWDTEN
Reset	-	-	-	0	1	0	0	0
Type	-	-	-	RW	RW	RW	RW	RW

Table 4-19. WDTCON Bit Function Description

Bit	Name	Function
7:5	-	Reserved-bits, read as 0
4:1	WDTPS<3:0>	Watchdog TimerPeriod Select Bits 0000 = 1:32 0001 = 1:64 0010 = 1:128 0011 = 1:256 0100 = 1:512 (Reset value) 0101 = 1:1024 0110 = 1:2048 0111 = 1:4096 1000 = 1:8192 1001 = 1:16384 1010 = 1:32768 1011 = 1:65536 11xx = 1:65536
0	SWDTEN	Software Enable or Disable the watchdog timer 1 = WDT is turned on 0 = WDT is turned off

4.1.12 CMCON0（Addr:0x19）

Table 4-20. CMCON0 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>		
Reset	0	0	0	0	1	0	0	0
Type	R	R	RW	RW	RW	RW	RW	RW

Table 4-21. CMCON0 Bit Function Description

Bit	Name	Function
7	C2OUT	Comparator2 Output bit When C2INV=0, 1：C2VIN+ ＞ C2VIN- 0：C2V IN+ ＜ C2VIN- When C2INV=1, 1：C2VIN+ ＜ C2VIN- 0：C2V IN+ ＞ C2VIN-
6	C1OUT	Comparator1Outputbit When C1INV=0, 1：C1VIN+ ＞ C1VIN- 0：C1V IN+ ＜ C1VIN- When C1INV=1, 1：C1VIN+ ＜ C1VIN- 0：C1V IN+ ＞ C1VIN-
5	C2INV	Comparator2 Output Inversion bit 0 = C2 output not inverted 1 = C2 output inverted
4	C1INV	Comparator1Output Inversion bit 0 = C1 output not inverted 1 = C1 output inverted
3	CIS	Comparator Input Switch bit When CM[2:0]=010, 1 = C1IN+ connects to C1VIN+, C2IN+ connects to C2VIN+ 0 = C1IN- connects to C1VIN-，C2IN- connects to C2VIN- When CM[2:0]=001, 1 = C1IN+ connects to C1VIN+ 0 = C1IN- connects to C1VIN-

2:0	CM<2:0>	Comparator Mode Select bits 000 = The comparator is turned off, and the CxIN pin is the analog IO pin. 001 = Three inputs multiplexed to two comparators 010 = Four inputs multiplexed to twocomparators 011 = Two common reference comparators 100 = Two independent comparators 101 = One independent comparator 110 = Two common reference comparatorswith outputs 111 = The comparator is turned off, and the CxIN pin is the digital IO pin.

4.1.13 PR0（Addr:0x1A）

Table 4-22. PRO Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PR0	PR0<7:0>							
Reset	0xFF							
Type	RW							

Table 4-23. PR0 Function Description

Bit	Name	Function
7:0	PR0<7:0>	Timer0 period (comparison) register

4.1.14 MSCKCON（Addr:0x1B）

Table 4-24. MSCKCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-
Reset	-	-	-	0	-	0	0	-
Type	-	-	-	RW	-	RW	RW	-

Table 4-25. MSCKCON Bit Function Description

Bit	Name	Function
7:5	-	Reserved-bits, can not be written as 1.
4	SLVREN	Software Control LVR Enable bit 1 = When UCFG<1:0> is 00, enable LVR. 0 = No matter what value of UCFG<1:0> is, disable LVR.
3	-	Reserved-bit, can not be written as 1.
2	CKMAVG	Measurement average mode of fast clock measuring slowclock period 1 = Open the average mode.(Automatically measure and accumulate four times) 0 = Close the average mode.

1	CKCNTI	Fast clock measuring slowclock period Enable bit 1 = Enable fast clock measuring slowclock period. 0 = Disable fast clock measuring slowclock period. Note: The bit will automatically return to zero after the measurement is completed.
0	-	Reserved-bit, can not be written as 1.

4.1.15 SOSCPR（Addr:0x1C/0x1D）

Table 4-26. SOSCPRL Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOSCPRL	SOSCPR<7:0>							
Reset	0xFF							
Type	RW							

Table 4-27. SOSCPRH Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOSCPRH	-				SOSCPR<11:8>			
Reset	-				1111			
Type	-				RW			

Table 4-28. SOSCPR Function Description

Bit	Name	Function
11:0	SOSCPR<11:0>	Low-frequency oscillator period (unit: fast clock period number) is used for slow clock measurement.

4.1.16 OPTION（Addr:0x81）

Table 4-29. OPTION Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS<2:0>		
Reset	1	1	1	1	1	111		
Type	RW	RW	RW	RW	RW	RW		

Table 4-30. OPTION Bit Function Description

Bit	Name	Function
7	/PAPU	PORTA Pull-up Enable bit. 1 = PORTA pull-ups are disabled 0 = PORTA pull-ups are enabled by individual port latch values

<table>
<tr><td>6</td><td>INTEDG</td><td>Interrupt Edge Select bit
1 = Interrupt on rising edge of PA2/INT pin
0 = Interrupt on falling edge of PA2/INT pin</td></tr>
<tr><td>5</td><td>T0CS</td><td>Timer0 Clock Source Select bit
1 = Transition on PA2/T0CKI bit
0 = Internal instruction cycle clock (FOSC/2)</td></tr>
<tr><td>4</td><td>T0SE</td><td>Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on PA2/T0CKI pin
0 = Increment on low-to-high transition on PA2/T0CKI pin</td></tr>
<tr><td>3</td><td>PSA</td><td>Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned tothe Timer0 module</td></tr>
<tr><td>2:0</td><td>PS<2:0></td><td>Prescaler Rate Select bits
<table>
<tr><th>BIT Value</th><th>Timer0 RATE</th><th>WDT RATE</th></tr>
<tr><td>000</td><td>1:2</td><td>1:1</td></tr>
<tr><td>001</td><td>1:4</td><td>1:2</td></tr>
<tr><td>010</td><td>1:8</td><td>1:4</td></tr>
<tr><td>011</td><td>1:16</td><td>1:8</td></tr>
<tr><td>100</td><td>1:32</td><td>1:16</td></tr>
<tr><td>101</td><td>1:64</td><td>1:32</td></tr>
<tr><td>110</td><td>1:128</td><td>1:64</td></tr>
<tr><td>111</td><td>1:256</td><td>1:128</td></tr>
</table></td></tr>
</table>

4.1.17 TRISA（Addr:0x85）

Table 4-31. TRISA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 4-32. TRISA Bit Function Description

Bit	Name	Function
7:6	TRISA<7:6>	PORTA<7:6> port direction Control bits 1 = Input 0 = Output
5	TRISA<5>	PORTA5 port direction Control bit Only as input, fixed to 1
4:0	TRISA<4:0>	PORTA<4:0> port direction Control bits 1 = Input 0 = Output

4.1.18 TRISC（Addr:0x87）

Table 4-33 TRISC Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 4-34. TRISC Bit Function Description

Bit	Name	Function
7:0	TRISC<7:0>	PORTC<7:0> port direction Control bits 1 = Input 0 = Output

4.1.19 PIE1（Addr:0x8C）

Table 4-35. PIE1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-
Reset	0	0	-	0	0	0	0	-
Type	RW	RW	-	RW	RW	RW	RW	-

Table 4-36. PIE1Bit Function Description

Bit	Name	Function
7	EEIE	EEPROM Write Complete Interrupt Enable bit 1 = Enable the EEPROM write complete interrupt 0 = Disable the EEPROM write completeinterrupt
6	CKMEAIE	Fast clock measuring slow clock operationInterrupt Enable bit 1 = Enable fast clock measuring slow clock operation interrupt 0 = Disable fast clock measuring slow clock operation interrupt
4	C2IE	Comparator2 Interrupt Enable bit 1 = Enable the comparator2 interrupt 0 = Disable the comparator2 interrupt
3	C1IE	Comparator1Interrupt Enable bit 1 = Enable the comparator1 interrupt 0 = Disable the comparator1 interrupt
2	OSFIE	Oscillator Fail Interrupt Enable bit 1 = Enable the oscillator fail interrupt 0 = Disable the oscillator fail interrupt

1	TMR2IE	Timer2 to PR2 Match Interrupt Enable bit 1 = Enable 0 = Disable

4.1.20 PCON（Addr:0x8E）

Table 4-37. PCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	-	-	-	-	-	-	/POR	/BOR
Reset	-	-	-	-	-	-	q	q
Type	-	-	-	-	-	-	RW	RW

Table 4-38. PCONBit Function Description

Bit	Name	Function
1	/POR	Power-onReset Status bit, active low 0 = A Power-onReset occured 1 = No Power-on Reset occured or software set it to 1. /POR is set to 0 after a Power-onReset occurs.After that, the software should set it to 1.
0	/BOR	Brown-out Reset Status bit, active low 0 = A Brown-out Reset occured 1 = No Brown-out Reset occurred or software set it to 1.

4.1.21 OSCCON（Addr:0x8F）

Table 4-39. OSCCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OSCCON	LFMOD	IRCF<2:0>			OSTS	HTS	LTS	SCS
Reset	0	101			1	0	0	0
Type	RW	RW			R	R	R	RW

Table 4-40. OSCCONBit Function Description

Bit	Name	Function
7	LFMOD	Internal Low Frequency OscillationMode: 1 = 256K oscillation frequency mode 0 = 32K oscillation frequency mode
6:4	IRCF<2:0>	Internal Oscillator Frequency Select bits 111 = 16MHz 110 = 8MHz 101 = 4MHz(default) 100 = 2MHz

		011 = 1MHz 010 = 500KHz 001 = 250KHz 000 = 32KHz（LFINTOSC）
3	OSTS	Oscillator Start-up Timeout Status bit 1 = Device is running from the external system clock defined by the FOSC<2:0>. 0 = Device is running from the internal oscillator
2	HTS	Internal High Frequency Clock Status bit 1 = HFINTOSC status is stable 0 = HFINTOSC status is not stable
1	LTS	Internal Low Frequency Clock Status bit 1 = LFINTOSC status is stable 0 = LFINTOSC status is not stable
0	SCS	System Clock Select bit 1 = Internal oscillator is used for system clock 0 = Clock sourcedefined by FOSC<2:0>

4.1.22 PR2（Addr:0x92）

Table 4-41. PR2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PR2	PR2<7:0>							
Reset	0xFF							
Type	RW							

Table 4-42. PR2Bit Function Description

Bit	Name	Function
7:0	PR2<7:0>	Timer2 cycle (comparison) register (See the Timer2 description chapter in details.)

4.1.23 WPUA（Addr:0x95）

Table 4-43. WPUA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
Reset	1	1	-	1	1	1	1	1
Type	RW	RW	-	RW	RW	RW	RW	RW

Table 4-44. WPUA Bit Function Description

Bit	Name	Function
7:6	WPUA<7:6>	PORTA Weak Pull-up Enable bit 1 = Enable 0 = Disable
4:0	WPUA<4:0>	PORTA Weak Pull-up Enable bit 1 = Enable 0 = Disable

4.1.24 IOCA（Addr:0x96）

Table 4-45. IOCA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IOCA	IOCA<7:0>							
Reset	0x00							
Type	RW							

Table 4-46. IOCABit Function Description

Bit	Name	Function
7:0	IOCA<7:0>	Interrupt-on-change PORTA Control bit 1 = Interrupt-on-change enabled 0 = Interrupt-on-change disabled

4.1.25 VRCON（Addr:0x99）

Table 4-47. VRCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VRCON	VREN	-	VRR	-	VR<3:0>			
Reset	0	-	0	-	0			
Type	RW	-	RW	-	RW			

Table 4-48. VRCONBit Function Description

Bit	Name	Function
7	VREN	CVref Enable bit 1 = CVref circuit powered on 0 = CVref circuit powered down, no I_{DD} drain
5	VRR	CVref Range Select bit 1 = Low level range 0 = High level range

3:0	VR[4:0]	CVref Value Select Control bit When VRR = 1，CVref =（VR<4:0>÷24）×VDD When VRR = 0，CVref =（VDD÷4）+（VR<4:0>÷32）×VDD

4.1.26 EEDAT（Addr:0x9A）

Table 4-49. EEDAT Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EEDAT	EEDAT<7:0>							
Reset	0x00							
Type	RW							

4.1.27 EEADR（Addr:0x9B）

Table 4-50. EEADR Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EEADR	EEADR<7:0>							
Reset	0x00							
Type	RW							

4.1.28 EECON1（Addr:0x9C）

Table 4-51. EECON1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD
Reset	-	-	0	0	X	0	-	0
Type	-	-	RW	RW	RW	RW	-	W

Table 4-52. EECON1 Bit Function Description

Bit	Name	Function
5,4,2	WREN<2:0>	EEPROM Write Enable bit 111 = Allow write to the data EEPROM. After the program is completed, each bit will automatically return to 0. Other values=Inhibit write to the data EEPROM
3	WRERR	EEPROM Write Error Flag bit 1 = A write operation is prematurely terminated (any /MCLR Reset, any WDT Reset during EEPROM programming period) 0 = The write operation completed during EEPROM programming period.
0	RD	EEPROM Read Control bit. This bit is written only, reading will always return to 0. 1 = Initiate an EEPROM read cycle 0 = Does not initiate an EEPROM read cycle

4.1.29 EECON2（Addr:0x9D）

Table 4-53. EECON2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON2	-	-	-	-	-	-	-	WR
Reset	-	-	-	-	-	-	-	0
Type	-	-	-	-	-	-	-	RW

Table 4-54. EECON2 Bit Function Description

Bit	Name	Function
0	WR	EEPROM Write Control bit Read operation, 1=Data EEPROM is in the programming cycle. 0=Data EEPROM is not in the programming cycle. Write operation, 1=Initiates a data EEPROM programming cycle 0=No function

4.1.30 Configuration Register UCFGx

The UCFG0, UCFG1or UCFG2 could not be programmed.They are only written by the hardware (burning) in the power-up process.

- **UCFG0 address is 0x2000in PROM**

Table 4-55. UCFG0 Configuration Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG0	-	CPB	MCLRE	PWRTEB	WDTE	FOSC<2:0>		

Table 4-56. UCFG0Bit Function Description

Bit	Name	Function
6	CPB	1 = Flash content is not protected 0 = Intiate the Flash content protection, MCU is able to access the content; the serial port is not able to access it. Note: The bit can only be rewritten from 1 to 0, but it can not be rewritten from 0 to 1.The only way to rewrite from 0 to 1 is to erase the register including USER_OPT, and the CPB becomes 1 after power-up again.
5	MCLRE	1 = The PA5/MCLR pin executes the MCLR function, which is the reset pin. 0 = The PA5/MCLR pinexecutes the PA5 function, which is the digital input pin.
4	PWRTEB	1 = Disable PWRT 0 = Enable PWRT

3	WDTE	1 = Enable WDT, the program cannot disable it. 0 = Disable WDT, but the program can enable WDT by setting the SWDTEN bit of the WDTCON
2:0	FOSC<2:0>	000 = 32K crystal oscillator mode, PA6/PA7 connects the low frequency crystal oscillator. 001 = 20MHz crystal oscillator mode, PA6/PA7 connects the high speed crystal oscillator. 010 = External clock mode, PA6 is the IO pin, PA7 is connected to the clock input. 011 = INTOSC mode, PA6 output the 2 frequency division of the system clock, PA7 is the IO pin; 1xx = INTOSCIO mode, both PA6 and PA7 are the IO pins

- **UCFG1 address is 0x2001in PROM**

Table 4-57. UCFG1 Configuration Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG1	-	-	TSEL	FCMEN	IESO	RD_CTRL	LVDEN<1:0>	

Table 4-58. UCFG1Bit Function Description

Bit	Name	Function
5	TSEL	Instruction PeriodSelect bit 1 = The instruction period is 2T. 0 = The instruction period is 4T.
4	FCMEN	Clock Fault Monitoring Enable bit 1 = Enable the clock fault monitoring 0 = Disable the clock fault monitoring
3	IESO	Two Speed Clock Enable bit 1 = Enable 0 = Disable
2	RD_CTRL	Read Port Control bit in output mode 1 = Read the value of the PAD returned from the data port. 0 = Read the value of the Latch returned from the data port.
1:0	LVDEN[1:0]	Low Voltage Reset Select bit 00 = Enable the low voltage reset. Others= Disable the low voltage reset.

- **UCFG2 address is 0x2002in PROM**

Table 4-59. UCFG2 Configuration Register

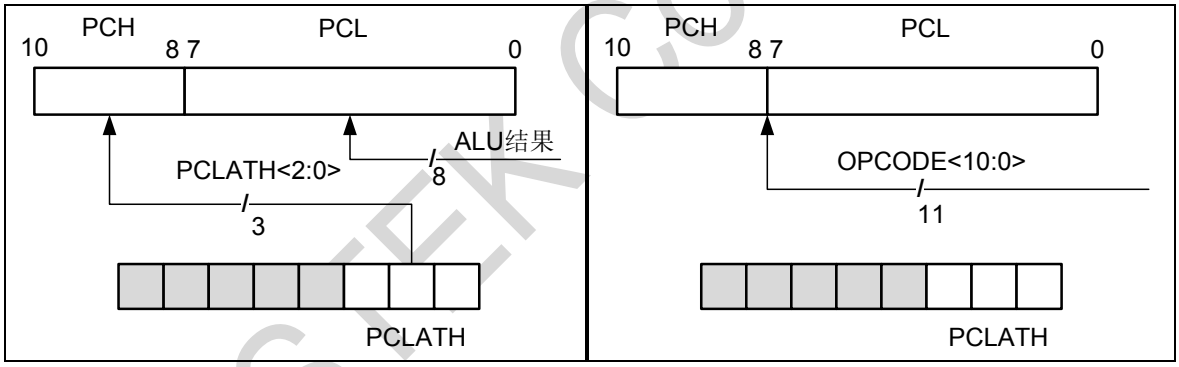
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG2	-	-	-	-	LVDS<3:0>			

Table 4-60. UCFG2Bit Function Description

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>7:4</td><td>-</td><td>Reserved-bit</td></tr>
<tr><td>3:0</td><td>LVDS[3:0]</td><td>Low voltage reset threshold selection
<table>
<tr><th>Value</th><th>Voltage</th></tr>
<tr><td>0010</td><td>1.8V</td></tr>
<tr><td>0011</td><td>2.0V</td></tr>
<tr><td>0100</td><td>2.2V</td></tr>
<tr><td>0110</td><td>2.8V</td></tr>
<tr><td>Others</td><td>Reserved</td></tr>
</table></td></tr>
</table>

4.1.31 PCL and PCLATH

The program counter (PC) is 11-bit.The lower 8-bit is from the PCL register, which is a readable and writable register. The higher 3-bit (PC<10:8>) is not directly readable and writable, it is from PCLATH. On any reset, PC will be cleared.The following figure shows the two situations for the loading of PC. Notice the LCALL and LJUMP instructions on the right side of the figure. Because the operating code in the instruction is 11-bit, and the PC of the chip is just 11-bit, so PCLATH is not needed.



Instruction aimed at PCL　　LJUMP、LCALL instruction

Figure 4-1.PC Loading DiagraminDifferent Situations

Modify PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<10:8> bits to be replaced by the contents of PCLATH register.This allows the entire contents of the program counter to be changed by writing the desired high 3-bit to the PCLATH register.

A computed LJUMP instruction is accomplished by adding an offset to the program counter (ADDWR PCL). Care should be exercised when jumping into the look-up table or the program branch table (computed LJUMP) by modifying the PCL register. Assuming that PCLATH is set as the table start address, if the table length is greater than 255 instruction, or if the lower 8-bit of memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and target location within the table.

4.1.32 INDFand FSR Register

INDF is not a physical register, and addressing the INDF will generate an indirect addressing, and the addressable range is 0~255. Any instruction that uses the INDF register is actually access to the unit that the file selection register FSR points to. Reading the INDF indirectly will return 0. Writing the INDF indirectly will cause the control operation. (It may affect the status flag bit.)

5 MCU SystemClock Source

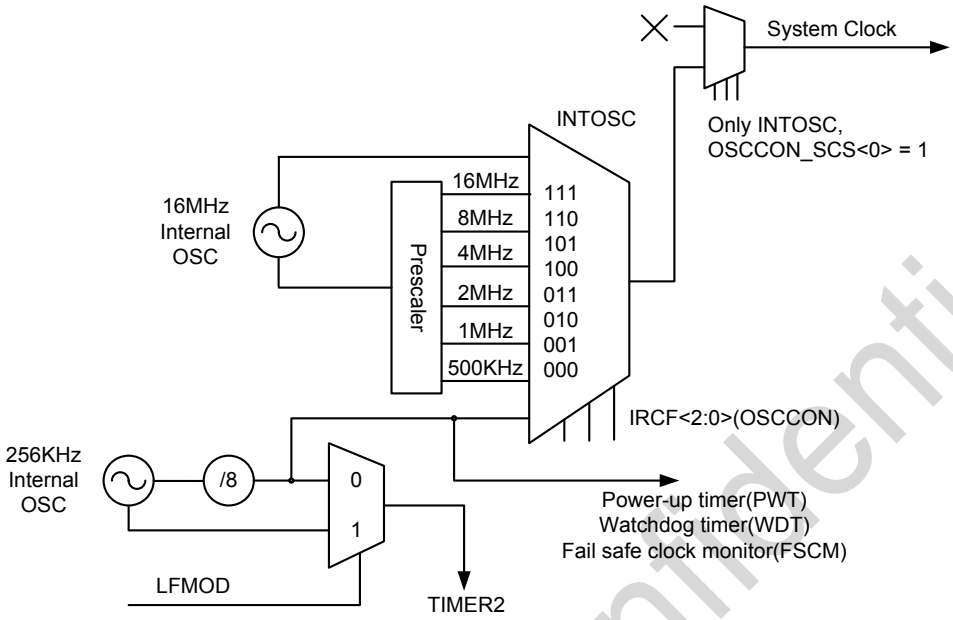


Figure 5-1. System Clock Source Diagram

The chip contains three clock sources: twobuilt-in oscillators as variousclock sources, and one external clock input source. The built-in oscillator includes one internal 16M high-frequency precise oscillator (HFINTOSC), and one internal 32K/256Klow-frequency and low-power oscillator (LFINTOSC).These clocks or oscillators, combined with prescaler, can provide the system with a variety of frequency clock sources. The prescaler ratio of the system clock source can be controlled by the IRCF<2:0> bit in the OPTION register.

Note:
The watchdog, the system clock source (IRCF=000) and the PWRT use the output uniformlyafter 8 frequency division, that is32KHz, regardless of the value of the LFMOD.

5.1 Clock Source Mode

Clock source mode can be classified as external or internal.

- The external clock mode relies on the external circuit forthe clock source, such as the external clock EC mode, the crystal oscillator XT and LP mode. But because the related pins are not drawn out, CMT2189C can not use the external clock mode, and can only use the internal clock mode.
- The internal clock mode is built in the oscillator module. The oscillator module has a 16MHz high frequency oscillator and a 32KHz low frequency oscillator.

The internal or external clock source can be selected by the System Clock Selectbit(SCS) of the OSCCON register.

5.1.1 Internal Clock Mode

The oscillator mode has two independent internal oscillators, which can be configured or selected as the system clock source.

- The high frequency internal oscillator(HFINTOSC) is factory calibrated and operates at 16MHz.
- The low frequency internal oscillator(LFINTOSC) is uncalibrated and operates at 32KHz. The Internal Oscillator Frequency Select bit IRCF<2:0> can be operated to select the system clock speed via programming.

The system clock can be selected between the external or internal clock source via System Clock Select bit (SCS) of the OSCCON register.

Note:
The LFMOD of the OSCCON register can select LFINTOSC as 32KHz or 256KHz, but the watchdog is fixed with 32KHz, regardless of the LFMOD value.

5.1.2 Frequency Select Bit（IRCF）

The output of 16MHz HFINTOSC and 32KHz LFINTOSC is connected to the prescaler and multiplexer (see Figure 5-1).The OSCCON register's internal oscillator frequency select bit IRCF<2:0> is used to select the frequency output of the internal oscillator. Select one of the following eight frequencies via the software:

- 16MHz
- 8MHz
- 4MHz）(Default value after reset)
- 2MHz
- 1MHz
- 500KHz
- 250KHz
- 32KHz

5.1.3 Clock Switch Timing of HFINTOSC and LFINTOSC

When switching between LFINTOSC and HFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-2). In this case, there is a delay afterthe IRCF bit of the OSCCON register is modified before the frequency selection takes place.The LTS and HTS bits of the OSCCON register will reflect the current active status of the LFINTOSC and HFINTOSC oscillators. The frequency selection timing is as follows:

1. The IRCF<2:0> bit of the OSCCON register is modified.
2. If the new clock is shut down, start a clock start-up delay.
3. The clock switch circuit waits for the arrival of the falling edge of the current clock.
4. Hold CLKOUT to low, the clock switch circuit waits for the arrival of the falling edge oftwo new clocks.
5. CLKOUT is now connected with the new clock, and the HTS and LTS bits of the OSCCON register are

updated as required.

6. Clock switch is complete.

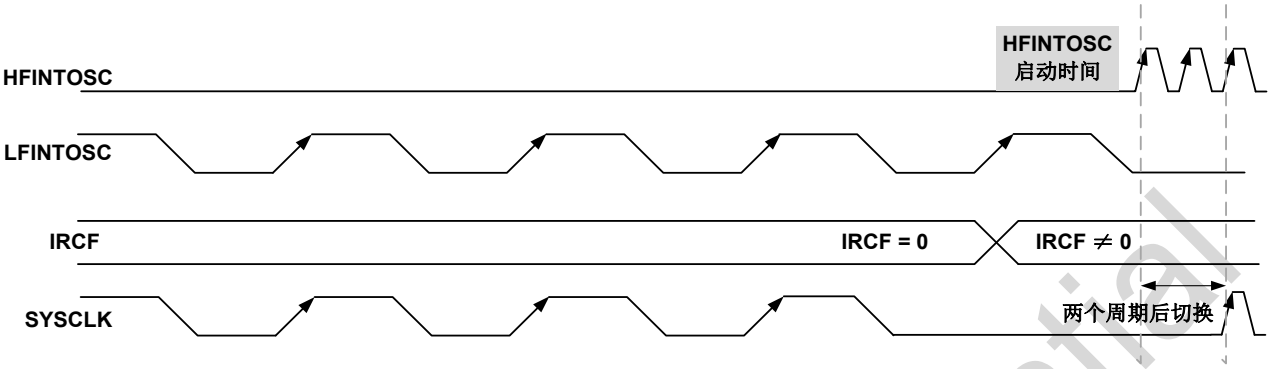


Figure 5-2. Switch from Slow Clock to Fast Clock Diagram

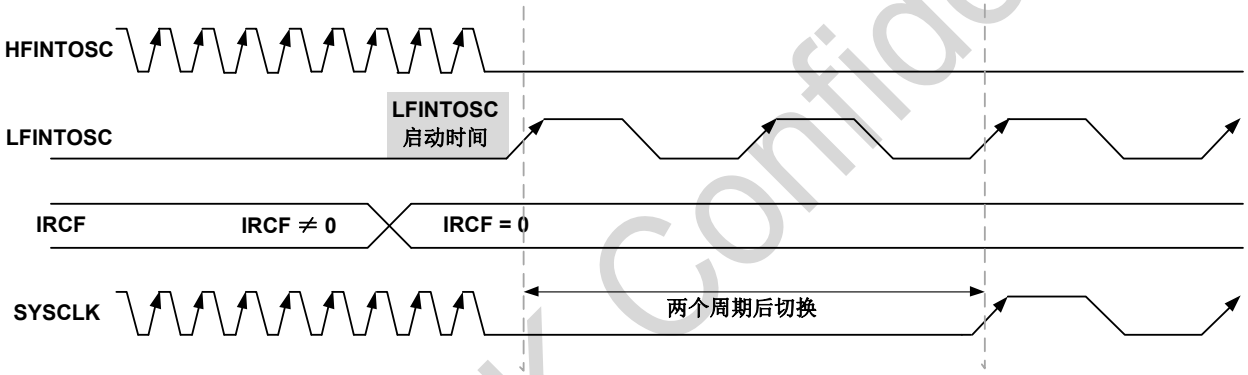


Figure 5-3. Switch from Fast Clock to Slow Clock Diagram

5.2 Clock Switching

The System Clock Select bit (SCS) of the OSCCON register is operated via software, and the system clock source can be switched between the external and internal clock sources.

5.2.1 System Clock Select Bit (SCS)

The System Clock Select bit(SCS) of the OSCCON register selects the system clock sourcethat is used for the CPU and peripherals.

- When the System Clock Select bit (SCS) of the OSCCON register is 0, the system clock source is determined by configuration of the FOSC<2:0> bit in the Configuration Word register (UCFG0).
- When the System Clock Select bit (SCS) of the OSCCON register is 1, the system clock source is selected according to the internal oscillator frequency selected by the IRCF<2:0> bit of the OSCCON register. After aReset, SCS is always cleared.

Note:

Any clock switching caused by the hardware (possibly from Two-Speed Start-up or Fail-Safe Clock Monitor) will not update the SCS bit of the OSCCON register. The user should monitor the OSTS bit of the OSCCON

register to determine the current system clock source.

5.2.2 Oscillator Start-up Timeout Status(OSTS) Bit

The Oscillator Start-up Timeout Status (OSTS) bit of the OSCCON register is used to indicate whether the system clock is from the external clock source or from the internal clock source.The external clock source is defined by the FOSC<2:0> bit in the Configuration Word register (UCFG0). OSTS also indicates whether the Oscillator Start-up Timer (OST) is timeout in the LP or XT mode.

5.3 Two-Speed Clock Start-up Mode

Two-Speed Start-upMode reduces the power consumption further by minimizing the latency between the external oscillator and the code execution.For using the sleep mode frequently, Two-Speed Start-upMode will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.This mode allows the application to wake-up from Sleep, use INTOSC as a clock source to execute several instructions, and then go back to the Sleep status without waiting for the stability of primary oscillator.

Note:
Executing a SLEEP instruction will abort the oscillator start-up time and clear the OSTS bit of the OSCCON register.

When the oscillator module is configured as LP mode or XT mode, enable the Oscillator Start-upTimer (OST). (See the section5.2.2 “OscillatorStart-up Timeout Status”). OST will suspend the program execution until the 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as OST is counting. When OST count reaches 1024 and the OSTS bit of the OSCCON register is set to 1, the program will switch to the external oscillator.

5.3.1 Two-Speed Start-up Mode Configuration

Two-Speed Start-up Modeis configured by the following settings:

- Configure the IESO bit in the Configuration Wordregister (UCFG1) as 1, Internal/External Switch Over bit. (Enable the Two-Speed Start-up Mode.)
- Configure the SCS bit of the OSCCON register as 0.
- Configure the F_{OSC}<2:0> in the Configuration Word register(CONFIG) as the LP or XT mode.

Two-Speed Start-up mode is entered after the following operation:

- Power-on Reset (POR) and, if enabled, after PWRT has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured as any mode except the LP or XT mode, the Two-Speed Start-up will be disabled. This is because the external clock oscillation does not require any stablilization time after

POR or an exit from Sleep.

5.3.2 Two-Speed Start-up Sequence

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<2:0> bit of the OSCCON register.
3. OST is enabled to count 1024 clock cycles.
4. OST is timeout and waiting for the falling edge of the internal oscillator.
5. OSTS is set to 1.
6. The system clock is held low until the arrival of the next falling edge of the new clock (LP or XT mode).
7. System clock is switched to external clock source.

5.4 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate in the event of anoscillator failure. FSCM can detect the oscillator failure at any time after the Oscillator Start-up Timer (OST) has expired. FSCM can be enabled by setting the FCMEN bit in the Configuration Word register（UCFG1）to 1. FSCM can be used for all external oscillator modes (LP, XT and EC).

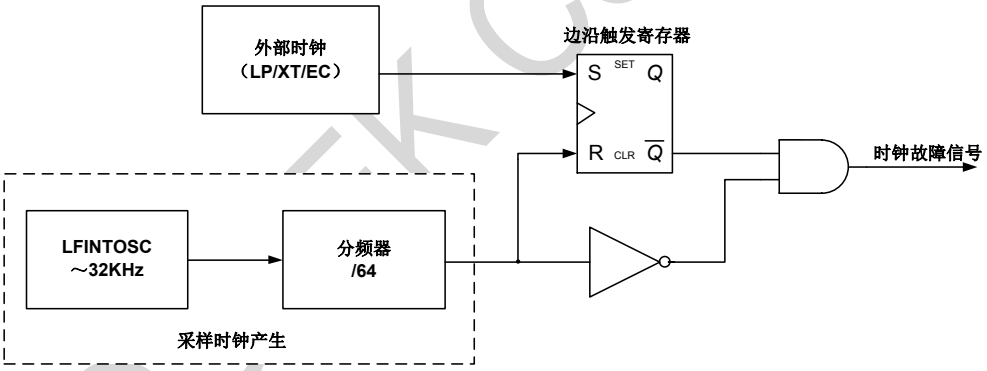


Figure 5-4. FSCM Schematic Block Diagram

5.4.1 Fail-Safe Detection

The FSCM module detects the oscillator fault by comparing the external oscillator with the FSCM sampling clock. LFINTOSC divided by 64 is the sampling clock. Please see Figure 5-4. There is a latch inside the fault detector. On each falling edge of the external clock, the latch is set to 1. On each rising edge of the sampling clock, the latch is cleared. If the entire half cycle of the sampling clock has passed and the main clock is still not in the low level, the fault is detected.

5.4.2 Fail-Safe Operation

When the external clock fault occurs, the FSCM switches the device clock to the internal clock source, and the OSFIF flag bit of the PIR1 register is set to 1. If setting the OSFIF flag bit to 1while setting the OSFIE bit of the

PIR1 register to 1, the interrupt will be generated. The device firmware will take the measure to alleviate the problem caused by the fault clock. The system clock will continue to come from the internal clock source until the device firmware restarts the external oscillator successfully and switches back to the external operation. The internal clock source selected by FSCM is determined by the IRCF<2:0>bit of the OSCCON register. It can be configured before the fault occurs.

5.4.3 Fail-Safe Condition Being Cleared

After reset, executing the sleep instruction or flipping the SCS bit of the OSCCON register, the fail-safe condition will be cleared. After the SCS bit of the OSCCON register is modified, the OST will be restarted. When OST runs, the device continues to operate with the INTOSC selected by the OSCCON.After the OST is timeout, the fail safe condition is cleared and the device will operate with the external clock source. The fail-safe condition must be cleared before clearing the OSFIF flag bit.

5.4.4 Reset or Wake-up from Sleep

FSCM is designed to detect the oscillator fault at any time after the oscillator timer (OST) has expired. OST is suitable for the wake-up occasion from the sleep status or any type of reset situation. OST can't be used in the EC clock mode, so once the reset or wake-up is done, FSCM is in the active status.When FSCM is enabled, the dual speed start-up is also enabled. Therefore, when OST runs, the program is always in the operation.

Note:
Because the range of oscillator start-up time varies in big range, the Fail-Safe circuit is not active during the oscillation start-up period (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit of the OSCCON register to verify whether the oscillator has successfully started and whether the system clock has been switched successfully.

6 Reset Timing

CMT2189C has several different Resets:

1. Power-on Reset(POR)
2. WDT Reset during normal operation
3. WDT Wake-up during Sleep
4. /MCLR Reset during normal operation
5. /MCLR Reset during Sleep
6. Brown-out Reset（BOR/LVR）
7. Error instruction Reset (Disable)

Some registers are not affected in any Reset condition.The status of these registers is unknown on POR, and is not affected by the Reset event.Most of the other registers are restored to their "reset status" at the time of the following reset event.

- Power-on Reset
- WDT Reset during normal operation
- WDT Reset during Sleep
- /MCLR Reset during normal operation
- Brown-out Reset（BOR）
- Error instruction Reset

When WDT is used as a timer, it can wake up MCU from Sleep. The MCU continues to run after Wake-up from Sleep, while in normal operation, WDT (watchdog) is timeout and reset, so the system will run over again. Because WDT Sleep Wake-up means that MCU continues to run rather than clear the settings of the /TO and /PD bits. The reset action under different conditions is different. See Table 6-1 and Table 6-2 in details.

The /MCLRB pin corresponding circuit has the anti shake function. It can filter the sharp pulse signal caused by the interference. The following figure is the overall block diagram of the reset circuit:

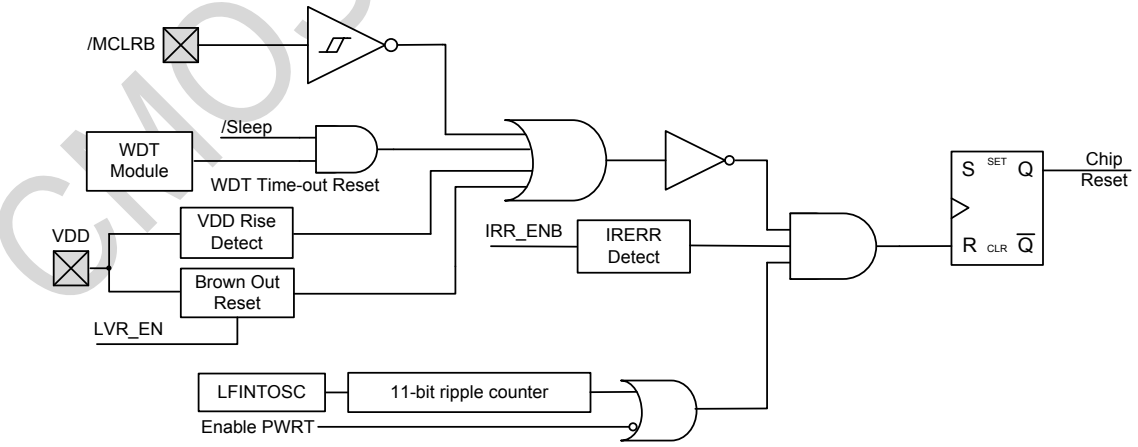


Figure 6-1. Reset Function Block Diagram

6.1 Power-on Reset (POR)

The on-chip POR circuit will hold the chip in the Reset status until the VDD has reached a high enough level. In order to take advantage of the POR, the user can simply connect the /MCLR pin through a resistor to VDD. This will eliminate external RC Reset circuit, but a maximum rise time for VDD is required. After the power-up is done, the system reset will not be released immediately, and a delay of about 4ms is needed, while the digital circuit is held in the reset status.

6.2 External Reset (MCLR)

It should be noted that a WDT Reset does not pull the /MCLRB pin down.Voltages applied to the pin that exceed its specification (such as ESD event) can result in both /MCLRB Reset and excessive current beyond the device specification. Therefore, we recommend that users no longer connect /MCLRB to VDD directly with one resistor but use the following circuit.

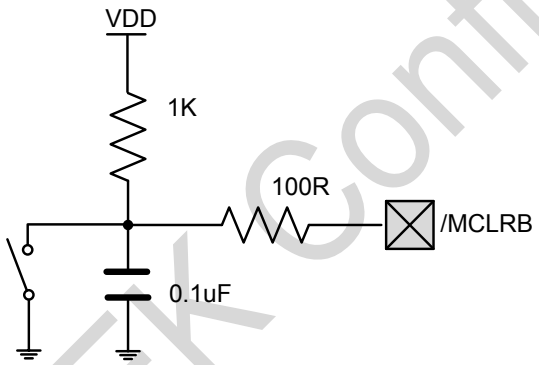


Figure 6-2. External Reset Reference Circuit Diagram

The chip's CONFIG OPTION register (UCFG0) has a MCLRE Enable bit. When this bit is 0, the reset signal is generated inside the chip. When this bit is 1, the PA5/MCLR pin of the chip becomes the external reset pin.In this mode, the /MCLR pin has a Weak-Pull on the VDD.

6.3 Power-up Timer (PWRT)

PWRT provides a fixed 64ms timing (normal) for Power-on Reset and Brown-out Reset. This timer is driven by an internal slow clock.The chip is held in a reset status before the timeout of the timer.This time ensures that the VDD will rise to a sufficiently high voltage to make the system work properly.PWRT can also be enabled by the system CONFIG register (UCFG0).When the low voltage reset function is opened, the user should also open the PWRT. The PWRT timing is triggered by the VDD voltage exceeding the VBOR threshold. In addition, it should be noted that the actual time varies with the conditions of temperature and voltage due to the internal slow clock drive. This time is not a precise parameter.

6.4 Brown-out Reset (BOR)

Low Voltage Reset is controlled by UCFG1<1:0> bit. Low voltage reset refers to the reset that the power supply voltage is lower than the VBOR threshold voltage.However, low voltage reset may not occur when the VDD voltage is lower than VBOR and the time does not exceed TBOR. The VBOR voltage needs to be calibrated before the chip is shipped. The calibration can be completed by writing the internal calibration register through the serial port. If the BOR (Brown-out Reset) is enabled (UCFG1<1:0>=00), the requirement for the maximum VDD voltage rising time will not exist. The BOR circuit will control the chip in the reset status until the VDD voltage exceeds the VBOR threshold voltage. It should be noted that the POR circuit does not generate a reset signal when the VDD is lower than the threshold of the system that can work normally.If the reset signal is generated by the BOR circuit, the VDD voltage must hold for more than 100us at the VSS level.

6.5 Error Instruction Reset

When the instruction register of CPU obtains the undefined instruction, the system will be reset. Using this function can increase the anti-interference ability of the system.

6.6 Timeout Action

On power-up, the timeout sequence is as follows: PWRT timing is invoked after POR has expired. Since the timing is invoked after POR has expired, the timeout event will occur if the /MCLR holds at a low level for a long time. If /MCLR is pulled up, CPU will begin to execute immediately. This will be useful in the case of test or multiple MCU synchronization.

PCON（Power Control Register）

There are two status bits in the PCON register to indicate what type of Reset has occurred. Bit0 is the /BOR bit, which is an unknown status on Power-on Reset, and the software must set it to 1 and check if it is 0. Bit1 is the /POR bit, which is 0 on Power-on Reset, and the software must set it to 1.

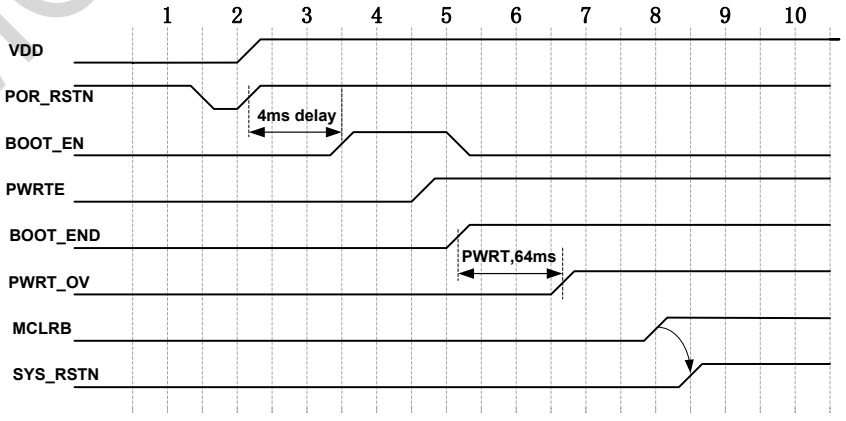


Figure 6-3. Power-on Reset with MCLRB

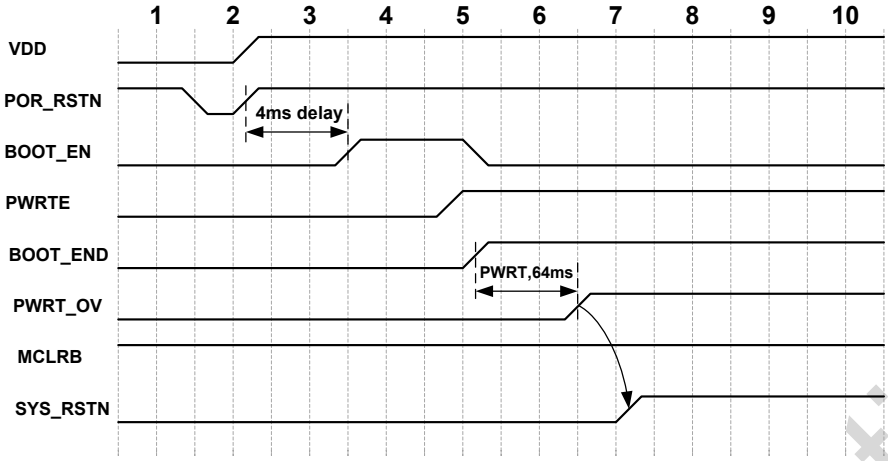


Figure 6-4. Power-on Reset without MCLRB

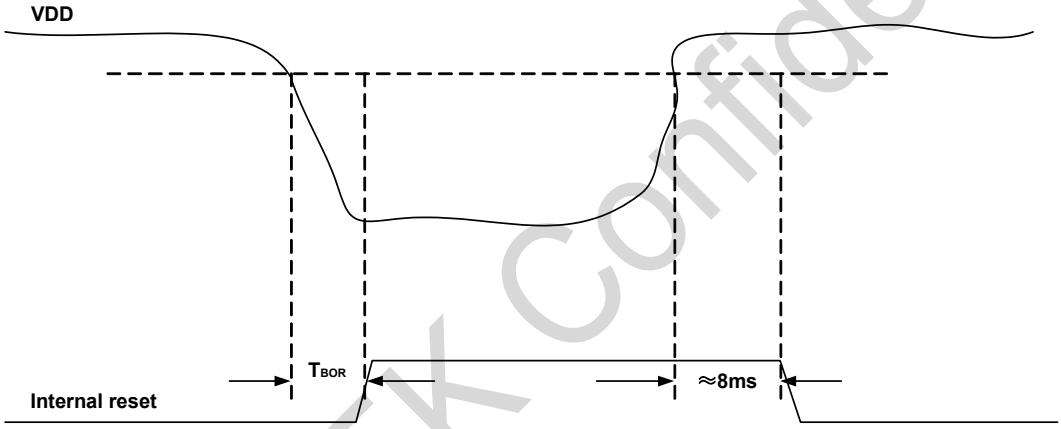


Figure 6-5. BOR Reset

Note:

1. After power on reset or low voltage reset, and when PWRTEB (UCFG0.4) is low, PWRT is active.It is 2048 internal slow clock cycles, about 64ms.
2. The TBOR time is about 157us.
3. After the voltage is restored to normal, the internal reset will not be released immediately, but wait for about 8ms.

Table 6-1. Timeout in aVariety of Cases

Oscillator configuration	Power-on Reset		Brown-out Reset		Sleep Wake-up
	/PWRTEB=0	/PWRTEB=1	/PWRTEB=0	/PWRTEB=1	
INTOSC	TPWRT	-	TPWRT	-	-

Table 6-2. STATUS/PCON Bit and Significance（U-No change，X-Unknown）

/POR	/BOR	/TO	/PD	Condition
0	X	1	1	POR
U	0	1	1	BOR
U	U	0	U	WDT Reset
U	U	0	0	WDT Wake-up
U	U	U	U	/MCLR Reset during normal operation
U	U	1	0	/MCLR Reset during Sleep

7 BOOT

After POR or BOR, inserting a status, the unit of EEPROM is mapped into a configuration register. The address of EEPROM starts from 2000H. The system reset is released until the end of the BOOT, as shown in Figure 6-3 and Figure 6-4. The process needs about 17us.

8 Watchdog Timer

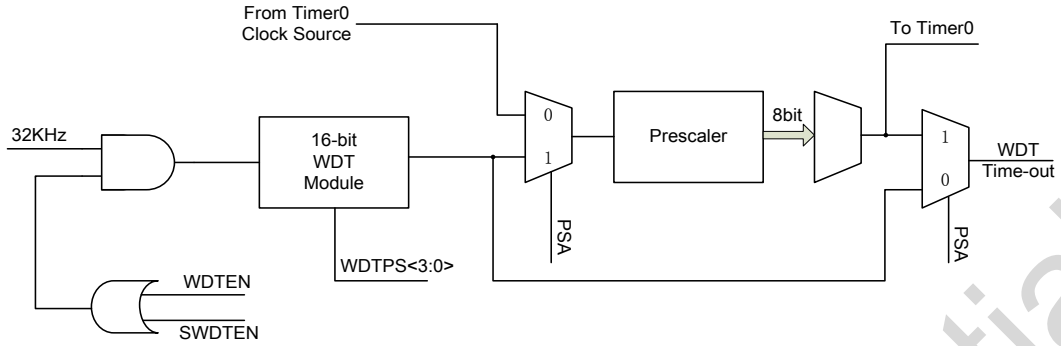


Figure 8-1. Watchdog and Timer0 Diagram

The watchdog's clock source is the internal slow clock (32KHz), which is a 16-bit counter.It shares an 8-bit prescaler with the timer0. The enabled bit WDTEN is the third bit of the configuration register UCFG0.When WDTEN is 1, enable the watchdog. When it is 0, disable the watchdog. It is determined by the BOOT during the power start-up process, or it can be written through the external serial port.Clearing the watchdog instruction CLRWDT and SLEEP will clear the watchdog counter.In the case of enabling the watchdog, the watchdog overflowing can be used as a wake-up source when the MCU is in sleep, and the watchdog can be used as a reset source when the MCU works well.

Table 8-1. Watchdog Status

Condition	Watchdog Status
WDTEN and SWDTEN are 0 at the same time	Clear
CLRWDT instruction	
Enter the SLEEP, exit the SLEEP	

Note:
If the internal slow clock switches from 32K to 256K mode (or vice versa from 256K to 32K mode), it doesn't affect the watchdog timing, because WDT is fixed to use the 32K clock source.

9 Timer0

9.1 Timer0 Introduction

The timer0 is 8-bit and can be configured as the counter or the timer. When it is configured as the external event (T0CKI) counter, it can count at the rising edge or the falling edge. When it is configured as the timer, the counting clock is 2 frequency division of the system clock, which is, it increases once in each instruction cycle. There is an 8-bit prescaler shared with WDT. When the PSA bit is 0, the prescaler is assigned to the timer0.

Note: When the value of PSA is changed, the hardware will automatically clear the prescaler.

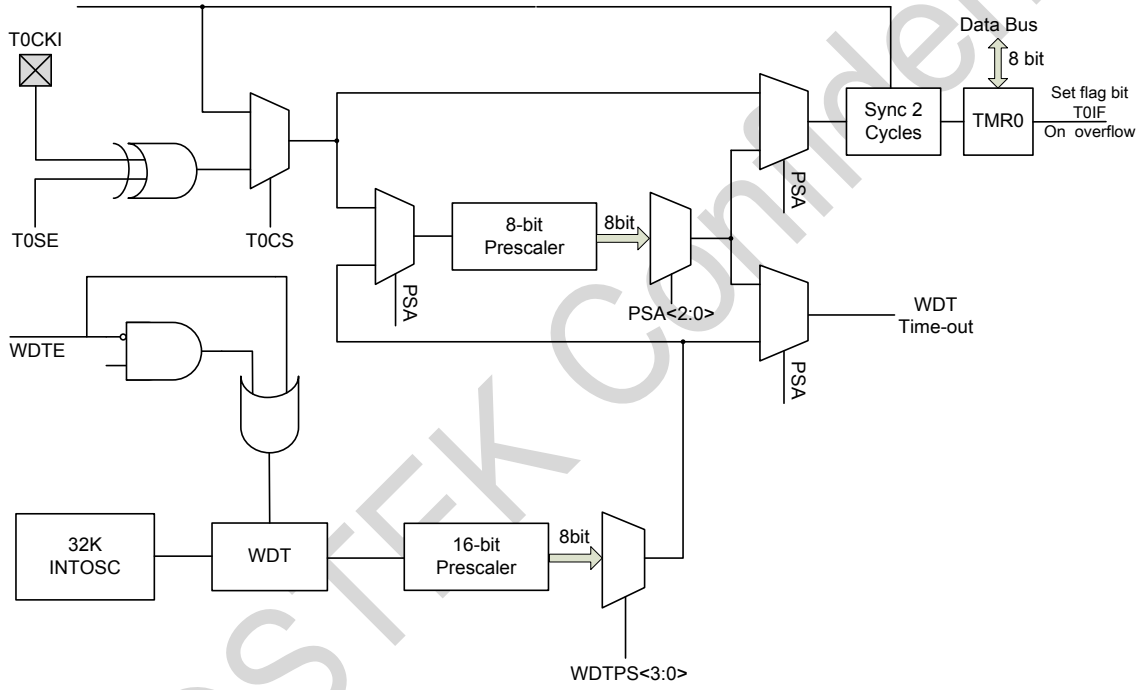


Figure 9-1. Watchdog and Timer0 Diagram

9.2 Timer0 Timer Mode

In this mode, the timer0 adds 1 (without prescaler) in each instruction cycle. The software can clear the T0CS bit of the OPTION register to enter the timer mode.When the software writes to TMR0, the timer does not increase progressively in the following 2 cycles.

9.3 Timer0 Counter Mode

In this mode, the timer0 adds 1 when it is triggered by the rising or falling edge of each T0CKI pin (without

prescaler). The T0SE bit of the OPTION register determines which edge to trigger. The software can set the T0CS bit of OPTION register to 1 to enter the counter mode.

9.3.1 Software Configuring Prescaler Circuit

The chip has a prescaler circuit in front of the Timer0 and WDT timer, which can be assigned to Timer0 or WDT timer, but the two can not use the prescaler at the same time. Specifically assigning to Timer0 or WDT is determined by the PSA bit of the OPTION register. When the PSA is 0, the prescaler is assigned to Timer0. In the Timer0 prescaler mode, there are 8 prescale rate (1:2 to 1:256). It can be set by the PS<2:0> bit of the OPTION register.

Note:

1. The prescaler circuit is neither readable nor writable. Any write operation to the TMR0 register will clear the prescaler circuit.
2. When the prescaler circuit is assigned to WDT, one CLRWDT instruction can clear the prescaler circuit.
3. The prescaler circuit can be assigned to Timer0 or WDT timer, the switching of the prescaler between the timer0 and the WDT may result in a false reset.

When the prescaler assignment is switched from TMR0 to WDT, please execute the following instruction sequence.

```
BANKSEL   TMR0
CLRWDT                          ；Clear WDT
CLRR      TMR0                  ；Clear TMR0 and prescaler
BANKSEL   OPTION_REG
BSR       OPTION_REG,  PSA      ；Select WDT
CLRWDT

LDWI      b'11111000'；Mask prescaler bits
ANDWR     OPTION_REG,  W
IORWI     b'00000101'；Set WDT prescaler to 1:32
LDWI      OPTION_REG
```

When the prescaler assignment is switched from WDT to TMR0, please execute the following instruction sequence.

```
CLRWDT                          ；Clear WDT and prescaler
BANKSEL   OPTION_REG
LDWI      b'11110000'；Mask TMR0 select and prescaler bits
ANDWR     OPTION_REG,  W
IORWI     b'00000011'；Set prescaler to 1:16
STR       OPTION_REG
```

9.3.2 Timer0 Interrupt

An interrupt is generated (if enabling the interrupt) when the TMR0 timer overflows from 0xFF to 0x00. This overflow sets the T0IF bit.

Note: Timer0 interrupt cannot wake up the CPUfrom Sleep since the timer is shut off during Sleep.

9.3.3 Drive Timer0 with an External Clock

In the counter mode, the synchronization between T0CKI pin input and Timer0 register is accomplished by sampling the output on the Q1 and Q2 cycles of the internal clock phase, so the high level time and low level time of the external clock source cycle must meet the relevant timing requirement.

10 Timer2

The timer2 is the 8-bit timer, which contains the following functions:

- 8-bit timer register
- 8-bit period register
- Interrupt on TMR2 match with PR2
- Software programmable prescaler(1:1，1:4，1:16)
- Software programmable postscaler(1:1 to 1:16)

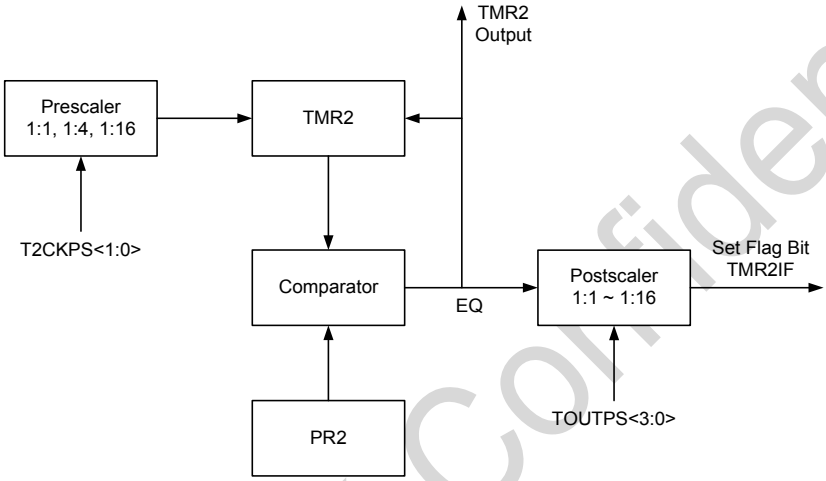


Figure 10-1. Timer2 Diagram

Timer2 Operation Principle

The clock input of the Timer2 module is the system instruction clock (FOSC/2).The clock is sent to the Timer2 prescaler, and its prescale rate has three options of 1:1, 1:4 and 1:16. The output of the prescaler is used to increase the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when to match. TMR2 will increase from 00h until it matches PR2. The following two cases will occur when matching:

- TMR2 is reset to 0x00 on the next increment cycle.
- Timer2 postscale rate increases progressively.

The matching output of comparing Timer2 and PR2 is sent to the Timer2 postscaler.The option range of the postscaler is from 1:1 to 1:16.The output of the Timer2 postscaler is used to set the interrupt flag bit TMR2IF of the PIR1 register to 1.

Note:

1. Both TMR2 and PR2 are read-write registers. Their values are initialized to 0 and 0xFF respectively upon Reset.
2. Setting the TMR2ON bit of the T2CON register to 1 can open Timer2, and conversely clearing the

TMR2ON bit can close the Timer2.

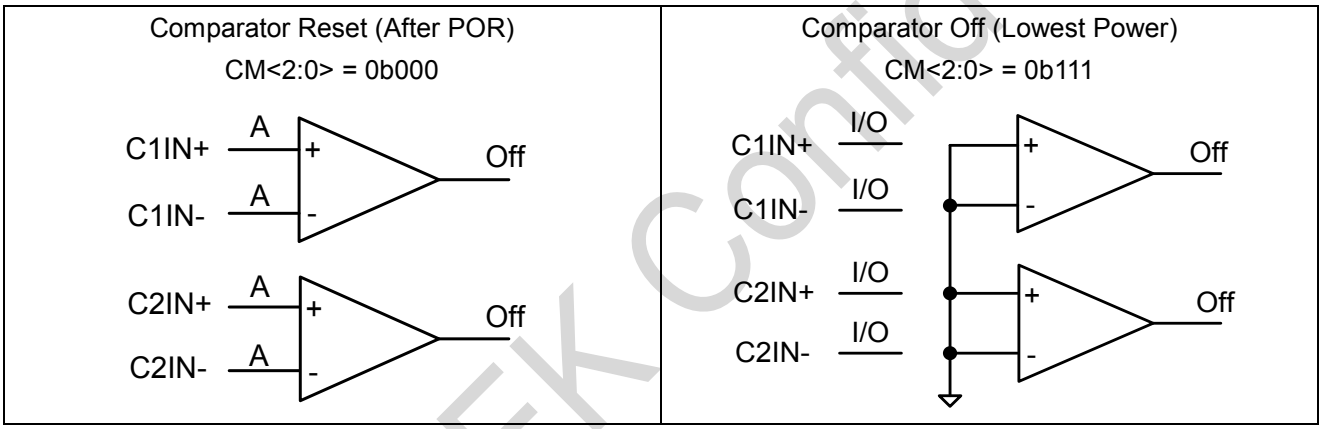
3. The Timer2 prescaler is controlled by the T2CKPS bit of the T2CON register.
4. The Timer2 postscaler is controlled by the TOUTPS bit of the T2CON register.
5. The prescaler counter and postscaler counter will be cleared when the following register is written:
   - Write TMR2
   - Write T2CON
   - Any Reset action
6. Writing T2CON does not clear the TMR2 register.

11 Comparator

The chip is integrated with 2 analog comparators. Since the function pins of the comparator2 are used for the RF serial control bus at the same time, the 2 comparators can not be used.

It should be noted that when reading a port register, the value that the software read is 0 if the pin is configured as an analog signal pin.When the pin is set to the digital input pin, the comparator will still think that the pin will input an analog signal and output the corresponding result.If a pin is set to the digital input, and the actual voltage on this pin is still an analog voltage, it may cause the input buffer circuit to consume more current than that in the specifications.

The analog comparator has 8 configuration modes. They are selected by the CM<2:0> bit of the CMCON0 register. Because the functional pins are used in the RF serial control bus, there are only two statuses as follows:



- Analog function (A): The digital input cache is masked.
- Digital function (D): The comparator digital output will cover the other functions in the pin.
- Normal port function (I/O): Be independent of the comparator.

When the word "A" is marked on the port, the status of the current pin or the statusof the TRIS bit of the I/O control register will return to 0 when reading.The user should set the TRIS bit corresponding to the the analog input pin to 1 to close its digital output drive circuit.

When the word "D" is marked on the port, the user should set the corresponding TRIS bit to 0 to open the digital output driver circuit.

In addition, the comparator configuration switching should mask the comparator interrupt to avoid unnecessary mistrigger events.

12 Data EEPROM

The chip is integrated with 256 bytes of EEPROM, which is accessed through the EEADR. The software can program EEPROM through EECON1 and EECON2.The hardware implements its own timing function of erasing and programming without software query, and saves the limited code space.At the same time, using this feature, after starting the programming cycle, the chip can enter the sleep mode to reduce the power consumption.

The following initialization operations must be performed before the data EEPROM is used (either read or write): Two times 0xAA is written for a certain unit of EEPROM that is not used, and the subsequent program no longer operates on this unit. Such as:

```
SYSTEM_INIT
……
……
LDWI      0x55
STR       EEROM_ADDR
LDWI      0xAA
STR       EEPROM_DATA
LCALL     EEPROM_WRITE
LCALL     EEPROM_WRITE
```

Programming data EEPROM steps

In order to read the data memory unit, the user must write the address into the EEADR register, and then set the control bit RD of the EECON1 register to 1. In the next cycle that follows, the user can write the EEPROM data into the EEDAT register.This data can therefore be read by the next instruction. EEDAT will keep this value until the user reads or writes data to the unit next time (during the write operation).

```
BANKSEL   EEADR
LDWI      dest_addr
STR       EEADR
BSR       EECON1,   RD
LDR       EEDAT,   W
```

13 Clock Measurement

This function can accurately measure the internal slow clock period.

In this mode, the prescaler and postscaler configuration of TIMER2 is automatically changed to 1:1. They make up a 12-bit timer. The TIMER2 count clock is the system clock Fosc, not the instruction clock Fosc/2 under the ordinary mode.After the end of the calculation, the result is automatically stored in the SOSCPR register. The unit is the number of the system clock Fosc.

Operation steps:

1. In order to improve the measurement accuracy, it is suggested that IRCF is set to 111 and SCS is set to 1, and the system clock of 16M is selected.
2. Set T2CON.2 to 1, enable TIMER2.
3. If selecting the average of the four times, set MSCKCON.2 to 1, and otherwise clear it.
4. Set MSCKCON.1, start measuring.
5. After the end of the measurement, MSCKCON.1 is automatically cleared, and the interrupt flag is set to 1.
6. The user can end the measurement in a query or interrupt manner.
7. When the interrupt flag is checked to be 1, the read SOSCPR is the final result.

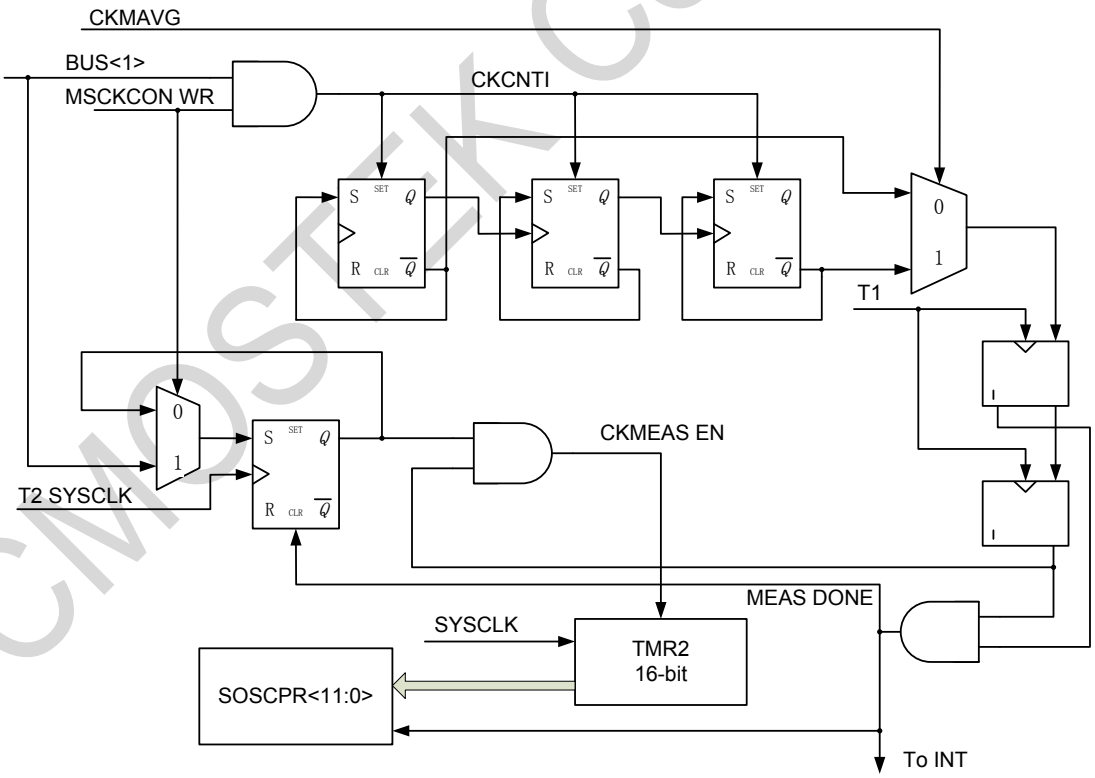


Figure 13-1. Slow Clock Measurement Mode Block Diagram

14 Interrupt Mode

CMT2189C has the following interrupt sources:

- External Interrupt from PA2/INT
- Timer0 Overflow Interrupt
- PORTA ChangeInterrupt
- Timer2 MatchInterrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- Comparator Interrupt

The Interrupt Control Register (INTCON) and the Peripheral Interrupt Request Register (PIR1) record the interrupt flag bit. INTCON also contains the Global Interrupt Enable bit (GIE).

When the interrupt is served, the following action occurs automatically:

- GIE is cleared to close the interrupt.
- The return address is pushed onto the stack.
- The program pointer is loaded to the 0004h address.

The Return from Interrupt instruction (RETFIE) exits the interrupt routine, as well as sets the GIE bit, which re-enable unmasked interrupt.

The INTCON register contains the following interrupt flag bit:

- INT pin interrupt
- PORTA change interrupt
- Timer0 overflow interrupt

PIR1 includes the Peripheral Interrupt Flag bit. PIE1 includes its corresponding Interrupt Enable bit.

14.1 INT Interrupt

The external interruptof the INT pin is triggered by the edge. When the INTEDG bit of the OPTION register is set to 1, it is triggered at the rising edge. And when the INTEDG bit is cleared, it is triggered at the falling edge.When an effective edge occurs on the INT pin, the INTF bit of the INTCON register is set to 1.The interrupt can be disabled by clearing the INTE control bit of the INTCON register. Before the interrupt is reallowed, the INTF bit must be cleared by the software in the interrupt service program.If the INTE bit is set to 1 before entering the sleep status, the INT interrupt can wake up the MCU from the sleep status.

Note: When INT interrupt is used, the ANSEL and CM2CON0 registers must be initialized so that the analog channel is configured as a digital input.The pin configured as an analog input is always read to 0.

14.2 PORTA Level Change Interrupt

The input change on PORTA canset the PAIF bit of the INTCON register.The interrupt can be enabled or disabled by setting/clearingthe PAIE bit. In addition, each pin of the port can be configured through the IOCA register.

Note:

1. When using the PORTA level change interrupt, the ANSEL and CM2CON0 registers must be initialized so that the analog channel is configured as a digital input.The pin configured as an analog input is always read to 0.
2. When initializing the level change interrupt, first configure it as a digital input IO, and set the corresponding IOCA to 1, and then read the PORTA.
3. When the IO level changes, the PAIF bit is set to 1.
4. Read the PORTA before clearing the interrupt flag, and then clear the PAIF.

14.3 Interrupt Response

The external interrupt includes the interrupt from the INT pin or the PORTA change interrupt, and the interrupt delay is usually 1 to 2 instruction cycles.It depends on the actual situation of the interrupt.

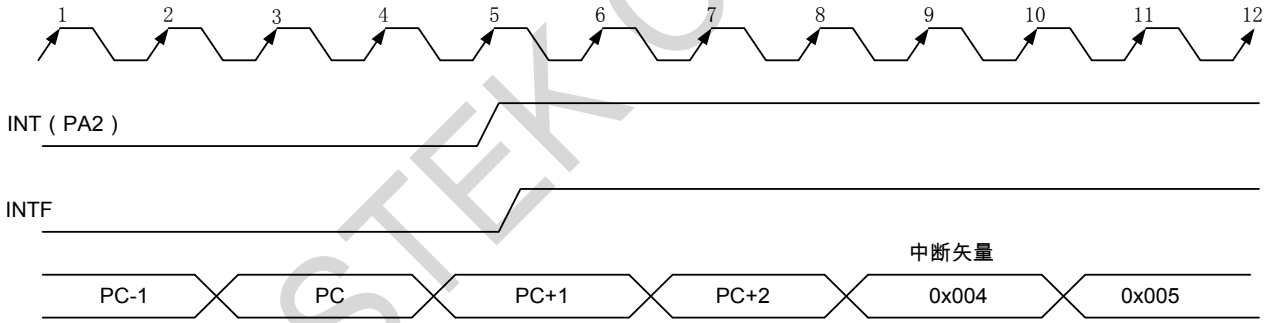


Figure 14-1. Interrupt Response Timing Diagram

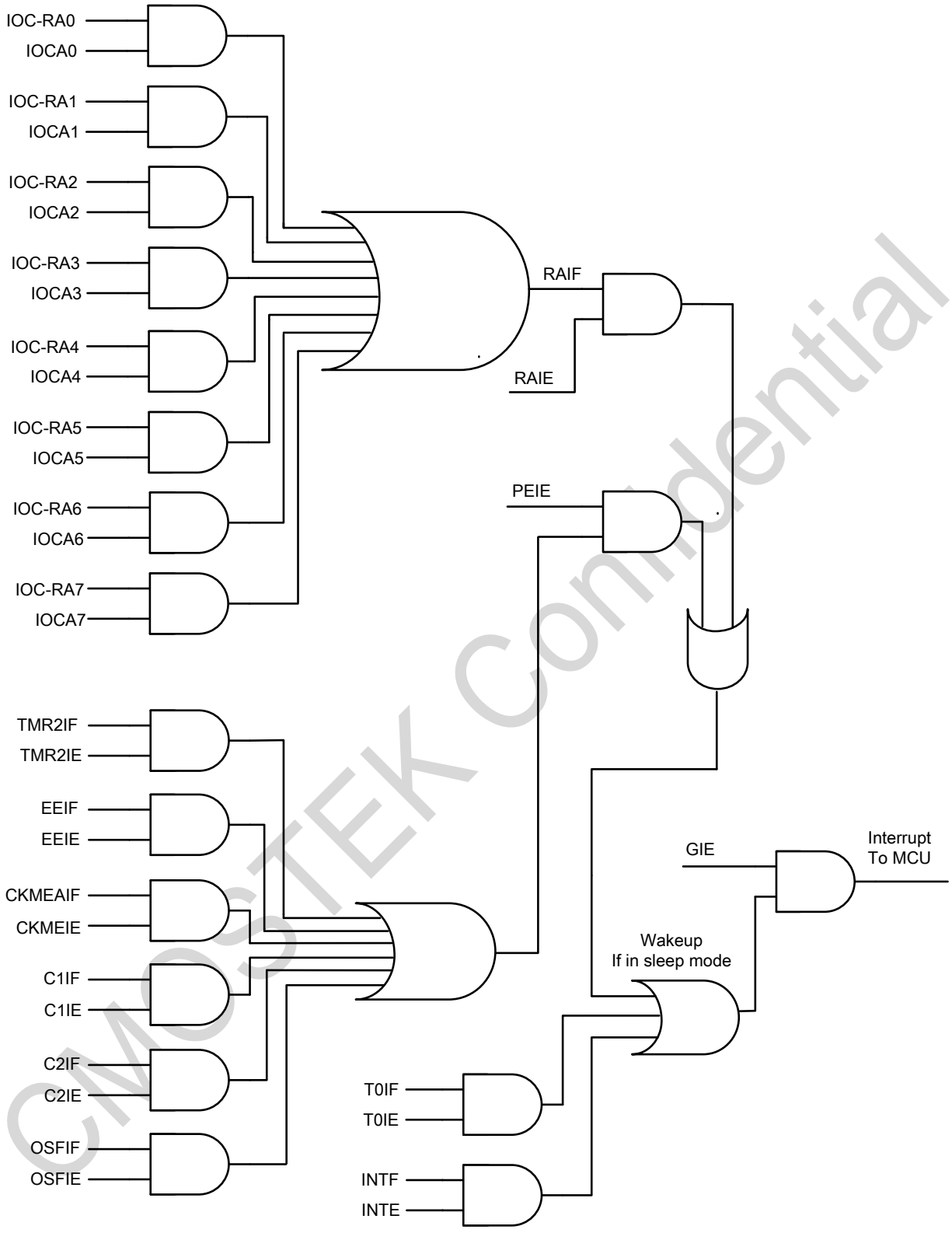


Figure 14-2. Interrupt Generation Circuit Block Diagram

14.4 Context Saving During Interrupts

During an interrupt, only the return PC is automatically saved on the stack.In general, users may wish to savethe key register value on the stack, such as W, STATUS register, and so on.These must be implemented insoftware. The temporary registers W_TEMP and STATUS_TEMP should be placed in the last 16bytes of the GPR. The 16bytes of GPR crosses two pages, so users can save a little bit of code space.

15 MCU Sleep Saving Mode

The chip enters the sleep status after the execution of the SLEEP instruction.

In order to achieve minimum sleep power consumption, the software should set all IO to high or low, and there is no the external circuit consumption from the IO pin. I/O is the input pin, and the external circuit should pull it high or low to avoid flipping the level and increasing the power consumption. /MCLR should be set to high level.

In order to achieve the lowest sleep power consumption, it is recommended that when the configuration is the crystal mode or external clock mode, the clock loss detection is turned off, that is, the FCMEN bit of UCFG1 is cleared. Meanwhile, the configuration bit CM<2:0> of the comparator is written as 0b111, and the comparator module is closed.

15.1 Wake-up Mode

The following events can wake up the chip:

- There is an external reset on the /MCLR pin.
- WDT is timeout
- There is the interrupt on the PA2/INT pin. There is the PORTA change interrupt or other peripheral interrupt.

Clearing watchdog (CLRWDT), entering the sleep mode (SLEEP) or waking up the sleep mode will clear the watchdog counter.

15.2 Watchdog Wake-up

The watchdog works in the internal slow clock (32KHz). It is a 16-bit counter, and shares an 8-bit prescaler with the timer0. Enable bit is the third bit WDTEN of the configuration register UCFG0. When it is 1, enable the watchdog; when it is 0, whether or not to enablethe watchdog is determined by the SWDTEN bit. SWDTEN is located in the WDTCON register.

Clearing watchdog (CLRWDT) and SLEEP instruction will clear the watchdog counter.

When enabling the watchdog, the watchdog overflowing event can be used as a wake-up source when MCU is in Sleep, while it can be used as a reset source when MCU works normally.

16 I/O Port

There are 16 GPIO portsin the chip. But limited to the packagesize, only 6 IO ports of PORTA[2:0], PORTA5, PORTC2 and PORTC4 have the package terminals, and the othersare inside the chip and have no the package terminals.In addition to being an ordinary input / output port, these IO ports usually have some functions to communicate with the kernel peripheral circuits, see the following in details.

16.1 PORTA Port and TRISA Register

PORTA is an 8-bit bi-directional port.The corresponding data direction register is TRISA. However, it is important to note that the fifth bit is not used here because PORTA<5> is a single input directional port.Setting a certain bit to "1" in the TRISA register will set the corresponding PORTA port as the input port (at this time, the output driver will be turned off). Conversely, setting a certain bit to "0" will set the corresponding PORTA port as the output port.When configurated as the output port, the output drive circuit is opened and the data in the output register will be sent to the output port.When reading the PORTA, the PORTA content will reflect the status of the input port.When writing the PORTA, the PORTA content will be written to the output register.All operations follow the "read-modify-write" micro process, namely the data is read, and then is modified, and then is written to the output register.When MCLRE is 1, the value read from PORTA<5> is 0, which is as the external reset pin at this time.

16.2 Other Functions of the Port

Each port of the PORTA has a status change interrupt option and a weak pull-up option.

16.2.1 Weak Pull-Up

Each port of the PORTA (except for PORTA<5>) has an internal weak pull-up function that can be set individually. Controlling the bit of the WPUAx register can enable or turn off the weak pull-up circuit.When the GPIO is set as output, these weak pull-up circuits are automatically turned off.The weak pull-up circuit can be turned off during the power-upreset period.This is determined by the /PAPU bit of the OPTION register.There is also a weak pull-up function inside PORTA<5>. The weak pull-up function will be automatically enabled when the PORTA<5> is set as /MCLR. When the PORTA<5> is set as GPIO, the weak pull-up circuit will be automatically turned off.

16.2.2 Interrupt-On-Change

Each port of the PORTA can be separately set as an interrupt source (interrupt-on-change).Controlling the bitof the IOCAx register can enable or turn off the interrupts of these ports. The interrupt-on-change is invalid on Power-on Reset.

When enabling the interrupt-on-change function, the current port level value is compared to the old value of

the data register read by the last reading action.All error matching results will be OR to form an interrupt flag bit. The PAIF flag bit of the INTCON register can wake the chip from the sleep status.The user needs to execute the following program to clear the flag bit:

1. A read or write operation to the PORTA will end any mismatched status;
2. Clear the PAIF flag bit.

The error matching result will always set the PAIF bit. Reading the PORTA once can end any status of error matching and clear the PAIF bit. The last read value kept in the data register will not be affected by /MCLR or BOR. As long as the error matching status exists, the PAIF bit is set to 1.

16.3 Port Description

Each port of PORTA and PORTC contains different reuse functions. Its specific functions and controls are described in this section.

16.3.1 PORTA<2:0>

The following figure describes the internal circuit architecture of the port, and PA<2:0> can be configured as the following functional port:

- GPIO
- Debug serial clock (PA0)
- Debug serial data (PA1)
- External interrupt input (PA2)
- Timer0 external clock source (PA2)

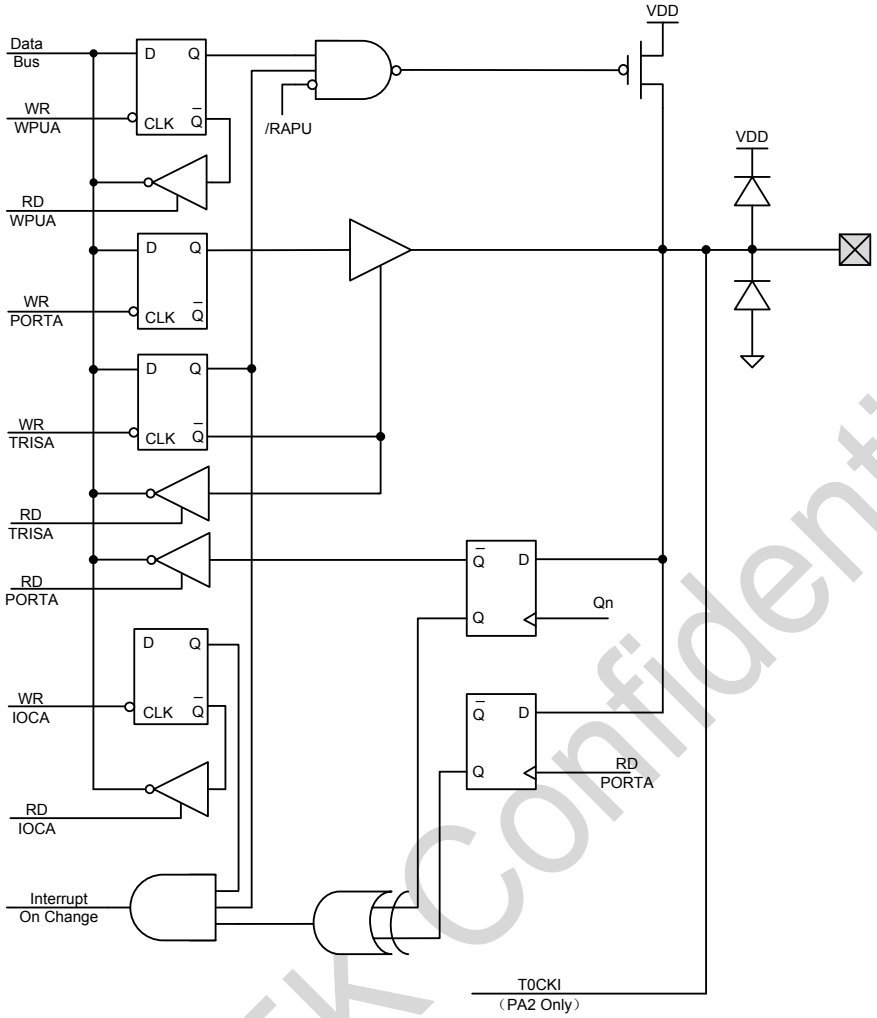


Figure 16-1. PA<2:0> Architecture Block Diagram

16.3.2 PORTA5

The following figure describes the internal circuit architecture of the port, and PA5 can be configured as the following functional port:

- Digital Input
- External Reset

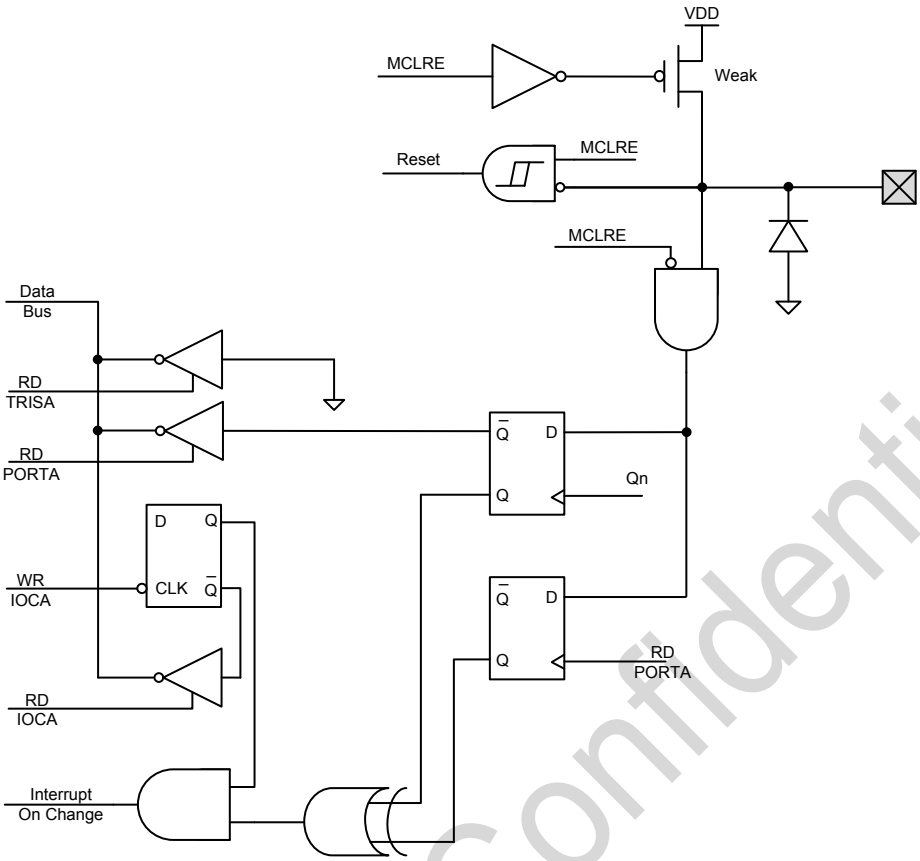


Figure 16-2. PA5 Architecture Block Diagram

16.3.3 PORTC4 and PORTC2

The following figure describes the internal circuit architecture of the port, and PC4 and PC2 can be configured as the following functional ports:

- GPIO
- RFDAT, that is the TWI data and direct mode data input (only PC4)
- RFCLK, that is the clock line of TWI (only PC2)
- Comparator output (only PC4, but not available, because it is used to control the RF part)

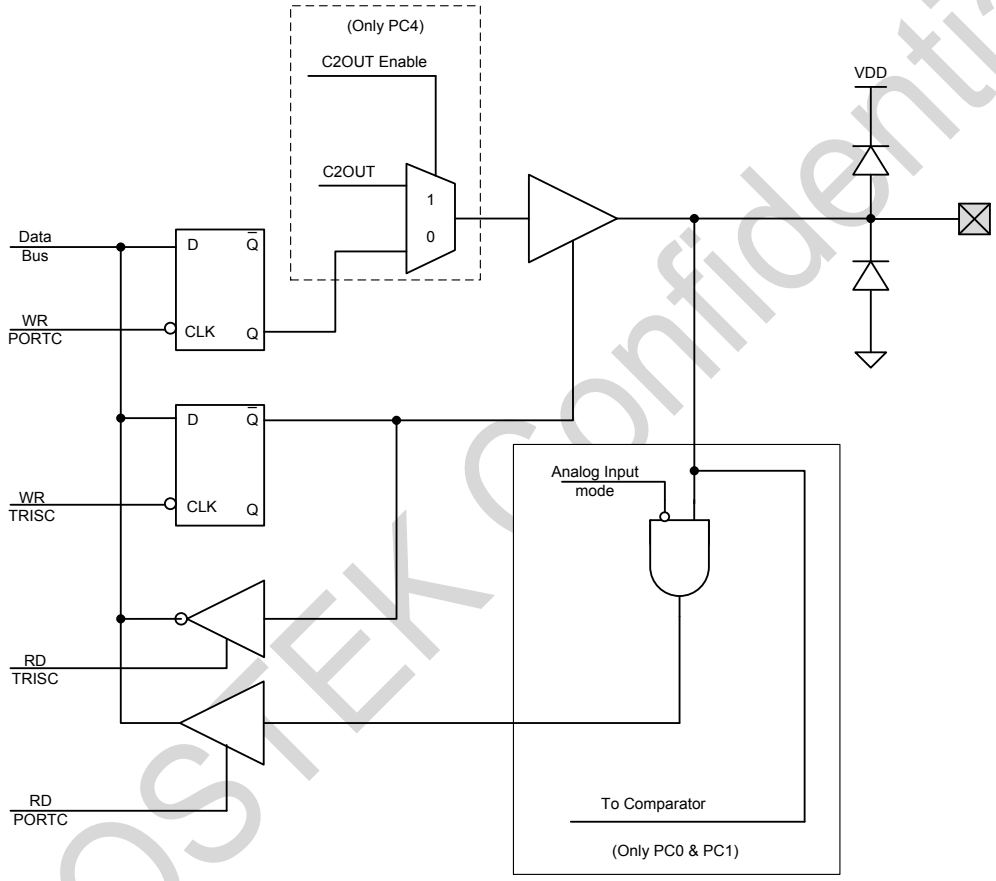


Figure 16-3. PC4~PC0 Architecture Block Diagram

17 Instruction Set List

CMT2189C uses the reduced instruction set architecture with a total of 37 instructions, and the following is the description of the instructions.

Table 17-1. Instruction Set Table

CMT	Instruction Period	Function	Operation	Status
BCR R, b	1	Bit clear	0-> R(b)	NONE
BSR R, b	1	Bit set	1-> R(b)	NONE
BTSC R, b	1（2）	Bit test, skip if 0	Skip if R(b)=0	NONE
BTSS R, b	1（2）	Bit test, skip if 1	Skip if R(b)=1	NONE
NOP	1	No operation	None	NONE
CLRWDT	1	Clear WDT	0-> WDT	/PF, /TF
SLEEP	1	ENTER SLEEPMODE	0-> WDT, STOP OSC	/PF, /TF
STTMD	1	Store W TO TMODE	W-> TMODE	NONE
CTLIO R	1	Control IO direction reg	W-> IODIRr	NONE
STR R	1	Store W to reg	W-> R	NONE
LDR R, d	1	Load reg to d	R-> d	Z
SWAPR R,d	1	Swap halves reg	[R(0-3)R(4-7)]-> d	NONE
INCR R, d	1	Increment reg	R+ 1-> d	Z
INCRSZ R, d	1（2）	Increment reg, skip if 0	R+ 1-> d	NONE
ADDWR R, d	1	Add W and reg	W+ R-> d	C, HC, Z
SUBWR R, d	1	Sub W from reg	R- W-> d R+ /W+ 1-> d	C, HC, Z
DECR R, d	1	Decrement reg	R- 1-> d	Z
DECRSZ R, d	1（2）	Decrement reg, skip if 0	R- 1-> d	NONE
ANDWR R, d	1	AND W and reg	R& W-> d	Z
IORWR R, d	1	Inclu.OR W and reg	W| R-> d	Z
XORWR R, d	1	Exclu.OR W and reg	W^ R-> d	Z
COMR R, d	1	Complement reg	/R-> d	Z
RRR R, d	1	Rotate right reg	R(n)-> R(n-1), C-> R(7), R(0)-> C	C
RLR R, d	1	Rotate left reg	R(n)-> R(n+1), C-> R(0), R(7)-> C	C
CLRW	1	Clear working reg	0-> W	Z
CLRR R	1	Clear reg	0-> R	Z
RETI	2	Return from interrupt	Stack-> PC,1-> GIE	NONE
RET	2	Return from subroutine	Stack-> PC	NONE
LCALL N	2	Long CALL subroutine	N-> PC, PC+1-> Stack	NONE
LJUMP N	2	Long JUMP address	N-> PC	NONE
LDWI I	1	Load immediate to W	I-> W	NONE
ANDWI I	1	AND W and imm	W& I-> W	Z
IORWI I	1	Inclu.OR W and imm	W| I-> W	Z

CMT	Instruction Period	Function	Operation	Status
XORWI I	1	Exclu.OR W and imm	W^ I-> W	Z
RETW I	2	Return, place imm to W	Stack-> PC, I-> W	NONE
ADDWII	1	Add imm to W	W+I-> W	C, HC, Z
SUBWI I	1	Subtract W from imm	I-W-> W	C, HC, Z

Note: The TMODE register of the chip refers to the OPTION, that is, the operation of the STTMD instruction is to save the W to OPTION.

18 Document Modification Record

Table 18-1. Document Modification Record Sheet

Version	Chapter	Modification descriptions	Date
1.0	All	Initial release	2018-05-17

19 Contact Information

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