CMT2210LH单接收芯片原理图及PCB版图设计指南

1. Summary

This application note provides basic schematic and PCB layout design guidelines for users of product development using the CMOS TEK NextGenRFTM series of single-receiver chipsets, in order to help users quickly achieve the performance metrics required by the application: such as improved sensitivity, reduced power consumption and system cost , improve anti-jamming capabilities.

The product models covered in this document are shown in the table below.

Table1. Product models covered by this document

Product model	Operating Frequency（MHz）	Modulation Mode	Main Function	Configuration Method	Package
CMT2210LH	315/433.92	OOK	Stand-alone receiver	-	SOP8

This document will use the CMT221xLx EM schematics and PCB design as a reference to illustrate the following considerations for using the CMOSTEK NextGenRFTM series of single-receiver chips:

- RF input design
- Crystal circuit design
- Digital signal design
- Power and ground design
- sensitivity optimization considerations
- Test circuit design
- Design check items

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2. RF impedace matching

The matching network achieves the design goal of improving the receiving sensitivity by matching the impedance matching value of the antenna to the RF input impedance of the chip.

CMOSTEK NextGenRFTM 2210Lx series single-receiver products use a single-ended LNA input. Only one capacitor, C0, and one inductor, L2, are required to implement the matching function. Most of the time, adding a band-pass filter network composed of L2 and C1 at the input of the antenna can effectively filter the interference from the complex electromagnetic environment to the receiver. The complete matching network is shown below.

According to different package types and different application frequency bands, users need to use different component values for matching

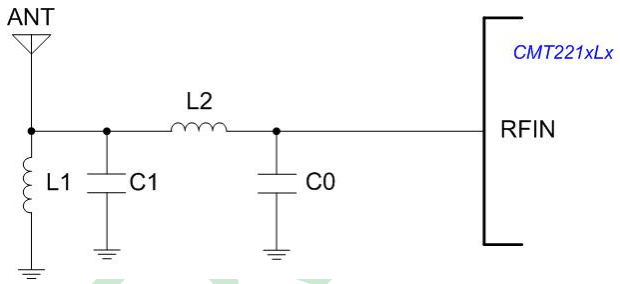

Figure 1. CMT221xLx RF Input Matching Network

Described as follows:

1. The figure above is not related to other circuits outside the RF matching network.
2. The matching network component values for different packages and different frequencies are shown in the following table. among them:
   a) L2, L2 specifications: ± 5%, 0603 multiplayer chip inductors;
   b) The specifications of C0 and C1 are: ±0.25 pF, 0603 NP0, 50 V.

Table 2. Single Receive Matching Network Values

Product Model	Package	Band(MHz)	Recommended Match			
			L1 (nH)	C1 (pF)	C0 (pF)	L2 (nH)
CMT2210LH	SOP8	315	62	12	3	68
		433	36	10	3	36

The equivalent impedance of the RF input at different frequencies is shown in the following table.

Table 3. Input Equivalent Impedance

Frequency (MHz)	RFIN equivalent impedance	
	Z_{RFIN}	R_{RFIN} // C_{RFIN}
315	120 – j*98	200 Ω // 2.0 pF
433.92	79 – j*106	220 Ω // 2.2 pF

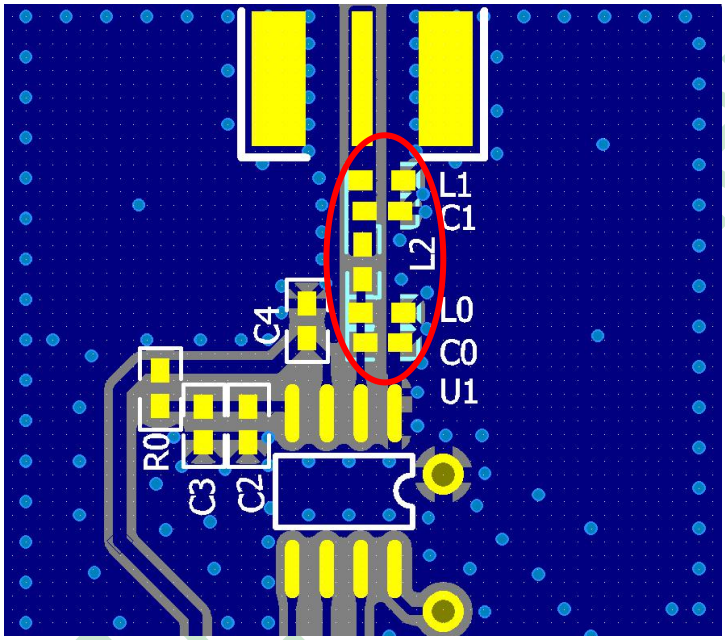

Figure 2. Layout design reference for matching networks

The figure above shows the layout of the single-receiver product matching network, based on the layout design of the CMT221xLx-EM. among them:

1. Keep the RF signal path as short as possible to reduce the loss of signal energy transmission.
2. Place L1, L2, C0, and C1 as close as possible and as close to the RF input port as possible.
3. L1 and L2 are placed vertically to each other to reduce the mutual inductance between them.
4. The RF input impedance of the chip is much high, and the transmission line close

to the RF input end uses a narrower line width. The reference design used in the above figure uses a 0.2 mm line width; the transmission line between L2 and the antenna interface (P1) uses 1 Mm wide transmission line to match the 50 Ω impedance of the antenna.

5. Try not to screen lable on RF devices and traces. Thick screen lable will affect the dielectric constant factor and RF output impedance of the PCB.。

6. GND plane and RF routing should be as flat as possible to reduce impedance fluctuations on the transmission line。

7. 1/4-wavelength (λ/4) monopole antenna is a very common antenna. It is actually a dipole antenna. Half is made up of a 1/4 wavelength antenna and the other half is made up of the ground plane of the imaginary 1/4 wavelength antenna. Therefore, for the design of a monopole antenna, the performance is good or bad depending on the GND plane size. Considering different costs, performance, and time to market, users can choose different types of monopole antennas, such as PCB antennas, chip antennas, whip antennas, and wire antennas. In this reference design, P1 is an SMA connector used to connect the antenna. The connector is connected to a 50 ohm whip antenna to maximize the performance of the reference design.

3. Crystal circuit design

In order to reduce the number of pins, the CMT221xLx uses a single-ended crystal design. In addition, the required load capacitance of the crystal has been integrated inside the chip, and the PCB only needs to connect the crystal to the ground. The recommended crystal specifications are as follows:

Table 4. Crystal Oscillator Specifications

Parameters	Symbol	Condition	Min	Typical	Max	Unit
Frequency[1]	F_{XTAL}	@433.92 MHz		27.1412		MHz
		@315 MHz		19.7029[2]		MHz
Frequency accuracy[3]				±20		ppm
Load capacitance	C_{LOAD}			22		pF
equivalent resistance	Rm				60	Ω
start-up time[4]	t_{XTAL}			400		us

Remarks:

[1]. All series models support the direct drive of the XOSC pin with an external clock (a series coupling capacitor is required). The peak-to-peak amplitude requirement is between 0.3 and 0.7 V.

[2]. If the user chooses to configure the chip via RFPDK, the required crystal frequency is 26.2774 MHz when operating at 315 MHz.

[3]. This refers to all frequency accuracy tolerances, including (1) initial tolerance; (2) crystal loading; (3) aging; and (4) temperature variation. Acceptable crystal tolerances depend on factors such as radio frequency, channel spacing, and bandwidth settings.

[4]. This parameter has a great relationship with the crystal used.

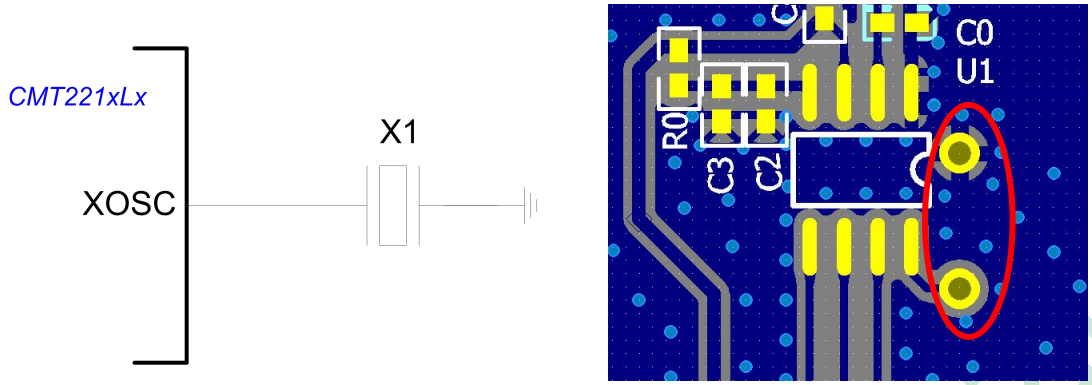

Figure 3. Schematic and layout of a crystal circuit

Design considerations:

1. Because the required load capacitance of the crystal has been integrated into the chip and fixed at 22 pF, the user needs to take into account that different PCB designs may result in variations in the on-board parasitic capacitance when selecting the crystal, ensuring that the resulting frequency deviation is allowed in the application Within range.
2. The crystal should be placed as close as possible to the receiving chip pin XOSC to reduce the trace length. The purpose of doing so is to reduce the possibility of external interference of the crystal, while reducing the distributed capacitance and improving the frequency accuracy.
3. The crystal circuit should be as far away as possible from radio frequency signals, digital signals, or other strong high-frequency interference signals, and should be grounded as much as possible in order to prevent interference to the RF signal or interfere with it to affect the quality of the reference clock.
4. The metal shell of the crystal needs to be grounded.

4. Digital signal design

Digital signal traces, including DATA and various TP (Test Point) signals, are handled as follows:

1. The digital signal trace should be far away from the RF and crystal trace areas.
2. Digital signals should be surround ground as much as possible to reduce crosstalk.。

5. Power and ground design

5.1 Power Filter Circuit Design

In order to reduce the impact of noise and ripple on the power supply, the user should add a suitable filter capacitor to the power supply pin.

The CMT221xLx can operate at supply voltages of 3.0 ~ 5.5 V or 2.0 ~ 3.6 V. When the user wants their design to be compatible with these two power supply schemes, it is considered to reserve the location of R0. When the operating voltage is 3.0 ~ 5.5 V, R0 is not soldered; when the operating voltage is 2.0 ~ 3.6 V, R0 soldering is 0 Ω, then C4 can be omitted or retained. The circuit is schematically as follows:

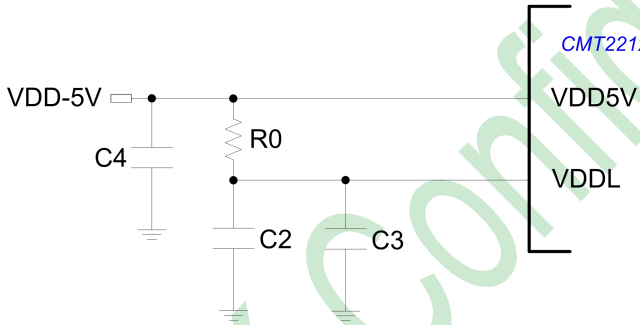

Figure 4. Power Filter Circuit Schematic

5.2 GND plane design

Matters needing attention:

1. Try to use a large number of continuous GND plane design.
2. The trace of the ground wire should minimize the area of the path loop of the current returning to the power supply to reduce the electromagnetic radiation of the power supply loop to the external space.
3. Spread the ground just below the chip as much as possible to reduce the influence on the impedance continuity of the RF transmission line.

4. Place no more than λ/10 size vias at PCB edge as many as possible to reduce high-order harmonic radiation on the PCB edge.

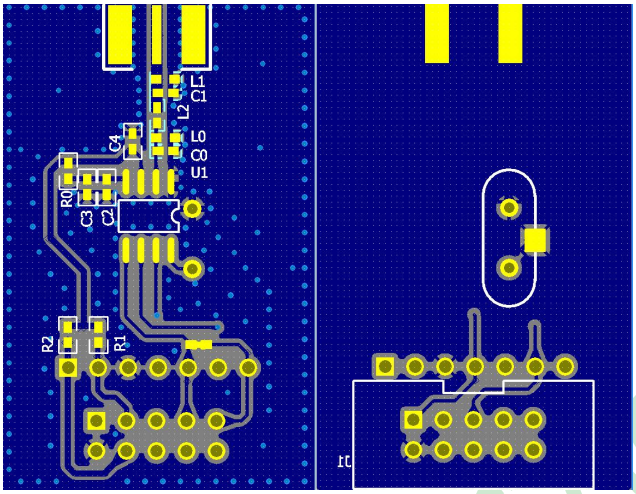

Figure 5. Pour GND plane

6. Sensitivity optimization considerations

The matching network recommended in Chapter 2 can serve as a starting point for user design. In some applications, due to product structure and physical space constraints, the placement, distortion, and size of the RF antenna are no longer ideal, so that the antenna impedance changes accordingly, resulting in the assumption that the reference design is no longer Satisfaction, the actual communication distance can not meet the requirements. At this time, the user needs to adjust the matching parameters according to these changes so as to achieve the best receiving effect. In theory, the length of the 1/4-wavelength antenna is compared with the operating frequency as shown in the following table:

Table 5. Relationship between wavelength and frequency

Operating frequency(MHz)	λ (cm)	λ/4 (cm)
433.92	69.2	17.3
315	95.2	23.8

7. Test circuit design

One of the features of the CMOSTEK series is that it can change the function of the chip by burning the chip. Therefore, we strongly recommend that customers reserve test points for the chip when designing the PCB in order to complete the following two functions:

1. It is convenient to burn the chip during production to change the function of the chip.
2. easy to read the configuration of the chip to understand the chip configuration.

The test points that need to be reserved are shown in the following table.

Table 6. Test points

Model number	Reserved test pin
CMT2210LH	TP1, TP2, DATA, VDD, GND

8. Design check item

The user can compare these details by the following check items in the actual design.

Table 7. Design check items

RF input design	
☐	Whether the RF signal path is as short as possible to reduce the loss of RF signals.
☐	Will the matching networks L2, C0 and L1, C1 have been placed as close as possible and as close as possible to the RF input port.
☐	Check whether the L1 and L2 of the matching network are vertically to each other to eliminate mutual inductance.
☐	Whether the trace width of the RF transmission line has taken into account the size of the impedance (about 50Ω impedance with 1mm wide transmission line).
☐	Whether or not silk screen printing on RF devices and traces has been minimized.
☐	Whether the Ground covering and RF routing alignment have been as smooth as possible.
☐	Whether the antenna length is close to λ/4.
☐	Whether the crystal is as far away from the antenna as possible.
Crystal circuit design	
☐	Whether the crystal has been placed as close as possible to the XOSC pin of the chip to reduce the parasitic capacitance of the trace.
☐	Whether the crystal circuit has been as far away as possible from strong interference sources such as digital signals, and place as many GND plane around it as possible.
☐	Whether the metal housing of the crystal is grounded.。
Digital signal design	
☐	Whether the digital signal has been far away from the RF and crystal traces.
☐	Whether digital signals have been surround with ground as much as possible to reduce crosstalk.
Power and ground design	

☐	Whether the power supply filter capacitor is as close to the chip's power pin on the layout.
☐	Whether there is a 0Ω jumper position reserved for design reuse when there is a requirement for 5V or 3V dual power supply.
☐	Whether the design of the GND plane has been done as large as possible.
☐	Whether the ground routing has minimized the loop area of the current return path so that radiation from the power loop is minimized.。
☐	Whether the bottom of the chip has been pour ground as much as possible to reduce the impact on the impedance continuity of the RF ransmission line and enhance the ESD performance.
☐	Whether the PCB edge has place no more than λ/10 size vias as many as possible to reduce the higher harmonic radiation of the PCB edge.。
Test circuit design	
☐	Whether the PCB design has reserved the test burning point.

Reference design

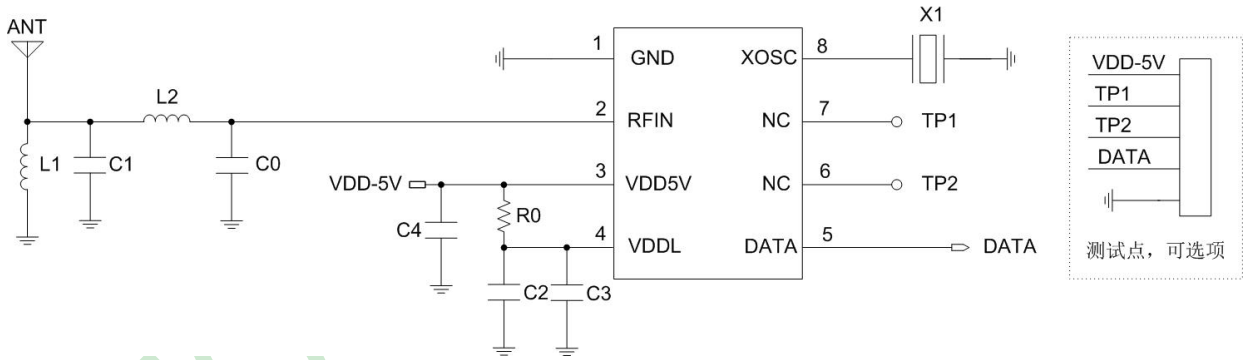

Figure 6. CMT2210LH EM Schematic Reference Design

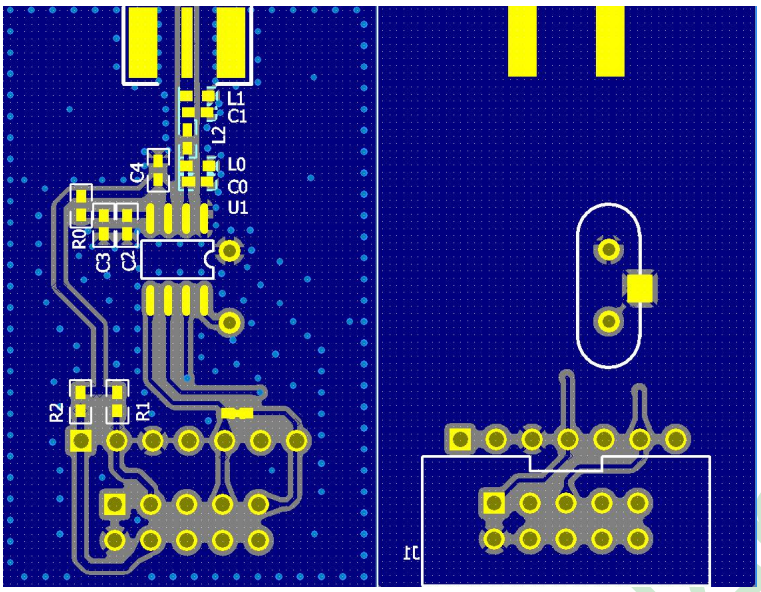

Figure 7. CMT2210LH EM Layout Reference Design

9. Document Change Record

Table 8. Document Change Record Table

Version Number	Section	Change Description	Date
0.8	All	Initial Release	2017-08-01

10. Contact information

Wuxi CMOSTEK Microelectronics Co., Ltd. Shenzhen Branch
Room 203, Hon Hai Building, Qianhai Road, Nanshan District, Shenzhen City, Guangdong Province, China
Zip code: 518000
Phone: +86-755 - 83235017
Fax: +86-755 - 82761326
Sales: sales@cmostek.com
Technical support: support@cmostek.com
Website: www.cmostek.com