Ultra-low Power Sub-1Ghz Wireless Transceiver SoC

MCU Feature

- **CPU core**
  - 32-bit ARM Cortex-M4 + FPU，single-cycle hardware multiplication and division instruction, support DSP instruction and MPU
  - Built-in 8KB instruction Cache, which support Flash acceleration unit to execute program 0 wait
  - Run up to 144 MHz，180 DMIPS
- **Encrypted memory**
  - Up to 128 Kbyte embeded Flash memory，support encrypted storage, multi-user partition management and data protection, hardware ECC check, 100,000 cycling and 10 years data retention.
  - 144 Kbyte in chip SRAM (including 16 Kbyte Retension RAM), Retention RAM support hardware parity check
- **Clock**
  - HSE: 4MHz~32MHz external high speed crystal
  - LSE: 32.768KHz external low speed crystal
  - HSI: internal high speed RC OSC 8 MHz
  - LSI: internal low speed RC OSC 40 KHz
  - Built in high speed PLL
  - Support 1 channel clock output, which can configure the system clock, HSE, HIS or PLL back divided frequency output
- **Reset**
  - Support power-on/power-down/external pin reset
  - Support programmable low voltage detection and reset
  - Support watchdog reset
- **High performance analog interface**
  - 4 x 12bit 5Msps high speed ADC，can be configured as 12/10/8/6bit mode，sampling rate up to 9 Msps in 6-bit mode, up to 11 external single-ended input channels, support differential mode
  - 4 x rail to rail operational amplifiers with built-in maximum 32x programmable gain amplifier
  - Up to 7 high-speed analog comparators with built-in 64-level adjustable comparison standard
  - Up to 24 channel capacitive touch keys, support low power consumption state wakeup
  - 2 x 12bit DAC, sampling rate 1Msps
  - Support external input independent reference voltage source
  - All analog ports support working at full voltage from1.8 to 3.6V
  - 1x 12bit DAC, sampling rate 1Msps
  - Internal 2.048V independent reference voltage reference source
  - Internal integrated low-voltage detection unit
- **Communication interface**
  - 7 x U(S)ART interfaces with data rate up to 4.5 Mbps, including 3 x USART interfaces（support 1 x ISO7816，1x IrDA, LIN）, and 4 x UART interfaces
  - 2 x SPI interfaces，with data rate up to 36 Mbps
  - 1 x QSPI interface，with data rate up to 144 Mbps
  - 2 x I2C interfaces，with data rate up to 1 MHz，master-slave mode is configurable, slave mode support dual-address response
  - 1 x USB 2.0 Full Speed Device interface
  - 1 x CAN 2.0A /B bus interface
  - 1 x Ethernet MAC interface，support 10M/100M Ethernet
- **2 x DMA controller, each controller support 8 channels, channel source adddress and destination address can be arbitrarily configurable**
- **1 x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **Time counter**
  - 2 x 16-bit advanced timer counters, support input capture, complementary output, quadrature encoder input, maximum control accuracy 6.9 ns; each timer has 4 independent channels, of which 3 channels support 6 complementary PWM outputs
  - 4 x 16-bit general purpose timer counters, each timer has 4 independent channels, support input capture/output comparison / PWM output / single pulse output
  - 2 x 16-bit basic timer counters
  - 1 x 24 bit SysTick
  - 1 x 7 bit Window Watchdog (WWDG)
  - 1 x 12 bit Independent Watchdog (IWDG)
- **Support up to 36 GPIOs，most of which support voltage of 5V**

- **Programming mode**
  - Support SWD/JTAG online debugging interface
  - Support UART，USB Bootloader
- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Support AES, DES, SHA, SM1, SM3, SM4, SM7, MD5 algorithms
  - Flash storage encryption
  - Multi-user partition management unit（MMU）
  - TRNG true random number generator
  - CRC16 / 32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support security start-up, program encryption download, security update
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**

RF Features

- Working frequency： 113 - 960 MHz
- Modulation style：OOK, 2 (G)FSK, 4 (G)FSK
- Data rate： 0.1 – 1000 kbps
- Sensitivity：2 FSK, -122 dBm DR=2.4 kbps, 433.92 MHz
  4 FSK, -88 dBm DR=1 Mbps,433.92 MHz
  OOK, -94 dBm DR= 300 kbps, 433.92 MHz
- RX current： 9.6 mA (DCDC)@ 433.92 MHz, FSK
  （only for RF working current）
- TX current：30 mA @ 13 dBm, 433.92 MHz, FSK
  82 mA@ 20 dBm, 433.92 MHz, FSK
  （only for RF working current）
- Supporting both direct and packet modes, with configurable packet handler and 256-Byte FIFO

System Features

- Working voltage：1.8 – 3.6 V
- Working temperature：- 40 – 85 ℃
- Package: QFN 68 7x7

Overview

CMT2392F512, integrated a 32-bit ARM Cortex-M4 core, is an ultra-low power, high-performance, OOK / (G)FSK / 4 (G)FSK based RF transceiver, applicable to various applications within the 113 - 960 MHz frequency band. The product is part of the CMOSTEK NextGenRF™ product family which covers a complete product line consisting of transmitters, receivers and transceivers. The high-density integration of CMT2392F512 simplifies the required BOM in system design. With Tx power reaching +20 dBm and sensitivity reaching -122 dBm, it can achieve optimized performance of application RF links. Through providing multiple data packet formats and code methods, this product ensures the flexible supporting of various applications. Besides, CMT2392F512 provides functions such as 128-byte Tx/Rx FIFO, multiple GPIO and interrupt configurations, Duty-Cycle mode, LBT (listen before talk), high-precision RSSI, LBD, power on reset, low-frequency clock output, quick frequency hopping, squelch, etc., which allows more flexible application design and gains more product differentiation capability.

Application

- Auto metering
- Home security and building automation
- Wireless sensor nodes and industrial monitoring
- ISM band data communication
- Tag reader and writer

Table 1-1. CMT2392F512 Resources List

Memory		Analog peripheral						Digital peripheral											Package
ROM	RAM	ADC	DAC	OPA	CMP	POR BOR	LVD LVR	RTC	WDT	Timer	UART	SPI	I2C	I2S	GPIO	ETH	USB	CAN	DMA	
512KB Flash	144KB	12bits 5Msps	12bits 1Msps	√	√	√	√	x1	x2	x8	x7	x2	x2	x	36	x1	x1	x1	x8ch	QFN68

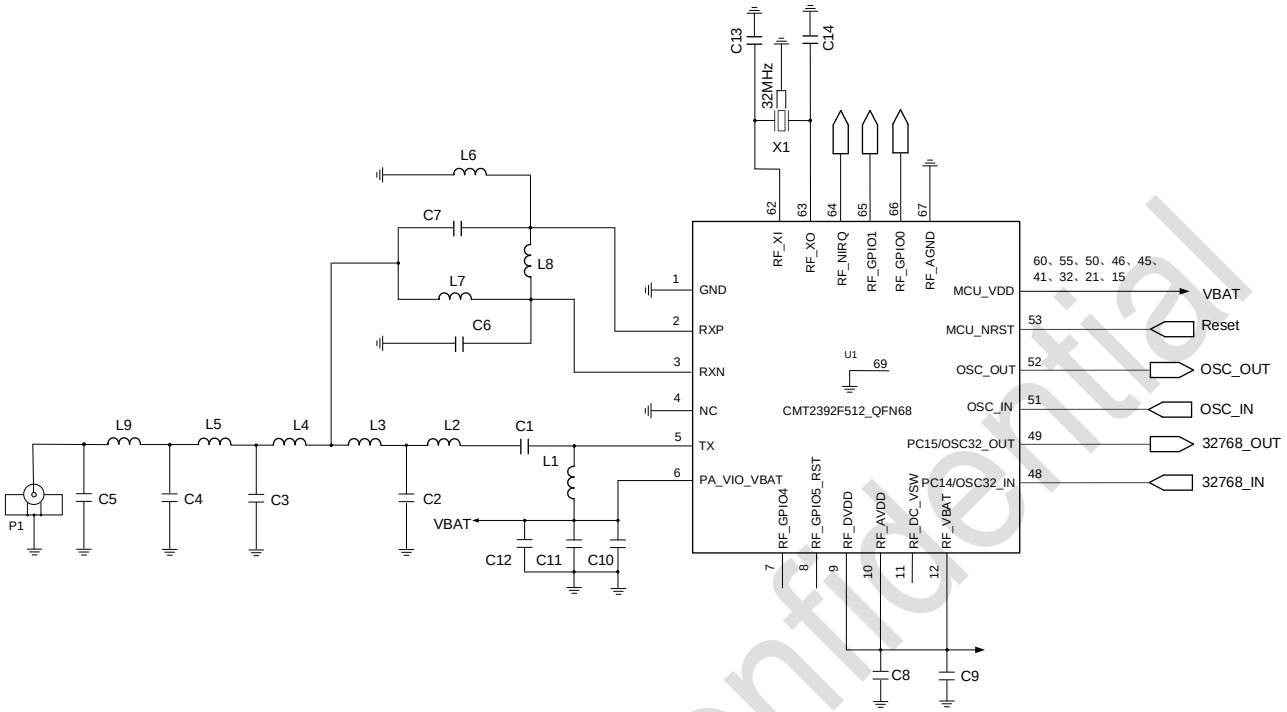


Figure 1-1. CMT2392F512（QFN 68 7x7）Typical Application Diagram（ DC-DC Disabled）

Table 1-2. BOM of 20 dBm Direct Tie（Disable DC-DC）

Signal	Description	Componet Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0402 NP0, 50 V	22	12	12	12	pF	
C2	±5%, 0402 NP0, 50 V	6.8	5.6	3.3	3.3	pF	
C3	±5%, 0402 NP0, 50 V	8.2	6.2	3.3	3.0	pF	
C4	±5%, 0402 NP0, 50 V	8.2	NC	NC	NC	pF	
C5	±5%, 0402 NP0, 50 V	NC	NC	NC	NC	pF	
C6	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C7	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C8	±5%, 0603 NP0, 50 V	2.2				uF	
C9	±5%, 0402 NP0, 50 V	1				uF	
C10	±5%, 0402 NP0, 50 V	220				pF	
C11	±5%, 0402 NP0, 50 V	100				nF	
C12	±5%, 0603 NP0, 50 V	4.7				uF	

Signal	Description	Componet Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C13	±5%, 0402 NP0, 50 V	NC				pF	
C14	±5%, 0402 NP0, 50 V	NC				pF	
L1	±5%, 0603 Ceramic Chip Inductor	220	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Ceramic Chip Inductor	68	47	15	12	nH	Sunlord SDCL
L3	±5%, 0603 Ceramic Chip Inductor	56	39	15	12	nH	Sunlord SDCL
L4	±5%, 0603 Ceramic Chip Inductor	33	33	8.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 Ceramic Chip Inductor	47	33	8.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L7	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L8	±5%, 0603 Ceramic Chip Inductor	220	68	33	33	nH	Sunlord SDCL
L9	±5%, 0603 Ceramic Chip Inductor	33	NC	NC	NC	nH	Sunlord SDCL
X1	±10 ppm, SMD	32				MHz	EPSON
U1	CMT2392F512 SoC					-	CMOSTEK

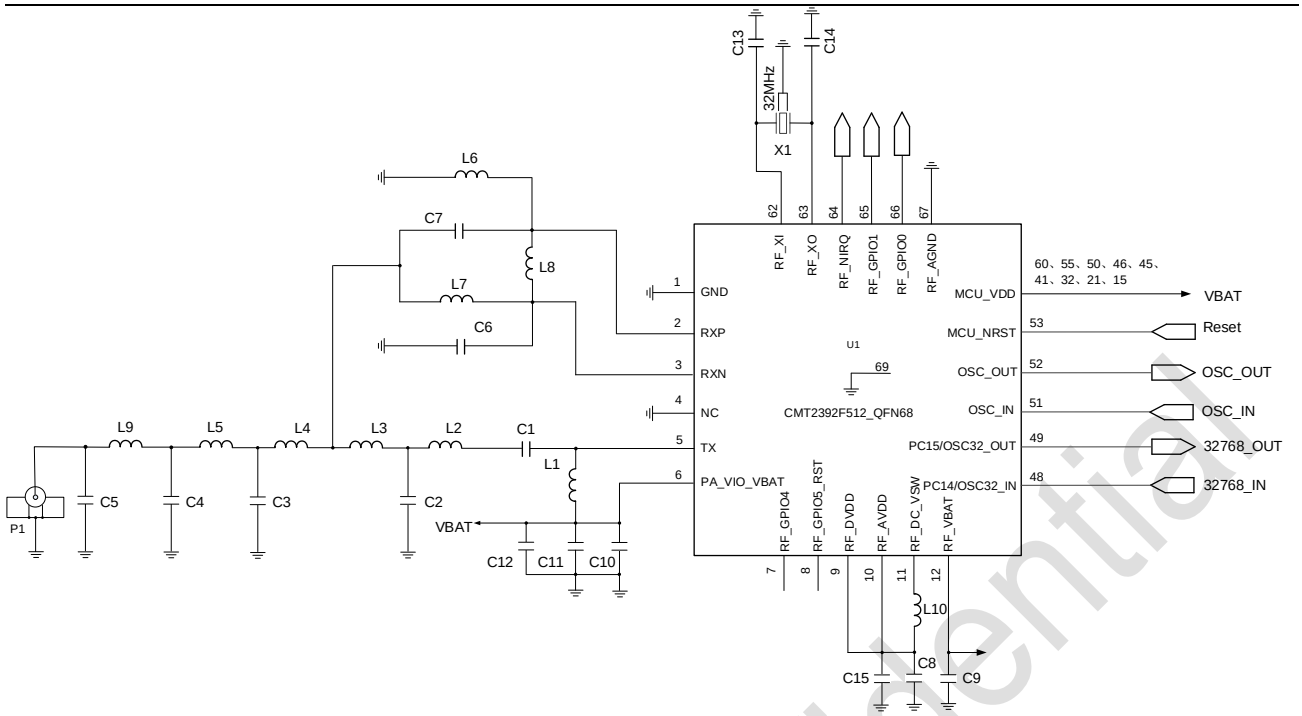


Figure 1-2. CMT2392F512（QFN 68 7x7）Typical Application Diagram（ DC-DC Enabled）

Table 1-3. BOM of 20 dBm Direct Tie（DC-DC Enabled）

Signal	Description	Component Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0402 NP0, 50 V	22	12	12	12	pF	
C2	±5%, 0402 NP0, 50 V	6.8	5.6	3.3	3.3	pF	
C3	±5%, 0402 NP0, 50 V	8.2	6.2	3.3	3.0	pF	
C4	±5%, 0402 NP0, 50 V	8.2	NC	NC	NC	pF	
C5	±5%, 0402 NP0, 50 V	NC	NC	NC	NC	pF	
C6	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C7	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C8	±5%, 0603 NP0, 50 V	2.2				uF	
C9	±5%, 0402 NP0, 50 V	1				uF	
C10	±5%, 0402 NP0, 50 V	220				pF	
C11	±5%, 0402 NP0, 50 V	100				nF	
C12	±5%, 0603 NP0, 50 V	4.7				uF	

Signal	Description	Component Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C13	±5%, 0402 NP0, 50 V	NC				pF	
C14	±5%, 0402 NP0, 50 V	NC				pF	
C15	±5%, 0402 NP0, 50 V	100				nF	
L1	±5%, 0603 Ceramic Chip Inductor	220	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Ceramic Chip Inductor	68	47	15	12	nH	Sunlord SDCL
L3	±5%, 0603 Ceramic Chip Inductor	56	39	15	12	nH	Sunlord SDCL
L4	±5%, 0603 Ceramic Chip Inductor	33	33	8.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 Ceramic Chip Inductor	47	33	8.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L7	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L8	±5%, 0603 Ceramic Chip Inductor	220	68	33	33	nH	Sunlord SDCL
L9	±5%, 0603 Ceramic Chip Inductor	33	NC	NC	NC	nH	Sunlord SDCL
L10	MPH252012C100MT, 10UH ± 20%, package 2520, direct current resistance 0.5Ω, Saturation current 0.5A	10				uH	
X1	±10 ppm, SMD	32				MHz	EPSON
U1	CMT2392F512 SoC					-	CMOSTEK

Table of Contents

1. Electrical Characteristic

V_{DD}= 3.3 V，T_{OP}= 25 °C，F_{RF} = 433.92 MHz, sensitivity is measured by receiving a PN9 coded data and matching impedance to 50Ω under 0.1% BER standard.Unless otherwise stated, all results are tested on the CMT2392F512-EM evaluation board.

1.1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		- 40		85	℃
Supply voltage slope			1			mV/us

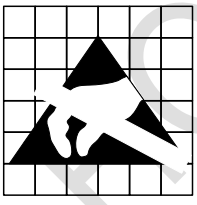
1.2 Absolute Maximum Rating

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	V_{DD}		- 0.3	3.6	V
Interface voltage	V_{IN}		- 0.3	3.6	V
Junction temperature	T_J		- 40	125	℃
Storage temperature	T_{STG}		- 50	150	℃
Soldering temperature	T_{SDR}	Last for at least 30 second		255	℃
ESD rating[2]		Human body model (HBM)	- 2	2	kV
Latch-up current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding the Absolute Maximum Ratings may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2392F512 is a high-performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Parameter	Symbol	Condition		Typ. (Disable DCDC)	Typ. (Enable DCDC)	Unit
Sleep current [1]	I_{SLEEP}	In sleep mode with sleep timer disabled		400		nA
		In sleep mode with sleep timer enabled		800		nA
Ready current [1]	I_{Ready}			2.1	1.9	mA
RFS current [1]	I_{RFS}		315 MHz	7.5	5.2	mA
			433 MHz	7.8	5.6	mA
			868 MHz	8.4	5.9	mA
			915 MHz	8.5	5.9	mA
TFS current [1]	I_{TFS}		315 MHz	7.5	5.2	mA
			433 MHz	7.8	5.6	mA
			868 MHz	8.4	5.9	mA
			915 MHz	8.5	5.9	mA
RX current [1]	I_{Rx}	DR = 10 kbps Dev =10 kHz	315 MHz	13.5	8.8	mA
			433 MHz	13.6	9.4	mA
			868 MHz	14.3	9.9	mA
			915 MHz	14.3	9.9	mA
TX current [1]	I_{Tx}	20 dBm[2]	315 MHz	74	/	mA
			433 MHz	82	81	mA
			868 MHz	88	87	mA
			915 MHz	88	87	mA
		13 dBm [3]	315 MHz	26.7	/	mA
			433 MHz	30	29	mA
			868 MHz	33	32	mA
			915 MHz	34	33	mA
		10 dBm [3]	315 MHz	21	15	mA
			433 MHz	25	24	mA
			868 MHz	27	26	mA
			915 MHz	27	26	mA
		-10 dBm [3]	315 MHz	10.3	7	mA
			433 MHz	11	10	mA
			868 MHz	12	11	mA
			915 MHz	12	11	mA

Notes:

[1]. 2 FSK, DR = 10 kbps, FDEV = 10 kHz, Vbat = 3.3 V.

[2]. Apply 20 dBm matching network.

[3]. Apply 13 dBm matching network.

[4]. Only apply for RF working current, not include working current of MCU.

1.4 RF Receiver Specification

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Data rate	DR	OOK		0.1		300	kbps
		2 (G)FSK		0.1		500	kbps
		4 (GFSK		0.1		1000	kbps
Deviation (RX)	F_{DEV}	(G)FSK, 4 (G)FSK[1]		0.5		350	kHz
Sensitivity @ 433 MHz (direct tie matching network)	S_{433}	FSK[2]	DR = 2.4 kbps, F_{DEV} = 1.2 kHz, BW= 4.8 kHz		-122		dBm
			DR = 10 kbps, F_{DEV} = 5 kHz		-114		dBm
			DR = 20 kbps, F_{DEV} = 10 kHz		-112		dBm
			DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
			DR = 100 kbps, F_{DEV} = 50 kHz		-106		dBm
			DR = 200 kbps, F_{DEV} = 100 kHz		-104		dBm
			DR = 500 kbps, F_{DEV} = 250 kHz		-98		dBm
		OOK[2]	5 kbps		-110		dBm
			50 kbps		-101		dBm
			100 kbps		-97		dBm
			200 kbps		-95		dBm
			300 kbps		-94		dBm
		4FSK[2]	DR = 10 kbps, F_{DEV}[3] = 10 kHz		-109		dBm
			DR = 100 kbps, F_{DEV}[3] =100 kHz		-99		dBm
			DR = 1 Mbps, F_{DEV}[3] = 250 kHz		-88		dBm
Sensitivity @ 868 MHz (direct tie matching network)	S_{868}	FSK[2]	DR = 2.4 kbps, F_{DEV} = 1.2 kHz, BW = 4.8 kHz		-120		dBm
			DR = 10 kbps,F_{DEV} = 5 kHz		-111		dBm
			DR = 20 kbps, F_{DEV} = 10 kHz		-110		dBm
			DR = 50 kbps, F_{DEV} = 25 kHz		-107		dBm
			DR = 100 kbps, F_{DEV} = 50 kHz		-104		dBm
			DR = 200 kbps, F_{DEV} = 100 kHz		-102		dBm
			DR = 500 kbps, F_{DEV} = 250 kHz		-96		dBm
		OOK[2]	5 kbps		-106		dBm
			50 kbps		-98		dBm
			100 kbps		-94		dBm
			200 kbps		-93		dBm
			300 kbps		-92		dBm
		4FSK[2]	DR = 10 kbps, F_{DEV}[3] = 10 kHz		-106		dBm
			DR = 100 kbps, F_{DEV}[3] = 100 kHz		-96		dBm
			DR = 1 Mbps, F_{DEV}[3] = 250 kHz		-85		dBm

Notes:

[1]. BT = 0.5 by default for Gaussian modulation.

[2]. In case of unspecified BW value, a crystal of 10 ppm is used and the BW value is automatically calculated by RFPDK.

[3]. For 4 FSK, FDEV represents the frequency difference between the frequency points at the far ends (left and right) and the centered frequency point.

Receiver channel bandwidth	BW	Receiver channel bandwidth	1.3		1168	kHz
Saturation input signal level	P_{LVL}				20	dBm

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
RSSI range	RSSI	By one step of 1 dB		-127		20	dBm
Co-channel rejection @ 433 MHz，868 MHz	CCR	DR = 2.4 kbps; FDEV = 1.2 kHz; BW = 4.8 kHz CW interference, BER<0.1%			-7		dB
Adjacent channel rejection @ 433 MHz	ACR-I_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz, Channel Space = 12.5 kHz， CW interference, BER<0.1%			62		dB
Adjacent channel rejection @ 868 MHz	ACR-I_{868}	DR = 2.4 kbps；F_{DEV} = 1.2 kHz; BW = 4.8 kHz, Channel Space = 12.5 kHz， CW interference, BER < 0.1%			56		dB
Blocking @ 433 MHz	BI_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz, CW interference, BER < 0.1%	±1 MHz offset		76		dB
			±2 MHz offset		80		dB
			±10 MHz offset		84		dB
Blocking @ 868 MHz	BI_{868}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz, CW interference, BER < 0.1%	±1 MHz offset		66		dB
			±2 MHz offset		76		dB
			±10 MHz offset		83		dB
Image Rejection @ 433 MHz	IMR_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz CW interference, BER < 0.1%	Before calibration		30		dB
			After calibration		56		dB
Image Rejection @ 868 MHz	IMR_{868}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz CW interference, BER < 0.1%	Before calibration		26		dB
			After calibration		51		dB
Input 3rd order intercept point @ 433 MHz	$IIP3_{433}$	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; two-tone test with 10 MHz and 20 MHz deviations.			-13		dBm
Input 3rd order intercept point @ 868 MHz	$IIP3_{868}$	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; two-tone test with 10 MHz and 20 MHz deviations.			-12		dBm
Receiver input impedance	Zin	RXP and RXN Differential input impedance	433 MHz	150 Ω// 0.8 pF			
			868 MHz	134 Ω// 1.0 pF			

1.5 RF Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Specific peripheral components are required according to different frequency bands.	-10		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-
Output power change in	$P_{OUT-TOP}$	Temperature range: -40 to +85 °C		1		dB

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
different temperature						
Spurious emissions		P_{OUT} = +13 dBm, 433 MHz, F_{RF} < 1 GHz			-54	dBm
		1 GHz to 12.75 GHz, including Harmonic			-36	dBm
Harmonic output[1] for FRF= 315 MHz	$H2_{315}$	2nd harmonic, +20 dBm P_{OUT}		-57		dBm
	$H3_{315}$	3rd harmonic, +20 dBm P_{OUT}		-75		dBm
Harmonic output[1] for FRF= 433 MHz	$H2_{433}$	2nd harmonic, +20 dBm P_{OUT}		-56		dBm
	$H3_{433}$	3rd harmonic, +20 dBm P_{OUT}		-71		dBm
Harmonic output[1] for FRF= 868 MHz	$H2_{868}$	2nd harmonic, +20 dBm P_{OUT}		-47		dBm
	$H3_{868}$	3rd harmonic, +20 dBm P_{OUT}		-72		dBm
Harmonic output[1] for FRF= 915 MHz	$H2_{915}$	2nd harmonic, +20 dBm P_{OUT}		-47		dBm
	$H3_{915}$	3rd harmonic, +20 dBm P_{OUT}		-73		dBm
Harmonic output[1] for FRF= 315 MHz	$H2_{315}$	2nd harmonic, +13 dBm P_{OUT}		-51		dBm
	$H3_{315}$	3rd harmonic, +13 dBm P_{OUT}		-72		dBm
Harmonic output[1] for FRF= 433 MHz	$H2_{433}$	2nd harmonic, +13 dBm P_{OUT}		-44		dBm
	$H3_{433}$	3rd harmonic, +13 dBm P_{OUT}		-58		dBm
Harmonic output[1] for FRF= 868 MHz	$H2_{868}$	2nd harmonic, +13 dBm P_{OUT}		-50		dBm
	$H3_{868}$	3rd harmonic, +13 dBm P_{OUT}		-71		dBm
Harmonic output[1] for FRF= 915 MHz	$H2_{915}$	2nd harmonic, +13 dBm P_{OUT}		-54		dBm
	$H3_{915}$	3rd harmonic, +13 dBm P_{OUT}		-73		dBm

Notes:

[1]. The harmonic level mainly depends on the quality of matching network. The parameters above are measured on CMT2392F512-EM.

1.6 Settling Time of RF Status Switching

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settling time	T_{SLP-RX}	From Sleep to RX		660		us
	T_{SLP-TX}	From Sleep to TX		660		us
	T_{STB-RX}	From Standby to RX		160		us
	T_{STB-TX}	From Standby to TX		160		us
	T_{RFS-RX}	From RFS to RX		16		us
	T_{TFS-RX}	From TFS to TX		16		us
	T_{TX-RX}	From TX to RX (Ramp down requires $2T_{symbol}$ time)		$2T_{symbol}$ +168		us
	T_{RX-TX}	From RX to TX		220		us

Notes:

[1]. T_{SLP-RX} and T_{SLP-TX} mainly depend on crystal oscillating, which is largely related to crystal itself.

1.7 RF Frequency Synthesizer

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Require different matching networks.	675		960	MHz
			338		640	MHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
			113		320	MHz
Frequency deviation range	F_{DEV_RNG} [1]	675 ~ 960 MHz		600		kHz
		450 ~ 640 MHz		400		kHz
		338 ~ 450 MHz		300		kHz
		225 ~ 320 MHz		200		kHz
		169 ~ 225 MHz		150		kHz
		135 ~ 169 MHz		120		kHz
		113 ~ 135 MHz		100		kHz
Frequency resolution	F_{RES}			60		Hz
Frequency tuning time	t_{TUNE}			60		us
Phase noise @ 433 MHz	PN_{433}	10 kHz Frequency Offset		-101		dBc/Hz
		100 kHz Frequency Offset		-114		dBc/Hz
		1 MHz Frequency Offset		-129		dBc/Hz
		10 MHz Frequency Offset		-134		dBc/Hz
Phase noise @ 868 MHz	PN_{868}	10 kHz Frequency Offset		-100		dBc/Hz
		100 kHz Frequency Offset		-109		dBc/Hz
		1 MHz Frequency Offset		-126		dBc/Hz
		10 MHz Frequency Offset		-129		dBc/Hz

Notes:

[1]. For 2 FSK and 4 FSK, F_{DEV} represents the frequency difference between the frequency points at the far ends (left and right) and the centered frequency point.

1.8 Crystal Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency [1]	F_{XTAL}			32		MHz
Crystal frequency precision [2]	$ppm_{\_XTAL}$		0	20	100	ppm
Load resistance	C_{LOAD_XTAL}			12		pF
Crystal equivalent resistance	Rm_{XTAL}			60		Ω
Crystal startup time [3]	t_{XTAL}			200		us

Notes:

[1]. The CMT2392F512 can utilize external reference clock to directly drive XIN pin through the coupling capacitor. The peak-to-peak value of external clock signal is required between 0.3 and 0.7 V.

[2]. It involves: (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[3]. This parameter is largely related to crystal.

1.9 Controller Operating Conditions

1.9.1 General Operating Conditions

Table 1-9-1. General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	16	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}	Analog operating of working voltage	Must be the same potential as VDD(1)	1.8	3.6	V
T_A	Ambient temperature (temperature number 7)		-40	105	℃
T_J	Junction temperature range	7 suffix version	-40	125	℃

1. It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

1.9.2 Operating Conditions at Power-on and Power-off

Table 1-9-2. Operating Conditions at Power-on and Power-off

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Supply voltage goes from 0 to V_{DD}	20	∞	μs/V
	V_{DD} fall time rate	Supply voltage drops from V_{DD} to 0	80	∞	

1.10 Embedded Reset and Power Control Module Characteristics

Table 1-10. Features of Embedded Reset and Power Control Modules

Signal	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (MSB of PWR_CTRL is 0)	PRS[2:0]=000 (rising edge)	2.09	2.18	2.27	V
		PRS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PRS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PRS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PRS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PRS[2:0]=010 (falling edge)	2.19	2.28	2.37	V
		PRS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PRS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PRS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PRS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PRS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PRS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PRS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PRS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PRS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PRS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
	Programmable voltage detector level selection (MSB of PWR_CTRL is 1)	PRS[2:0]=000 (rising edge)	1.7	1.78	1.85	V
		PRS[2:0]=000 (falling edge)	1.61	1.68	1.75	V
		PRS[2:0]=001 (rising edge)	1.8	1.88	1.96	V
		PRS[2:0]=001 (falling edge)	1.7	1.78	1.85	V
		PRS[2:0]=010 (rising edge)	1.9	1.98	2.06	V
		PRS[2:0]=010 (falling edge)	1.8	1.88	1.96	V
		PRS[2:0]=011 (rising edge)	2	2.08	2.16	V
		PRS[2:0]=011 (falling edge)	1.9	1.98	2.06	V
		PRS[2:0]=100 (rising edge)	3.15	3.28	3.41	V
		PRS[2:0]=100 (falling edge)	3.05	3.18	3.31	V
		PRS[2:0]=101 (rising edge)	3.24	3.38	3.52	V
		PRS[2:0]=101 (falling edge)	3.15	3.28	3.41	V
		PRS[2:0]=110 (rising edge)	3.34	3.48	3.62	V
		PRS[2:0]=110 (falling edge)	3.24	3.38	3.52	V
		PRS[2:0]=111 (rising edge)	3.44	3.58	3.72	V
		PRS[2:0]=111 (falling edge)	3.34	3.48	3.62	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
V_{POR}	VDD Power on/off Reset threshold	-	-	1.64/1.62	-	V
$T_{RSTTEMPO}$(2)	Reset duration	-	-	0.8	4	ms

1. The characteristics of the product are guaranteed by design to the minimum value $V_{POR/PDR}$。
2. Guaranteed by design, not tested in production.

1.11 Internal Reference Voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{REFBUFFER}$	Internal reference voltage	-40℃< TA< +105℃	1.16	1.20	1.26	V
		-40℃< TA< +85℃	1.16	1.20	1.24	V
TS_vrefint(1)	The sampling time of the ADC when reading the internal reference voltage	PLS[2:0]=001 (rising edge)	-	5.1	17.1(2)	μs

1. The shortest sampling time is obtained through multiple loops in the application.
2. Guaranteed by design, not tested in production.

1.12 Power Supply Current Characteristic

Current consumption is a combination of parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, turnover rate of I/O pins, program location in memory, and code executed.

1.12.1 Maximum current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting period is from 0 to 32MHz, 1 waiting period is from 32 to 64MHz, 2 waiting period is from 64 to 96MHz, 3 waiting period is from 96 to 128 MHz, 4 waiting period is from 128 to 144 MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enabled: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$.

Table 1-12-1. Maximum Current Consumption in Operating Mode when Data Processing in Internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}(2)	Supply current in operation mode	external clock, enable all peripherals	144MHz	32	mA
			72MHz	18	
			36MHz	11	
		external clock, disable all peripherals	144MHz	15.8	
			72MHz	9.7	
			36MHz	6.7	
1. Based on comprehensive evaluation, not tested in production. 2. Internal clock is 8MHz, enable PLL when f_{HCLK} > 8MHz.					

Table 1-12-2. Maximum Current Consumption in Sleep Mode, Data Run in Flash or RAM

Symbol	Parameter	Condition	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}(2)	Supply current in sleep mode	external clock, enable all peripherals	144MHz	27	mA
			72MHz	15.5	
			36MHz	10	
		external clock, disable all peripherals	144MHz	9.2	
			72MHz	6.6	
			36MHz	5.1	
1. Based on comprehensive evaluation, not tested in production. 2. Internal clock is 8MHz, enable PLL when fHCLK > 8MHz.					

1.12.2 Typical Current Consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- VDD or VSS (no load).
- All peripherals are disable unless otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting period is from 0 to 32MHz, 1 waiting period is from 32 to 64MHz, 2 waiting period is from 64 to 96MHz, 3 waiting period is from 96 to 128 MHz, 4 waiting period is from 128 to 144 MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$.

Table 1-12-3. Typical Current Consumption in Operating Mode,

When Data Processing in Internal Flash

Parameter	Symbol	Condition	f_{HCLK}	Typ (1)		Unit
				Enable all peripherals	Disable all peripherals	
Supply current in operation mode	I_{DD}	external clock,	144MHz	30.3	14.2	mA
			72MHz	17	8.1	
			36MHz	9.3	5.3	
		Operates in high speed internal RC oscillator (HSI), using AHB pre-division to reduce frequency	128MHz	30	12.7	
			72MHz	22.5	7.2	
			36MHz	8.8	3.9	

1.Typical values are measured at TA = 25 ℃ and V_{DD} = 3.3 V.
2.ADC of the anolog will add additional 0.8 mA current consumption. This part of current is increased only when ADC is enabled (set ADC_CTRL2.ON bit).
3.External clock is 8 MHz, enable PLL when f_{HCLK} > 8MHz.

Table 1-12-4. Typical Current Consumption in Sleep Mode,

Data Processing in Internal Flash or RAM

Parameter	Symbol	Condition	f_{HCLK}	Typ (1)		Unit
				Enable all peripherals	Disable all peripherals	
Supply current in sleep mode	I_{DD}	external clock,	144MHz	25.3	8	mA
			72MHz	13.9	5.3	
			36MHz	8	3.6	
		Operates in high speed internal RC oscillator (HSI), using AHB pre-division to reduce frequency	128MHz	24.2	6.1	
			72MHz	13.9	3.5	
			36MHz	7.2	2.2	

1.Typical values are measured at TA = 25 ℃ and V_{DD} = 3.3 V.
2.ADC of the anolog will add additional 0.2 mA current consumption. This part of current is increased only when ADC is enabled (set ADC_CTRL2.ON bit).
3.External clock is 8 MHz, enable PLL when f_{HCLK} > 8MHz.

1.12.3 Low power mode current consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level of -VDD or VSS (no load).
- All peripherals are off disabled otherwise noted.

Table 1-12-5. Typical and Maximum Current Consumption in Shutdown and Standby Mode

Symbol	Parameter	Condition	Typs (1)		Unit
			V_{DD}= 3.3V T_A =25℃	V_{DD}= 3.3V T_A =105℃	
I_{DD_STOP2}	Supply current in Stop mode 2 (STOP2)	The external low-speed clock is on, the RTC is running, SRAM2 is on, all I/O states are on, and the independent watchdog is off	3(1)	27(1)	
	Supply current in STANDBY	Low speed internal RC oscillator and independent watchdog are on	1.6(1)	7.6(1)	

$I_{DD\_STANDBY}$	mode	The low speed internal RC oscillator is on and the independent watchdog is off	1.5(1)	7.5(1)	μA
		The low speed internal RC oscillator and independent watchdog are closed, and the low speed oscillator and RTC are closed	1.4(1)	7.3(1)	
1. Guaranteed by characterization, not tested in production.					

1.13 External Clock Source Characteristics

1.13.1 High-speed external clock source (HSE)

Table 1-13-1. High-speed External User Clock Features

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency(1)	-	4	8	32	MHz
V_{HSEH}	OSC_IN Input pin high level voltage		0.8 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN Input pin low level voltage		Vss	-	0.3 V_{DD}	
$t_{w(HSE)}$	Time when OSC_IN is high or low(1)		16	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitive resistance (1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA
1. Guaranteed by design, not tested in production.						

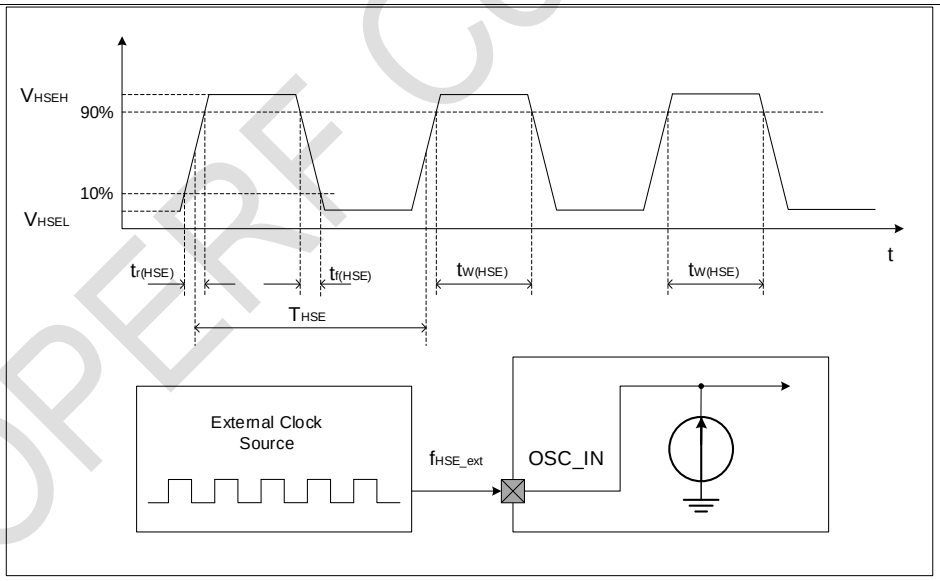


Figure 1-13-1. AC Timing Diagram of an External High-speed Clock Source

1.13.2 Low-speed External Clock Source (LSE)

Table 1-13-2. Features of Low-speed External User Clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit

f_{LSE_ext}	User external clock frequency(1)	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN Input pin high level voltage		0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN Input pin low level voltage			-	0.3	
$tw_{(LSE)}$	OSC32_IN High or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN Rise or fall time(1)		-	-	50	
$DuCy_{(LSE)}$	Duty ratio		30	-	70	%
I_L	OSC32_IN Input leakage current (1)	$V_{SS}≤V_{IN}≤V_{DD}$	-	-	±1	μA
1. Guaranteed by design, not tested in production.						

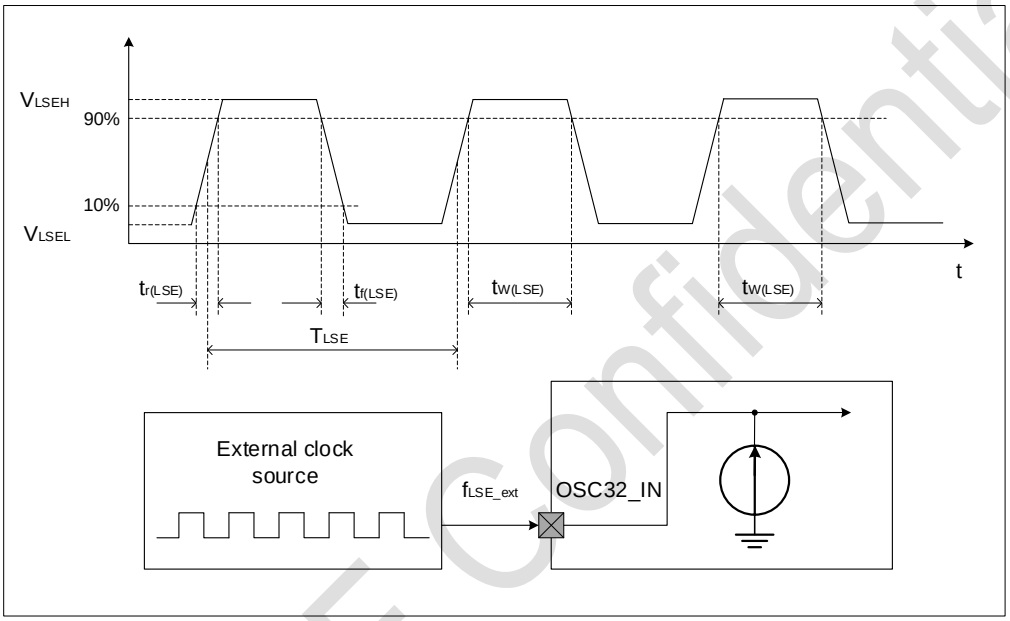


Figure 1-13-2. AC Timing Diagram of an External Low Speed Clock Source

1.13.3 High-speed external clock generated by using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Table 1-13-3. HSE 4～32 MHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	32	MHz
R_F	Feedback resistance		-	160	-	kΩ
C_{L1} C_{L2}(3)	The recommended load capacitance and the corresponding crystal serial impedance（R_S）	R_S = 30 Ω	-	20	-	pF
i_2	HSE drive current	V_{DD}=3.3 V, V_{IN}=V_{SS} 30 pF load	-	1.3	1.6	mA
g_m	Transconductance of the oscillator	startup	-	10	-	mA/V
$t_{SU(HSE)}$(4)	Startup time (8M crystal)	V_{DD} is stabled	-	3	5	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by characterization results, not tested in production.

3. For CL1 and CL2, it is recommended to use high quality ceramic capacitor between 5 pF and 25 pF designed for high frequency applications (typical value), and select a crystal or resonator that meets the requirements. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually give load capacitance parameters in a serial combination of CL1 and CL2. The capacitive reactance of PCB and MCU pins should be taken into account when selecting CL1 and CL2. (The capacitance between the pin and the PCB can be roughly estimated by 10pF)

4. The relatively low R_F resistance provides protection against the problems that arise when used in wet environments, where leakage and bias conditions change. However, if the MCU is used in harsh wet conditions, the design needs to take this parameter into account.

5. .t_{SU}(HSE) is the startup time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

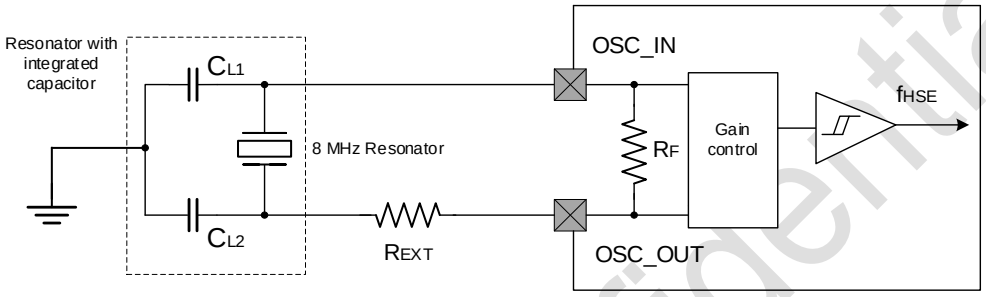


Figure 1-13-3. Typical Application by Using 8 MHz Crystal

Note：The R_{EXT} value depends on the properties of the crystal. Typical values are 5 to 6 times R_S.

1.13.4 Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric containers, and to select crystals or resonators that meet the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}.

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance, its typical value is between 2 pF and 7pF.

Warning: In order to avoid exceeding the maximum value of CL1 and CL2 (15pF), it is recommended to use resonator with load capacitor CL ⩽ 7pF, and cannot use a resonator with load capacitor of 12.5pF.

For example: If a resonator with load capacitance CL = 6pF is selected and Cstray = 2pF, then CL1 = CL2 = 8pF.

Table 1-13-4. LSE Oscillator Characteristics (f_{LSE}=32.768kHz)(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F	Feedback resistance		-	5	-	MΩ
C_{L1} C_{L2}(3)	The recommended load capacitance and the corresponding crystal serial impedance（R_S）	R_S :30 KΩ ~ 65 KΩ	-	-	15	pF
i_2	LSE drive current	VDD = 3.3 V CL1 = CL2 = 14 pF R_S = 30 KΩ	-	0.3	-	μA
g_m	Transconductance of the oscillator	-	5	-	-	μA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabled	-	2	-	s

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

2. Please refer to notes and warnings in the above table.

3. The high quality osillator (e.g. MSIV-TIN32.768 kHz) with relatively low Rs value provides optimized currrent consumption. For more informations please refer to crystal manufacture.

4. .t_{SU}(HSE) is the startup time, from the time when LSE is enabled by the software to the time when a stable 32.768 KHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

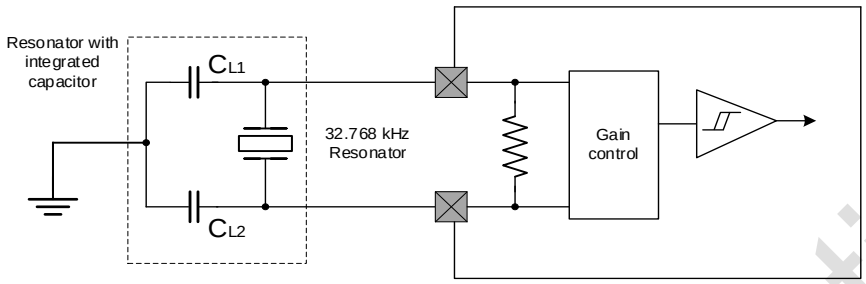


Figure 1-13-4. Typical Application of 32.768kH Crystal

1.14 Internal Clock Source Characteristics

1.14.1 High Speed Internal (HSI) RC Oscillator

Table 1-14-1. HSI Oscillator Characteristics (1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	VDD = 3.3 V，T_A = 25℃，after calibration	7.92	8	8.08	MHz
ACC_{HSI}	Temperature drift of HSI oscillator	VDD = 3.3 V，TA = - 40 ~ 105℃，temperature drift	-2.5	-	2.5	%
		VDD = 3.3 V，TA = -10 ~ 85℃，temperature drift	-2	-	2.2	%
		VDD = 3.3 V，TA = 0 ~ 70℃，temperature drift	-1.3	-	2	%
$t_{SU(HSI)}$	HSI oscillator start time		1	-	3	μs
$I_{DD(HSI)}$	HSI oscillator power consumption		-	40	100	μA

1. V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.
2. Guaranteed by design, not tested in production.

1.14.2 Low speed internal (LSI) RC oscillator

Table 1-14-2. LSI Oscillator Characteristics (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25℃ calibration, VDD = 3.3 V	38	40	42	KHz
		VDD = 1.8 V ~ 3.6 V, TA = -40 ~ 105℃	30	40	60	KHz
$t_{SU(LSI)}$ (3)	LSI oscillator startup time		-	30	80	μs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption		-	0.2	-	μA

1. VDD = 3.3V, TA = -40~105℃ unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.

1.14.3 Time to Wake up from Low Power Mode

The wake-up time listed belowed is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:：

- STOP2 or STANDBY mode: clock source is RC oscillator
- SLEEP mode: The clock source is the clock used to enter sleep mode

Table 1-14-3. Wake Time in Low Power Mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wake up from SLEEP mode	480	ns
$t_{WUSTOP0}$(1)	Wake up from STOP0 mode (The regulator is in running mode)	20	us
	Wake up from STOP0 mode (The regulator is in low power consumption mode)	22	
$t_{WUSTOP2}$(1)	Wake up from STOP2 mode	40	us
$t_{WUSTDBY}$(1)	Wake up from STANDBY mode	100	us
1. The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.			

1.15 PLL Characteristics

Table 1-16. PLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	4	8.0	32	MHz
	PLL Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL output clock(2)	32	-	144	MHz
t_{LOCK}	PLL Ready indicates signal output time(3)	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @144 MHz(1)	-	5	-	pS
Ipll	Operating Current of PLL @144 MHz VCO frequency.	-	-	700	uA
1. Based on comprehensive evaluation, not tested in production.					
2. Care needs to be taken to use the correct frequency doubling factor to input the clock frequency according to PLL so that f_{PLL_OUT} is within the allowable range.					

1.16 FLASH Memory Characteristics

Table 1-16-1. FLASH Memory Characteristics

Symbol	Parameter	Condition	Min	Typ	Max(1)	Unit
t_{prog}	32-bit programming time	T_A = -40 ~ 105℃	-	112	225	μs
t_{ERASE}	Page (2K bytes) erasure time	T_A = -40 ~ 105℃	-	2	20(2)	ms
					100(3)	
t_{ME}	Mass erase time	T_A = -40 ~ 105℃;	-	-	100	ms
Vprog	Programming voltage		1.8	3.0	3.6	V
I_{DD}	Power supply current (1)	Read mode, f_{HCLK} = 144 MHz，3 waiting cycles，V_{DD} = 3.3 V	-	-	3.62	mA
		Write mode，f_{HCLK} = 144 MHz，V_{DD} = 3.3 V	-	-	6.5	mA
		Erase mode，f_{HCLK} = 144 MHz，V_{DD} = 3.3 V	-	-	4.5	mA
		Power-down/stop mode，V_{DD} = 3.3~3.6 V	-	-	0.035	μA
1. Guaranteed by design, not tested in production.						
2. 10k storage space of erasure times.						

3. 100k storage space of erasure times.

Table 1-16-2. Flash Endurance and Data Retention Life

Symbol	Parameter	Condition	Min (1)	Unit
t_{RET}	Data retention period	TA =85℃	10	Year
N_{END}	Endurance (note: erasure times)	TA = - 40 ~ 105°C (suffix is 7); Flash storage is 256KB	10	Kcycle
		TA = -40~105°C(尾缀为7)； Flash storage is 512KB，among which storgae space is at the first 256KB.	100	
		TA = -40~105°C(尾缀为7)； Flash容量为512KB，among which storgae space is at the last 256KB	10	

1. Based on comprehensive evaluation, not tested in production.
2. Cycling performed over the whole temperature range.

1.17 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip and thus confirm its performance in terms of electrical sensitivity.

● Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples, the size of which is related to the number of power pins on the chip (3 x (n+1) power pins). This test conforms to JESD22-A114/C101 standard.

Table 1-17-1. Absolute Maximum ESD Value

Symbol	Parameter	Condition	Type	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	TA = +25 °C, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	TA = +25 °C, In accordance with ESDA/JEDEC JS -002-2018	C3	1000	

1.Based on comprehensive evaluation, not tested in production.

● Static switch lock

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin. This test conforms to JEDEC78E IC latch standard.

Table 1-17-2. Electrical Sensitivity

Symbol	Parameter	Condition	Type	Min
LU	Static locking classes	T_A(2) = +25 °C，in accordance with JESD7E	II class A	±100mA , 1.5*VDDMAX

1. Test is under normal temperature.

1.18 I/O Port Characteristics

● General input/output characteristics

All I/O ports are CMOS and TTL compatible.

Table 1-18-1. I/O Static Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{IL}	Input low level voltage	V_{DD}=3.3V	V_{SS}	0.8	V
		V_{DD}=2.5V		0.7	
		V_{DD}=1.8V		0.3*V_{DD}	
V_{IH}	Input high level voltage	V_{DD}=3.3V	2	V_{DD}	
		V_{DD}=2.5V	1.7	V_{DD}	
		V_{DD}=1.8V	0.7*V_{DD}	V_{DD}	
V_{hys}	Schmidt trigger voltage lag(1)	V_{DD}=3.3V	200	-	mV
		V_{DD}=2.5V	200	-	
		V_{DD}=1.8V	0.1*V_{DD} (2)	-	
I_{lkg}	Input leakage current(2)	V_{DD} = Maximum V_{PAD} = 0 or V_{PAD} = V_{DD}	-1	+1	μA
R_{PU}	Weak pull-up equivalent resistance(4)	V_{DD} = 3.3V, V_{IN} = V_{SS}	100	160	KΩ
R_{PD}	Weak pull-down equivalent resistance(4)	V_{DD} = 3.3V, V_{IN} = V_{DD}	100(6)	160(6)	
C_{IO}	Capacitance of I/O pins	-	-	0.1	pF

1. The hysteresis voltage of Schmitt trigger switching level. Based on comprehensive evaluation, not tested in production.
2. The leakage current may be higher than 100 mV.
3. If there is reverse current in the adjacent pins, the leakage current may be higher than the maximum
4. Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.
5. VPAD refers to the input voltage of the I/O pin.
6. PA11,PA12,PA14,PB2 are not included.

All I/O ports are CMOS and TTL compatible (no software configuration required). The features take most of the strict CMOS process or TTL parameters into account:

■ **For VIH：**

- If VDD is between [1.8V~3.08V]；Use CMOS features and include TTL.
- If VDD is between [3.08V~3.6V]；Use TTL features and include CMOS.

■ **For VIL：**

- If VDD is between [1.8V~2.28V]；Use TTL features and include CMOS.
- If VDD is between [2.28V~3.60V]；Use CMOS features and include TTL.

● **Output drive current**

GPIO (universal input/output port) can absorb or output up to +/-12mA current. In the user application, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings.

● **Output voltage**

All I/O ports are CMOS and TTL compatible.

Table 1-18-2. IO Output Driving Ability Characteristics

Drive class	I_{OH}(1), V_{DD}=3.3V	I_{OL}(1), V_{DD}=3.3V	I_{OH}(1), V_{DD}=2.5V	I_{OL}(1), V_{DD}=2.5V	I_{OH}(1), V_{DD}=1.8V	I_{OL}(1), V_{DD}=1.8V	Unit
2	-2	2	-1.5	1.5	-1	1	mA
4	-4	4	-3	3	-2	2	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7	8	mA

1. Guaranteed by design, not tested in production.

Table 1-18-3. Output Voltage Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low level	V_{DD} = 3.3 V, I_{OL}(3)= 2mA, 4mA, 8mA, and 12mA	V_{SS}	0.4	V
		V_{DD} = 2.5 V, I_{OL}(3)= 2mA, 4mA, 8mA, and 12mA	V_{SS}	0.4	

		V_{DD} = 1.8 V, I_{OL}[3]= 2mA, 4mA, 8mA, and 12mA	V_{SS}	0.2 * V_{DD}	
V_{OH}[2]	Output high level	V_{DD} = 3.3 V, I_{OH}[3]= 2mA, 4mA, 8mA, and 12mA	2.4	V_{DD}	
		V_{DD} = 2.5 V, I_{OH}[3]= 2mA, 4mA, 8mA, and 12mA	1.8	V_{DD}	
		V_{DD} = 1.8 V, I_{OH}[3]= 2mA, 4mA, 8mA, and 12mA	0.8 * V_{DD}	V_{DD}	

1. The current I_{IO} absorbed by the chip must always follow the absolute maximum rating, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.

2. The current I_{IO} output from the chip must always follow the absolute maximum rating, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.

- **Input/output AC Characteristics**

The definitions and values of the input and output AC characteristics are given below.

Table 1-18-4. Input/output AC Characteristics

PMODEy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 5pF, V_{DD} = 3.3V	-	75	MHz
			C_L = 5pF, V_{DD} = 2.5V	-	50	
			C_L = 5pF, V_{DD} = 1.8V	-	30	
	$t_{(IO)out}$	Output delay (A to pad)	C_L = 5pF, V_{DD} = 3.3V	-	3.66	ns
			C_L = 5pF, V_{DD} = 2.5V	-	4.72	
			C_L = 5pF, V_{DD} = 1.8V	-	7.12	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50fF, V_{DD} = 2.97V, V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	2	ns
01 (4mA)	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 10pF, V_{DD} = 3.3V	-	90	MHz
			C_L = 10pF, V_{DD} = 2.5V		60	
			C_L = 10pF, V_{DD} = 1.8V		40	
	$t_{(IO)out}$	Output delay (A to pad)	C_L = 10pF, V_{DD} = 3.3V	-	3.5	ns
			C_L = 10pF, V_{DD} = 2.5V		4.5	
			C_L = 10pF, V_{DD} = 1.8V		6.74	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50fF, V_{DD} = 2.97V, V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	2	ns
10 (8mA)	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 20pF, V_{DD} = 3.3V	-	100	MHz
			C_L = 20pF, V_{DD} = 2.5V	-	75	
			C_L = 20pF, V_{DD} = 1.8V	-	50	
	$t_{(IO)out}$	Output delay (A to pad)	C_L = 20pF, V_{DD} = 3.3V	-	3.42	ns
			C_L = 20pF, V_{DD} = 2.5V	-	4.73	
			C_L = 20pF, V_{DD} = 1.8V	-	6.53	
	$t_{(IO)in}$	Input delay (pad to Y)	C_L = 50fF, V_{DD} = 2.97V, V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	2	ns
11 (12mA)	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 30pF, V_{DD} = 3.3V	-	120	MHz
			C_L = 30pF, V_{DD} = 2.5V	-	90	
			C_L = 30pF, V_{DD} = 1.8V	-	60	
	$t_{(IO)out}$	Output delay (A to pad)	C_L = 30pF, V_{DD} = 3.3V	-	3.34	ns
			C_L = 3pF, V_{DD} = 2.5V	-	4.26	
			C_L = 3pF, V_{DD} = 1.8V	-	6.34	
	$t_{(IO)in}$	Input delay	C_L = 50fF, V_{DD} = 2.97V,	-	2	

PMODEy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
		(pad to Y)	V_{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated			
1. The speed of the I/O port can be configured via PMODEy[1:0]. 2. Guaranteed by design, not tested in production.						

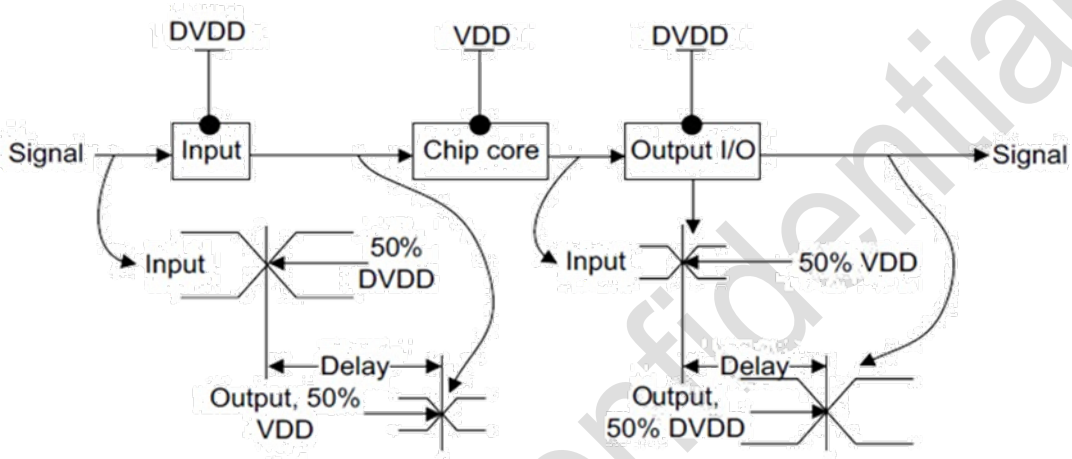


Figure 1-18-1. Definition of Input/Output AC Characteristics

1.19 MCU_NRST Pin Characteristics

The NRST pin input driver uses the CMOS techniques, which is connected to an unbreakable pull-up resistor

Table 1-19-1. NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	V_{DD} = 3.3 V	Vss	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	V_{DD} = 3.3 V	2	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	-	-	100		mV V
R_{PU}	Weak pull-up equivalent resistance(2)	VIN= VIH	30	50	70	KΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.

2. The pull-up resistor is designed as a real resistor in series for a switchable PMOS implementation. The resistance of PMON/NMOS switch is very small (in approximately 10%).

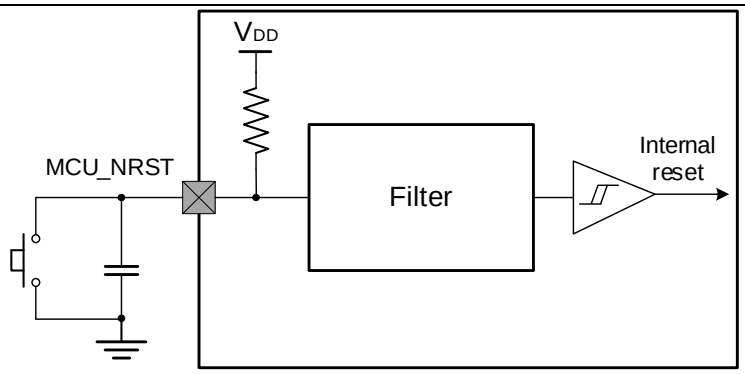


Figure 1-19-2. Recommended NRST Pin Protection

1.Resetting the network is to prevent parasitic resets.
2.The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$, otherwise the MCU cannot be reset.

1.20 Timer (TIM) Characteristics

Table 1-20-1. TIMx Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer time resolution		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144 MHz	6.95	-	ns
f_{EXT}	Timer CH1 to CH4 external clock frequency		0	fTIMxCLK/2	MHz
		$f_{TIMxCLK}$= 144 MHz	0	72	MHz
R_{esTIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle is enabled when internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	0.00695	455	μs
t_{MAX_COUNT}	Maximum count		-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	-	29.8	s

1.21 I²C Interface Characteristics

The I²C interface conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and VDD is closed, but still exists.

Table 1-21-1. I²C Interface Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast+ Mode		Mode
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I²C interface frequency	0	100	0	400	0	1000	KHz
$th_{(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data hold time	-	3.4	-	0.9	-	0.4	μs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1 Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20 + 0.1 Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	μs

Cb	Capacitive load per bus	-	400	-	400	-	100	pf
$t_{v(SDA)}$	Data validity time	3.45	-	0.9	-	0.45	-	μs
$t_{v(ACK)}$	Response time	3.45	-	0.9	-	0.45	-	μs
1. Guaranteed by design, not tested in production. 2. To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.								

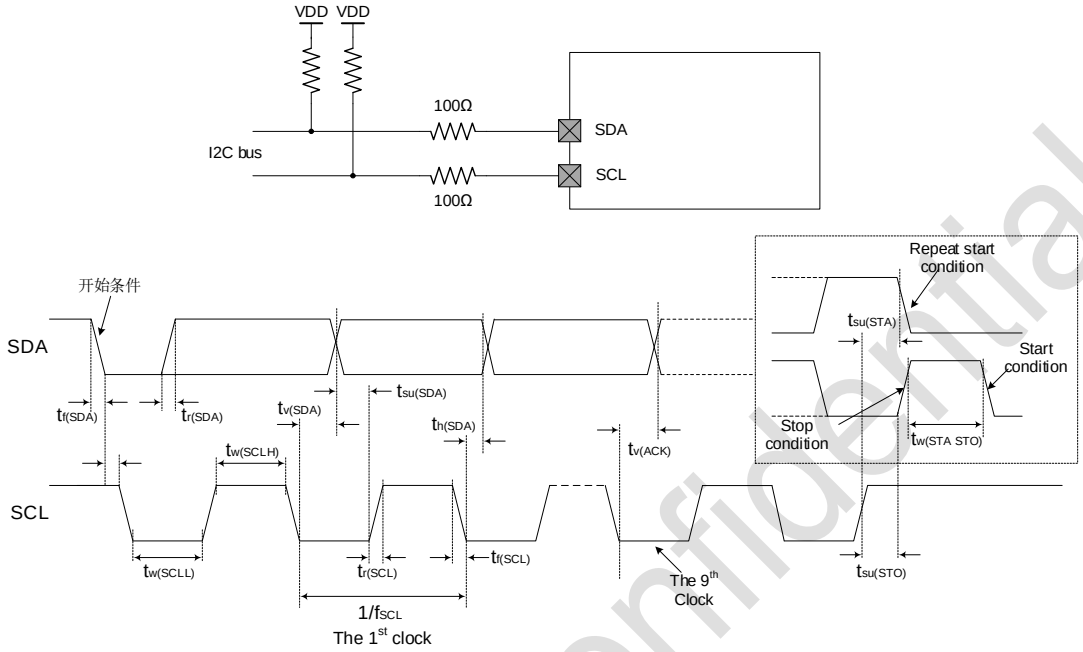


Figure 1-21-2. I2C Bus AC Waveform and Measuring Circuit (1)

1. The measuring point is set at the CMOS level: 0.3 VDD and 0.7 VDD.
2. The pull-up resistance depends on the I^2C interface speed.
3. The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

1.22 SPI/I^2S Interface Characteristics

Table 1-22-1. SPI Characteristic(4)

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	36	MHz
		Slave mode	-	36	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF	-	6	ns
DuCy(SCK)	SPI from the input clock duty cycle	SPI Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode	t_{PCLK}-2	t_{PCLK}+2	
$t_{su(MI)}$(1)	Data entry setup time	Master mode	3.5	-	
$t_{su(SI)}$(1)		Slave mode	3	-	
$t_{h(MI)}$(1)	Data entry hold time	Master mode	3	-	
$t_{h(SI)}$(1)		Slave mode	3	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode， f_{PCLK} = 20 MHz	0	3 t_{PCLK}	

Symbol	Parameter	Condition	Min	Max	Unit
$t_{dis(SO)}$(1)(3)	Disable time of data output	Slave mode	2	10	
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after enable edge)	-	12.5	
$t_{v(MO)}$(1)		Master mode (after enable edge)	-	6.5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	5	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	-0.5	-	

1. Guaranteed by design, not tested in production.

2. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the objective data.

3. The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Table 1-22-2. SPI2 Characteristic

Symbol	Parameter	Condition		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	18	MHz
		Slave mode		-	18	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30 pF		-	8	ns
DuCy(SCK)	SPI from the input clock duty cycle	SPI Slave mode		30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode		$2t_{PCLK}$	-	
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK}-2	t_{PCLK}+2	
$t_{su(MI)}$(1)	Data entry setup time	Master mode	SPI2	4	-	
			SPI3	5		
$t_{su(SI)}$(1)		Slave mode	SPI2	4	-	
			SPI3	5		
$t_{h(MI)}$(1)	Data entry hold time	Master mode	SPI2	2	-	
			SPI3	2.5		
$t_{h(SI)}$(1)		Slave mode	SPI2	2	-	
			SPI3	2		
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode，f_{PCLK} = 20 MHz		0	3 t_{PCLK}	
$t_{dis(SO)}$(1)(3)	Disable time of data output	Slave mode		2	10	
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after enable edge)	SPI2	-	13.5	
			SPI3	-	17.5	
$t_{v(MO)}$(1)		Master mode (after enable edge)	SPI2	-	6.5	
			SPI3	-	9	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	SPI2	4	-	
			SPI3	4		
$t_{h(MO)}$(1)		Master mode (after enable edge)	SPI2	1	-	
			SPI3	1		

1. Guaranteed by design, not tested in production.

2. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the objective data.

3. The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

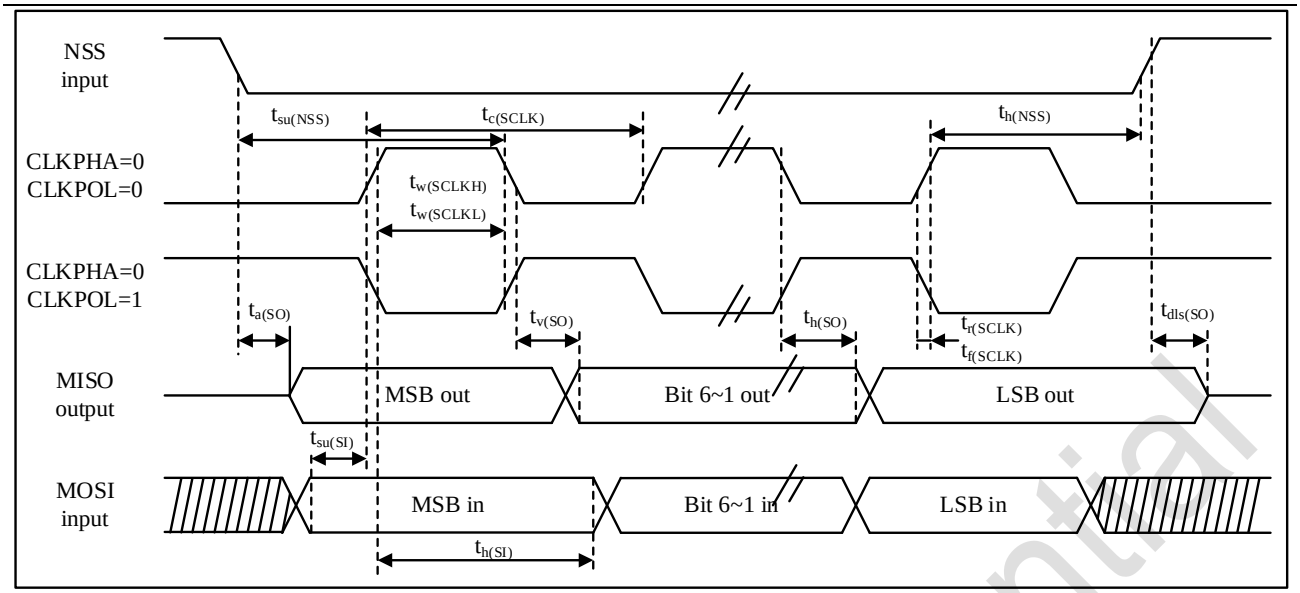
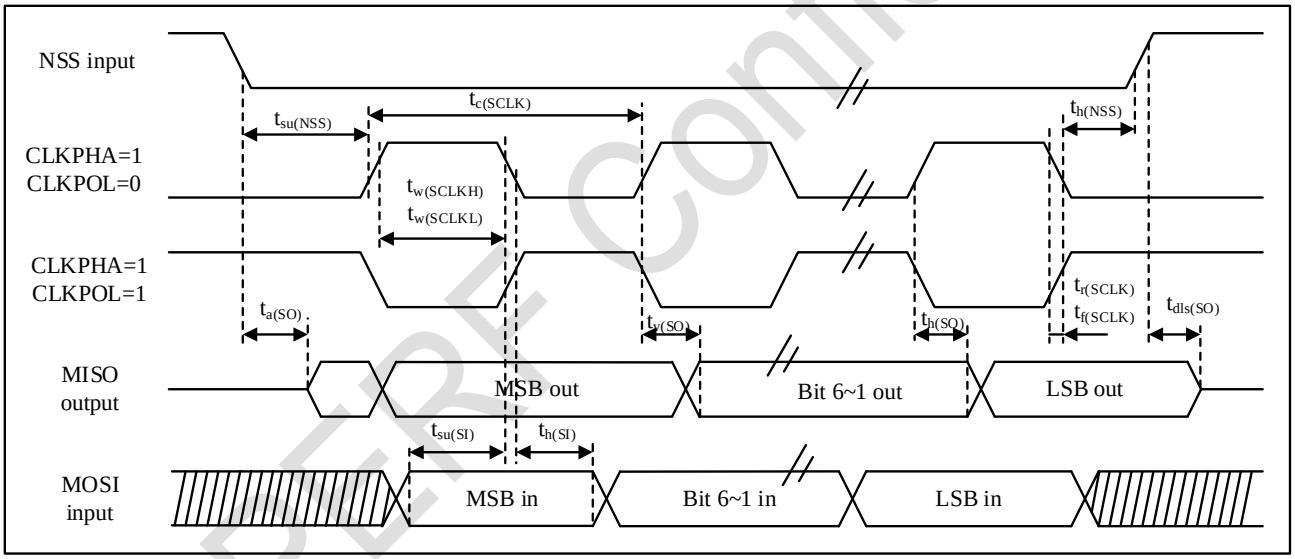
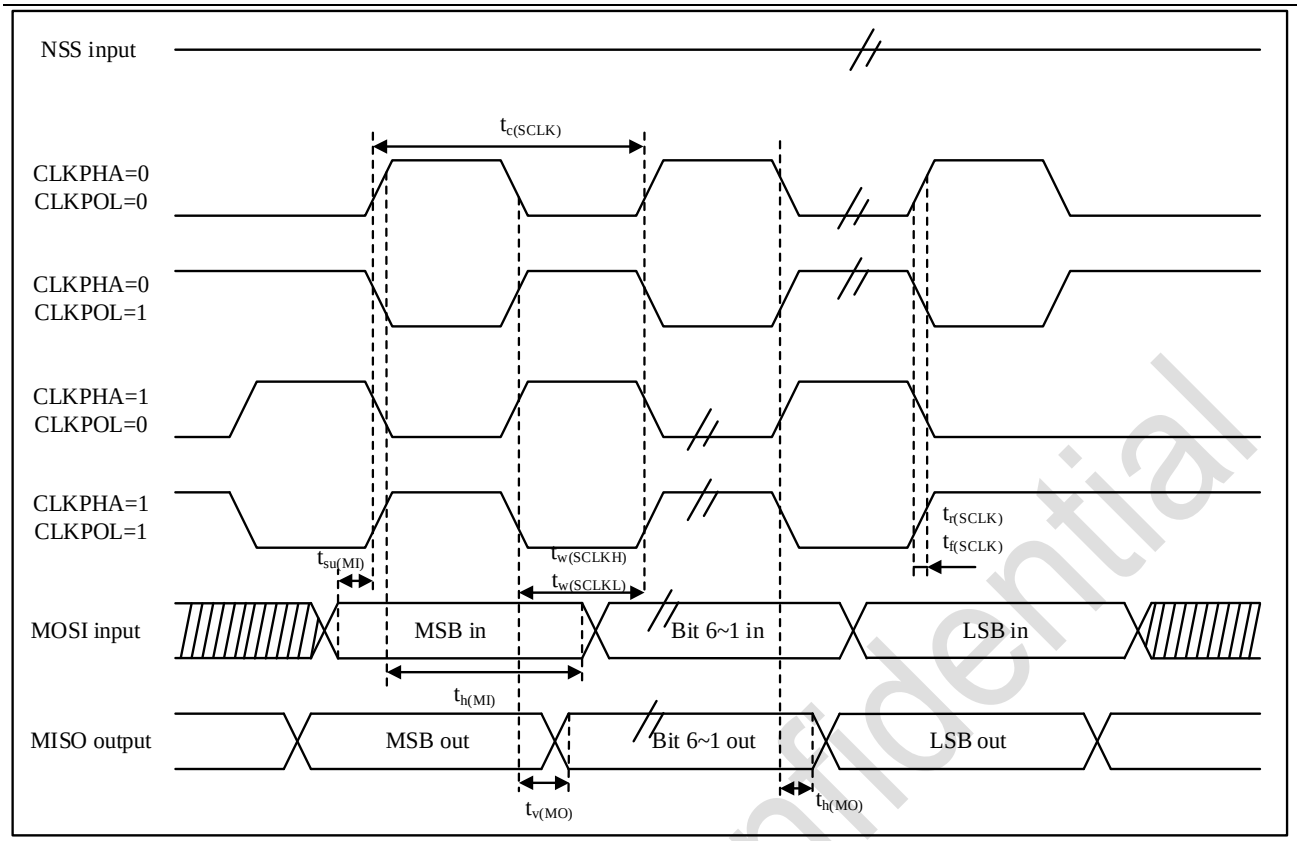


Figure 1-22-1. SPI Timing Diagram - Slave Mode and CPHA=0



1. The measuring point is set at the CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 1-22-2. SPI Timing Diagram-Slave Mode and CPHA = 1 (1)



1. The measuring point is set at the CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 1-22-3. SPI Timing Diagram-Master Mode (1)

Table 1-22-3. I²S Characteristics (1)

Symbol	Parameter	Condition		Min	Max	Unit
DuCy(SCK)	I²S clock duty cycle	I2S Slave mode		30	70	%
f_{CLK} $1/t_{c(CLK)}$	I²S clock frequency	Master mode (32 bit)		-	64*Fs(3)	MHz
		Slave mode (32 bit)		-	64*Fs(3)	
$t_{r(CLK)}$	I²S clock rise and fall time	Load capacitance：CL = 50pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	I²S2	5.3	-	
			I²S3	5	-	
$t_{h(WS)}$(1)	WS hold time	Master mode		0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I²S2	5.5		
			I²S3	5	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	I²S2	7	-	
			I²S3	3.6	-	
$t_{w(CLKH)}$(1)	CLK high and low times	Master mode, f_{PCLK} = 16MHz, audio 48kHz		312.5	-	

Symbol	Parameter	Condition		Min	Max	Unit
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Data entry setup time	The main receiver	I²S2	4	-	
			I²S3	5	-	
$t_{su(SD\_SR)}$(1)		Slave mode	I²S2	4	-	
			I²S3	4.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data entry hold time	Master receiver	I²S2	1.5	-	
			I²S3	1.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I²S2	1.5	-	
			I²S3	1.5	-	
$t_{v(SD\_ST)}$(1)(2)	Valid time of data output	Slave transmitter (after enable edge)	I²S2	-	14	
			I²S3	-	16.5	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave generator (after enable edge)	I²S2	3.5	-	
			I²S3	4.5	-	
$t_{v(SD\_MT)}$(1)(2)	Valid time of data output	Master generator (after enable edge)	I²S2	-	6.5	
			I²S3	-	6	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master generator (after enable edge)	I²S2	-0.5	-	
			I²S3	-0.5	-	

1. Guaranteed by design, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then $T_{PCLK}=1/f_{PCLK}$ =125ns.

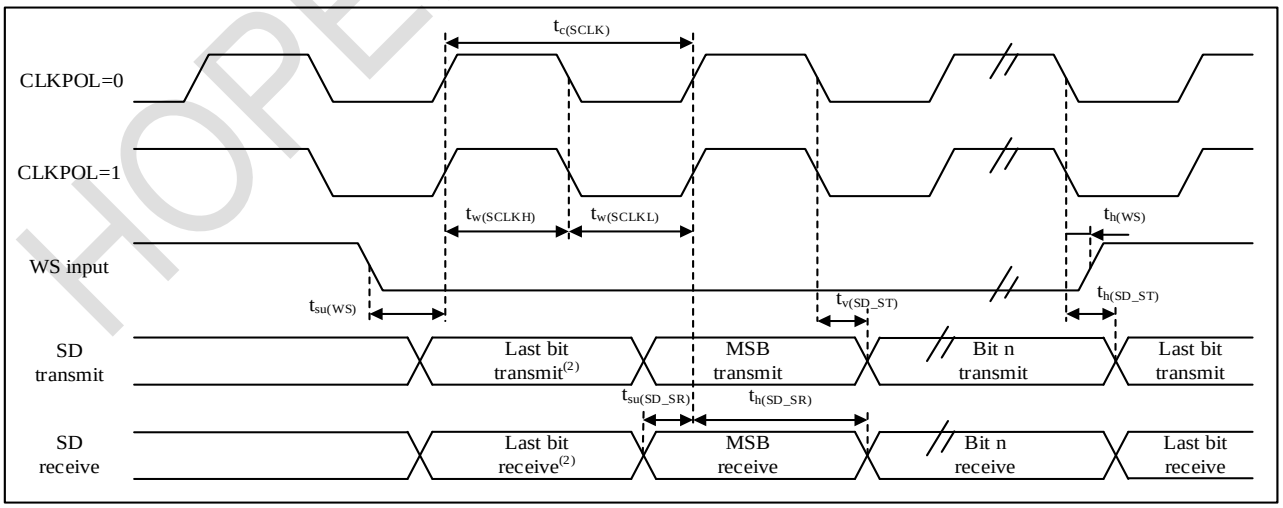


Figure 1-22-4. I²S Slave Mode Timing Diagram (Philips Protocol) (1)

1. The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.
2. Send/receive the loweast bit of the last byte. There is no lowest bit send/receive before the first byte.

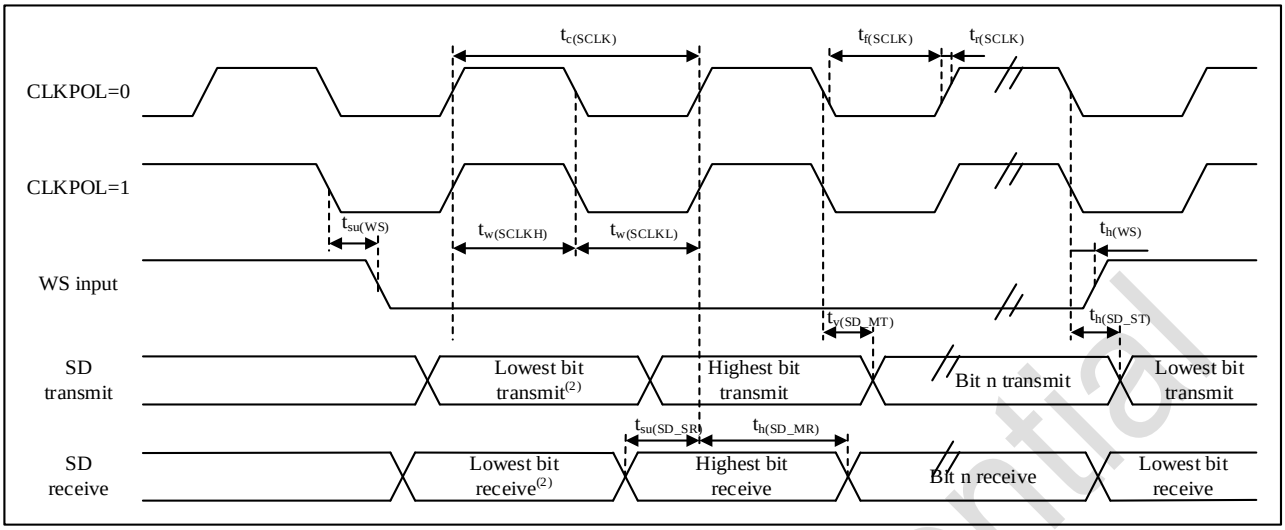


Figure 1-22-5. I²S Master Mode Timing Diagram (Philips protocol) (1)

1. The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Send/receive the loweast bit of the last byte. There is no lowest bit send/receive before the first byte.

1.23 QSPI Characteristic

Table 1-23-1. QSPI Characteristic under SDR Mode

Symbol	Parameter	Min	Max	Unit
f_{CK} $1/t_{(CK)}$	QSPI clock frequency	-	36	MHz
$t_{w(CKH)}$	SCK high and low time	$t_{(CK)}/2-2$	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2$	$t_{(CK)}/2+2$	ns
$t_{s(IN)}$	Input data setup time	4.5	-	ns
$t_{h(IN)}$	Input data hold time	4	-	ns
$t_{v(OUT)}$	Output data valid time	-	5.5	ns
$t_{h(OUT)}$	Output data hold time	-0.15	-	ns

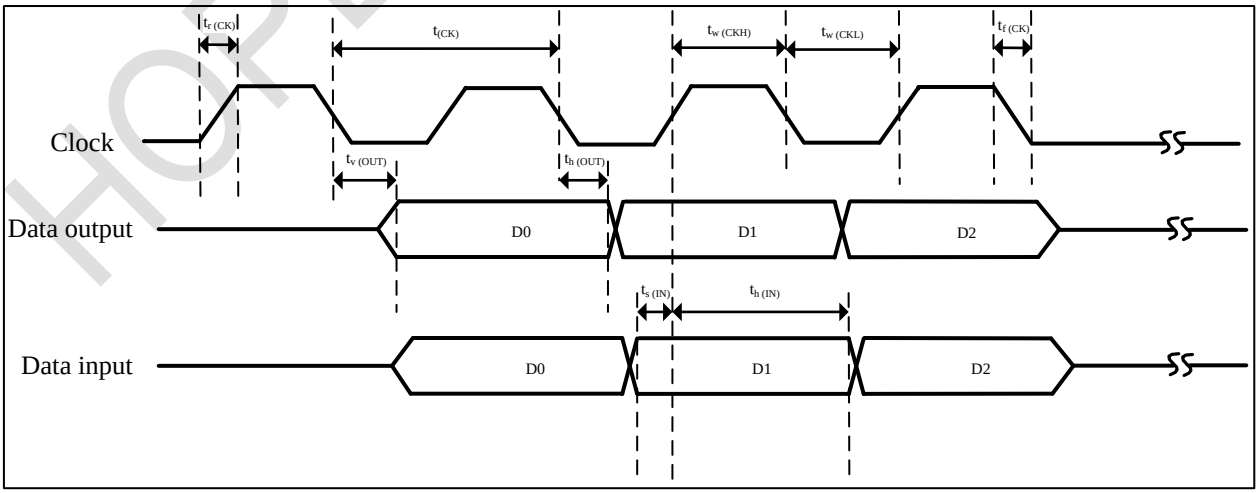


Figure 1-23-1. QSPI Sequence under SDR Mode

Table 1-23-2. QSPI Characteristic under DDR Mode

Symbol	Parameter	Min	Max	Unit
f_{CK} $1/t_{(CK)}$	QSPI clock frequency	-	36	MHz
$t_{w(CKH)}$	SCK high and low time	$t_{(CK)}/2-2$	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2$	$t_{(CK)}/2+2$	ns
$t_{sf(IN)};t_{sr(IN)}$	Input data setup time	4.5	-	ns
$t_{hf(IN)};t_{hr(IN)}$	Input data hold time	4.5	-	ns
$t_{vf(OUT)};t_{vr(OUT)}$	Output data valid time	-	12	ns
$t_{hf(OUT)};t_{hr(OUT)}$	Output data hold time	6	-	ns

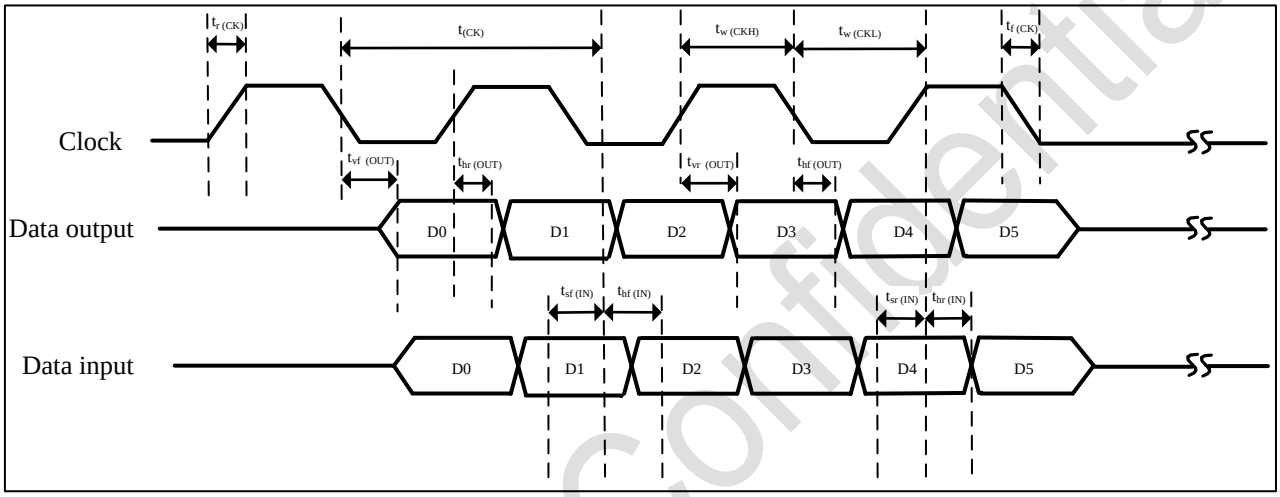


Figure 1-23-2. QSPI 在 DDR 模式下的时序

1.24 USB Characteristics

USB (full speed) interface is certified by the USB-IF.

Table 1-24-1. USB Startup Time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	μs
1. Guaranteed by design, not tested in production.			

Table 1-24-2. USB DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
Input level					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I (USBDP and USBDM)	0.2	-	V
V_{CM}(4)	Differential common model range	Contains VDI ranges	0.8	2.5	
V_{SE}(4)	Single-end receiver threshold		1.3	2.0	
Output level					
V_{OL}	Static output low level	1.5KΩ RL is connected to 3.6V(5)	-	0.3	V
V_{OH}	Static output high level	15KΩ RL is connected to	2.8	3.6	

Symbol	Parameter	Condition	Min	Max	Unit
		V_{SS}(5)			

1. All voltage measurements are based on the ground cable at the device end.
2. USB operating voltage is 3.0~3.6V in order to be compatible with USB2.0 full speed electrical specification.
3. Inorder to guaranteed the USB function, at 2.7V, electrical characteristic has to set at 2.7V, rather than reducing at 2.7-3.0V.
4. Based on comprehensive evaluation, not tested in production.
5. R_L is the load attached to the USB drive.

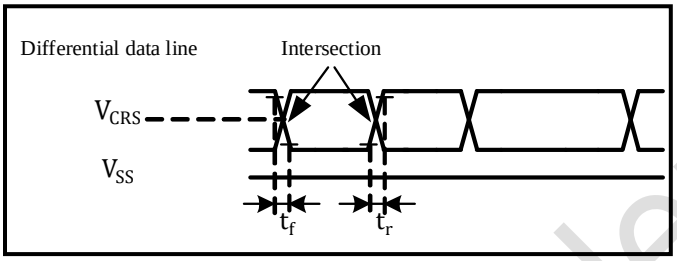


Figure 1-24-1. USB Timing: Definition of Rise and Fall Time of Data Signal

Table 1-24-3. Full Speed of USB Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_r	Rise time(2)	C_L ≤ 50pF	4	20	ns
t_f	Fall time(2)	C_L ≤ 50pF	4	20	ns
t_{rfm}	Rise and fall time match	t_r / t_f	90	110	%
V_{CRS}	Output cross voltage signal	-	1.3	2.0	V
R_S	Output series matching resistor	Match the external resistor, close to pins	27	39	Ohm

1. Guaranteed by design, not tested in production.
2. 10% to 90% of the measurement data signal. See Chapter 7 (Version 2.0) of the USB Specification for details.

1.25 Ethernet Interface Characteristic

Table 1-25-1. Ethernet DC Characteristic

Symbol	Parameter	Min (1)	Max (1)	Unit
V_{DD}	Ethernet operating voltage	3.0	3.6	V

1. All voltage measurements are based on ground of the device.

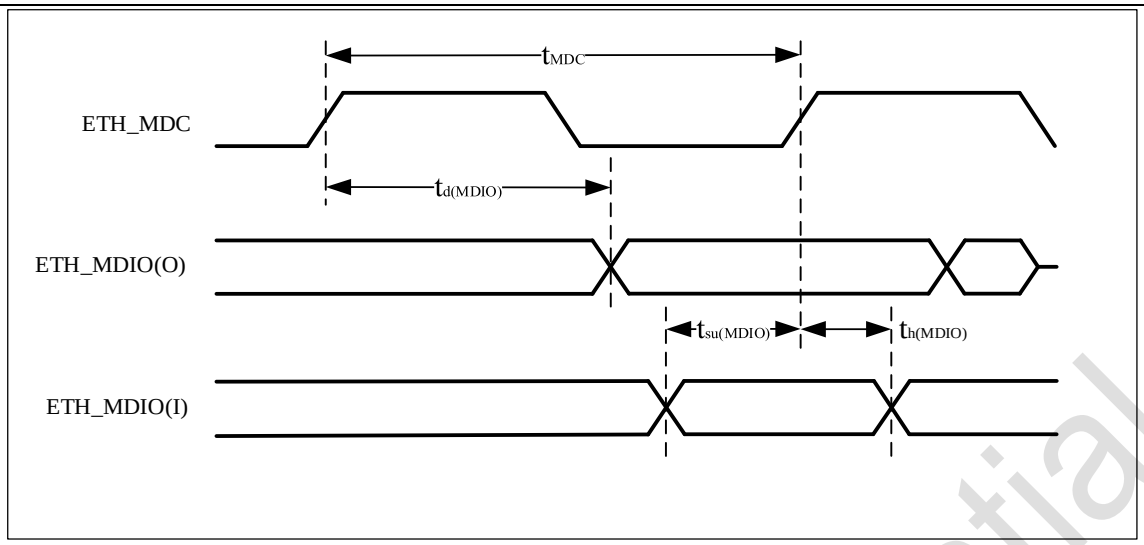


Figure 1-25-1. Ethernet SMI Sequence Diagram

Table 1-25-2. Ethernet SMI Signal Active Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC clock cycle time (2.38MHz)	400	400	403	ns
$t_{d(MDIO)}$	MDC write data valid time	4.5	10	12	ns
$t_{su(MDIO)}$	Read data setup time	14	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

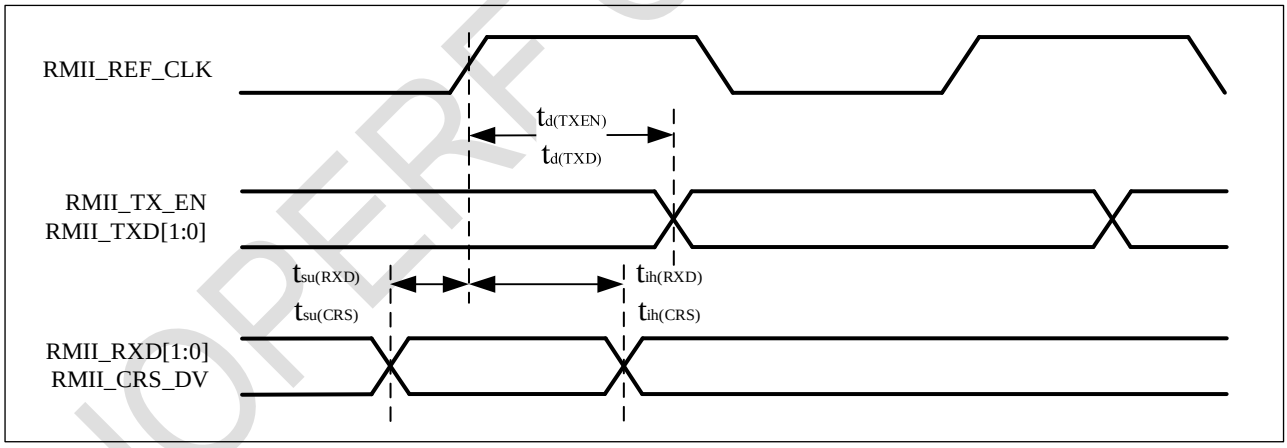


Figure 1-25-2. Ethernet RMII Sequence Diagram

Table 1-25-3. Ethernet RMII Signal Active Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Rx data setup time	3.5	-	-	ns
$t_{ih(RXD)}$	Rx data hold time	2	-	-	ns
$t_{su(DV)}$	Carrier sense setup time	4	-	-	ns
$t_{ih(DV)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Tx enable valid delay time	3.5	6.5	12.5	ns
$t_{d(TXD)}$	Tx data valid delay time	3	6.5	10.5	ns

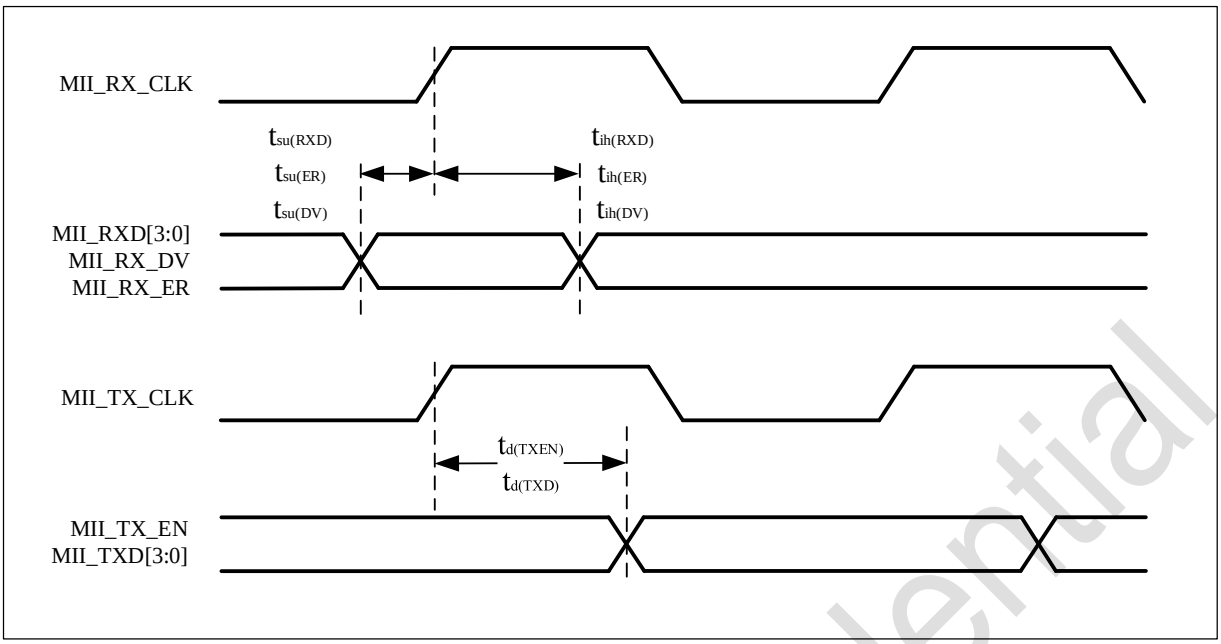


Figure 1-25-3. Ethernet MII Timing Diagram

Table 1-25-4. Ethernet MII Signal Active Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Rx data setup time	6.5	-	-	ns
$t_{ih(RXD)}$	Rx data hold time	3.5	-	-	ns
$t_{su(DV)}$	Carrier sense setup time	4.5	-	-	ns
$t_{ih(DV)}$	Carrier sense hold time	3.5	-	-	ns
$t_{su(ER)}$	Error setup time	2.5	-	-	ns
$t_{ih(ER)}$	Error hold time	3.5	-	-	ns
$t_{d(TXEN)}$	Tx enable valid delay time	4	10	14.5	ns
$t_{d(TXD)}$	Tx data valid delay time	3.5	10	15	ns

1.26 MCU CAN Interface Characteristic

For more information on the features of the input/output multiplexing function pins (CAN_TX and CAN_RX), please see at chapter 5.17.

1.27 ADC Characteristic

Table 1-27-1. ADC Characteristic

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	The power supply voltage		1.8	-	3.6	V
V_{REF+}	Positive reference voltage		1.8	-	V_{DDA}	V
f_{ADC}	ADC clock frequency		-	-	72	MHz
f_s(1)	Sampling rate		-	-	5	MHz
V_{AIN}	Switching voltage range(2)		0 (V_{SSA} or V_{REF-} connect to ground)	-	V_{REF+}	V
R_{ADC}(1)	Sampling switch resistance	Fast channel, under 3.3V	-	-	70	ohm

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{ADC}(1)	Sampling switch resistance	Slow channel, under 3.3V	-	-	0.25	KΩ
C_{ADC}(1)	Internal sampling and holding capacitors	-	-	5	-	pF
SNDR	Singal noise distortion rate	-	-	65	-	dBFS
T_{cal}	Calibration time	-	82			$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 72 MHz (fast channel)	0.0208	-	8.35	us
		f_{ADC} = 72 MHz (slow channel)	0.0625	-	8.35	
Ts(1)	Sampling cycles	fast channel	1.5	-	601.5	$1/f_{ADC}$
		slow channel	4.5	-	601.5	
t_{STAB}(1)	Power on time	-	0	0	20	μs
t_{CONV}(1)(3)	Total conversion time (including sampling time)	-	14~614 (Sampling T_S + gradually close to 12.5)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. Accoring to different package, V_{REF+} is connected internally to $V_{DDA,}$ and V_{REF-} is connected internally to $V_{SSA.}$
3. Single conversion mode has 3 more $1/f_{ADC}$ than continuous conversion mode

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB.,where N=12 (representing 12-bit resolution).

Table 1-27-2. ADC Accuracy-Limited Test Conditions (1)(2)

Symbol	Parameter	Test Condition	Typ	Max(3)	Unit
ET	Comprehensive error(4)	f_{HCLK} = 72 MHz, f_{ADC} = 72 MHz, sample Rate = 1.75m SPS, V_{DDA} = 3.3V, T_A = 25 °C Measurements are made after calibration of ADC V_{REF+} = V_{DDA}	±1.3	±5	LSB
EO	Offset error(5)		±1	±2	
ED	Differential linear error		±0.7	±1	
EL	Integral linear error		±0.8	±2	

1. The DC accuracy of the ADC is measured after internal calibration.
2. ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin. It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current.
3. The forward injection current does not affect the ADC accuracy so long as it is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in chapter 1.19.
4. Based on comprehensive evaluation, not tested in production.

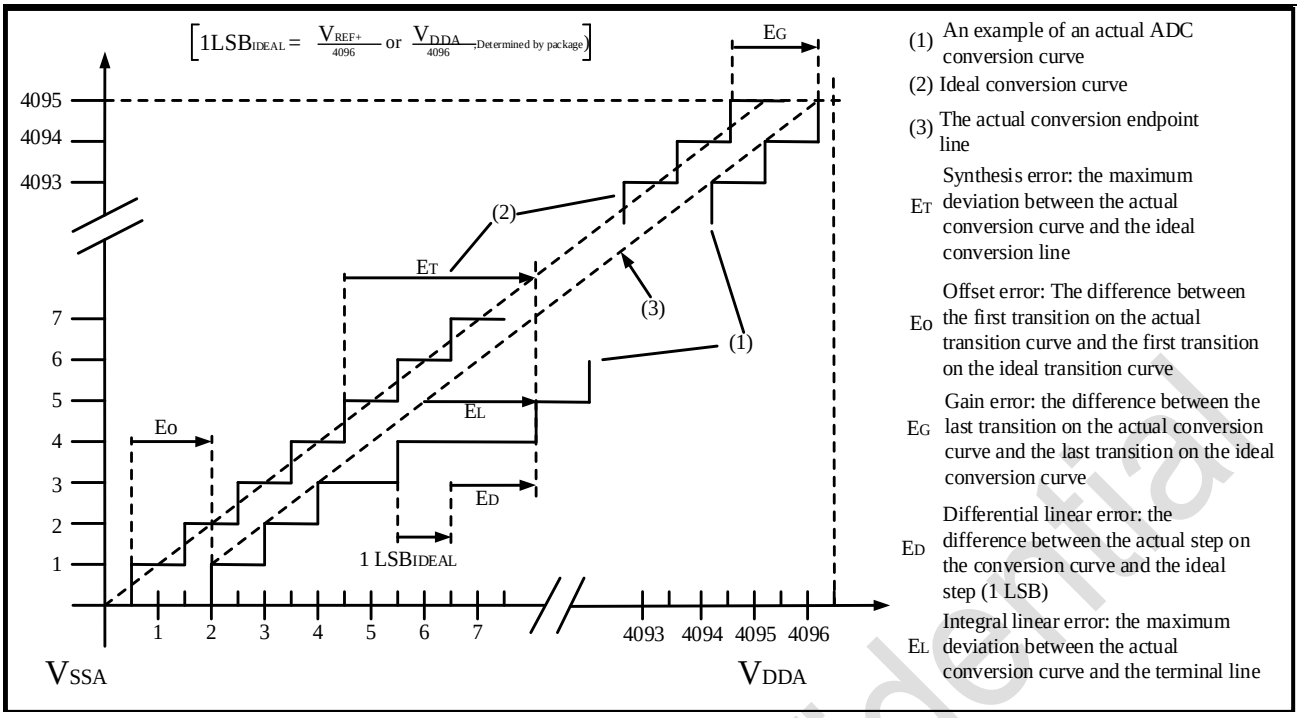


Figure 1-27-1. ADC Precision Characteristics

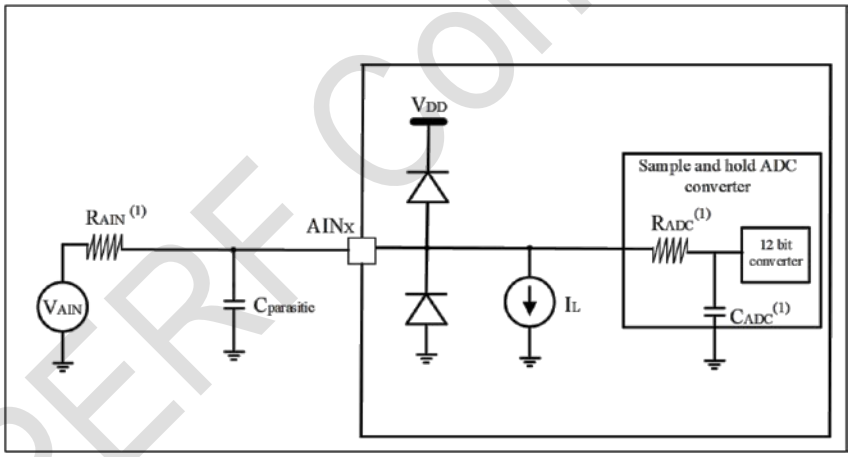


Figure 1-27-2. ADC Typical Connection Diagram

1. Cparasitic indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF). A larger Cparasitic value would reduce the accuracy of the conversion and the solution is to reduce value of f_{ADC}.

Note: Input voltage less than -0.2V is prohibited on ADC channel

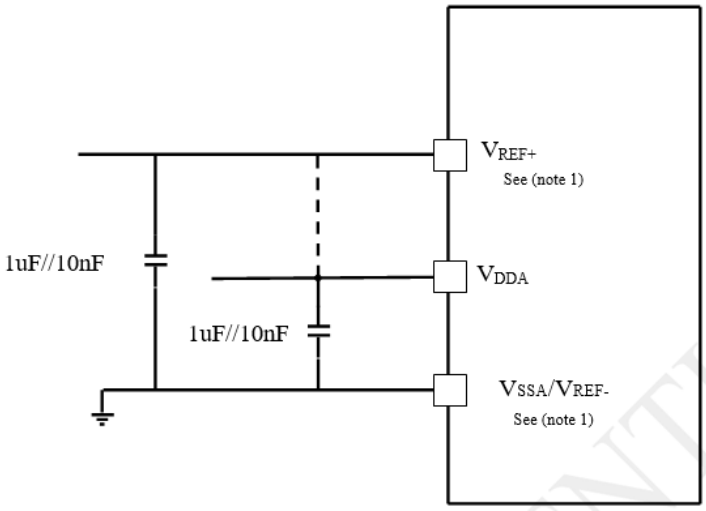


Figure 1-27-3. Decoupling Circuit of Power Supply and Reference Power Supply (V_{REF+} is not connected to V_{DDA})

1. V_{REF+} and V_{REF-} are input pins applied in products with more than 100 pins.

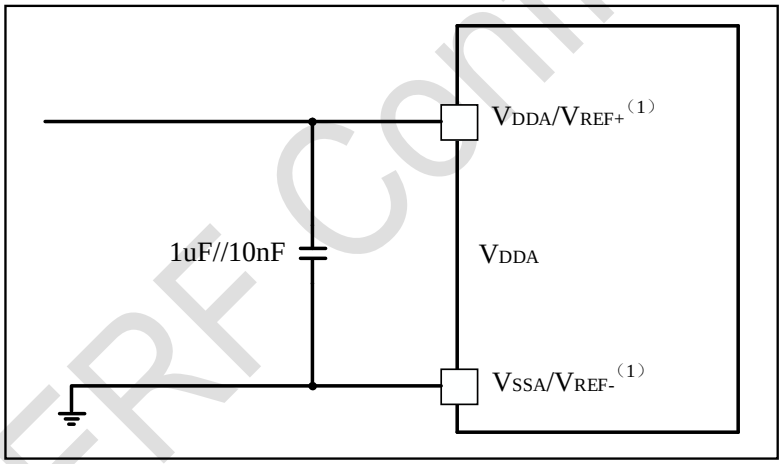


Figure 1-27-4. Decoupling Circuit of Power Supply and Reference Power Supply (V_{REF+} is connected to V_{DDA})

1. V_{REF+} and V_{REF-} are internally connected to V_{DDA} and V_{SSA}.

1.28 Operational Amplifier (OPAMP) Electrical Parameters

Table 1-28-1. OPAMP Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode voltage input range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage (after calibration)	-	-	±1	±3.5	mV
ΔVI_{OFFSET}	Input offset voltage temperature drift	-	-	10	-	UV / ° C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{LOAD}	Drive current	-	-	-	0.5	mA
I_{DDA}	Operational amplifier current consumption	No load, quiescent mode	-	-	1.5	mA
TS_OPAMP_VOUT	ADC sampling time as opamp output	-	400	-	-	ns
CMMR	Common mode rejection ratio	-	-	84	-	dB
PSRR	Power rejection ratio	-	-	100	-	dB
GBW	Gain bandwidth	-	-	4	-	MHz
SR	Conversion rate	-	-	2.5	-	V/us
R_{LOAD}	Minimum impedance load	-	4	-	-	KΩ
C_{LOAD}	Maximum capacitive load	-	-	-	50	pF
$t_{STARTUP}$	Start-up setup time	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	3	-	μs
PGA Gain error	Programmable gain error	Input signal amplitude > 100mV	-	±2.5	-	%
PGA BW	PGA bandwidth for different noninverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	2	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload =4 KΩ	-	1	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.25	-	
		PGA Gain = 32, Cload = 50pF, Rload = 4KΩ	-	0.125	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	111	-	nV/$\sqrt{\text{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	44	-	
1. Guaranteed by design, not tested in production.						

1.29 Comparator (COMP) Electrical Parameters

Table 1-29-1. COMP Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	
$t_{STAR}{}^{(1)}{}_{T}$	Comparator startup setup time	VDDA>=2.7V	-	-	5	us
		VDDA<2.7V	-	-	7	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	VDDA>=2.7V	-	50	65	ns
		VDDA<2.7V	-	60	80	
V_{OFFSET}	Comparator input offset error	Full common mode range	-	±8	±20	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{hys}	Comparison hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	20	-	
		Medium hysteresis		-	30	-	
		High hysteresis		-	40	-	
I_{DDA}	Comparator current consumption	High speed mode	Static	-	50	70	μA
			With 50 kHz ±100 mV overdrive square signal	-	60	-	
1. Guaranteed by design, not tested in production.							

1.30 12-bit DAC Electrical Parameters

Table 1-30. DAC Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit	Annotation
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{DDD}	Digital supply voltage	1.0	1.1	1.2	V	-
V_{REF+}	Reference voltage	2.4	-	3.6	V	V_{REF+} is lower than V_{DDA}
V_{SSA}	Ground wire	0	-	0	V	
R_L	Load resistance when buffer is open	5	-	-	KΩ	Minimum load resistance between DAC_OUT and V_{SSA}
C_L	The load capacitance	-	-	50	pF	The maximum capacitance on the DAC_OUT pin
I_{DD}	In work mode DAC DC consumption (V_{DDA} +V_{REF+})	-	425	600	μA	No load. The input value is 0x800
			500	700		No load, when VREF+ = 3.6V, input the maximum value
I_{DDQ}	In power down mode, DAC DC consumption (V_{DDA} +V_{REF+})	-	5	-	nA	No load
DAC_OUT Min	The low-end DAC_OUT voltage when the buffer is closed	VSS+1LSB	-	-	V	Provide the largest DAC output range. When VREF+=3.6V, corresponding to 12-bit input value 0x0E0~0xF1C. When VREF+=2.4V, corresponding to 12-bit input value 0x155~0xEAB.
	The low-end DAC_OUT voltage when the buffer is opened	0.2	-	-		
DAC_OUT Max	The low-end DAC_OUT voltage when the buffer is closed	-	-	VREF+ -5LSB		
	The low-end DAC_OUT voltage when the buffer is opened	-	-	VREF+- 0.2		
DNL	Differential non-linearity (Difference between two consecutive code)	-	±2	-	LSB	The DAC configuration is 12 bits
INL	Integral non-linearity (difference between measured value at Code I and Code i drawn on a line between Code 0 and last Code 4095)	-	±7	-	LSB	The DAC configuration is 12 bits
The offset	Offset error	-	±15	-	mV	The DAC configuration is 12 bits
	(difference between measured value at Code (0x800) and the ideal value = VREF+/2)	-	±18	-	LSB	When V_{REF+} is 3.6V, the DAC is configured as 12 bits

Symbol	Parameter	Min	Typ	Max	Unit	Annotation
Gain error	Gain error	-	±0.5	-	%	The DAC is configured as 12 bits
Amplifier Gain	Amplifier gain in open loop	80	85	-	dB	5KΩ load (maximum load), input mid-value 0x800
$t_{SETTLING}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB)	-	5	7	μs	C_{LOAD}≤50pF R_{LOAD}≥5KΩ
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	C_{LOAD}≤50pF R_{LOAD}≥5KΩ
t_{WAKEUP}	Wake up time from closed state (set CHxEN bit in DAC control register)	-	6.5	10	μs	C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5KΩ The input code is between the minimum and maximum possible values
PSRR+	Power supply rejection ratio (to VDDA) (static DC measurement	-	-67	-40	dB	No R_{LOAD}, C_{LOAD} ≤ 50pF

1. Guaranteed by design, not tested in production.

1.31 Temperature Sensor (TS) Characteristics

Table 1-32. Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
TL(1)	V_{SENSE} linearity with temperature	-	±1	±4	ºC
Avg_Slope(1)	Average slope	-3.7	-4.1	-4.3	mV/ºC
V_{25}(1)	Voltage at 25ºC	-	1.33	-	V
t_{START}(1)	Startup time	4	-	10	μs
T_{S_temp}(2)(3)	ADC sampling time when reading the tempearture	8.2	-	17.1	μs

1. Based on comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

2. Pin Description

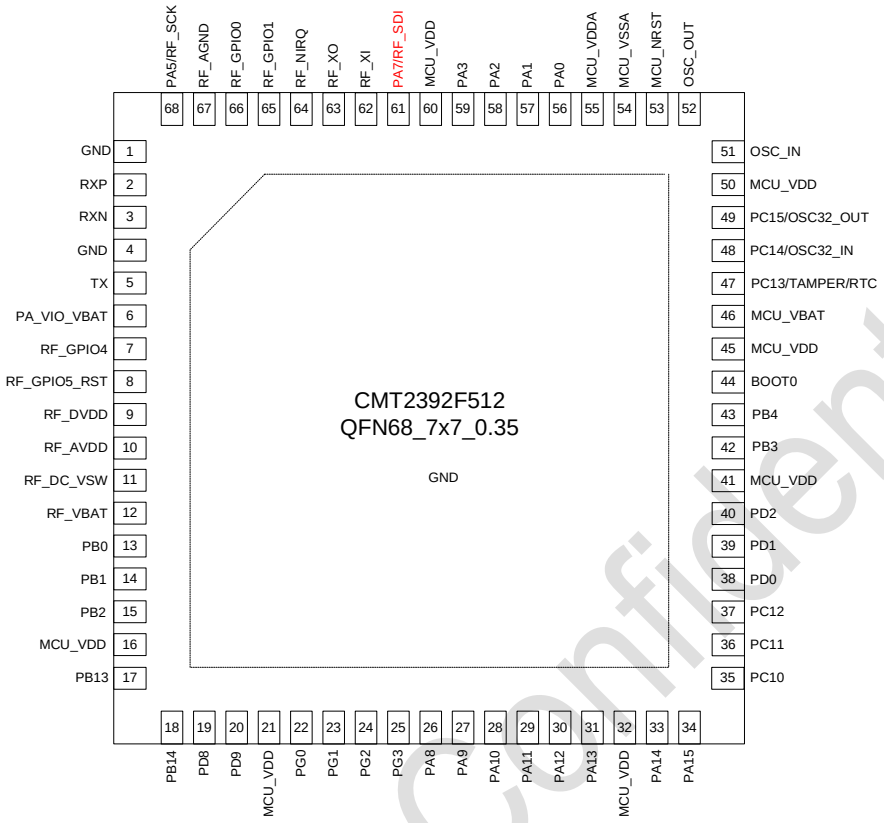


Figure 2-1. CMT2392F512 Pin Diagram

Table 2-1. CMT2392F512 Pin Description

Pin No.	Pin Name	I/O	Function Description
1	GND	I	GND
2	RXP	I	Rx signal input P
3	RXN	I	RX signal input N
4	GND	I	GND
5	TX	O	Output
6	PA_VIO_VBAT	IO	IO VDD
7	RF_GPIO4	IO	IO VDD
8	RF_GPIO5_RST	IO	Configurable
9	RF_DVDD	I	RF module digital VDD
10	RF_AVDD	I	RF circuit VDD
11	RF_DC_VSW	I	DCDC
12	RF_VBAT	I	Analog VDD
13	PB0	IO	ADC3_IN12 TIM3_CH3 TIM8_CH2N ETH_MII_RXD2

Pin No.	Pin Name	I/O	Function Description
			COMP5_OUT TIM1_CH2N UART6_TX OPAMP2_VINP COMP3_INP
14	PB1	IO	ADC2_IN3 TIM3_CH4 TIM8_CH3N ETH_MII_RXD3 TIM1_CH3N OPAMP2_VOUT UART6_RX COMP2_INM COMP1_OUT
15	PB2	IO	ADC2_IN13 UART4_TX SPI1_NSS
16	MCU_VDD	S	MCU power supply
17	PB13	IO	SPI2_SCK I2S2_CK USART3_CTS TIM1_CH1N CAN2_TX ETH_MII_TXD1 ETH_RMII_TXD1 ADC3_IN5 UART5_TX COMP4_INM
18	PB14	IO	SPI2_MISO TIM1_CH2N USART3_RTS ADC4_IN4 TSC_CHN2 COMP3_INP UART5_RX
19	PD8	IO	ADC4_IN12 TSC_CHN4 USART3_TX ETH_MII_RX_DV ETH_RMII_CRS_DV OPAMP4_VINM SPI3_NSS I2S3_WS CAN1_RX COMP6_INM
20	PD9	IO	ADC4_IN13 TSC_CHN5 USART3_RX ETH_MII_RXD0 ETH_RMII_RXD0 SPI3_SCK I2S3_CK CAN1_TX COMP6_INP
21	MCU_VDD	S	MCU power supply
22	PG0	IO	UART7_TX
23	PG1	IO	UART7_RX
24	PG2	IO	I2C2_SCL
25	PG3	IO	I2C2_SDA
26	PA8	IO	USART1_CK TIM1_CH1 MCO
27	PA9	IO	USART1_TX TIM1_CH2 TSC_DOUT I2C4_SCL

Pin No.	Pin Name	I/O	Function Description
28	PA10	IO	USART1_RX TIM1_CH3 I2C4_SDA
29	PA11	IO	USART1_CTS USBDM CAN1_RX TIM1_CH4 COMP5_OUT COMP1_OUT
30	PA12	IO	USART1_RTS USBDP CAN1_TX TIM1_ETR COMP6_OUT COMP2_OUT
31	PA13	IO	UART4_TX JTMS/SWDIO
32	MCU_VDD	S	MCU power supply
33	PA14	IO	UART4_RX JTCK/SWCLK
34	PA15	IO	SPI3_NSS I2S3_WS TIM2_CH1_ETR JTDI SPI1_NSS USART2_CTS TIM8_CH1N
35	PC10	IO	UART4_TX SDIO_D2 TSC_CHN12 USART3_TX SPI3_SCK I2S3_CK QSPI_NSS COMP3_OUT
36	PC11	IO	UART4_RX SDIO_D3 TSC_CHN13 USART3_RX SPI3_MISO QSPI_SCK COMP4_OUT
37	PC12	IO	UART5_TX SDIO_CK TSC_CHN14 USART3_CK SPI3_MOSI I2S3_SD QSPI_IO0 TIM8_CH2N
38	PD0	IO	CAN1_RX UART4_TX QSPI_IO1
39	PD1	IO	CAN1_TX UART4_RX QSPI_IO2
40	PD2	IO	TIM3_ETR UART5_RX SDIO_CMD TSC_CHN15 SPI3_NSS I2S3_WS QSPI_IO3 TIM8_CH3N
41	MCU_VDD	S	MCU power supply
42	PB3	IOI	SPI3_SCK I2S3_CK JTDO

Pin No.	Pin Name	I/O	Function Description
			TRACESWO TIM2_CH2 SPI1_SCK USART2_RTS TIM8_BKIN
43	PB4	IO	SPI3_MISO nJTRST TIM3_CH1 SPI1_MISO USART2_TX TIM8_ETR
44	BOOT0	I	-
45	MCU_VDD	S	MCU power supply
46	MCU_VBAT	I	Analog VDD
47	PC13/TAMPER/RTC	IO	TAMPER-RTC
48	PC14/OSC32_IN	IO	OSC 32_IN
49	PC15/OSC32_OUT	IO	OSC 32_OUT
50	MCU_VDD	S	MCU power supply
51	OSC_IN	I	OSC_IN
52	OSC_OUT	O	OSC_OUT
53	MCU_NRST	I	MCU reset terminal, low level effective
54	MCU_VSSA	S	-
55	MCU_VDDA	S	MCU ADC reference power supply
56	PA0	IO	WKUP USART2_CTS ADC1_IN1 TIM2_CH1_ETR TIM5_CH1 TIM8_ETR ETH_MII_CRS_WKUP COMP1_OUT COMP1_INM SPI3_MISO
57	PA1	IO	USART2_RTS ADC1_IN2 TIM5_CH2 TIM2_CH2 ETH_MII_RX_CLK ETH_RMII_REF_CLK COMP1_INP OPAMP1_VINP OPAMP3_VINP SPI3_MOSI I2S3_SD
58	PA2	IO	USART2_TX TIM5_CH3 ADC12_IN11 TIM2_CH3 ETH_MII_MDIO ETH_RMII_MDIO OPAMP1_INM OPAMP2_INM COMP3_OUT
59	PA3	IO	USART2_RX TIM5_CH4 ADC1_IN4 TIM2_CH4 ETH_MII_COL OPAMP1_VINM OPAMP1_VINP COMP5_INP
60	MCU_VDD	S	MCU power supply

Pin No.	Pin Name	I/O	Function Description
61	PA7/RF_SDI	IO	RF_SDI occupied
62	RF_XI	I	Crystal circuit input
63	RF_XO	O	Crystal circuit output
64	RF_NIRQ	I	Function configurable（not connect to MCU GPIO）
65	RF_GPIO1	IO	Configurable（not connect to MCU GPIO）
66	RF_GPIO0	IO	Configurable（not connect to MCU GPIO）
67	RF_AGND	I	Analog GND
68	PA5/RF_SCK	IO	RF_SCK occupied

Pin No.（Internal pin）	Pin Name	I/O	Function Description
1	PF0	IO	Spi nor-Flash CS
2	PF1	IO	Spi nor-Flash SCK
3	PF2	IO	Spi nor-Flash SI/IO0
4	PF3	IO	Spi nor-Flash SO/IO1
5	PF4	IO	Spi nor-Flash WP/IO2
6	PF5	IO	Spi nor-Flash HOLD/IO3
7	PA4	IO	RF_CSB
8	PA6	IO	RF_SDO
9	PC4	IO	RF_GPIO2
10	PC5	IO	RF_GPIO3

3. Chip Frame

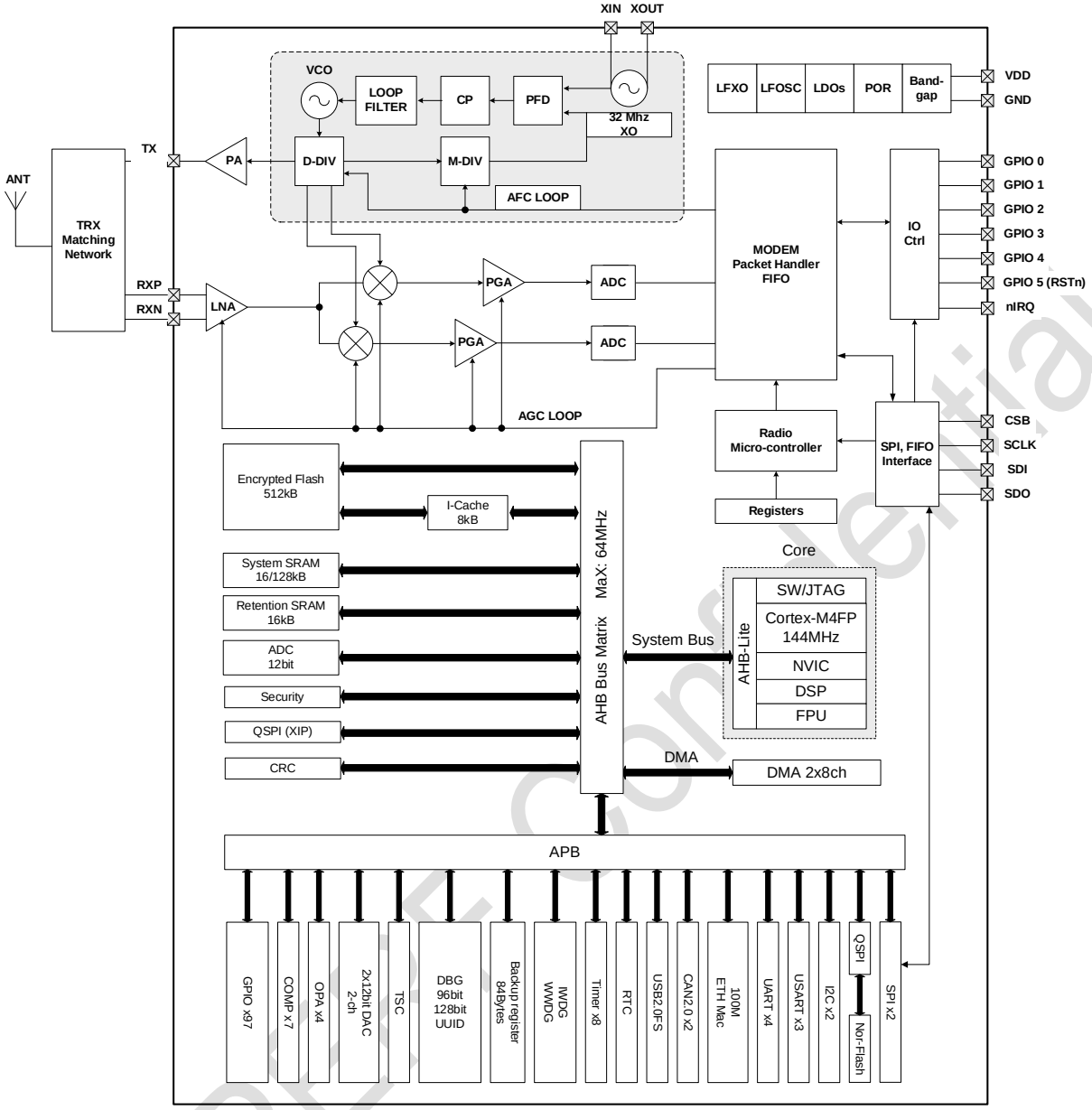


Figure 3-1. Functional Block Diagram

CMT2392F512 is an integrated Sub-G high-performance wireless transceiver single chip. The internal system block diagram of CMT2392F512 is shown in the above figure 3-1.

- **Low power high performance Sub-G transceiver**

Sub-G wireless transceiver supports 113 to 960 MHz, OOK, 2(G)FSK, 4 (G)FSK and other modulation modes, low power consumption, high performance, suitable for all kinds of wireless communication applications. The product belongs to CMOSTEK Next GenRFTM series, which includes a complete product series including transmitters, receivers and transceivers.

- **ARM Cortex-M4FP high performance 32e bit micro-processor**

The CMT2392F512 controller uses a 32-bit ARM Cortex®-M4FP kernel, with a maximum operating frequency of 144MHz, up to 512 KB encrypted Flash memory, and a maximum of 144 KB SRAM. It has a built-in high-speed AHB bus, two low-speed peripherals APB and bus matrix, supports up to 36 general I/Os, provides a wealth of high-performance analog interface, including a 12-bit 4.5 Msps ADC. Besides, it supports up to 11 external input channels, independent operational amplifier, high-speed comparator, and provides a variety of digital communication interfaces, including peripherals of seven U(S)ART, two I2C, two SPI, and one CAN as well as one USB.

CMT2392F512 resources are shown as the following table.

Table 3-1. CMT 2392F512 External Resources

Project Name		CMT2392F512 External Resources	Notes
Flash capacitance (KB)		512	
SRAM capacitance (KB)		128+16	
CPU kernal and frequency		ARM Cortex-M4 @ 144 MHz	
Operating environment		1.8～3.6 V / -40～85℃	
	High level	2	
	General	4	
	Basic	2	
	RTC	Support	
Communication interface	SPI	2	
	QSPI	1	
	I2C	2	
	USART	7	
	CAN	1	
	USB	1	
	Ethernet	1	
GPIO		36+6+6	36 of them completely independent control by the MCU; while RF part and internal nor Flash control 6 respetively
DMA		2 series with 8 channels	
12 bit ADC		11-ch	4.5 Msps
OPA/ COMP		2 / 2	
Algorithmic support		TRNG, AES, DES, SHA, SM1/3/4/7, MD5	
Security protection		Read/write protect (RDP / WRP), Storage encryption	

4. Sub-G Transceiver

4.1 Transmitter

The CMT2392F512 transmitter is based on direct frequency synthesis technology. The carrier is generated by a low noise fractional-N frequency synthesizer. The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written via registers, step by step from -10 dBm to +20 dBm with 1 dB.

In OOK mode, when PA is switched on and off rapidly according to the transmitted data, it is easy to cause spectral spurts and burrs near the carrier. These spurts and burrs can be minimized by a Ramping mechanism. In FSK mode, CMT2392F512 supports signal transmission after Gaussian filtering, namely GFSK, so that the transmission spectrum is more concentrated.

According to different application requirements, users can design a PA matching network to optimize the transmitting efficiency. The transmitter can operate in direct mode and packet mode. In direct mode, the data can be sent to the chip by the DIN pin and transmitted directly. In the packet mode, the data can be pre-loaded into theTX FIFO in STBY state, and transmitted together with other package elements. Data can only be transmitted from FIFO in 4 FSK mode.

4.2 Receiver

CMT2392F512 has a built-in ultra-low power, high performance low-IF OOK, FSK receiver. The RF signal induced by the antenna is amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation. During power on reset (POR) each analog block is calibrated to the internal reference voltage. This allows the chip to remain its best performance at different temperatures and voltages. Baseband filtering and demodulation is done by the digital demodulator. The AGC loop adjust the system gain by the broad band power detector and attenuation network nearby LNA, so as to obtain the best system linearity,selectivity, sensitivity and other performance.

Owing to CMOSTEK's low power design technic, the receiver consumes very low power when it is turned on.The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application with strict requirements of power consumption.

Similar to the transmitter, the CMT2392F512 receiver can operate in direct mode and packet mode. In the direct mode,the demodulator output data can be directly output through the DOUT pin of the chip.DOUT can be assigned to GPIO1/2/3. In the packet mode, the demodulator data output is sent to the data packet handler, get decoded and is filled in the FIFO. MCU can read the FIFO by the SPI interface.

4.3 Power-on Reset (POR)

The Power-On Reset circuit detect the change of the VDD power supply, and generate the reset signal for the entire CMT2392F512 system. After the POR, the MCU must go through the initialization process and re-configure the CMT2380F64. There are two circumstances which will lead to the generation of POR.

The first case is a very short and sudden decrease of VDD. The POR triggering condition is, VDD dramatically decreases by 0.9 V +/- 20% (e.g.0.72 V–1.08 V) within 2 us. To be noticed, it detects a decreasing amplitude of the VDD, not the absolute value of VDD as shown in the below figure.

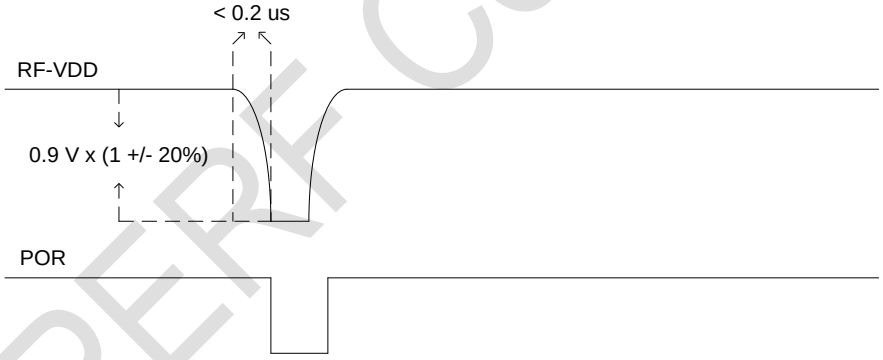


Figure 4-1. POR Reset Causing from Sudden Decreasing

The second case is：a slow decrease of the VDD. The POR triggering conditionis, RF-VDD decreases to 1.45 V+/-20% (e.g.1.16 V–1.74 V) within no less than 2 us. To be noticed, it detects absolute value of RF-VDD rather than decreasing amplitude. This situation is shown as below:

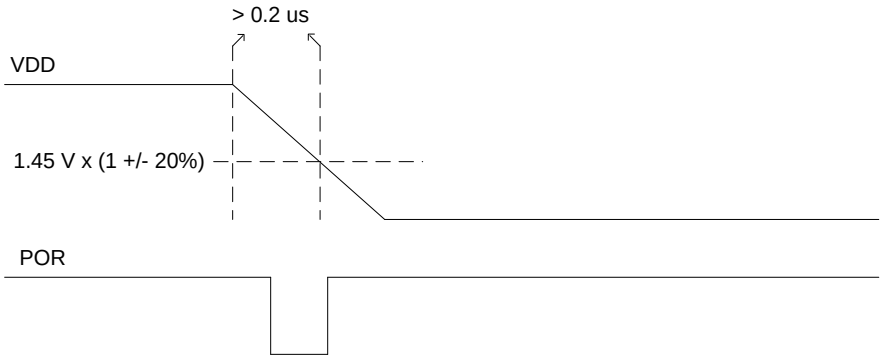


Figure 4-2. POR Reset Causing from Slow Decreasing

4.4 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for the digital circuits. The value of load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL to make the crystal accurately oscillate at 32 MHz.

$$C_L = \frac{C_{on\_chip} + C_{off\_chip} + C_{par}}{2}$$

The Conchip is the Load capacitor mounted to the ground at both ends of the crystal provided inside the CMT2392F512. The Conchip can be configured with the Xtal Cap Load on the RFPDK to be adjustable from 23 to 29 pF, and the step is about 190 fF.

Coffchip is the load capacitor that connects both ends of the external crystal to the ground, which can be chosen by customers whether to increase it or not. Cpar is the parasitic capacitance from both ends of the crystal to the ground, which is about 2 ~ 6 pF. A 12pF loaded crystal oscillator is recommended for use with the CMT2392F512. In addition, the lower the ppm of the crystal, the better the receiver performance.

4.5 Low Power Frequency Oscillator (LPOSC)

The CMT2392F512 RF system integrates a sleep timer driven by a 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer periodically wakes the chip from sleep. When the chip is operating in periodic operation mode, the sleep time can be configured from 62.5 us to 8585740.288 s. Since the frequency of the low power oscillator will drift with temperature and voltage, it will be automatically calibrated during the power-up phase and will be periodically calibrated. The calibration will keep the frequency tolerance of the oscillator within 1%.

4.6 Internal Low Power Detection

The chip sets up low voltage detection. When the chip is tuned to a certain frequency, the test is performed once. Frequency tuning occurs when the chip jumps from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The result can be read by the LBD_DATA register.

4.7 Received Signal Strength Indicator (RSSI)

RSSI is used to evaluate the signal strength inside the channel with detection range from –127dBm to 20 dBm. Users can configure the RSSI Detect Mode in RFPDK to choose whether to output the RSSI value in real time or to lock the RSSI value at each stage when receive data packets.

CMT2392F512 allows users to setup a threshold RSSI Compare TH in RFPDK to compare with the real-time RSSI value. If the RSSI is larger than the threshold it outputs logic 1, otherwise, it outputs logic 0. The results can be output to RSSI VLD interrupt and to assist the operation of internal super-low power (SLP) mode.

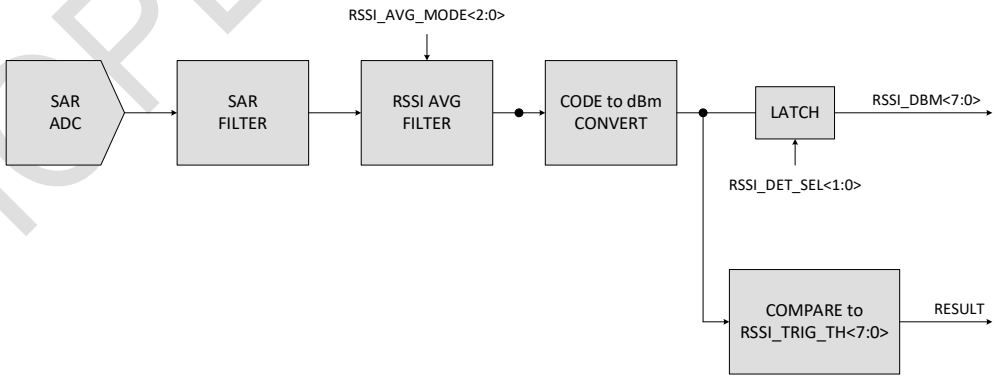


Figure 4-3. RSSI Measurement and Comparison Circuit

CMT2392F512 has done a certain degree of calibration before delivery. To obtain more accurate RSSI measurement results, users need to recalibrate the RSSI circuit in their dedicated applications.

4.8 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in 2-FSK demodulation, it can automatically observe the phase jump characteristics of the received signal to identify whether it is a wanted signal or an unwanted noise. OOK and 4-FSK demodulation do not support this function.

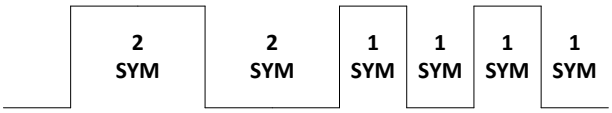


Figure 4-4. Received Signal Jump Diagram

The PJD mechanism defines that the input signal switching from 0 to 1 or from 1 to 0 is a phase jump. Users can configure the PJD_WIN_SEL<1:0> to determine the number of detected jumps for the PJD to identify a wanted signal. As shown in the above figure, although 8 symbols are received, only 6 phase jumps appeared 6. Therefore, the number of jumps is not equal to the number of symbols. Only when preamble is received, the jumps and signal numbers are equal. In general, the more jumps are used to identify the signal, the more reliable the result is; the less jumps are used, the faster the result is obtained. If the RX timeis set to are latively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps will achieve reliable result, e.g. the chip will not mistakenly treat an incoming noise as a wanted signal, and vice versa.

Detecting the phase jump of a signal, is identical to detect whether the signal is the expected data rate. In fact, at the same time, the PJD will also detect the FSK deviation and see if it is valid, as well as to see if the SNR is over 7 dB. According to detect result of the data rate and the Deviation as well as SNR, if it is detected as a reliable signal, it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, or the receive time extending condition in thesuper low power (SLP) mode. In direct data mode, by setting the DOUT_MUTE register bit to 1, the PJD can mute the FSK demodulated data output while there is not wanted signal received.

The PJD technique is similar to the traditional carrier sense technique, while more reliable. When users combine the RSSI detection and PJD technique, they can precisely identify the status of the current channel.

4.9 Clock Data Recovery（CDR）

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate, while receiving the data. Not only for decoding inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data. So CDR's task is simple and important. If the recovered clock frequency is in error with the actual symbol rate, it will cause data acquisition errors at the time of reception.

CMT2392F512 has designed three types of CDR systems, which is shown as followed:

- **COUNTING system** – The system is designed for the symbol rates to be more accurate. If the symbol rate is100% aligned, the unlimited length of 0 can be received continuously without error.
- **TRACING system** – The system is designed to correct the symbol rate error. It has the tracking function. It can automatically detect the symbol rate transmitted byTX, and adjust quickly the local symbol rate of RX at the sametime, so as to minimize the error between them. The system can withstand up to 15.6% symbol rate error. Other similar products in the industry cannot reach this level.
- **MANCHESTER system**–This system evolves from the COUNTING system. The basic feature is the same. The only difference is that the system is specially designed for Manchester codec. Special processing can be done when the TX symbol rate has unexpected changes

4.10 Fast Frequncy Hopping

The mechanism of fast frequency hopping is based on the frequency configured on the RFPDK, for instance, the MCU can simply set 1 or 2 registers to quickly switch to another frequency points during applications at 433.92 MHz. This simplifies the way of change the RX or TX frequency in multiple channels application.

$$\mathbf{FREQ = Base\ Freq + 1\ kHz \times FH\_OFFSET<7:0> \times FH\_CHANNEL<7:0>}$$

In general, users can configure FH_OFFSET<7:0> during the chip initialization process. And then in the application, users can switch the channel by changing FH_CHANNEL<7:0>.

4.11 Chip Operation

4.11.1 SPI Interface

The chip communicates with the outside through the 4-wire SPI interface (FCSB、CSB、SDA、SCLK). It is defaulted set as 4-wire SPI and then configured as 3-wire after power on. The CSB is the active-low chip select signal for accessing to the registers.

The SCLK is the serial clock. Its highest speed is 10 MHz.The chip itself and the external MCU send the data at the falling edge of SCLK and capture the data at the rising edge. The SDI is for data input and SDO is for data output. In 3-wire mode, SDI is used for both data input and output, and SDO is idle. Both the address and data parts are transmitted from the MSB.

When accessing to the register, CSB is pulled low. A R/W bit is sent first, followed by a 7-bit register address. After the external MCU pulls down the CSB, it must wait for at least half a SCLK cycle, and then send the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle, and then pull the CSB high.

Noted that for the 4-wire register write operation below, while SDI writes data, SDO will output the current value of the register (old register read data), and the MCU can decide whether to read it as needed.

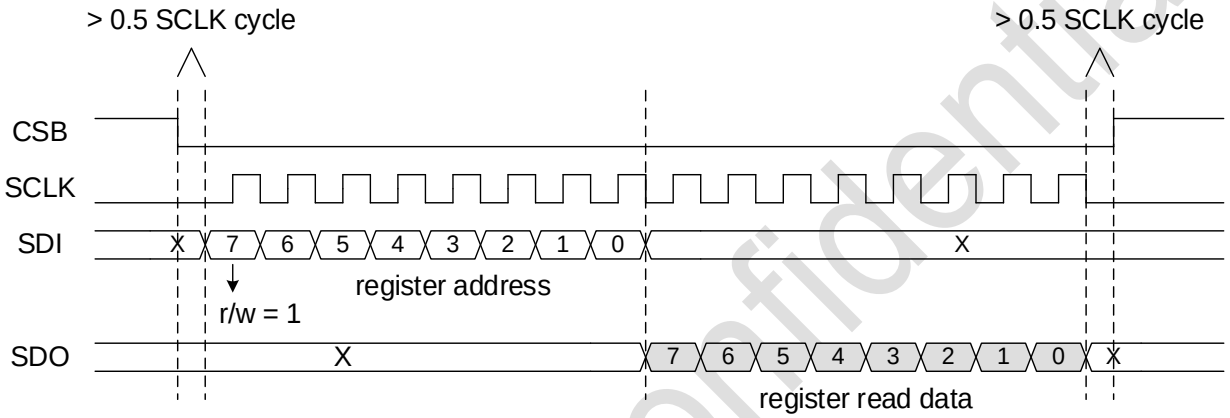


Figure 4-11-1. SPI Read Register Timing

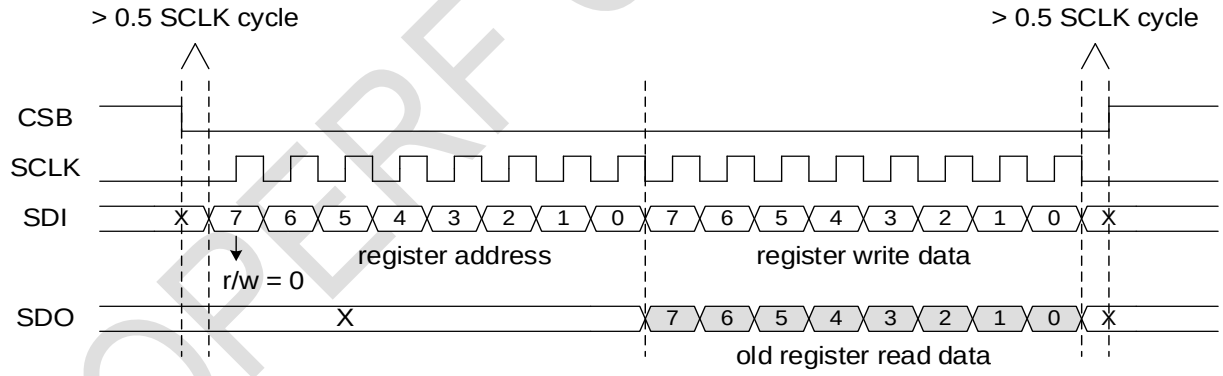


Figure 4-11-2. SPI Write Register Timing

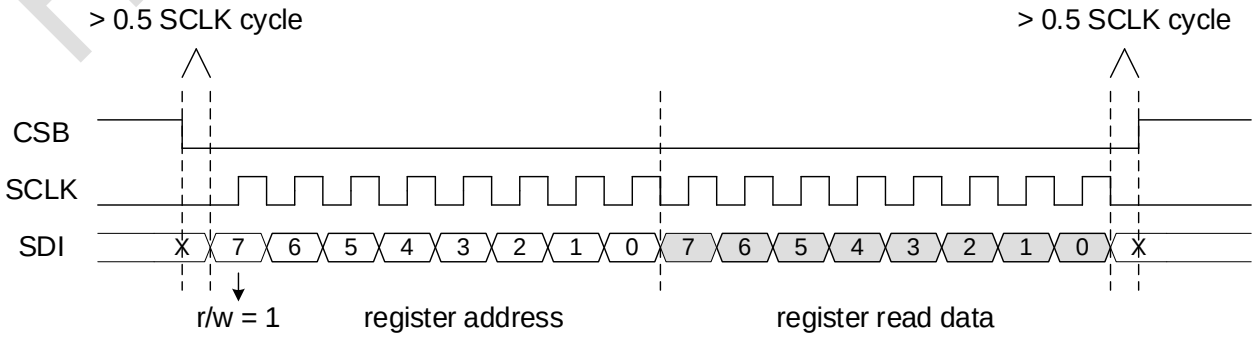


Figure 4-11-3. SPI (3-wire) Read Register Timing

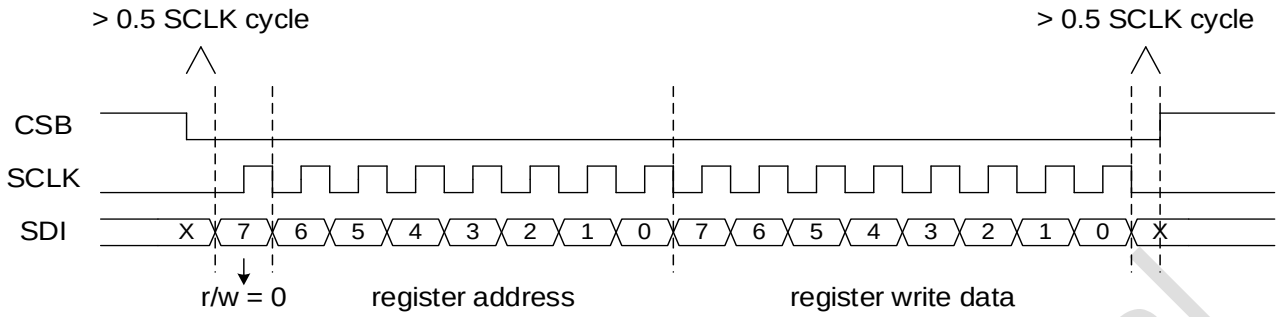


Figure 4-11-4. SPI (3-wire) Write Register Timing

For 3-wire read register, both MCU and CMT2392F512 will switch the IO (SDIO) port between address 0 and 7. At this point, CMT2392F512 will switch the IO port from input to output, and MCU will switch the IO port from output to input. Please note the dotted line in the middle. It is strongly recommended that MCU switch the IO port to input before sending out the falling edge of SCLK. The CMT2392F512 does not switch IO to output until a falling edge happened. This avoids the situation when both of the MCU and CMT2392F512 sets SDIO to output at the same time, which will result in electrical conflict. For some MCUs, this may cause a reset or other abnormal behavior.

4.11.2 FIFO Interface

CMT2392F512 provides two separated 128-byte FIFO by defaul for RX and TX respectively. RX FIFO is used to store the received data in RX mode and TX FIFO is used to store the transmitting data in TX mode. Users can also set FIFO_MARGE_EN to1 to merge the two separated FIFO into one 256-byte FIFO. It can be used both underTX and RX. By configuring the FIFO_RX_TX_SEL to indicate whether it is currently used as TX FIFO or RX FIFO. When the two FIFO are not merged, users can fill in the next time 128 byte TX FIFO while the 128 byte RX FIFO is filled in the RX mode to save operation time.

FIFO can be accessed via the SPI interface. Users can clear FIFO by setting FIFO_CLR_TX or FIFO_CLR_RX. Also, users can re-send the old data in FIFO_RESTORE without re-filling the data.

Users can configure PD_FIFO to control whether the FIFO saves content in the SLEEP mode. PD_FIFO = 0 means that FIFO can save contents in SLEEP state, but it will consume about 200 nA of leakage current.

When MCU accesses FIFO, users must first configure a few registers to set up the FIFO read/write mode, as well as some other working mode. Below is the read-write timing diagram. The FIFO operation is triggered by writing address 0x7A of Page 0. When r/w bit is 0, the FIFO operation is written, and when R/W bit is 1, the FIFO operation is read.

FIFO read and write can also be operated by using 3-wire SPI. When in 3-wire, read data output and write data input are carried out on the SDI pin. When in 4-wire, write data is input from SDI and read data is output from SDO. The FIFO operation process is to access the FIFO operation port at address 0x7A, where the read and write bits determine whether to write or read data at the following. For the following continuous read or write phase, it is up to users.

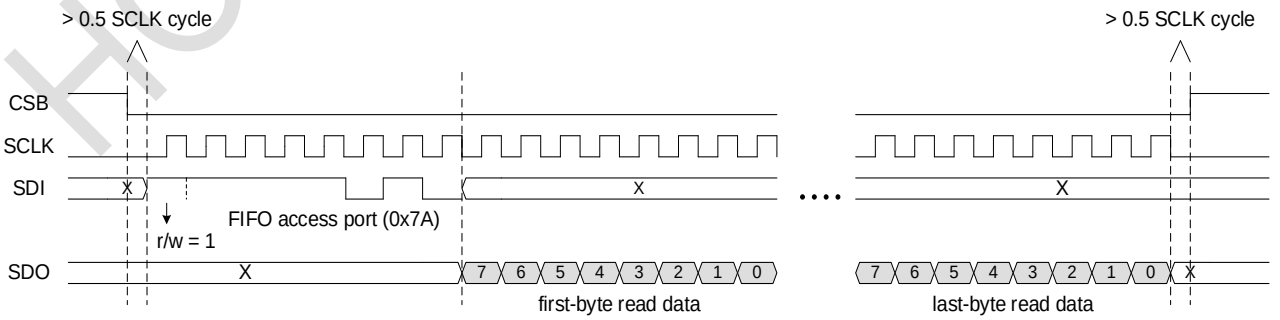


Figure 4-11-5. SPI (4-wire) Read FIFO Timing

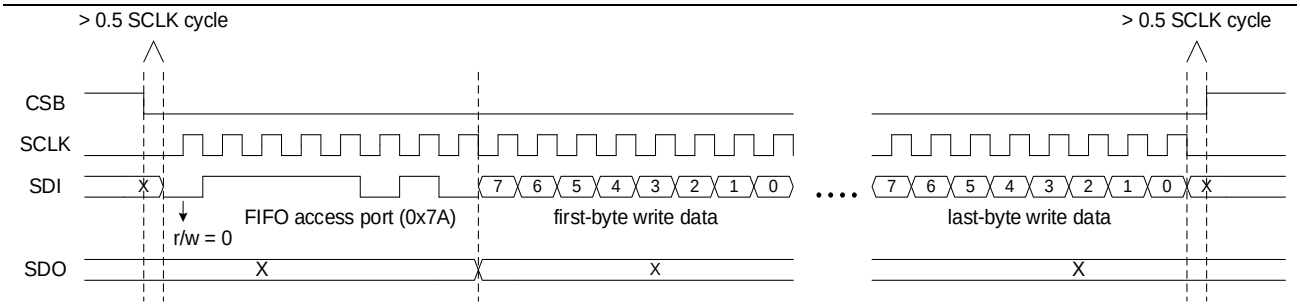


Figure 4-11-6. SPI (4-wire) Write FIFO Timing

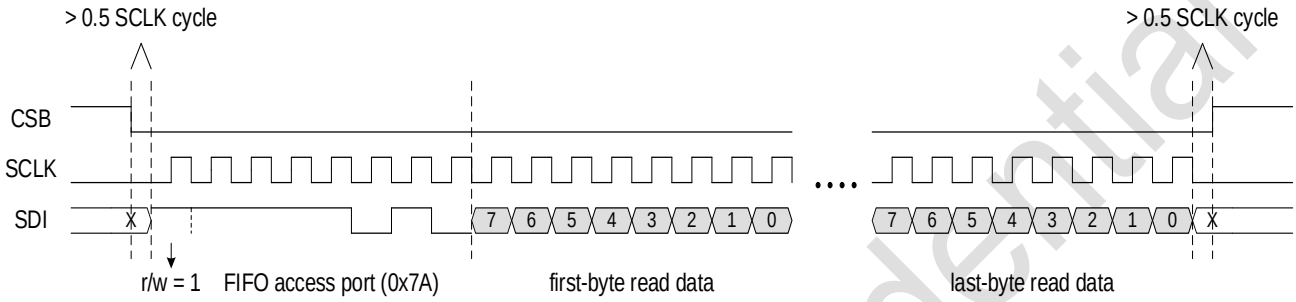


Figure 4-11-7. SPI (3-wire) Read FIFO Timing

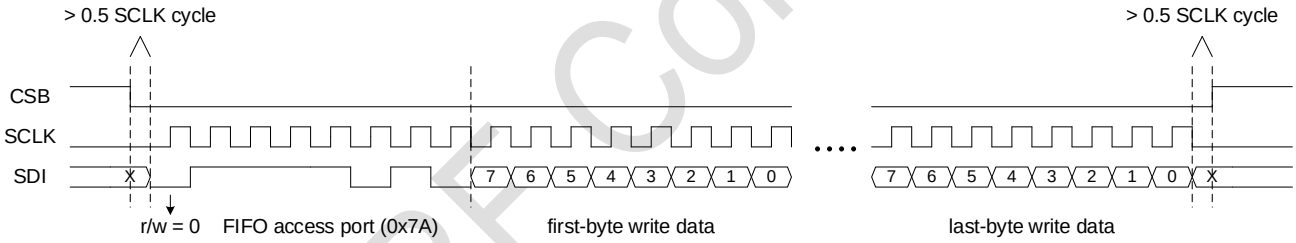


Figure 4-11-8. SPI (3-wire) Write FIFO Timing

Transceivers provide a numbers of FIFO related interrupt sources as auxiliary tools for efficient chip operation. The FIFO interrupt timing sequence related to Rx and Tx is shown in the figure below.

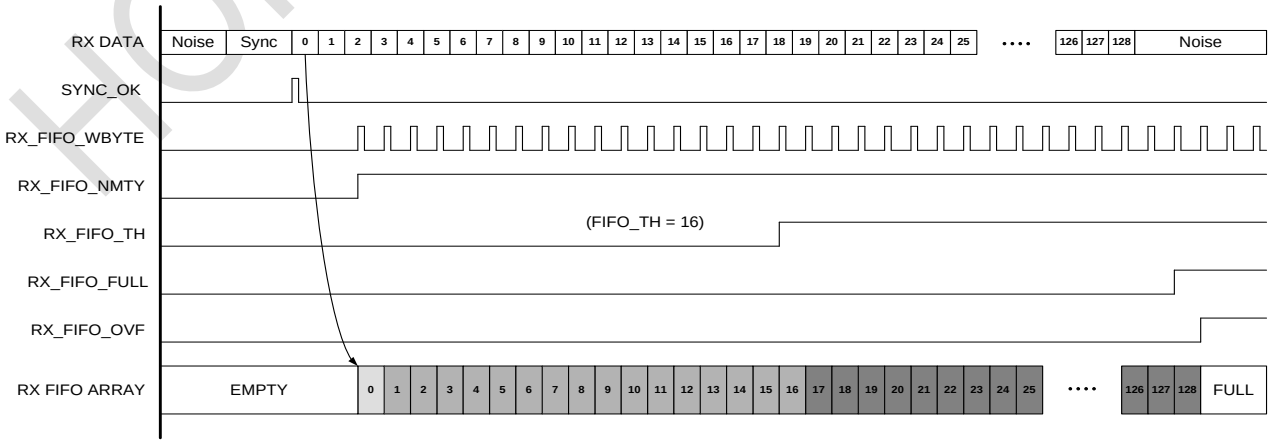


Figure 4-11-9. Transceiver RX FIFO Interrupt Sequence Diagram

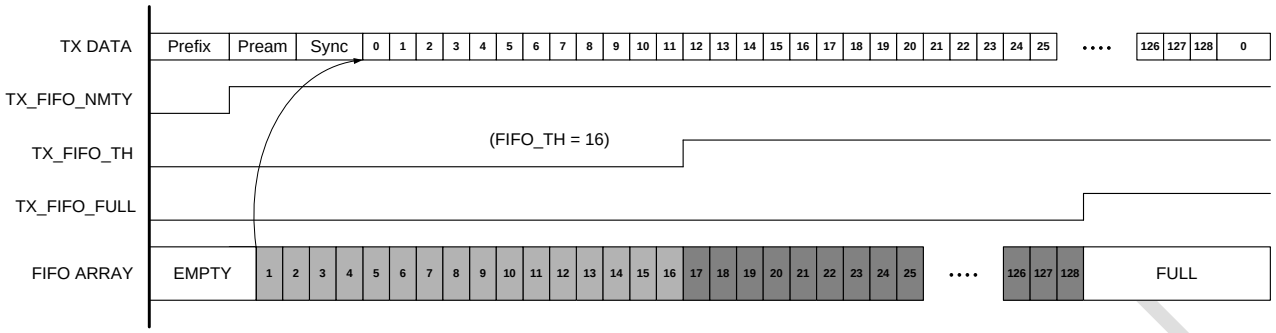


Figure 4-11-10. Transceiver TX FIFO Interrupt Sequence Diagram

4.11.3 Transceiver Working Status, Timing and Power Consumption

- Startup time

After the transceiver is powered on RF-VDD, it usually needs to wait for about 1ms until POR released. After the RELEASE of POR, the crystal will also start. Users will set the power_up command and the chip will leave IDLE and start to do the calibration of each module. After the calibration, the chip will stay in SLEEP, waiting for the user to initialize the chip. The chip returns to IDLE and starts the power-on process again.

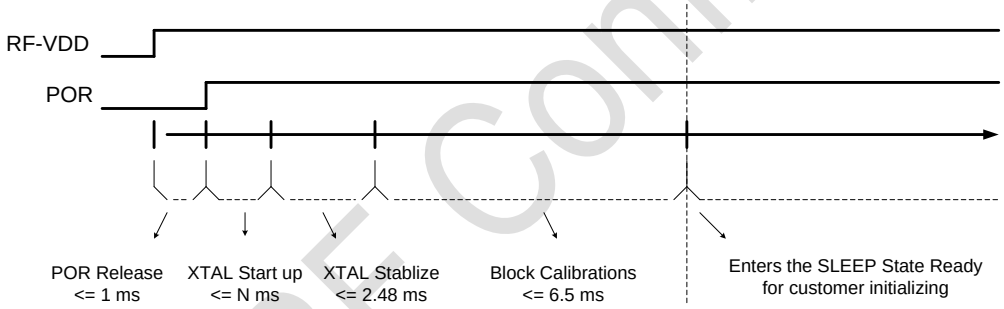


Figure 4-11-11. Power On Timing

The chip enters SLEEP state after calibration. And then, the MCU can control the chip to switch to different operation states through setting the register CHIP_MODE_SWT<7:0>.

- Operation State

CMT2392F512 has 7 operation states: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as shown below.

Table 4-11-1. Transceiver State and Corresponding Active Module

State	Binary code	Switch command	Active module	Optional module
IDLE	0x00	soft_rst	SPI, POR	None
SLEEP	0x81	go_sleep	SPI, POR	LFOSC, FIFO, Sleep Timer
READY	0x82	go_ready	SPI, POR, XTAL, FIFO	None
RFS	0x84	go_rfs	SPI, POR, XTAL, PLL, FIFO	None
TFS	0x88	go_tfs	SPI, POR, XTAL, PLL, FIFO	None
RX	0x90	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+ADC, FIFO	RX Timer
TX	0xA0	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	None

The following table lists the time it takes to switch states, with the starting states listed on the left:

Table 4-2. Transceiver State and State Switching Time

	Ideal State					
Starting State	**SLEEP**	**READY**	**RFS**	**RX**	**TFS**	**TX**
SLEEP		660 us	770 us	820 us	770 us	820 us
READY	Immediately		110 us	160 us	110 us	160 us
RFS	Immediately	Immediately		20 us	Cannot switch	Cannot switch
RX	Immediately	Immediately	Immediately		Cannot switch	160 us
TFS	Immediately	Immediately	Cannot switch	Cannot switch		20 us
TX	Immediately	Immediately	Cannot switch	160 us	Immediately	

Note：

In Direct mode, if the chip is in transmission, it will exit TX state as it receives command of switching.
In Packet mode, if the chip is in transmission, it will exit TX state after transmission complete must complete.

Below shows the state switching diagram and status signal：

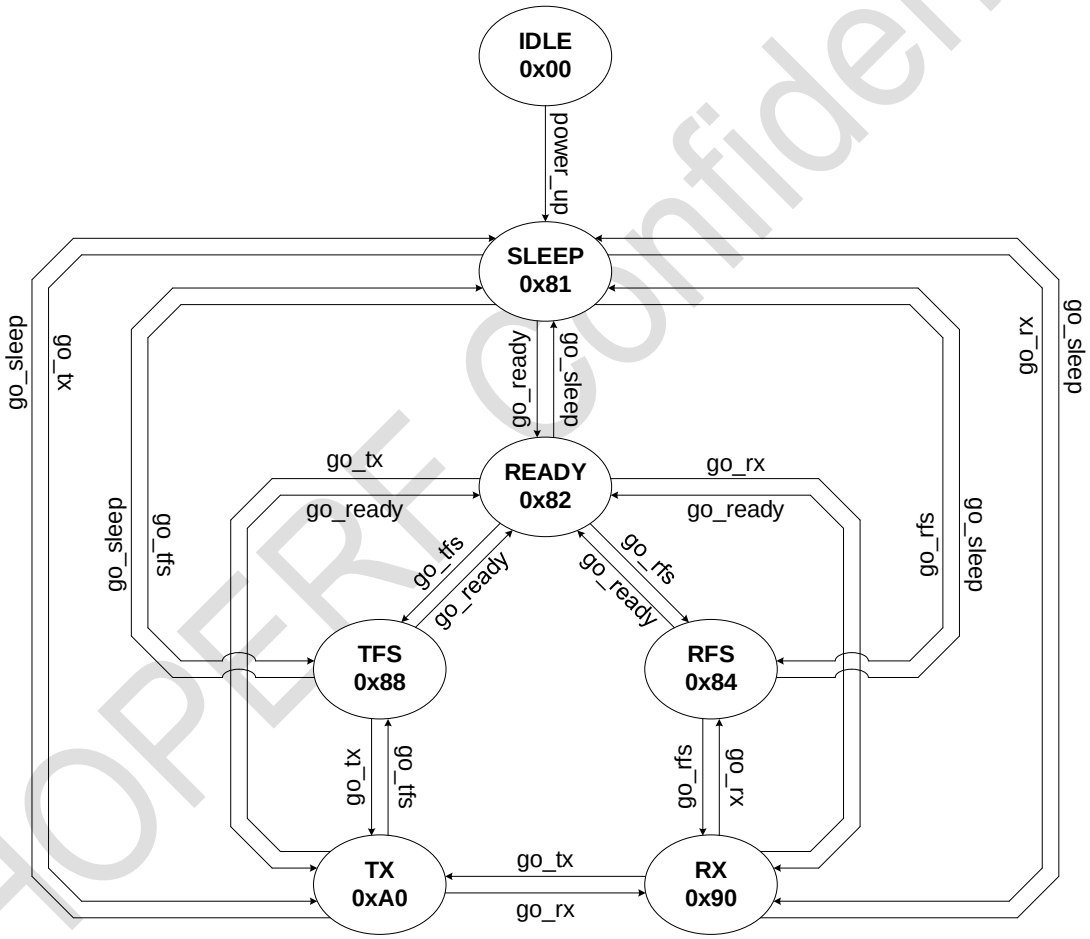


Figure 4-11-12. State Switch Diagram

➢ SLEEP State

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. SPI is open, the registers of the configuration bank and control bank 1 will be saved, and the contents filled in the FIFO before will remain unchanged. However, users cannot operate the FIFO and cannot change the contents of the register. If the user opens the wake-up function, the LFOSC and the sleep counter will turn on and start working. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.。

➢ RFS State

RFS is a transition state before switching to RX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the RX frequency, RFS cannot switch to TX. Switching

from STBY to RFS probably requires PLL calibration and stability time of 350 us. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from other state to RFS will be completed immediately.

- **TFS State**

TFS is a transition state before switching to TX. Except that the transmitter RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the TX frequency, TFS cannot switch to RX. Switching from STBY to TFS probably requires PLL calibration and stability time of 350us. Switching from SLEEP to TFS needs to add the crystal start-up and settled time. Switching from other state to TFS will be completed immediately.

- **RX State**

All modules on the receiver will be opened in RX state. Switching from RFS to RX requires only 20 us. Switching from STBY to RX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to RX needs to add the crystal start-up and settled time. TX can be quickly switched to RX by sending go_switch command. Whether the TX and RX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully.

- **TX State**

All modules on the transmitter will be opened in TX state. Switching from TFS to TX requires only 20 us. Switching from STBY to TX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to TX needs to add the crystal start-up and settled time. RX can be quickly switched to TX by sending go_switch command. Whether the RX and TX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully.

4.11.4 GPIO Function and Interrupt Mapping

CMT2392F512 has 7 GPIO ports（GPIO0～GPIO5 and NIRQ）. Each GPIO can be configured as a different input or output. CMT2392F512 has 3 interrupt ports（INT1、INT2、INT3）. They can be configured to different GPIO mapping output.

Table 4-11-3. CMT2392F512 GPIO Function

Pin No.	Pin Name	I/O	Function
48	GPIO0	IO	Can be configured as：DOUT，INT1，INT2，INT3，DCLK，TRX_SWT
47	GPIO1	IO	Can be configured as：DCLK，INT1，INT2，DOUT，TRX_SWT
12	GPIO2	IO	Can be configured as：INT1，INT2，INT3，DCLK，DOUT，ANTD1
13	GPIO3	IO	Can be configured as：INT1，INT2，DCLK，DOUT，DIN，ANTD2
7	GPIO4	IO	Can be configured as：DOUT，INT1，INT2，DCLK，DIN，CLKO，LFCLKO
8	GPIO5	IO	Can be configured as：RSTn，INT1，INT2，DOUT，DCLK
46	NIRQ	IO	Can be configured as：INT1，INT2，DCLK，DOUT，DIN，TCXO

Below shows the Interrupt mapping. INT 1 and INT 2 mapping is the same. Take INT 1 as an example.

Table 4-11-4. Transeiver Interrupt Mapping

Name	INT1_SEL	Interrupt Descriptions	Clearing Method
INT_MIX	000000	Compounded interrupt, INT_MIX will be valid if any one of the interrupts below is enabled.	Auto/By MCU
ANT_LOCK	000001	Antenna lock interrupt is active after enabling the antenna diversity function.	By MCU
RSSI_PJD_VALID	000010	Interrupt valid for RSSI and/or PJD.	Auto
PREAM_PASS	000011	Successfully receive the Preamble interrupt.	By MCU
SYNC_PASS	000100	Successfully receive the Sync Word interrupt.	By MCU
ADDR_PASS	000101	Successfully receive the Addr interrupt.	By MCU
CRC_PASS	000110	Successfully receive interrupt of passing the CRC check.	By MCU
PKT_OK	000111	Successfully receive interrupt of receiving an entire and correct packet.	By MCU
PKT_DONE	001000	Indicates that the current data packet has been received with the following 4 cases. 1. A complete and correct packet is received. 2. Manchester decoding error occurs and the decoding circuit restarts automatically. 3. NODE ID receiving error occurs and the decoding circuit restarts automatically. 4. A signal conflict is found and the decoding circuit does not	By MCU

Name	INT1_SEL	Interrupt Descriptions	Clearing Method
		restart automatically but waits for the MCU to process.	
SLEEP_TMO	001001	Interrupt indicating SLEEP timer timeout.	By MCU
RX_TMO	001010	Interrupt indicating RX timer timeout.	By MCU
RX_FIFO_NMTY	001011	Interrupt indicating RX FIFO is not full.	Auto
RX_FIFO_TH	001100	Interrupt indicating the unread content of RX FIFO exceeding FIFO TH.	Auto
RX_FIFO_FULL	001101	Interrupt indicating RX FIFO is full	Auto
RX_FIFO_WBYTE	001110	Interrupt generated every time a BYTE is written into RX FIFO, i.e., it is a pulse.	Auto
RX_FIFO_OVF	001111	Interrupt indicating RX FIFO is overflow	Auto
TX_DONE	010000	Interrupt indicating TX complete.	By MCU
TX_FIFO_NMTY	010001	Interrupt indicating TX FIFO is not full.	Auto
TX_FIFO_TH	010010	Interrupt indicating the unread content of TX FIFO exceeding FIFO TH.	Auto
TX_FIFO_FULL	010011	Interrupt indicating TX FIFO is full.	Auto
STATE_IS_READY	010100	Interrupt indicating that the current state is READY.	Auto
STATE_IS_FS	010101	Interrupt indicating that the current state is RFS or TFS.	Auto
STATE_IS_RX	010110	Interrupt indicating that the current state is RX.	Auto
STATE_IS_TX	010111	Interrupt indicating that the current state is TX.	Auto
LBD_STATUS	011000	Interrupt indicating that low voltage detection being active (VDD is lower than the set TH).	By MCU
API_CMD_FAILED	011001	Interrupt indicating API command execution error.	By MCU
API_DONE	011010	Interrupt indicating API command completion.	By MCU
TX_DC_DONE	011011	Interrupt for Duty Cycle TX mode complete	By MCU
ACK_RECV_FAILED	011100	Interrupt indicating ACK receiving failure.	By MCU
TX_RESEND_DONE	011111	Interrupt for repeated TX complete	By MCU
NACK_RECV	011110	Interrupt indicating receipt of NACK.	By MCU
SEQ_MATCH	011111	Interrupt indicating successful serial number matching.	By MCU
CSMA_DONE	100000	Interrupt for CSMA complete	By MCU
CCA_STATUS	100001	Signal channel sensing interrupt.	By MCU

Interrupt is enabled when register value is 1 by default. Users can set the INT_POLAR register bit to 1 to make all interrupts enabled when the register value is 0. Take INT1 as an example, the control and selection of two different types of interrupt sources is shown in the figure below. The control and mapping ofINT1 and INT2 is the same and both can be mapped to any GPIO.INT_MIX is the only source for INT3, which can only be mapped to GPIO0 and GPIO2. In application, users can choose either to map all interrupt sources to the interrupt port through INT_MIX (identify which interrupt is valid by checking the interrupt flag) or directly map a specific interrupt source to the interrupt port.

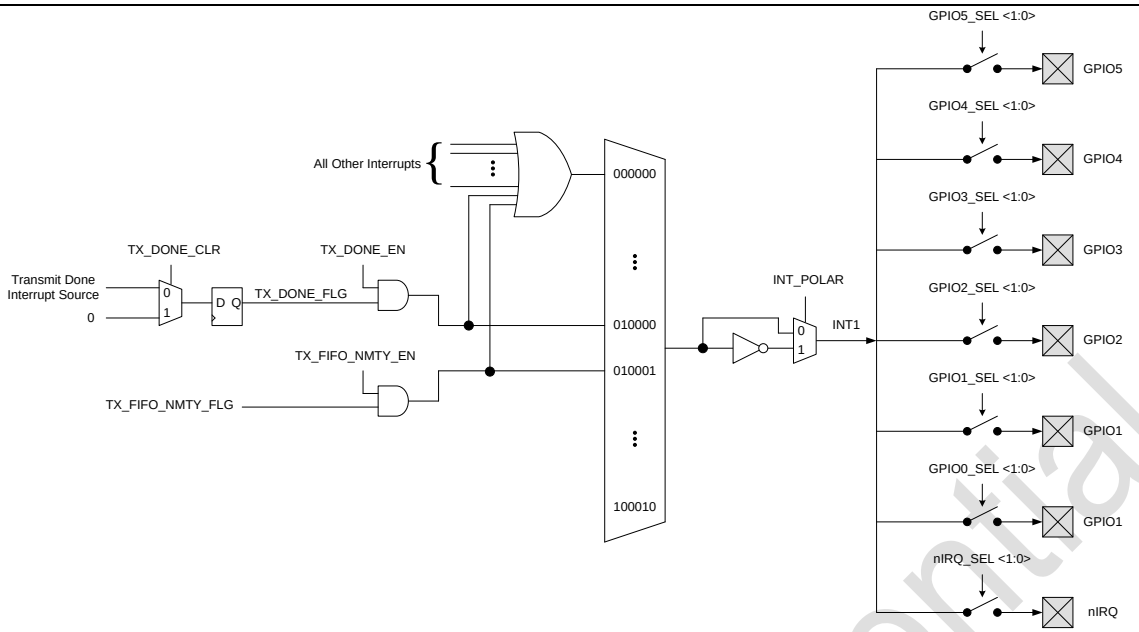


Figure 4-11-13. CMT2392F512 INT 1 Interrupt Mapping

5. Controller Function

5.1 Flash Memory

CMT2392F512 includes embedded encrypted flash memory (Flash) and embedded SRAM, Figure 5-1-1 below shows the memory address map.

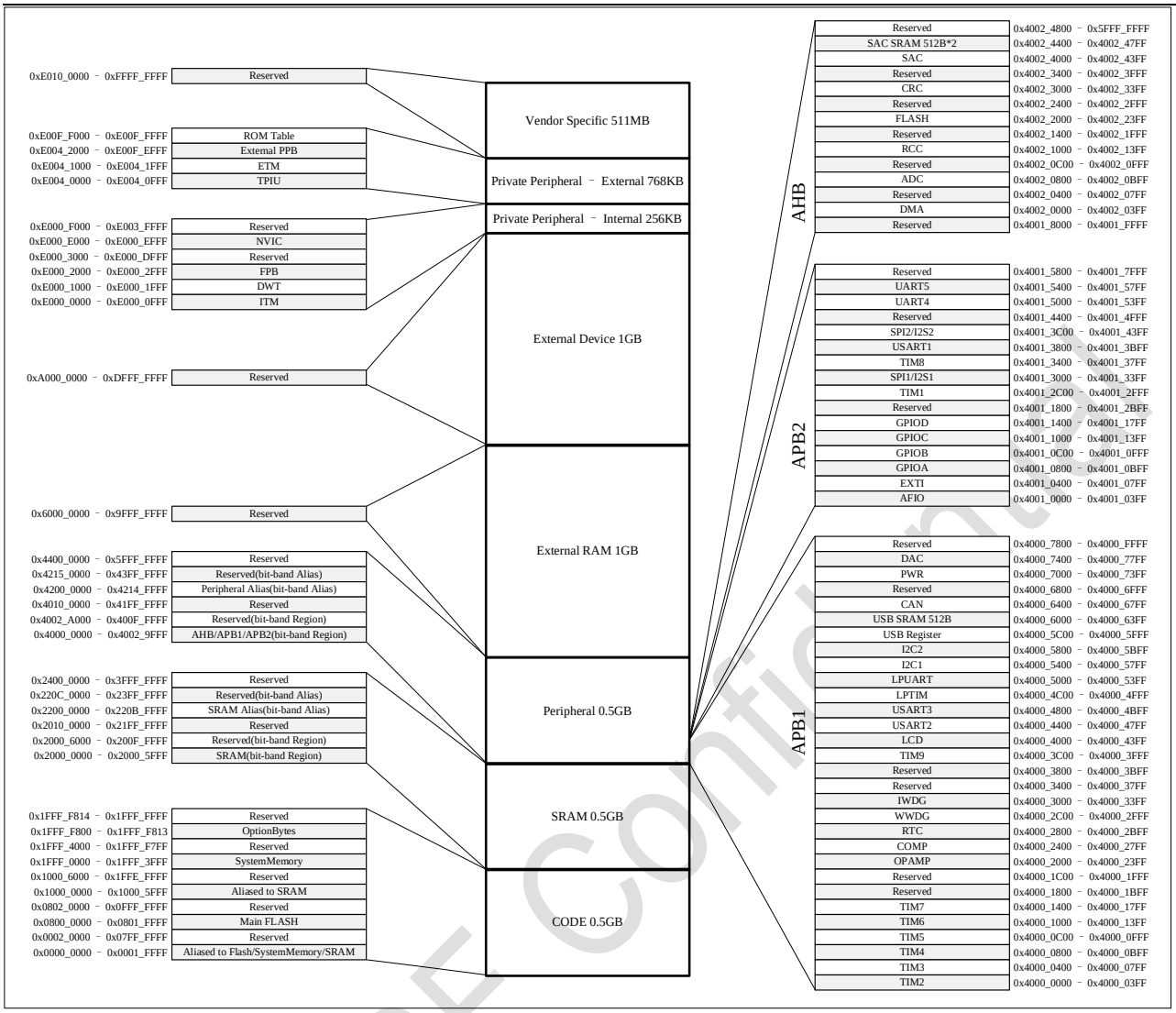


Figure 5-1-1. Memory Address Map

5.1.1 Embedded Flash Memory

Integrated from 256K to 512K bytes embedded encryption FLASH, used to store programs and data, page size of 2Kbyte, supporting page erasing, word writing, word reading, half word reading, byte reading operations. Support user partition management, can be divided into a maximum of three user partitions, different users cannot access each other's data (only executable code).

5.1.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 144K bytes, including SRAM and R-SRAM. The maximum size of SRAM1 is 16K bytes, and that of SRAM2 is 8K bytes. In STOP2 mode, SRAM1 and SRAM2 can retain data. While in STANDBY mode, only SRAM2 can retain data.

5.1.3 Nested Vector Interrupt Controller (NVIC)

Built-in nested vector interrupt controller, capable of handling up to 86 maskable interrupt channels (not including the 16 Cortex™-M4F interrupts) and 16 priorities.

- Tightly coupled NVIC enables low latency interrupt response processing
- Interrupt vector entry address directly into the kernel
- Tightly coupled NVIC interface
- Allows early handling of interrupts
- Handles late arriving higher-priority interrupts

- Support interrupt tail link function
- Automatically saves processor state
- Automatically resumes when the interrupt returns with no additional instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

5.2 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains 22 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its triggering event (rising edge or falling edge or bilateral edge) and can be individually shielded. There is a suspended register that maintains the state of all interrupt requests. EXTI can detect clock cycles with pulse widths smaller than internal APB2. Up to 64 universal I/O ports are connected to 16 external interrupts.

5.3 Clock System

The device provides a variety of clocks for users to choose from, including internal high speed RC oscillator HSI (16MHz), internal multi-speed clock MSI (100K~4MHz configurable), internal low speed clock LSI (40KHz), external high speed clock HSE (4MHz~32MHz), external low speed clock LSE (32.768KHz), PLL.

During reset, the internal MSI clock is set as the default CPU clock, and then the user can choose the external HSE clock with failure monitoring function. When an external clock failure is detected, it will be isolated, the system will automatically switch to MSI, and if interrupts are enabled, the software can receive the corresponding interrupt. Also, complete interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).

MSI clock can be used to wake up quickly and execute instructions in STOP2 state, or provide clock for the system in low power operation state, and some other scenarios with low clock accuracy and high power consumption requirements.

The built-in clock security system detects whether the external HSE or LSE fails in real time. If the external clock fails, the system automatically switches to the internal clock and generates an interrupt alarm. Multiple prescalers are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1) regions. AHB has a maximum frequency of 64MHz, APB2 has a maximum frequency of 32MHz and APB1 has a maximum frequency of 16MHz.

When using USB function, both HSE and PLL must be used and the CPU frequency must be 48MHz.

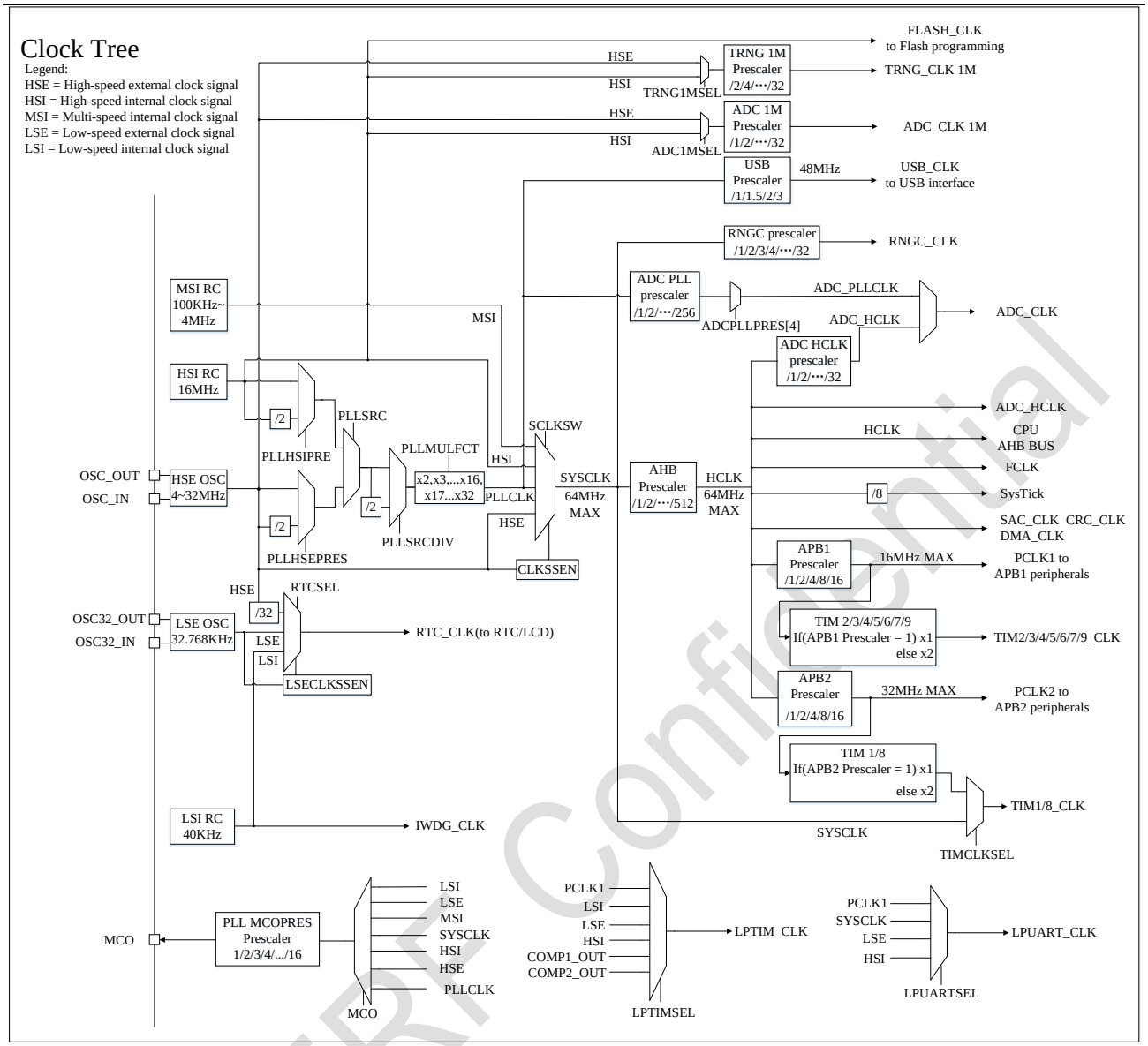


Figure 5-3-1. Clock Tree

5.4 Boot Mode

At BOOT time, the BOOT mode after reset can be selected with the BOOT0 pin and option byte BOOT configuration (USER2):

- Boot from program FLASH memory
- Boot from system memory
- Boot from internal SRAM

The Bootloader is stored in the system memory and can program the flash memory through USART1 or USB interface.

5.5 Power Supply Scheme

- VDD = 1.8~3.6V： The VDD pin supplies power to the I/O pin and the internal voltage regulator.
- VSSA，VDDA = 1.8~3.6V: provides power supply for ADC, DAC, OPAMP, COMP and TSC. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.

5.6 Programmable Voltage Detector

The device intigrates power on reset (POR) and power down reset (PDR) circuits, which are always in working state to ensure the power supply exceeds 1.8V. When VDD is under threshold (VPOR/PDR), the device is in the reset state without the need to use an external reset circuit. There is a programmable voltage monitor (PVD) in the device, which monitors the VDD/VDDA power supply and compares it to the threshold VPVD. When the VDD below or above the threshold VPVD, an interrupt occured with a warning message. The PVD function needs to be enabled through program.

5.7 Voltage Regulator

The voltage regulator has 3 control modes: Master mode（MR）, Low power mode (LPR), Shutdown mode

- Master mode（MR），MCU runs in normal modes
- Low power mode (LPR), MCU runs in STOP2, and STANDBY mode: The output of the regulator is in high resistance state and power supply of core circuit is cut off, the regulator is in no consumption state (the data of registers and SRAM will be lost).
- Shutdown mode, MCU runs in STOP2 and STANDBY mode：The output of the regulator is in high resistance state and power supply of core circuit is cut off, the regulator is in no consumption state (the data of registers and SRAM will be lost).

The voltage regulator is always in master mode after the MCU reset, while shutdown in STANDBY mode in high resistance output state.

5.8 Low Power Mode

CMT2392F512 supports five low-power modes.

- SLEEP mode

In SLEEP mode, only MCU stop, all peripherals are configurable and can wake up the MCU when an interrupt/event occurs.

- STOP0 mode

Based on the Cortex-M4F deep sleep mode, the STOP0 mode achieves low power consumption while keeping SRAM and register contents intact. In STOP0 mode, the clock in main power domain stopped, the PLL, HSI RC oscillator and HSE crystal oscillator are turned off, and the main regulator MR can be placed in normal mode or low power mode.

Wake up: The microcontroller can be awakened from STOP0 mode by any of the signals configured as EXTI, EXTI signals can be 16 external EXTI signals (I/O related), PVD output, RTC wake up, RTC clock, touch wake up, ETH MAC wake up from ETH PHY, or USB wake up signals. 16K bytes of R-SRAM are retained, and other SRAM and register data are lost. 84 bytes backup register hold.

- STOP2 mode

STOP2 mode is based on the Cortex®-M4F deep sleep mode, and all the core digital logic areas are powered off. Main voltage regulator (MR) is off, HSE/HSI/PLL is off. MCU register retention, LSE/LSI optional work, all GPIO retention, peripheral I/O multiplexing function is not maintained.

Wakeup: The microcontroller can be woken up from STOP2 mode by any signal configured as EXTI, which can be 16 external EXTI signals (I/O related), PVD output, RTC wakeup, RTC clock, or touch wakeup.

- STANDBY mode

In STANDBY mode, the current consumption is low. Internal voltage regulator is turned off, PLL, HSI RC oscillator and HSE crystal oscillator are also turned off. After entering STANDBY mode, the register content will be lost, while contents of the backup register will still be retained, R-SRAM can be retained, and the standby circuit will still work.

- VBAT mode

MCU will enter into VBAT mode at anytime once the VDD is off. Most of the I/O pins are in a high resistance state except for NRST, PA0-WKUP, PC13_TAMPER, PC14, and PC1 under VBAT mode.

Note: RTC, IWDG, and the corresponding clock can not be stopped when entering shutdown or standby mode.

5.9 Direct Memory Access（DMA）

The device integrates 2 flexible general-purpose DMA controllers that supports eight DMA channels to manage data transfers from memory to memory, peripherals to memory, and memory to peripherals. 2 DMA controller support the management of ring buffers, avoiding interruptions when controller transfers reach the end of the buffer.
Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.
DMA can be used with major peripherals: SPI, I2C, USART, TIMx (general, basic and advanced timers), DAC, I2S, ADC and DVP.
Note:

5.10 Real Time Clock（RTC）

RTC is a set of continuously running counters with a built-in calendar clock module that provides a perpetual calendar function, as well as alarm interrupt and periodic interrupt (minimum 2 clock cycles) functions. RTC can be powered by VDD or VBAT pin,

select VDD power supply when VDD is effective, otherwise select VBAT pin, automatically selected and switched by the hardware. RTC will not be reset by the system or power reset source, nor will it be reset when it wakes up from STANDBY mode.

The RTC can be driven by either a 32.768kHz external crystal oscillator, an internal low-power 40kHz RC oscillator, or a high-speed external clock with 128 frequency divisions. For application scenarios requiring very high timing accuracy, it is recommended to use an external 32.768kHz clock as the clock source. Meanwhile, to compensate for the clock deviation of natural crystal, a 512Hz signal can be output to calibrate the clock of RTC. The RTC has a 22-bit predivider for a time-based clock, which will produce a 1-second long time reference at 32.768kHz by default. In addition, RTC can be used to trigger wake up in low-power mode and wakeup the RTC module on time.

5.11 Timer and Watchdog

Up to 2 advanced control timers, 4 general-purpose timers and 2 basic timers, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 5-1. Comparison of Timer Functions

Timer	Counter resolution	Counter type	Prescaler factor	Generate DMA requests	Capture/compare channels	Complementary output
TIM1 TIM8	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	Y
TIM2 TIM3 TIM4 TIM5	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	N
TIM6 TIM7	16	up	Any integer between 1 and 65536	Y	0	N

5.11.1 Basic Timer (TIM6 and TIM7)

Basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter. These two timers are independent of each other and do not share any resources. The basic timer can provide a time reference for general purpose timers, and particularly can provide a clock for a digital-to-analog converter (DAC). The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

- 16-bit auto-reload up-counting counters
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- Generate interrupt/DMA as updating event (with counter overflow)

5.11.2 General-purpose Timer TIMx

The device integrates 4 general-purpose timers (TIM2, TIM3, TIM4 and TIM5) that can work synchronously. The 4 timers are indepently. Each timer has a 16-bit auto-reload counters, a 16-bit programmable prescaler as well as 4 independent channels. Each channel can be used for input capture (for measuring pulse width) , output comparision, PWM and single pulse mode output. The timer can provide up to 16 input capture, output comparison, or PWM channels in the largest package configuration.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- 4 Independent channel:
  - Input capture
  - Output comparision
  - PWM generation (Edge or center alignment mode)
  - Single pulse mode output

- Synchronization circuits that use external signals to control timers and timer interconnections;
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output comparision
- Support for incremental (orthogonal) encoders and Hall sensor circuits for positioning;
- Trigger the input as an external clock or periodic current management

The device can also work with advanced control timers via the timer link function to provide synchronization or event link functionality. In debug mode, counters can be frozen. Any general-purpose timer can be used to generate PWM output. Each timer has its own DMA request mechanism.

5.11.3 Low Power Timer LPTIM

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes except for Standby mode. The clock source can come from a LSE, LSI, internal high-speed clock, or external clock. LPTIM can not only realize the basic timing count, input capture function, but also can be used as a pulse counter, supporting single pulse or quadrature/non-quadrature pulse counting function. Also, the LPTIM can wake up the system from STOP2 low-power modes.

Main features:

- 16-bit up counter
- 3-bit prescaler, 8 kinds of prescale factors (1, 2, 4, 8, 16, 32, 64, 128)
- Multiple clock sources:
  - Internal clock source: LSE, LSI, HSI, COMP1_OUT or APB clock
  - External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for pulse counter applications)
- 16-bit auto-load register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous or one-shot trigger mode
- Programmable software or hardware input trigger
- Programmable digital anti-glitch filtering
- Configurable output (square wave, PWM)
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

5.11.4 Advanced control timer (TIM1 and TIM8)

There are two independent advanced timers (TIM1/TIM8), each consists of a 16-bit automatic loading counter driven by a programmable pre-divider. Supports a variety of functions, including measuring the pulse width of the input signal (input capture), or generating the output waveform (output comparison, PWM, complementary PWM output with embedded dead time, etc.). Using timer predivider and RCC clock to control the predivider, the pulse width and waveform period can be adjusted from a few microseconds to a few milliseconds. Each timer is completely independent and does not share any resources with each other.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Supports up to 144MHz as the input clock
- TIM1 and TIM8 up to 6 capture/compare channels:
  - Input capture
  - Ouput compare
  - PWM output (Edge or center alignment mode)
  - One-pulse mode output
- PWM trigger ADC sampling

- The trigger time point is firmware configurable throughout the PWM cycle
- Dead-zone programmable complementary output;
- Use external signals to control timer and timer interconnection synchronization circuit;
- Allows the repeat counter of the timer register to be updated after a specified number of counter cycles;
- The events that generate the interrupt/DMA are as follows:
  - Update event (counter up overflow/down overflow, counter initialization (triggered by software or internal/external);
  - Trigger event (The counter starts, stops, initializes or is internally/externally triggered to count)
  - Input capture
  - Output comparision
  - Break input
- Support for incremental (orthogonal) encoders and Hall sensor circuits for positioning.
- Trigger the input as an external clock or periodic current management
- Hall sensor interface: used to do three-phase motor control

In debug mode, the counter can be frozen while the PWM outputs are disabled, thus cutting off the switches controlled by these outputs. Many of the functions are the same as standard TIM timers, and the internal structure is the same, so advanced control timers can operate in conjunction with TIM timers through the timer link function to provide synchronization or event link functions.

5.11.5 Systick Timer（Systick）

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24 bit down-counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

5.11.6 Watchdog (WDG)

Support for two watchdog: independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

- **Independent watchdog（IWDG）**

The independent watchdog is based on a 12-bit down-counter and a 8-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP0, STOP2 and STANDBY modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

- **Window watchdog（WWDG）**

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the down-counter value is flushed before the T6 bit becomes 0, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit down-counter value (in the control register) is flashed before the down-counter reaches the window register value, then an MCU reset will also occur. This indicates that the down-counter needs to be refreshed in a finite time.

Main features:

- The clock of the window watchdog (WWDG) is driven by the clock after dividing from the APB1 clock frequency.
- Programmable free-running down-counter
- Reset condition:
  - When the down-counter is less than 0x40, a reset occurs (if the watchdog is started)
  - A reset occurs when the down-counter is reloaded outside the window (if the watchdog is started)
  - If the watchdog is enabled and at the same time interrupts are allowed, an early wake up interrupt (EWINT) occurs when the down-counter reach to 0x40, which can be used to reload the counter to avoid WWDG reset

5.12 I²C Bus Interface

The device integrates up to 4 independent I²C bus interfaces, which provide multi-host function and control all I²C bus-specific timing, protocol, arbitration and timing. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, SMBus (System Management Bus) and PMBus (Power Management Bus).

Main features:

- Multi-master function: this module can be used as master device or slave device
- I²C master device function:
  - Generate a clock
  - Generate start and stop signals
- I²C slave device function:
  - Programmable address detection
  - The I²C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode
  - Stop bit detection
- Generate and detect 7-bit/10-bit addresses and broadcast calls
- Support different communication speeds
  - Standard speed (up to 100 kHz)
  - Fast (up to 400 kHz)
  - Fast+ (up to 1MHz)
- Status flags:
  - Transmitter/receiver mode flag
  - Byte transfer complete flag
  - I²C bus busy flag
- Error flags:
  - Arbitration loss in master mode
  - Acknowledge (ACK) fail after address/data transfer
  - Error start or stop condition detected
  - Overrun or underrun when clock extending is disable
- Two interrupt vectors:
  - 1 interrupt for address/data communication success
  - 1 interrupt for an error
- Optional extend clock function
- DMA of single-byte buffers
- Generation or verification of configurable PEC (Packet error detection)
  - In transmit mode, the PEC value can be transmitted as the last byte
  - PEC error check for the last received byte
- SMBus 2.0 compatible
  - Timeout delay for 25ms clock low
  - 10ms accumulates low clock extension time of master device
  - 25ms accumulates low clock extension time of slave device
  - PEC generation/verification of hardware with ACK control
  - Support address resolution protocol (ARP)
- Compatible with the SMBus

5.13 Universal Synchronous/Asynchronous Transceiver（USART）

CMT2392F512 integrates up to 7 serial transceiver interfaces, including 3 universal synchronous/asynchronous transceivers (USART1, USART2 and USART3) and 4 universal asynchronous transceivers (UART4 and UART5, UART6, UART7). All these 7 interfaces provide asynchronous communication, support for IrDA SIR ENDEC transmission codec, multi-processor communication mode, single-wire half-duplex communication mode, and LIN master/slave function.

The communication rate of USART1, UART6, and UART7 interfaces is up to 4.5Mbit/s, and the communication rate of other interfaces is up to 2.25Mbit/s.

The USART1, USART2, and USART3 interfaces have hardware CTS and RTS signal management, ISO7816-compatible smart card mode, and is similar to SPI communication mode, all of which can use DMA operations.

Main features:

- Full duplex, asynchronous communication
- NRZ standard format
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving, up to 4.5 Mbits/s.
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates a 13-bit interrupters and detects 10/11 bit interrupters
- Output clock for synchronous transmission
- IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode
- Smart card simulation function:
  - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3
  - 0.5 and 1.5 stop bits for smart cards
- Single-wire half duplex communication
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer
- Independent transmitter and receiver enable bits
- Detect flag:
  - Receive buffer is full
  - Send buffer empty
  - Transmission complete
- Parity control:
  - Send parity bit
  - Check the received data
- Four error detection flags:
  - Overflow error
  - Noise error
  - Frame error
  - Parity error
- 10 USART interrupt sources with flags:
  - CTS change
  - LIN break detection
  - Send data register empty
  - Send complete
  - Received data register is full
  - Bus was detected to be idle
  - Overflow error
  - Frame error

- Noise error
- Parity error

- Multi-processor communication, if the address does not match, then enter the silent mode
- Wake up from silent mode (via idle bus detection or address flag detection)
- Two ways of waking up receiver: address bit (MSB, bit 9), bus idle
- Mode configuration:

USART modes	USART1	USART 2	USART 3	UART4	UART5	UART6	UART7
Asynchronous mode	support	support	support	support	support	support	support
Hardware flow control	support	support	support	not support	not support	not support	not support
Multiple buffer communication (DMA)	support	support	support	support	support	support	support
Multiprocessor communication	support	support	support	support	support	support	support
Synchronous mode	support	support	support	not support	not support	not support	not support
Smart card	support	support	support	not support	not support	not support	not support
Half duplex (Single wire mode)	support	support	support	support	support	support	support
IrDA	support	support	support	support	support	support	support
LIN	support	support	support	support	support	support	support

5.14 Serial Peripheral Interface（SPI）

The device integrates 3 SPI interfaces, which allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial mode. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

Main features:

- 3-wire full-duplex synchronous transmission
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8 or 16 bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- 8 master mode baud rate predivision frequency coefficient (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/2$)
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag
- Hardware CRC for reliable communication:
  - In send mode, the CRC value can be sent as the last byte
  - In full-duplex mode, CRC is automatically performed on the last byte received
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests

- Maximum interface speed: the SPI1 interface is 36Mbps and SPI2/SPI3 interfaces are 18Mbps.

5.15 Serial Audio Interface（I²S）

I²S is a 3-pin synchronous serial interface communication protocol. The device integrates two standard I²S interfaces (multiplexed with SPI2 and SPI3) and can operate in master or slave mode. The two interfaces can be configured as 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8kHz to 96kHz. It supports four audio standards, including Philips I²S, MSB and LSB alignment, and PCM standard.

It can work under master and slave mode in half duplex communication. When it acts as a master device, it provides clock signals to external slave devices through an interface.

Main features:

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8KHz to 96KHz)
- The data format can be 16, 24, or 32 bits
- Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)
- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel
- Supported I²S protocols:
  - I²S Philips standard
  - MSB alignment standard (left aligned)
  - LSB alignment standard (right aligned)
  - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256 x Fs (Fs is the audio sampling frequency)

5.16 Quard Serial Peripheral Interface (QSPI)

Supports 1-way QSPI single master mode and can work in both indirect and memory-mapped modes.

Main features:

- Can be configured under Single SPI/Dual SPI/Quard SPI mode. In Single mode, support standard SPI operation, can work in half duplex, full duplex mode;
- The SPI operation mode can be configured in indirect mode or memory mapping mode. The command code can be configured in the instruction phase, and the alternate byte or mode byte of the alternate byte or mode phase can be configured;
- Supports 8-bit, 16-bit, and 32-bit data access modes；
- FIFO with data transceiver；
- supports DMA operation；
- Support FIFO interrupt, operation complete interrupt, timeout interrupt, data access error interrup；
- Support maximum speed of 4×36Mbps;
- In indirect mode or memory-mapped mode, the operation is divided into instruction phase, address phase, alternate byte phase, Dummy phase, and data phase, which can be configured to be skipped.

5.17 Controller Area Network（CAN）

Device integrates a CAN bus interface compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1 Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

Main features:

- Support CAN protocol 2.0A and 2.0B active mode
- Baud rate up to 1Mbps
- Supports time-triggered communication
- Transmission
  - 3 Tx mailboxes
  - The priority of sending packets can be configured by software.
  - Records the timestamp of SOF Transmission
- Receive:
  - 2 receiving FIFO of third level depth
  - Variable filter group
  - 14 filter groups
  - Identifier list
  - The FIFO overflow processing mode is configurable
  - Record the timestamp of SOF receiving
- Time-triggered communication mode:
  - Disable automatic retransmission mode
  - 16-bit free run timer
  - Timestamp can be sent in the last 2 bytes of data
- Management:
  - Interrupt masking
  - The mailbox occupies a separate address space to improve software efficiency

5.18 Universal Serial Bus（USB）

Device is embedded with a full speed USB compatible device controller that follows the full speed USB device (12Mbit/s) standard. The endpoint can be configured by software and has suspend/resume function. The USB dedicated 48MHz clock is generated directly from the internal PLL. (The clock source must be HSE external high-speed crystal to ensure communication stability,)

Main features:

- Comply with the technical specifications of USB2.0 full-speed equipment
- 1 to 8 USB endpoints can be configured
- CRC (cyclic redundancy check) generation/check, reverse non-return to zero (NRZI) encoding/decoding and bit filling
- Double buffer mechanism for bulk/synchronous endpoints
- Support USB suspend/resume operation
- Frame lock clock pulse generation
- Integrated USB DP signal line pull-up 1.5K resistor (user can enable or disable through software control) with accuracy of ±5%.

5.19 General Purpose Input/Output Interface （GPIO）

Support up to 36 GPIO, which is divided into seven groups (GPIOA/GPIOB/GPIOC GPIOD/GPIOE/GPIOF/GPIOG), each group has 16 ports (10 of F group and 7 of G group). Each GPIO pin can be configured by software as an output (push-pull or open-drain), input (with or without pull or down), or a multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals, and some I/O pins are also multiplexed with clock pins. All GPIO pins have high current flow

capability except for the analog input function port.

Main features：

- GPIO can be configured to the foloowing modes by software：
  - Input float
  - Input pull up（weak pull up）
  - Input pull down（weak pull down）
  - Analog input
  - Open drain output
  - Push pull output
  - Push-pull multiplexing function
  - Open drain multiplexing function
- General I/O (GPIO)
  - I/O ports are configured in analog input mode except for BOOT0 and BOOT1 (BOOT0 and BOOT1 are in input pull down modes) with multiplexing function disabled during and after reset;
  - I/O ports are configured in analog input mode with multiplexing function disabled during and after reset, the JTAG pin is placed in input pull-up or pull-down mode after reset;
  - ✓ JTDI is in pull up mode；
  - ✓ JTCK is in pull down mode；
  - ✓ JTMS is in pull up mode；
  - ✓ JNTRST is in pull up mode;
  - When configured as an output, the value written to the output data register is output to the corresponding I/O pin. Output can be in push-pull mode or open-drain mode
- Individual bit setting or bit clearing function；
- External interrupt/Wake up: All ports have external interrupt capability. Ports needs to configured to input mode for using the external interrupt line;
- Multiplexing function：(The port bit configuration register must be programmed before using the default multiplexing function)
  - For the input multiplexing function, ports must be configured in input mode (floating, pull-up, or pull-down) and input pins must be driven externally;
  - For the output multiplexing function, ports must be configured in output mode (push pull and open drain);
  - For bidirectional multiplexing, the port bits must be configured with the multiplexing function output mode (push-pull or open drain). At the same time, the input drive is configured to float input mode.
- The software remaps the I/O multiplexing function
- GPIO locking mechanism, which allows to freeze I/O configurations. When a LOCK procedure is performed on a port bit, the configuration of the port bit cannot be changed until the next reset

5.20 Analog/Digital Converter（ADC）

The device supports 4 12-bit sequential comparison ADC with a sampling rate of 5Msps, which supports single-end and differential inputs, measuring 40 external and 7 internal signal sources, ADC1 supports 11 external channels, ADC2 supports 13 external channels, ADC3 supports 15 external channels, and ADC4 supports 13 external channels.

Main features:

- Support 12/10/8/6-bits resolution configurable
  - The maximum sampling rate at 12bit resolution is 5.14 MSPS
  - The maximum sampling rate at 10bit resolution is 6 MSPS
  - The maximum sampling rate at 8bit resolution is 7.2 MSPS
  - The maximum sampling rate at 6bit resolution is 9 MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the working clock source, up to 144 MHz
  - PLL can be configured as a sampling clock source, up to 72 MHz, support 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256 frequency division
  - The AHB_CLK can be configured as the sampling clock source, up to 72 MHz, and supports 1,2,4,6,8,10,12,16,32 frequency division.
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports timer trigger ADC sampling
- Support 2.048V internal reference voltage $V_{REFBUFFER}$
- Interrupts triggered when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes

- Automatic scan mode from channel 0 to channel N
- Support for self-calibration
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel
- Both regular conversions and injection conversions have external triggering options
- Continuous mode
- Break mode
- Double mode:combination of ADC1 and ADC2, combination od ADC3 and ADC4.
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: VREF- ≤ VIN ≤ VREF+
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion
- Analog watchdog function can monitor one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will occur

5.21 Digital/Analog Converter（DAC）

The device integrates two digital-to-analog converters (DAC), which is a 12-bit digital input, voltage output digital/analog converter, DAC module has two output channels, each channel has a separate converter, two DACs can be used independently. The DAC can input the reference voltage V_{REF+} through the pin for more accurate conversion results.

Main features:

- Both of the 2 converters have one output channel independently
- Configurable 8/12-bits output
- Configurable left and right data alignment in 12-bit mode
- Synchronous update function
- Generate noise wave
- Generate triangle wave
- Dual DAC channel can be used independently or in syncronous conversion
- DMA function can be used by every channel
- External trigger conversion
- Input reference voltage VREF+

5.22 Operational Amplifier（OPAMP）

The device integrates up to 4 independent operational amplifiers with multiple operating modes such as external amplifier, internal follower and programmable amplifier (PGA) (or both internal amplifier and external filter).

Main features:

- Support rail to rail input
- It can be configured as independent op amp and programmable gain op amp;
- Forward and reverse input checkboxes
- OPAMP working mode can be configured as:
  - Independent mode (external gain setting)
  - PGA mode, programmable gain 2X, 4X, 8X, 16X, 32X
  - Follower mode
- The internally connected ADC channel is used to measure the output signal of the operational amplifier

5.23 Analog Comparator（COMP）

The device integrates up to 7 comparators, which can be used as a separate device (all ports of the comparator are plugged into the I/O) or combined with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

Main features:

- Rail to rail comparators are supported
- The reverse and forward sides of the comparator support the following inputs

- Optional I/O
- DAC channel output
- Internal 64 level adjustable voltage input reference (there are 2 internal ajustable voltage VREF1 and VREF2, which can be used for all 7 comparators.)

- Programmable hysteresis can be configured as no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
- The comparator can output to EITHER I/O or timer input for triggering
  - Capture events
  - OCREF_CLR events (for periodic current control)
  - The brake events
- The comparator supports output filtering, including analog and digital filtering. The filter frequency is 50K-144Mhz configurable
- COMP1/COMP2, COMP3/COMP4 and COMP5/COMP6 can form window comparator independently.
- Support comparator output with blanking,both of the disable blanking or Timer1_OC5, Timer8_OC5 input blanking are allowed.
- Each comparator have interrupt wake up capability, support wake up from SLEEP mode.

5.24 Temperature Sensor（TS）

The temperature sensor generates a voltage that varies linearly with temperature in the range of 1.8V<VDDA< 3.6V. The temperature sensor is internally connected to the ADC_IN16 input channel for converting the output of the temperature sensor to digital values.

5.25 Ethernet Interface

The chip contains an Ethernet MAC module, which contains 10/100Mbps Ethernet MAC (Media Access Controller), adopts DMA to optimize data frame transmitting and receiving performance, supports two standard interfaces for communication with the physical layer (PHY): MII (Media Independent interface) and RMII (simplified media independent interface) to implement Ethernet data frame transmitting and receiving. Ethernet modules comply with IEEE 802.3-2008 and IEEE 1588-2008 standards.

Main features:

- 10/100Mbps data transfer rate
- Support MII/RMII interface
- Apply to CSMA/CD protocal half duplex operation
- Apply to IEEE 802.3 flow control full duplex operation
- In full duplex mode, the received PAUSE control frames can be selectively forwarded
- Automatically calculates CRC and generates controllable fill bits on a frame basis
- Automaticly remove the optional fill bit of /CRC when in receiving frames
- Frame length can be programmed to support standard frames up to 16K bytes
- Programmable frame gaps (40-96 bits, varying in 8-bit units)
- Supports multiple flexible address filtering modes
- Return to 32 bit state information while transmitting and receiving data packets
- Supports detection of IEEE 802.1Q VLAN tags for received frames
- The application has separate transmit, receive and control interfaces
- Supports mandatory network statistics by RMON/MIB counters (RFC2819/RFC2665)
- Configure and manage PHY by MDIO interface
- Detect LAN wake-up frames and AMD Magic PacketTM frames
- Verification and offloading of IPv4 and TCP packets encapsulated by Ethernet frames
- Advanced receive and check for IPv4 packet head and TCP, UDP, or ICMP in IPv4 or IPv6 data packet
- Supports Ethernet frame timestamps defined by IEEE 1588-2002, a 64-bit timestamp is added to every received and transmitting frame.
- In store-and-forward mode, the header checksum of IP and the checksum of TCP, UDP, or ICMP are calculated and inserted in the transmitting frame.

5.26 Touch Sensor Controll (TSC)

TSC is mainly used in capacitive touch key application scenarios. When the hardware detects a hand touch, the CPU wakes up for more accurate touch detection and subsequent algorithm processing.

Main features：

- Support capacitive touch function, support up to 24 channels, each channel is individually enabled；
- Interrupt is generated and the CPU is woken up when the touch operation is detected in low power mode (SLEEP, STOP0, STOP2)；
- The CPU is notified of an interrupt/event when a touch operation is detected under normal working mode；
- When a touch operation is detected, status register will indicate the corresponding channel and generate their wake-up states and each channel has a wake-up indicator sign；
- Programs are configurable at the touch wakeup detection cycle and the channel detecting time；
- Chanel detection ensitivity is configurable and each channel has its own threshold；
- Support callibration function；
- Switch to timer
- The input capture channel is implemented by the firmware touch control algorithm；

5.27 Cyclic Redundancy Check Calculation Unit（CRC）

Integrated CRC32 and CRC16 functions, the cyclic redundancy check (CRC) caculating unit is based on a fixed generation polynomial to obtain any CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides methods of detecting flash memory errors, CRC cells can be used to calculate signatures of software in real time and compare them with signatures generated when linking and generating the software.

Main features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + 1$
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC calculation time: 4 AHB clock cycles (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

5.28 Algorithmic hardware acceleration engine（SAC）

The embedded algorithm hardware acceleration engine supports a variety of international algorithms and national cryptographic symmetric cryptographic algorithms and hash cryptographic algorithm acceleration, which can greatly improve the encryption and decryption speed compared with pure software algorithms.

- The hardware support algorithms are as followed：
  - Supports DES symmetric algorithm
    - Supports DES and 3DES encryption and decryption operations
    - TDES supports 2KEY and 3KEY mode
    - Supports CBC and ECB mode
  - Supports AES symmetric algorithm
    - Support 128bit/192bit/ 256bit key length
    - Supports CBC/ECB/CTR mode
  - Supports SHA hash algorithm
    - Supports SHA1/SHA244/SHA256
  - Supports MD5 digest algorithm
  - Supports symmetric SM1, SM4, SM7 algorithms and SM3 hash algorithms

5.29 Unique Device Serial Number（UID）

CMT2392F512 has two built-in unique device serial numbers of different lengths, which are 96-bit unique device ID (UID) and 128-bit unique customer ID (UCID). These two device serial numbers are stored in the system configuration block of flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in flash memory. It can also be used to activate Secure Bootloader with security functions.

UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains the information related to chip production and version.

5.30 Serial Single-wire JTAG Debug Port（SWJ-DP）

Embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

6 Order Information

Table 6-1. CMT2392F512 Order Information

Type	Description	Package	Packet Option	Operation Condition	MOQ
CMT2392F512-EQR[1]	CMT2392F512, low power consumption Sub-1GHz RF transceiver SoC	QFN 68 (7x7)	Make up with disk	1.8 to 3.6 V, - 40 to 85℃	3,000

Remark:
[1]. “E” represents the extended industrial product grade，with supported temperature range from - 40 to +85 ℃.
“Q” represents package type of QFN 68.
“R” represents the tape and tray type with MOQ as 3,000.

For more information, please refer to official website: www.hoperf.com
For any other requirements, please contact sales@hoperf.com or your local sales representatives.

7 Package Outline

Package information of CMT2392F512 is shown as followed.

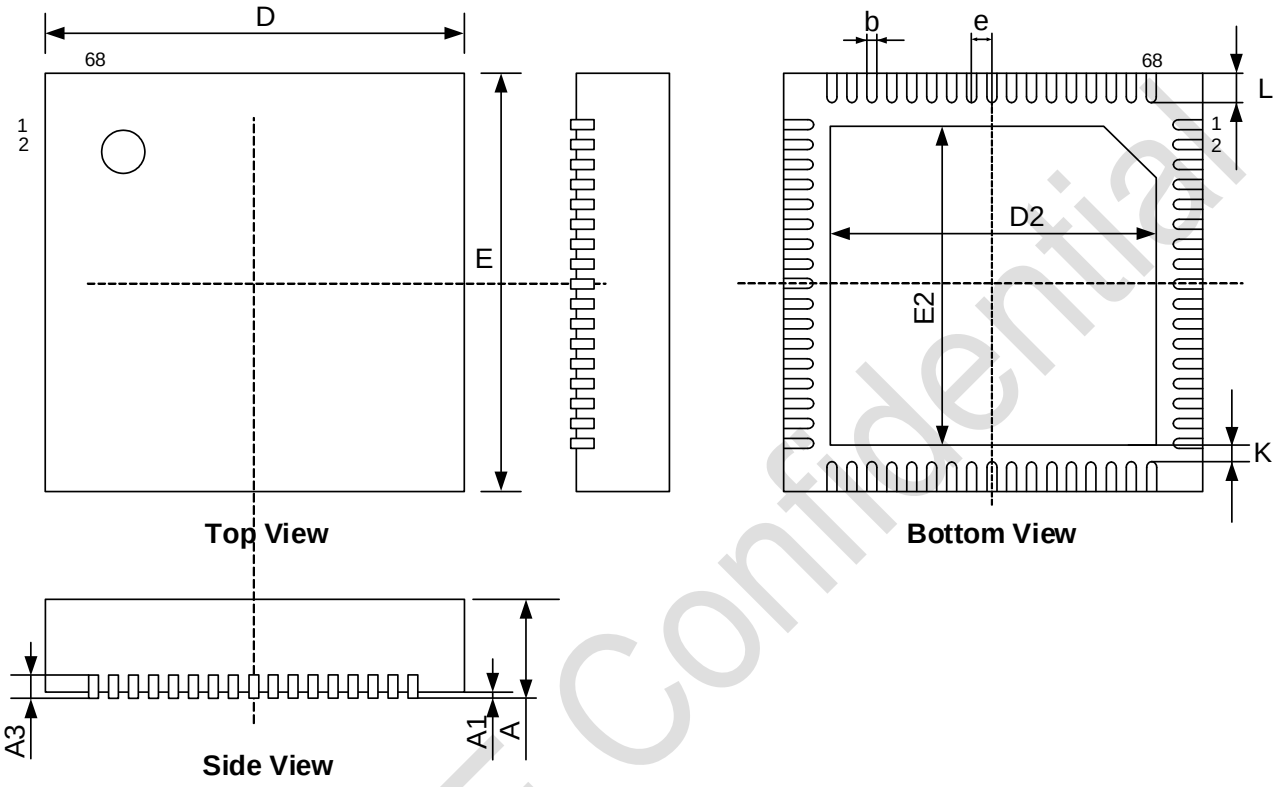


Figure 7-1. CMT2392F512 Package Outline

Table 7-1. CMT2392F512 Package Size

Symbol	Size (mm)		
	Min.	Typ.	Max.
A	0.65	0.75	0.85
A1	--	0.02	0.05
A3	0.18	0.203	0.25
b	0.10	0.15	0.20
D	6.90	7.00	7.10
E	6.90	7.00	7.10
e	--	0.35	--
D2	5.39	5.49	5.59
E2	5.39	5.49	5.59

L	--	0.40	--
K	0.20	--	--

8 Silk Printing Information

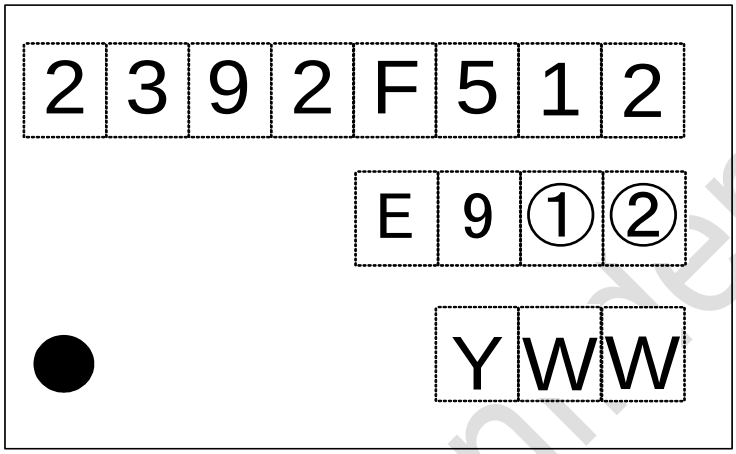


Figure 8-1. CMT2392F512 Top Mark

Table 8-1. CMT2392F512 Top Mark Description

Printing method	Laser
Pin 1 marking	Circle diameter = 0.3 mm
Font size	0.5 mm, right alignment
First line silk printing	2392F512, Representative model CMT2392F512
Second line silk printing	E9①② Internal tracking code
Third line silk printing	Date code, assigned by packaging plant, Y represents the last digit of the year and WW represents the working week

9 Revise History

Table 10-1. Revise History

Version	Chapter	Modify	Date
0.1	All	Initial	2024-01-30

10 Contacts

Shenzhen Hope Microelectronics Co., Ltd.

Address: 30th floor of 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China

Tel: +86-755-82973805 / 4001-189-180
Fax: +86-755-82973550
Post Code: 518052
Sales: sales@hoperf.com
Website: www.hoperf.com