Accessing the CMT218xA EEPROM

1. Introduction

The purpose of this document is to provide the guidelines to access the embedded EEPROM of CMT218xA. The products covered in this document are listed in the table below.

Table 1. Products Covered in this Document

Product	Frequency	Modulation	Tx Current Consumption	Flash	PA Output
CMT2180A	240-480 MHz	OOK	13.4 mA (+10 dBm, 433.92 MHz, OOK)	1024 words	Single-ended/ Differential
CMT2189A	240-960 MHz	(G)FSK/OOK	27.6 mA (+10 dBm, 868.35 MHz, FSK)		

2. Getting Started

The CMT218xA offers 11 words (16 bits each word) of EEPROM memory for customers which need to store a few bytes of key information by means of security or/and anything that requires to change time to time during the application.

Both system control EEPROM and the customer EEPROM shares one EEPROM but locates different address. The customer bank locates address from 0x00 to 0x0A. Cares should be taken in the application to avoid overwriting any bit inside system control bank. Otherwise, unexpected error will happens

2.1 Accessing Registers with TWI

For CMT218xA, the PA4 and PA5 ports of the microcontroller core are used as CLK and DATA function to control RF section, see the table below. The rest of this document uses CLK and DATA instead of PA4 and PA5 to describe how to access the embedded EEPROM.

Table 2. Port Function Mapping

Port Name	Function
PA4	CLK
PA5	DATA

The EEPROM can be accessed through the two-wire interface (TWI): CLK and DATA. The TWI is designed to operate at a maximum of 1 MHz. The timing requirement and data transmission control through the TWI are shown in this section.

Table 3. TWI Timing Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	V_{IH}		0.8			V_{DD}
Digital Input Level Low	V_{IL}				0.2	V_{DD}
CLK Frequency	F_{CLK}		10		1,000	kHz
CLK High Time	t_{CH}		500			ns
CLK Low Time	t_{CL}		500			ns
DATA Delay Time	t_{DD}	The data delay time from the last CLK rising edge of the TWI command to the time DATA return to default state			15,000	ns
DATA Setup Time	t_{DS}	From DATA change to CLK falling edge	20			ns
DATA Hold Time	t_{DH}	From CLK falling edge to DATA change	200			ns

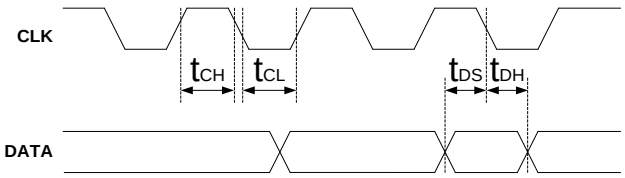

Figure 1. Two-wire Interface Timing Diagram

Once the device is powered up, TWI_RST and SOFT_RST should be issued to make sure the device works in SLEEP state robustly. On every transmission, TWI_RST and TWI_OFF should be issued before the transmission to make sure the TWI circuit functions robustly. TWI_RST and SOFT_RST should be issued again after the transmission for the device going back to SLEEP state reliably till the next transmission.

The TWI includes an input port CLK and a bi-directional port DATA. A complete Write/Read (W/R) process has 16 clock cycles. For the first 8 clock cycles, the DATA is used as input port for writing register address; and for the last 8 clock cycles, the DATA is used as input port during write process, and output port during read process. The timing chart for the TWI W/R is shown as the figure below.

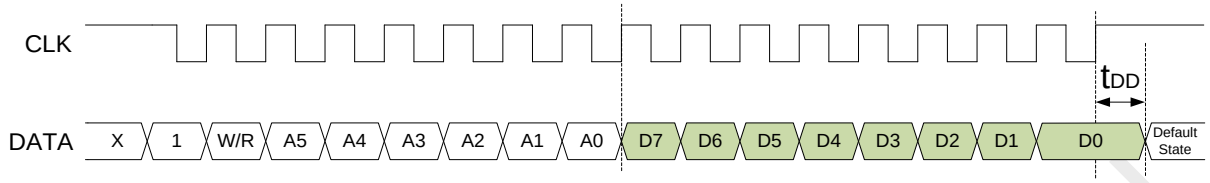

Figure 2. TWI W/R Timing Chart (Except for TWI_RST Command)

Notes:

1. The timing requirement is shown as Table 2.
2. At the end of each command, the DATA should return to its default state after the last CLK rising edge within the time t_{DD}.
3. The command always start with "1", the first 8 clock cycle includes the W/R control and address bits A[5:0]. It is a Read command when W/R is 1, and Write command when W/R is 0. The range of the address bits is from 0x00 to 0x0A.
4. In a Write command, D[7:0] is the data to be written into the register. In a Read command, D[7:0] is the data to be read from the register.
5. The DATA pin is a bi-directional port, and it will be switched to output port in the last 8 clock cycle of a Read command. At this time, the host MCU should switch the corresponding port which is connected to the DATA pin to input port at the coming CLK rising edge, shown as dash line in the middle of Figure 2, so that there is no voltage conflict between the two ports and the read out function is correctly behaved.
6. To simplify the expression, this datasheet is using the TWI_WRREG and TWI_RDREG to represent the write and read command to specified registers, as shown in the table below.

Table 4.TWI_WRREG and TWI_RDREG

Command	Description
TWI_WRREG	TWI write command. TWI_WRREG(XX, YY) means clocking in 16b'10xx xxxx yyyy yyyy, which xx xxxx is the register address to be written, ranging from 0x00 to 0x3F; yyyy yyyy is the register content to be written ranging from 0x00 to 0xFF. For example, TWI_WRREG(0x12, 0xAA) means clocking in 0x92AA.
TWI_RDREG	TWI read command, TWI_RDREG(XX, ZZ) means clocking in 8b'11xx xxxx and read out zzzz zzzz, which xx xxxx is the register address to be written, ranging from 0x00 to 0x0A; zzzz zzzz is the read out value from the register, ranging from 0x00 to 0xFF For example, TWI_RDREG(0x2A, DAT), means clocking in 0xEA, and read out DAT which is an 8-bit value.

7. Specific commands TWI_RST, TWI_OFF and SOFT_RST are also used in the on-line register configuration, see table below for the definition of the 3 commands.

Table 5. TWI Commands Descriptions

Command	Descriptions
TWI_RST	Implemented by pulling the DATA pin low for 32 clock cycles and clocking in 0x8D00, 48 clock cycles in total. It only resets the TWI circuit to make sure it functions correctly. The DATA pin cannot detect the Rising edge to trigger transmission after this command, until the TWI_OFF command is issued. Please ensure the DATA pin is firmly pulled low during the first 32 clock cycles. See Figure 3.

Command	Descriptions
TWI_OFF	Implemented by clocking in 0x8D02, 16 clock cycles in total. It turns off the TWI circuit, and the DATA pin is able to detect the Rising edge to trigger transmission after this command, till the TWI_RST command is issued. The command is shown as Figure 4.
SOFT_RST	Implemented by clocking in 0xBD01, 16 clock cycles in total. It resets all the other circuits of the chip except the TWI circuit. This command will trigger internal calibration for getting the optimal device performance. After issuing the SOFT_RST command, the host MCU should wait 1 ms before sending in any new command. After that, the device goes to SLEEP state. The command is shown as Figure 5.

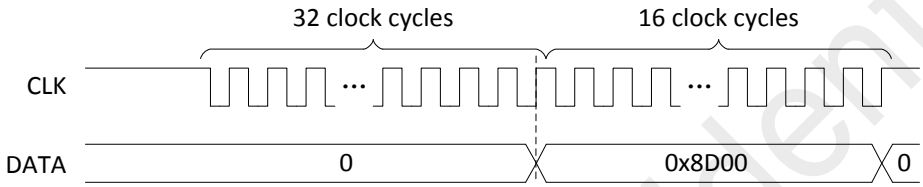

Figure 3. TWI_RST Command

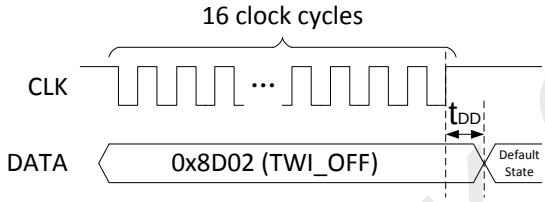

Figure 4. TWI_OFF Command

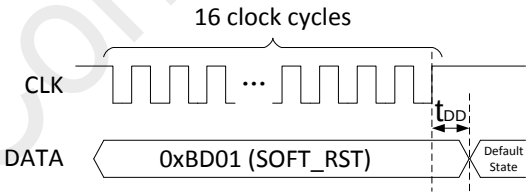

Figure 5. SOFT_RST Command

Table 6. Control Bank Registers

Addr.	Default	W/R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02	0x7F	w/r	RESV_0	PD_DIG	RESV_1	RESV_1	RESV_1	PD_DLDO	PD_XO_BUF	PD_XO
0x16	0x30	w/r	RESV_0	RESV_0	PD_USR_EE	RESV_1	ERASE	PROG	READ	IP_EN
0x17	0x00	w/r	RESV_0	RESV_0	RESV_0	EE_ADDR				
0x19	0x00	w/r	EE_DIN0							
0x1A	0x00	w/r	EE_DIN1							
0x1B	0x00	r	EE_DOUT0							
0x1C	0x00	r	EE_DOUT1							
0x1F	0x00	r	RESV	RESV	RESV	RESV	READY	RESV	RESV	RESV
0x2F	0x00	w/r	PD_DIG_SEL	RESV_0	RESV_0	RESV_0	RESV_0	RESV_0	RESV_0	RESV_0
0x3F	0x00	w/r	RESV_0	RESV_0	RESV_0	RESV_0	RESV_0	RESV_0	RESV_0	EE_PROT_DIS

Note:

[1]. Both RESV_0 and RESV_1 in this table are reserved bits, RESV_0 must be kept as logic “0” and RESV_1 must be kept as logic “1”. Values change of these bits and any bit other than the addresses listed in this table may cause unexpected error. RESV are reserved bits that might have different read-out values.

The detailed descriptions of each register are given below.

Table 7. 0x02 Register

Register	Bit	RW	Bit Name	Descriptions
0x02	7	r/w	RESV_0	Reserved bit, always set it to 0.
	6	r/w	PD_DIG	Digital circuit power down control. 1: Turns off the digital circuit (Default); 0: Turns on the digital circuit.
	5:3	r/w	RESV_1	Reserved bits, always set them to 1.
	2	r/w	PD_DLDO	Digital LDO power down control. 1: Turns off the digital LDO (Default); 0: Turns on the digital LDO.
	1	r/w	PD_XO_BUF	Crystal oscillator driving buffer power down control. 1: Turns off the crystal oscillator driving buffer (Default); 0: Turns on the crystal oscillator driving buffer.
	0	r/w	PD_XO	Crystal oscillator power down control. 1: Turns off the crystal oscillator (Default); 0: Turns on the crystal oscillator.

Table 8. 0x16 Register

Register	Bit	RW	Bit Name	Descriptions
0x16	7:6	r/w	RESV_0	Reserved bits, always set them to 0.
	5	r/w	PD_USR_EE	Power down control of the EEPROM user bank. 1: Turns off the user bank of EEPROM(Default); 0: Turns on the user bank of EEPROM.
	4	r/w	RESV_1	Reserved bit, always set it to 1.
	3	r/w	ERASE	The EEPROM erase control signal. The ERASE action must be taken before programming any content to each word of the EEPROM. The user should not set the three EEPROM access commands (ERASE, PROG and READ) or any two of the three commands as logic “1” at the same time. 1: Erase the specified address of EEPROM; 0: Not erase the EEPROM (Default).
	2	r/w	PROG	The EEPROM programming control signal. A program operation takes effect only after the erase operation issued. 1: Program the given value to specified address of the EEPROM; 0: Not programming the EERPOM (Default)
	1	r/w	READ	The EEPROM read control signal. 1: Read from specified address of the EEPROM; 0: Not reading the EEPROM (Default).
	0	r/w	IP_EN	The EEPROM enable control. Set this bit to “1” before ERASE, PROG or READ the EEPROM. 1: Enable the EEPROM; 0: Disable the EEPROM (Default).

Table 9. 0x17 Register

Register	Bit	RW	Bit Name	Descriptions
0x17	7:5	r/w	RESV_0	Reserved bits, always set them to 0.
	4:0	r/w	EE_ADDR	The EEPROM address. The customer bank locates address from 0x00 to 0x0A.

Table 10. 0x19 Register

Register	Bit	RW	Bit Name	Descriptions
0x19	7:0	r/w	EE_DIN0	The lower 8-bit data to be written to the EEPROM.

Table 11. 0x1A Register

Register	Bit	RW	Bit Name	Descriptions
0x1A	7:0	r/w	EE_DIN1	The higher 8-bit data to be written to the EEPROM.

Table 12. 0x1B Register

Register	Bit	RW	Bit Name	Descriptions
0x1B	7:0	r	EE_DOUT0	The lower 8-bit data to be read out from the EEPROM.

Table 13. 0x1C Register

Register	Bit	RW	Bit Name	Descriptions
0x1C	7:0	r	EE_DOUT1	The higher 8-bit data to be read out from the EEPROM.

Table 14. 0x1F Register

Register	Bit	RW	Bit Name	Descriptions
0x1F	7:4	r	RESV	Reserved bits. The user can ignore the readout values.
	3	r	READY	This bit indicates the EEPROM status. 1: Indicates the user can issue ERASE, PROG or READ command to the EEPROM; 0: Indicates the EEPROM is busy. The user has to wait this signal going logic “1” before issue any commands (Default).
	2:0	r	RESV	Reserved bits. The user can ignore the readout values.

Table 15. 0x2F Register

Register	Bit	RW	Bit Name	Descriptions
0x2F	7	r/w	PD_DIG_SEL	Control bit of a 2-to-1 Mux, to choose the powered down control of the digital circuit is done automatically or controlled by PD_DIG. 1: The power down of digital circuit is controlled by PD_DIG; 0: The power down of digital circuit is controlled automatically (Default).
	6:0	r/w	RESV_0	Reserved bits, always set them to 0.

Table 16. 0x3F Register

Register	Bit	RW	Bit Name	Descriptions
0x3F	7:1	r/w	RESV_0	Reserved bits, always set them to 0.
	0	r/w	EE_PROT_DIS	EEPROM content protection bit, need to remove the protection before writing the EEPROM. 1: The EEPROM protection is removed and user can write content to it; 0: The EEPROM is protected. User can read from the EEPROM but its content cannot be erased or programmed (Default).

2.2 Start to Access the EEPROM

The user should make sure the CMT218xA get ready before accessing the EEPROM. Please follow below steps to access the embedded EEPROM.

Step - 1. Enable the EEPROM

- TWI_WRREG(8'h02, 8'h3B); # Turn the DLDO, crystal oscillator and its buffer on.
- wait_us(10); # Wait for 10 us to get DLDO settled.
- TWI_WRREG(8'h2F, 8'h80); # Select the power down of digital circuit to be controlled by PD_DIG.
- TWI_WRREG(8'h3F, 8'h01); # Remove the EEPROM protection.
- wait_us(10); # Wait for removing protection action taking effect .
- TWI_WRREG(8'h16, 8'h11); # Enable the EEPROM.

Step - 2. ERASE, PROG and READ the EEPROM (Take the PROG as an example)

- TWI_WRREG(8'h17, EE_ADDR); # Write the EEPROM address (EE_ADDR, ranges from 0x00 to 0x0A) that the user want
  # to program to register address 0x17.
- TWI_WRREG(8'h19, DIN0); # Write the lower 8-bit data to register 0x19; ERASE and READ can ignore this step.
- TWI_WRREG(8'h1A, DIN1); # Write the higher 8-bit data to register 0x1A; ERASE and READ can ignore this step.
- TWI_WRREG(8'h16, 8'h15); # Set PROG bit as “1”, start to program DIN1, DIN0 to address EE_ADDR of EEPROM.
  # The user should ERASE the word of the EEPROM before programming it.
- TWI _RDREG(8'h1F, DAT); # Read the READY bit’s status, wait for the READY bit getting “1”. The user needs to
  # check the READY bit only and ignores the value of the other bits.
  # Normally the READY bit goes “1” within 7 ms in both ERASE and PROG operations.
  # Waiting time should less than 800 ns for a read operation.
- TWI_RDREG(8'h1B, DAT); # Read the lower 8-bit data from register address of 0x1B.
- TWI_RDREG(8'h1C, DAT); # Read the higher 8-bit data from register address of 0x1C. READ is not necessary after
  # the ERASE, as the read-out value might be random, but the user should READ the
  # value out after PROG to check if the PROG is correctly done.
- TWI_WRREG(8'h16, 8'h31); # Clear the PROG bit. The user should clear this bit after programming/erasing/reading
  # each word of the EEPROM.

Step - 3. Disable EEPROM and Protects the EEPROM from being erased or programmed

- TWI_WRREG(8'h16, 8'h30); # Disable the IP_EN and PD_USR_EE.
- TWI_WRREG(8'h3F, 8'h00); # Enable EEPROM protection.
- TWI_WRREG(8'h2F, 8'h00); # Select the power down of digital circuit to be controlled automatically.
- TWI_WRREG(8'h02, 8'h7F); # Turns off DLDO, crystal oscillator and its buffer.

3. Document Change List

Table 17. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.8	All	Initial released version	2015-06-26

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