ES_CMT453x Series Errata Sheet V1.1.0

Contents

1 ERRATA LIST 3
2 BLUETOOTH 4
2.1 HSE AS SYSTEM CLOCK 4
2.2 EXTI4_12 INTERRUPTS WHILE BLUETOOTH PROTOCOL STACK IS USED 4
2.3 LSI ISSUE AFFECT WAKE-UP 4
3 RESET AND CLOCK CONTROL 5
3.1 NOTE TO USE OF RCC_LSCTRL REGISTER 5
3.2 RCC_AHBRST'S ABNORMAL ADCRST BIT 5
4 SYSTEM CACHE MANAGEMENT (CACHE) 5
4.1 THERE IS ABNORMAL FETCH INSTRUCTION WHEN THE BUS ACCESSES THE SPECIAL CODE LOGIC 5
5 LOWER POWER UNIVERSAL ASYNCHRONOUS RECEIVER-TRANSMITTER (LPUART) 5
5.1 LSI 32K IS USED AS CLOCK SOURCE, TRANSMISSION AT 9600 BAUD RATE AND WAKE-UP BYTE ARE ABNORMAL 5
6 SERIAL PERIPHERAL INTERFACE (SPI) 6
6.1 SPI 6
6.1.1 SPI baud rate setup 6
6.1.2 CRC calibration in slave mode 6
6.1.3 When the Bluetooth protocol stack is used, SPI1 interrupts and fails to respond 6
7 I2C INTERFACE 6
7.1 ABNORMAL SIGNAL INTERFERENCE 6
8 KEY SCAN (KEYSCAN) 7
8.1 RETENTION VOLTAGE REQUIREMENT FOR KEYSCAN IN SLEEP MODE 7
9 MARKING INFORMATION 7
10 VERSION HISTORY 7
11 NOTICE 8

1 Errata List

Errata links			Chip version		
			Version B	Version C	Version D
2：Bluetooth Function (BLE)	2.1: HSE as system clock		●	●	●
	2.2: EXTI4_12 interrupts while Bluetooth protocol stack is used		●	●	●
	2.3: LSI glitch is abnormal		●	●	/
3: Reset and Clock Control (RCC)	3.1：Note to use of RCC_LSCTRL register		●	●	●
	3.2：RCC_AHBRST's ADCRST bit is abnormal		●	●	●
4: System Cache Management (CACHE)	4.1: There is abnormal fetch instruction when the bus accesses the special code logic		●	/	/
5: Lower Power Universal Asynchronous Receiver-Transmitter (LPUART)	5.1: When LSI 32K is used as clock source, transmission at 9600 baud rate and wake-up byte are abnormal		●	●	●
6: Serial Peripheral Interface (SPI)	6.1: SPI	6.1.1: SPI baud rate setup	●	●	●
		6.1.2: CRC calibration in slave mode	●	●	●
		6.1.2: When the Bluetooth protocol stack is used, SPI1 interrupts and fails to respond	●	●	●
7: I2C Bus Interface	7.1: Abnormal signal interference		●	●	●
8: Key Scan (KEYSCAN)	8.1: When entering the Sleep mode, part of chips cannot wake up through KEYSCAN.		●	●	●

Table 1-1 Errata Overview

Note: " /" means this version is not applicable；"●" means this version is applicable to this erratum description.

2 Bluetooth

2.1 HSE as system clock

Description

When the Bluetooth protocol function is used, HSE 32M as system clock speed cannot meet the demand for performance.

Solution

When the Bluetooth protocol function needs to be used, HSE cannot be directly used as system clock, and HSI should be selected as system clock.

2.2 EXTI4_12 interrupts while Bluetooth protocol stack is used

Description

When the Bluetooth protocol stack function is used, the protocol will reconfigure the EXTI4_12 interrupt, which makes the configuration of EXTI4_12 interrupt during startup invalid.

Solution

When the Bluetooth protocol stack function needs to be enabled, the protocol stack initialization will configure EXTI4_12 interrupt and use the EXTI11 interrupt function. The user needs to configure this interrupt after the protocol stack initialization and add EXTI1 clear flag byte in the interrupt processing function.

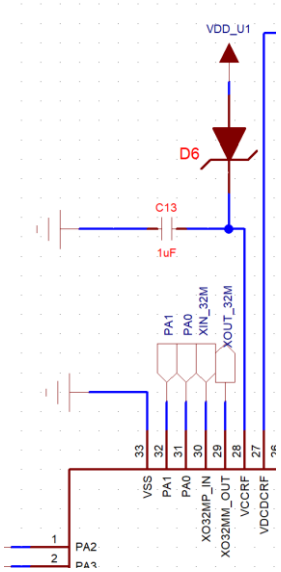
2.3 LSI issue affect wake-up

Description

For chip version B and C, when the power supply VCCRF over 3V, there is risk of LSI, which will lead to abnormal wake-up of the Bluetooth protocol stack.

Solution 1

Ensure that the power supply VCCRF is lower than 3V. We recommend that VCC be connected to VCCRF after a diode to reduce the voltage, as shown in the following reference figure. The recommended diode models are BAV21W, BZT52C3V6 and BAP1321.



Solution 2

Use LSE as low speed clock source.

Solution 3

Use the chip of new version D.

3 Reset and Clock Control

3.1 Note to use of RCC_LSCTRL register

Description

After waking up from the Sleep mode, if we operate the register RCC_CFG, the register RCC_LSCTRL will reset to the default value.

Solution

After waking up from the Sleep mode, first write in the register RCC_LSCTRL, and then operate the register RCC_CFG.

3.2 RCC_AHBRST's abnormal ADCRST bit

Description

Setting the RCC_AHBPRST register's ADCRST bit cannot correctly reset the ADC module.

Solution

When we need to reset the ADC module, manually assign default value to all ADC module registers.

4 System Cache Management (CACHE)

4.1 There is abnormal fetch instruction when the bus accesses the special code logic

Description

When chip of version B implements the special instruction sequence, there is abnormal fetch instruction, which is demonstrated by the stop of core, and then the SWD interface can access the JTAG IDCODE interface, but not the chip's core ID.

Solution

Use the chip of new version D.

5 Lower Power Universal Asynchronous Receiver-Transmitter (LPUART)

5.1 LSI 32K is used as clock source, transmission at 9600 baud rate and wake-up byte are abnormal

Description

When 32K is used as clock source for LPUART, due to indivisibility between baud rate and clock source, the baud rate will be devious, resulting in wrong byte judgement when waking up, so it cannot wake up.

Solution 1

When LSI needs to be used as LPUART clock source, calibrate LSI to 32.768K for use.

Solution 2

Use LSE as the clock source of LPUART.

6 Serial Peripheral Interface (SPI)

6.1 SPI

6.1.1 SPI baud rate setup

Description

When in the SPI master mode and CRC calibration function are enabled, and the SPI clock frequency is above 8MHz, the CRC calibration is abnormal.

Solution

When in the SPI master mode and CRC calibration function are enabled, the SPI clock frequency is no more than 8MHz.

6.1.2 CRC calibration in slave mode

Description

When SPI works in the slave mode and has enabled CRC calibration, even the NSS pin is of high level, as long as SPI receives the clock signal, it will still conduct CRC calculation.

Solution

Before CRC calibration, clear the CRC data register first, so that the master and slave devices are synchronized in CRC calibration.

6.1.3 When the Bluetooth protocol stack is used, SPI1 interrupts and fails to respond

Description

When the Bluetooth protocol stack is enabled, the ROM interrupt vector table is used, but this interrupt vector table does not map out SPI1 interrupt callback function, so it cannot be called back.

Solution

Use DMA receiver or SPI2 module.

7 I2C Interface

7.1 Abnormal signal interference

Description

During the I2C operation process, SCL and SDA might be disturbed by glitch during communication, resulting in abnormal communication.

Solution

Use IO software to simulate I2C.

8 Key Scan (KEYSCAN)

8.1 Retention voltage requirement for KEYSCAN in Sleep mode

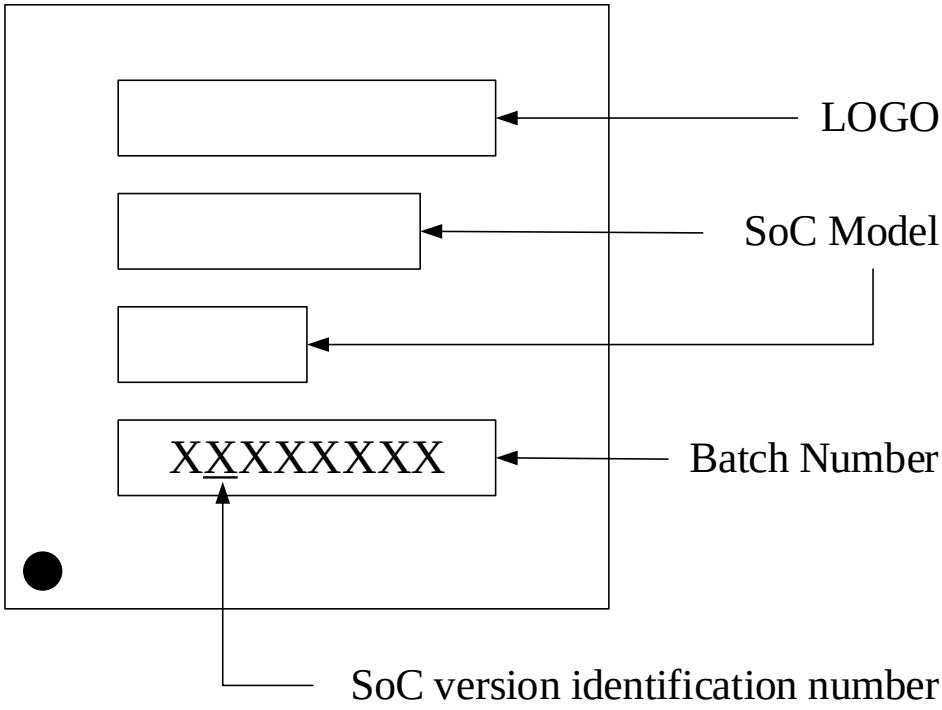
Description

Under the sleep mode, KEYSCAN requires higher retention voltage, or there might be the risks that KEYSCAN and EXTI3 functions cannot wake up the chip.

Solution

Increase the retention voltage, register configuration is *(uint32_t*)0x40007014 = 0x00000814. After use this configure, the sleep power consumption increase 200nA.

9 Marking information



10 Version History

Date	Version	Modification
2023/05/23	V1.1.0	Initial version

11 Notice

Liability Disclaimer

Shenzhen Hope Microelectronics Co., Ltd reserves the right to make changes without further notice to the product to improve reliability, function or design. Shenzhen Hope Microelectronics Co., Ltd does not assume any liability arising out of the application or use of any product or circuits described herein.

Life Support Applications

Shenzhen Hope Microelectronics Co., Ltd's products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Shenzhen Hope Microelectronics Co., Ltd customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Shenzhen Hope Microelectronics Co., Ltd for any damages resulting from such improper use or sale.

Contact Information

Shenzhen Hope Microelectronics Co., Ltd.
Address: 30th floor of 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China
Tel: +86-755-82973805
Post Code: 518055
Email: sales@hoperf.com
Website: www.hoperf.com