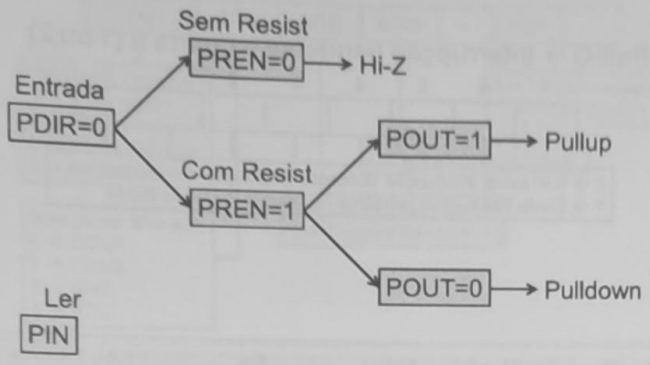
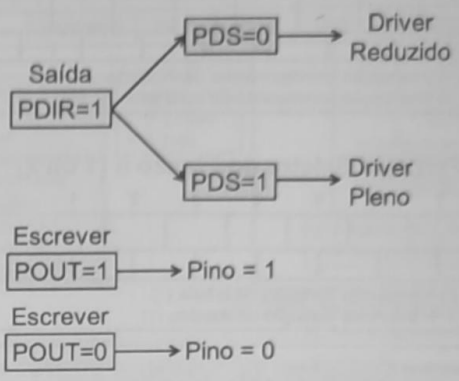
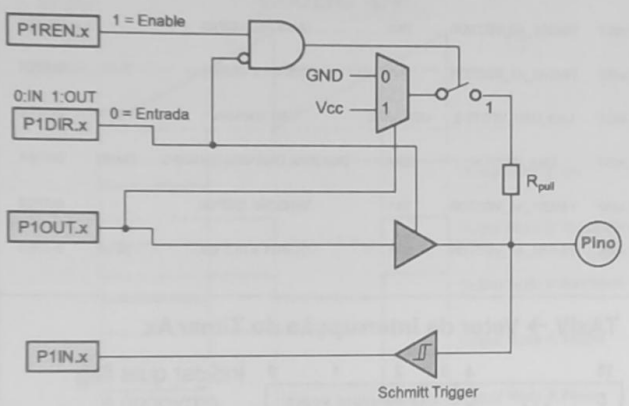
MSP430 – GPIO – Entrada: Resumo

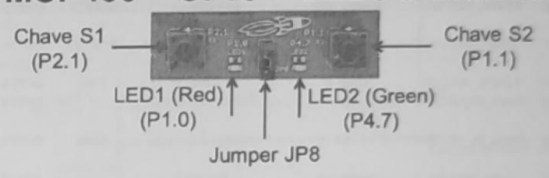


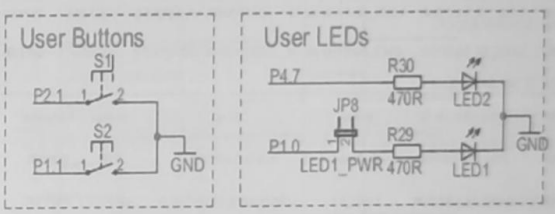
MSP430 – GPIO – Saída: Resumo





MSP430 – GPIO – LEDs e Chaves





MSP430 – Mapeamento de P4

Como mapear P4.7 para saída OUT0 do Timer B0?

Acesso ao mapeamento é habilitado com chave.

Tranca automaticamente após 32 ciclos.

```
P4DIR |= BIT7;      //P4.7 como saída
P4SEL |= BIT7;      //P4.7 recebe saída alternativa

PMAPKEYID = 0X02D52; //Liberar mapeamento
P4MAP7 = PM_TB0CCR0A;      //Sair por P4.7
```

Table 10. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_C0OUT0	-	Comparator_B output
	PM_TB0CLK	TB0 clock input	
2	PM_ADC12CLK	-	ADC12CLK
	PM_DMAE0	DMAE0 input	
3	PM_SVMOUT	-	SVM output
	PM_TB0OUTH	TB0 high impedance input TB0OUTH	
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI - input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA1TXD	USCI_A1 UART TXD (Direction controlled by USCI - output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
14	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	
	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
15	PM_UCB1SCL	USCI_B1 I2C clock (open drain and direction controlled by USCI)	
	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
16	PM_UCB1SDA	USCI_B1 I2C data (open drain and direction controlled by USCI)	
	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
17	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
	PM_C0OUT1	None	Comparator_B output
18	PM_MCLK	None	MCLK
19 - 30	Reserved	None	DVSS
31 (0FFh)[15]	PM_ANALOG	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

MSP430 – Mapeamento P1 e P2

Porta	IN	OUT
P1.0	TA0CLK	ACLK
P1.1	TA0 CCI0A	TA0 OUT0
P1.2	TA0 CCI1A	TA0 OUT1
P1.3	TA0 CCI2A	TA0 OUT2
P1.4	TA0 CCI3A	TA0 OUT3
P1.5	TA0 CCI4A	TA0 OUT4
P1.6	TA1CLK	Comparador B
P1.7	TB0 CCI0A	TB0 OUT0

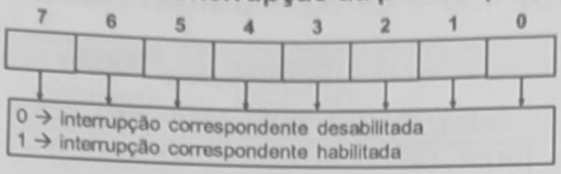
Porta	IN	OUT
P2.0	TA1 CCI1A	TA1 OUT1
P2.1	TA1 CCI2A	TA1 OUT2
P2.2	TA2 CLK	SMCLK
P2.3	TA2 CCI0A	TA2 OUT0
P2.4	TA2 CCI1A	TA2 OUT1
P2.5	TA2 CCI2A	TA2 OUT2
P2.6	DMA TRG	RTC CLK
P2.7	SPI USCI_A0	SPI USCI_B0 SPI USCI_A0

MSP430 – Exemplo Interrupção P2.1

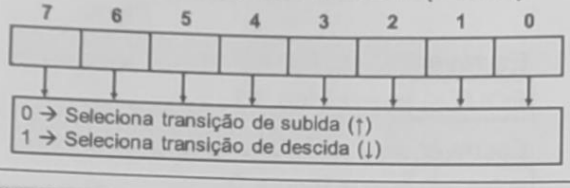
C

```
//Também pode-se usar: #pragma vector = 42
#pragma vector = PORT2_VECTOR
__interrupt void port2(void){
   int n;
   n = __even_in_range(P2IV,0x10);
   switch(n){
         ...
   }
}
```

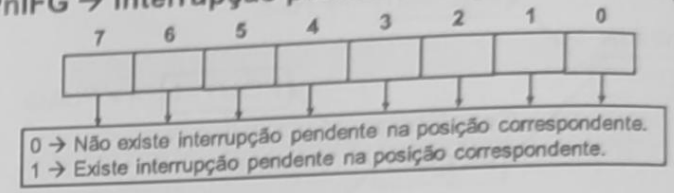
PnIE → Habilita interrupção da porta n (1 ou 2)



PnIES → Seletor do Flanco n (1 ou 2)



PnIFG → Interrupção pendente na porta n (1 ou 2)

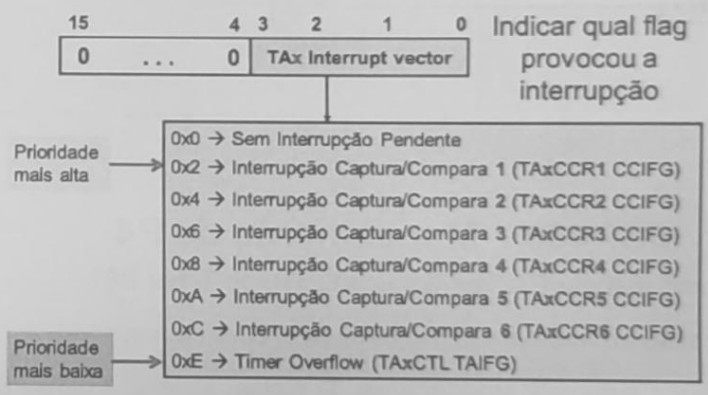


Pri	ASM	Vetor ISR em C	Fonte	Flag	IV Reg	Endereço
63	".int63"	RESET_VECTOR	Reset	WDTIFG, KEYV	SYSRSTIV	0xFFFE
62	".int62"	SYSNMI_VECTOR	System NMI	SVMLIFG, ...	SYSSNIV	0XFFFC
61	".int61"	UNMI_VECTOR	User NMI	NMIIFG, OFIFG, ...	SYSUNIV	0xFFFA
60	".int60"	COMPB_VECTOR	Comp_B	CBIV	CBIV	0xFFF8
59	".int59"	TIMER_B0_VECTOR	TB0	TB0CCR0 CCIFG0	-	0xFFF6
58	".int58"	TIMER_B1_VECTOR	TB0	CCIFG1 a CCIFG6	TB0IV	0xFFF4
57	".int57"	WDT_VECTOR	Watch Dog	WDTIFG	-	0xFFF2
56	".int56"	USCI_A0_VECTOR	USCI_A0 T=Rx ou Tx	UCA0RXIFG, UCA0TXIFG	UCA0IV	0xFFF0
55	".int55"	USCI_B0_VECTOR	USCI_B0 T=Rx ou Tx	UCB0RXIFG, UCB0TXIFG	UCB0IV	0xFFEE

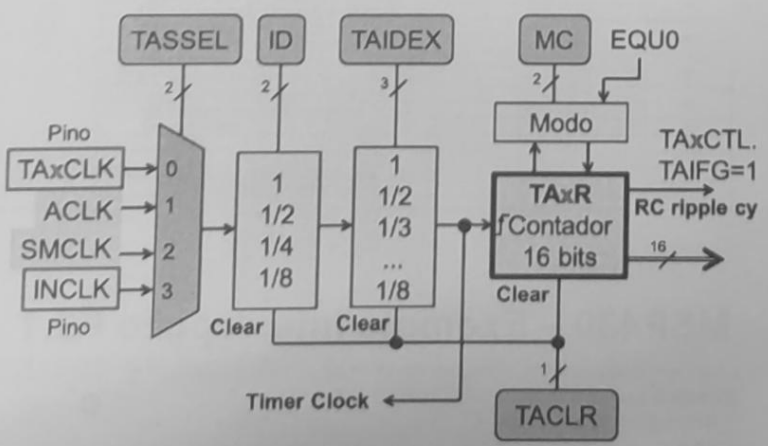
Pri	ASM	Vetor ISR em C	Fonte	Flag	IV Reg	Endereço
54	".int54"	ADC12_VECTOR	ADC12_A	ADC12IFG0 a ADC12IFG15	ADC12IV	0XFFEC
53	".int53"	TIMER0_A0_VECTOR	TA0	TA0CCR0 CCIFG0	-	0xFFEA
52	".int52"	TIMER0_A1_VECTOR	TA0	CCIFG1 a CCIFG6	TA0IV	0xFFE8
51	".int51"	USB_UBM_VECTOR	USB_UBM	USB interrupts	USBIV	0xFFE6
50	".int50"	DMA_VECTOR	DMA	DMA0IFG, DMA1IFG, DMA2IFG	DMAIV	0xFFE4
49	".int49"	TIMER1_A0_VECTOR	TA1	TA1CCR0 CCIFG0	-	0xFFE2
48	".int48"	TIMER1_A1_VECTOR	TA1	CCIFG1 a CCIFG6	TA1IV	0xFFE0

Pri	ASM	Vetor ISR em C	Fonte	Flag	IV Reg	Endereço
47	".int47"	PORT1_VECTOR	I/O Port 1	P1IFG.0 a P1IFG.7	P1IV	0xFFDE
46	".int46"	USCI_A1_VECTOR	USCI_A1 T=Rx ou Tx	UCA1RXIFG, UCA1TXIFG	UCA1IV	0XFFDC
45	".int45"	USCI_B1_VECTOR	USCI_B1 T=Rx ou Tx	UCB1RXIFG, UCB1TXIFG	UCB1IV	0xFFDA
44	".int44"	TIMER2_A0_VECTOR	TA2	TA2CCR0 CCIFG0	-	0xFFD8
43	".int43"	TIMER2_A1_VECTOR	TA2	CCIFG1 a CCIFG6	TA2IV	0xFFD6
42	".int42"	PORT2_VECTOR	I/O Port 2	P2IFG.0 a P2IFG.7	RTCIV	0xFFD4
41	".int41"	RTC_VECTOR	RTC_A	RTCRDYIFG, RTCTEVIFG, ...	-	0xFFD2
...	-	-	-	-	-	-
0	-	-	-	-	-	-

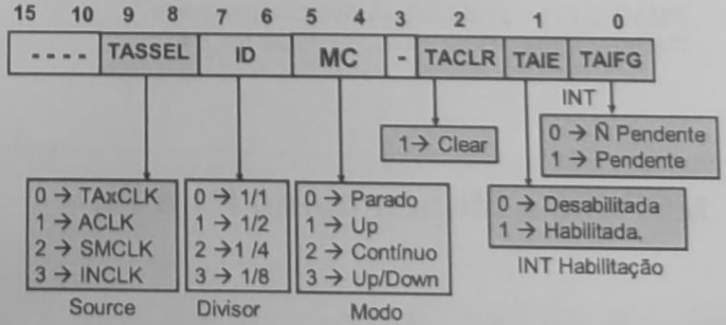
TAxIV → Vetor de Interrupção do Timer Ax



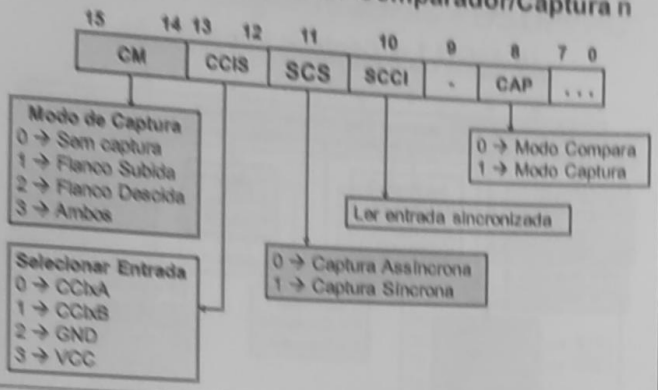
Seleção do clock para TAxR



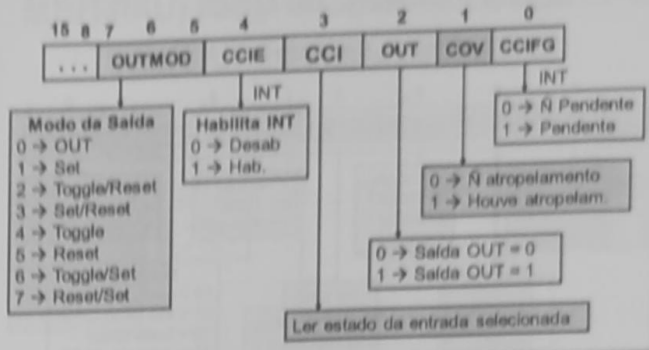
TAxCTL → Controle do Timer Ax



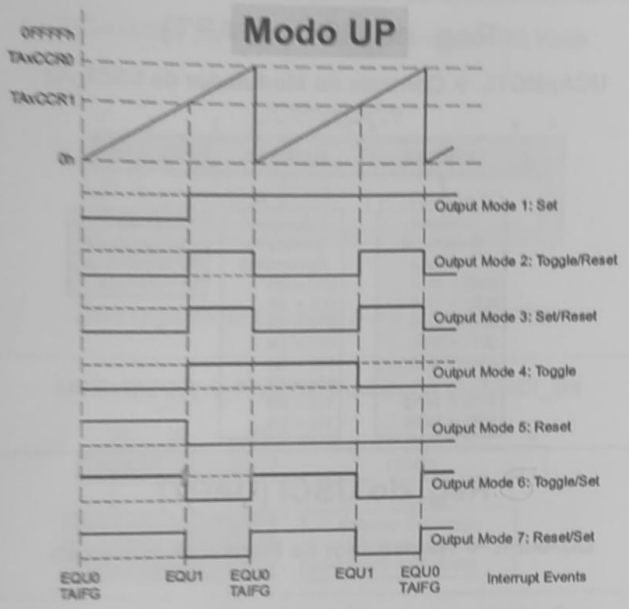
TAxCCTLn → Controle do Comparador/Captura n



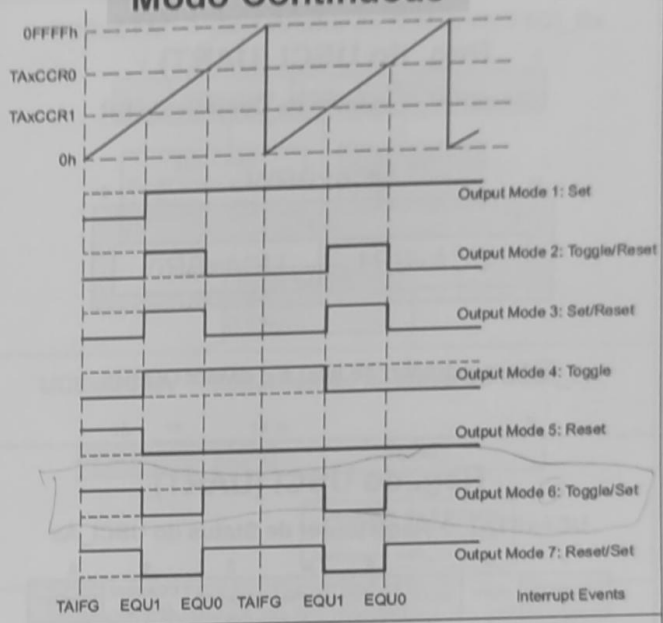
TAxCCTLn → Controle do Comparador/Captura n



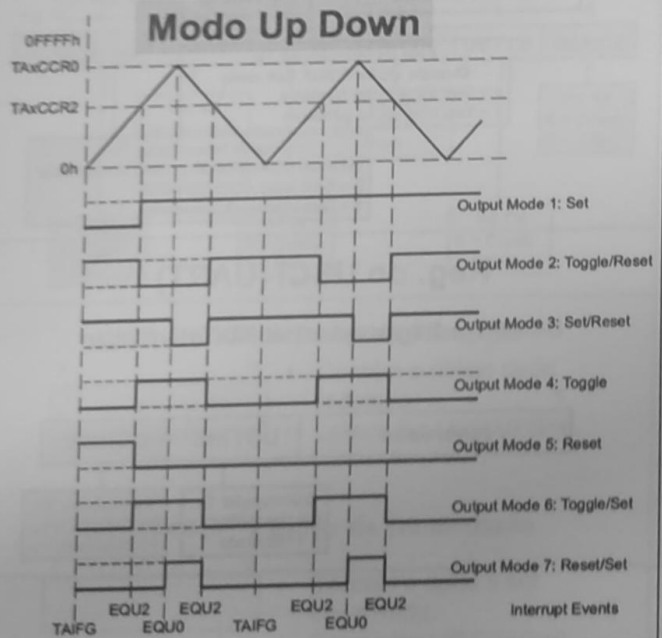
Modo UP



Modo Continuous



Modo Up Down



MSP430 – F5529 Timers

TA0
Instância 0 do Timer A
TA0R
TA0CCR0
TA0CCR1
TA0CCR2
TA0CCR3
TA0CCR4

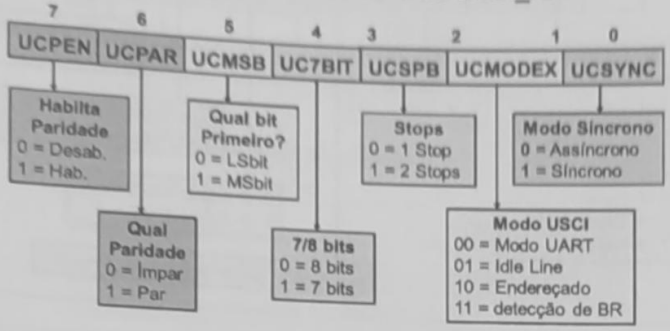
TA1
Instância 1 do Timer A
TA1R
TA1CCR0
TA1CCR1
TA1CCR2

TA2
Instância 2 do Timer A
TA2R
TA2CCR0
TA2CCR1
TA2CCR2

TB0
Instância 0 do Timer B
TB0R
TB0CCR0
TB0CCR1
TB0CCR2
TB0CCR3
TB0CCR4
TB0CCR5
TB0CCR6

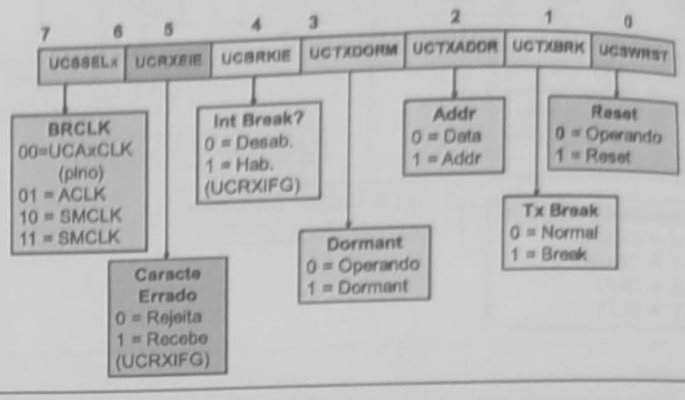
MSP430 – Reg. do USCI (UART)

UCAxCTL0 → Controle 0 do USCI_Ax



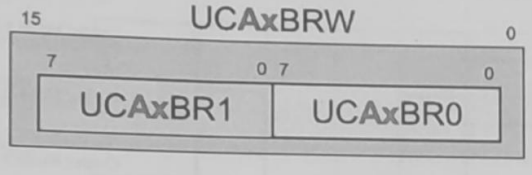
MSP430 – Reg. do USCI (UART)

UCAxCTL1 → Controle 1 do USCI_Ax



Reg. do USCI (UART)

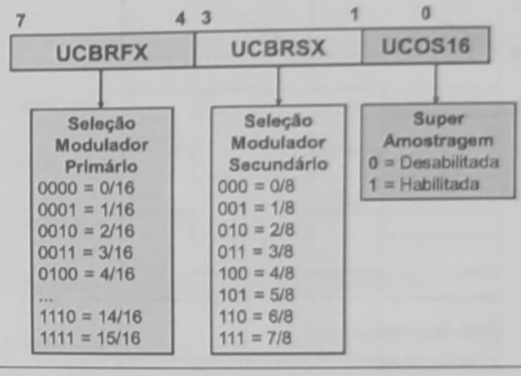
UCAxBRW → Palavra de Controle do BR



Este registrador (16 bits) é o divisor UCBRx

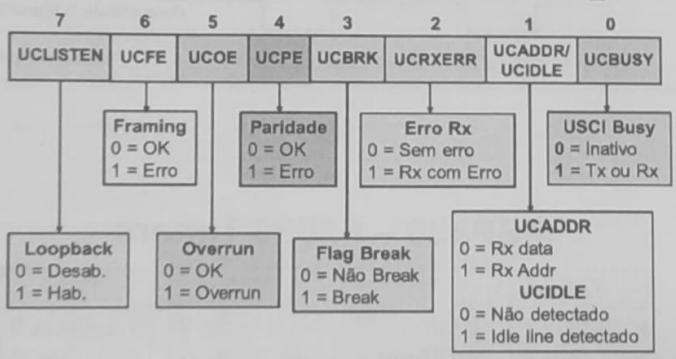
Reg. do USCI (UART)

UCAxMCTL → Controle do Modulador de USCI_Ax



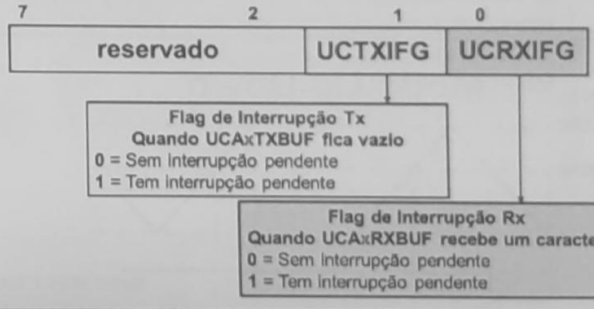
Reg. do USCI (UART)

UCAxSTAT → Registrador de Status do USCI_Ax



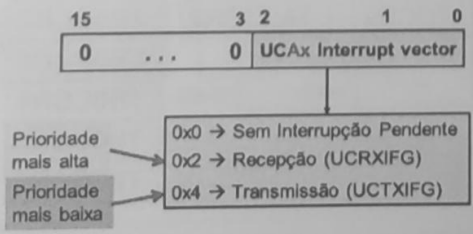
Reg. do USCI (UART)

UCAxIFG → Registrador de Flags de Interrupção



Reg. do USCI (UART)

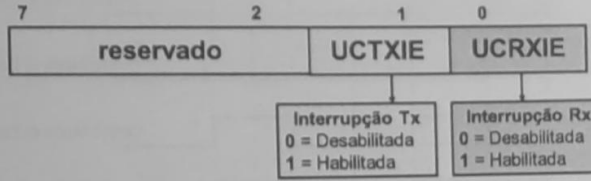
UCAxIV → Vetor de Interrupção do UCA



Indicar qual flag provocou a interrupção

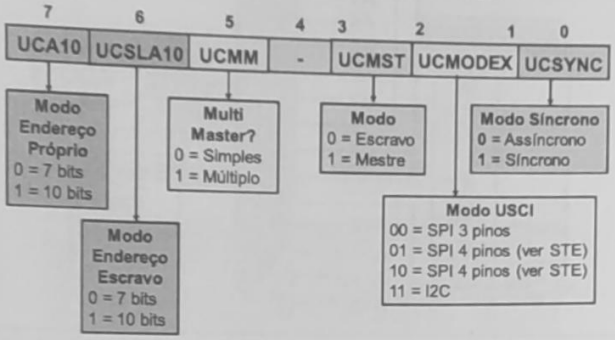
Reg. do USCI (UART)

UCAxIE → Registrador Habilita Interrupção



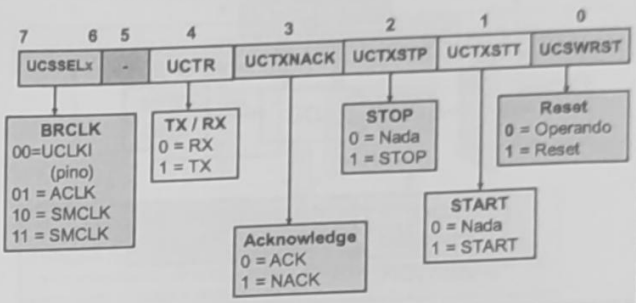
MSP430 – Registradores - USCI - I²C

UCBxCTL0 → Controle 0 do USCI_Bx

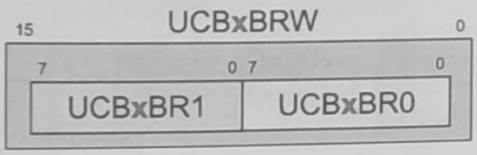


MSP430 – Registradores - USCI - I²C

UCBxCTL1 → Controle 1 do USCI_Bx

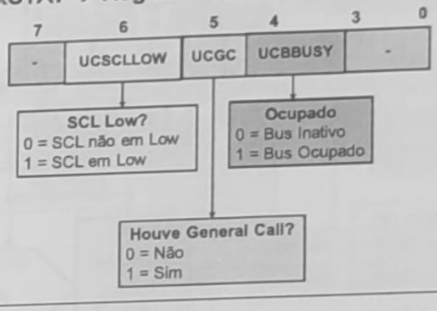


UCAxBRW → Palavra de Controle de Bit Rate

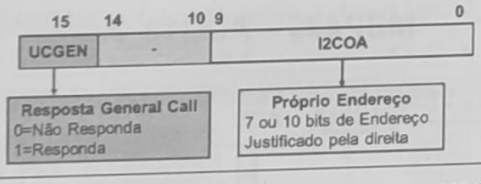


Este registrador (16 bits) é o divisor UCBRx

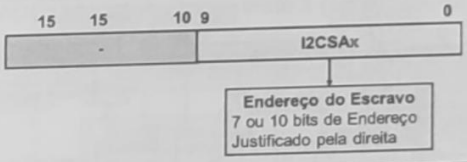
UCBxSTAT → Registrador de Status do USCI_Bx



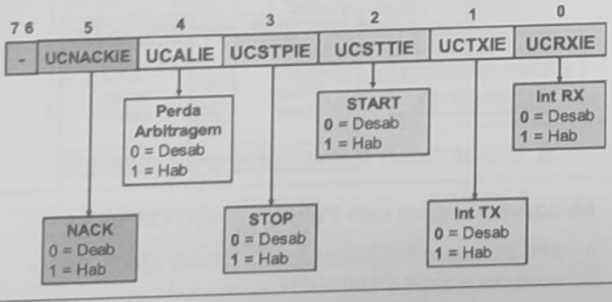
UCBxI2COA → Próprio Endereço do USCI_Bx



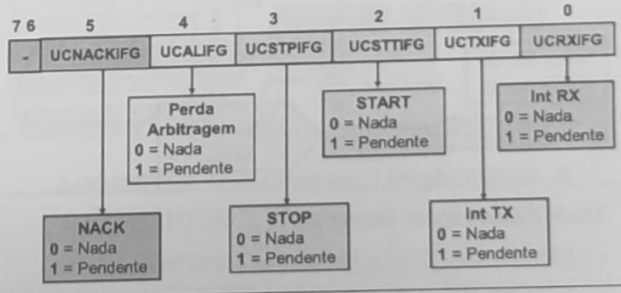
UCBxI2CSA → Endereço do Escravo do USCI_Bx



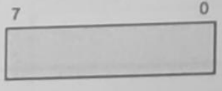
UCBxIE → Habilitação de Interrupções do USCI_Bx



UCBxIFG → Flags de Interrupções do USCI_Bx

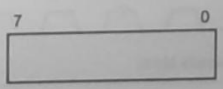


UCBxRXBUF → Buffer de Recepção



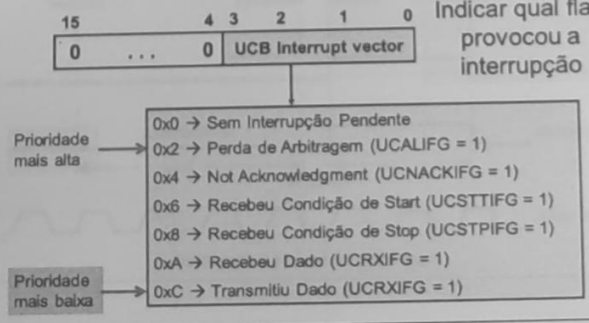
- Contém o último dado recebido.
- Leitura faz UCRXIFG=0.

UCBxTXBUF → Buffer de Transmissão

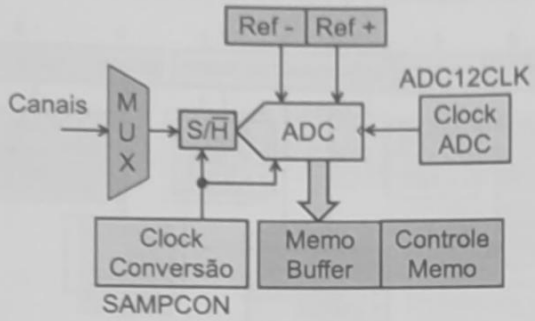


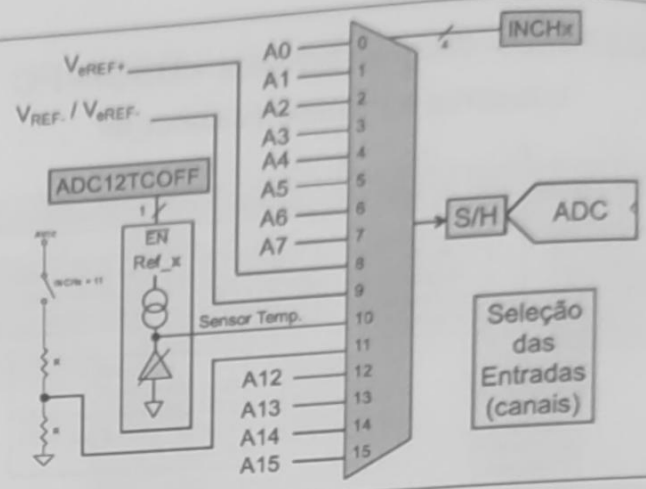
- Contém o dado a ser transmitido.
- Escrita faz UCTXIFG=0.

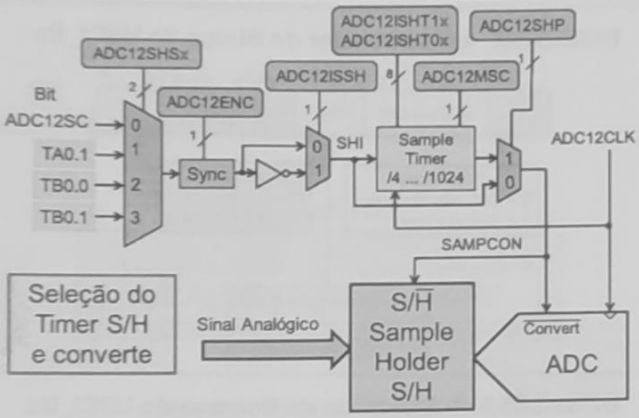
UCBxIV → Vetor de Interrupção do USCI_Bx

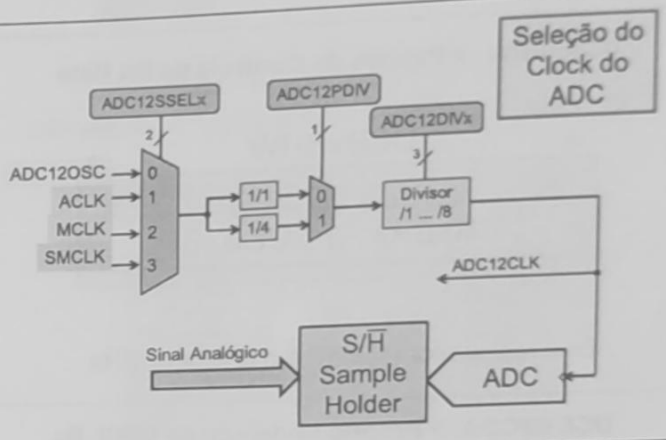


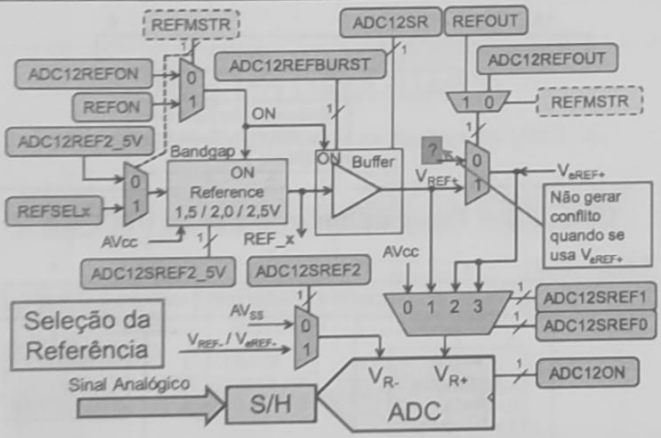
MSP430 – ADC12_A

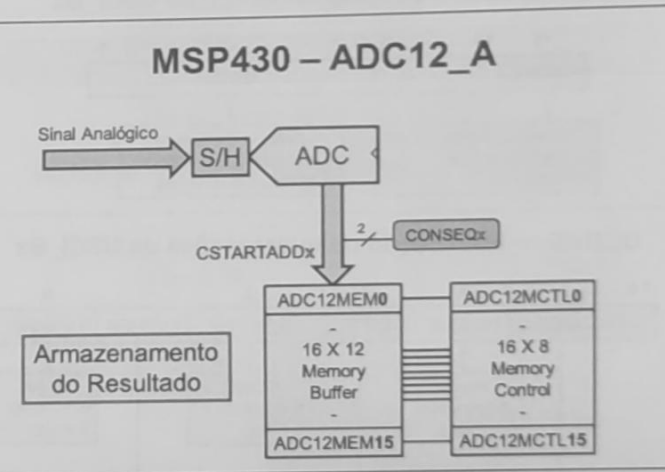












Modo Amostragem Estendida ADC12SHP = 0

- SHI = SAMPCON e determina o intervalo de amostragem.

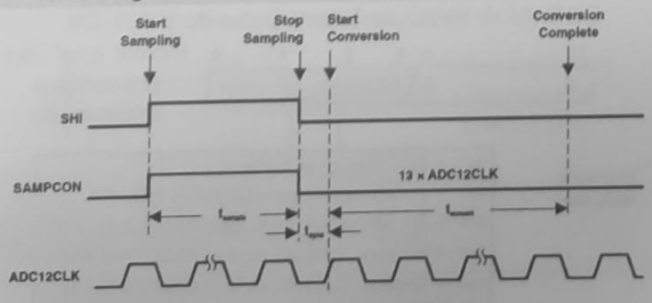


Figure 28-4. Extended Sample Mode

Modo Amostragem com Pulso ADC12SHP = 1

- SHI dispara o temporizador de amostragem, que controla o sinal SAMPCON.

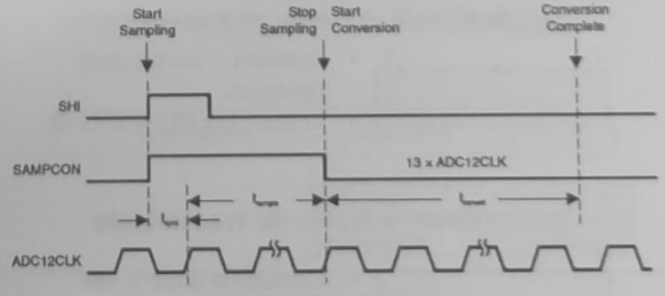
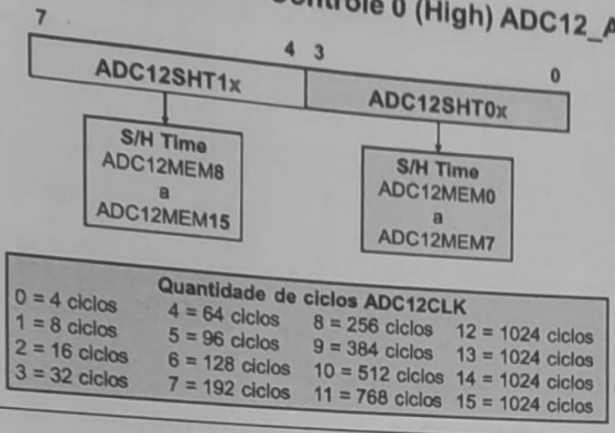


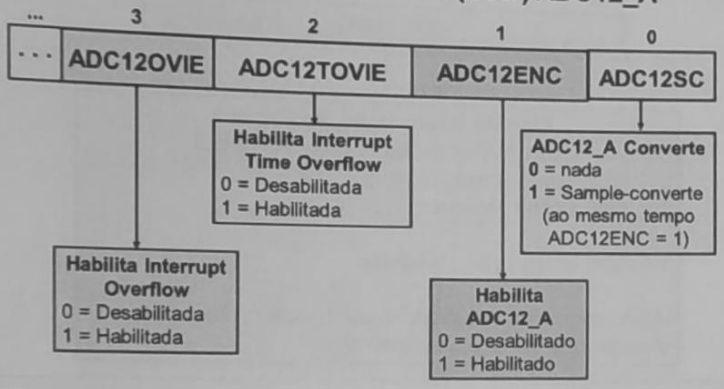
Figure 28-5. Pulse Sample Mode

MSP430 – ADC12_A - Registradores

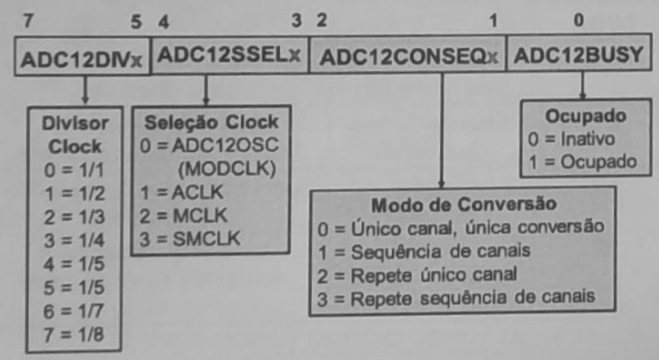
ADC12CTL0_H → Controle 0 (High) ADC12_A



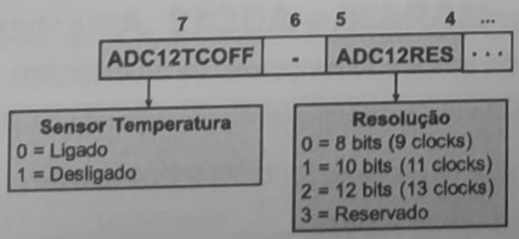
ADC12CTL0_L → Controle 0 (Low) ADC12_A



ADC12CTL1_L → Controle 1 (Low) ADC12_A

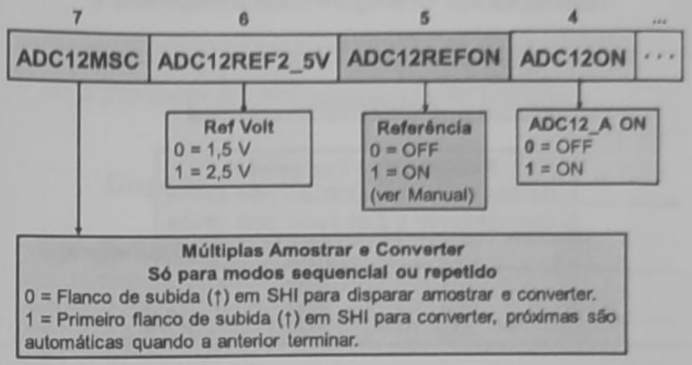


ADC12CTL2_L → Controle 2 (Low) ADC12_A

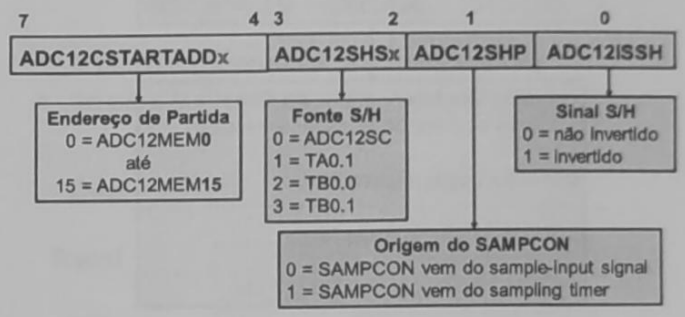


MSP430 – ADC12_A - Registradores

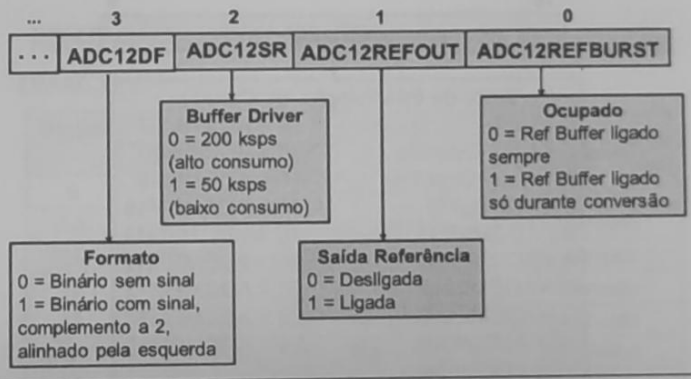
ADC12CTL0_L → Controle 0 (Low) ADC12_A



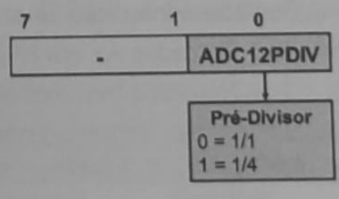
ADC12CTL1_H → Controle 1 (High) ADC12_A



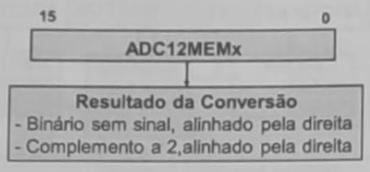
ADC12CTL2_L → Controle 2 (Low) ADC12_A



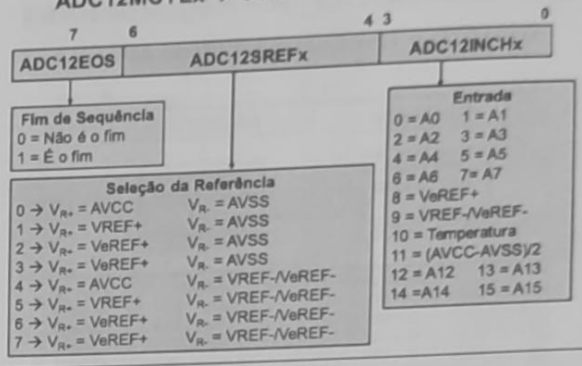
ADC12CTL2_H → Controle 2 (High) ADC12_A



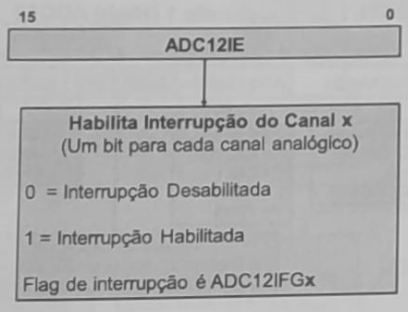
ADC12MEMx → Registrador Conversão x



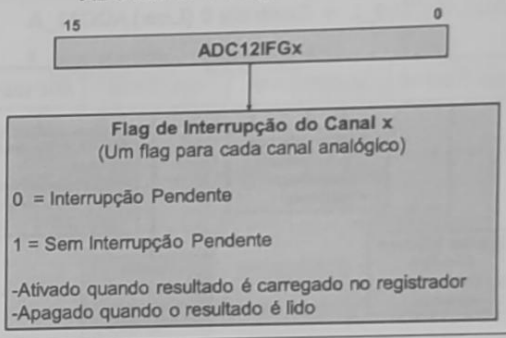
ADC12MCTLx → Controle x Reg de Memória



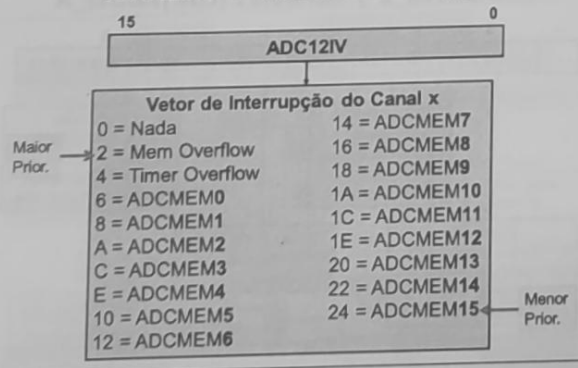
ADC12IE → Habilita Interrupções



ADC12IFG → Flags de Interrupção



ADC12IFG → Vetores de Interrupção



ADC12CONSEQx	Modo	Operação
00	Um canal, uma conversão	Um único canal é convertido uma única vez
01	Seq. de Canais (Autoscan)	Uma seq. de canais é convertido uma única vez
10	Repete um canal	Um único canal é convertido repetidamente
11	Repete Seq. de Canais (Rep. Autoscan)	Uma seq. de canais é convertida repetidamente

MSP430 – ADC12_A

Considerações sobre intervalo de amostragem

- SAMPCON = 0 → Entradas Ax em Hi-Z.
- SAMPCON = 1 → Entradas têm modelo abaixo.
- Capacitor do S/H precisa de tempo para se carregar de tal forma que $V_S - V_C < ½$ bit V_S.

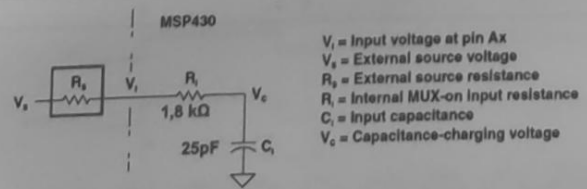


Figure 28-6. Analog Input Equivalent Circuit

MSP430 – ADC12_A

Considerações sobre intervalo de amostragem

- Cálculo do tempo de amostragem depende de R_S

$$t_{sample} > (R_S + R_I) \times ln(2^{n+1}) \times C_I + 800\,ns$$

- Substituindo os valores:

$$t_{sample} > (R_S + 1{,}8\,k) \times ln(2^{n+1}) \times 25\,p + 800\,ns$$

- Por exemplo, para R_S = 10 kΩ e n = 12 bits:

$$t_{sample} > 3{,}46\,\mu s$$

MSP430 – DMA - Modos

DMADT	Modo	Descrição
000	Simples	Um disparo para cada transferência. Se DMAxSZ = 0 → DMAEN = 0.
001	Bloco	Um disparo para transferir todo o bloco. Ao final do bloco → DMAEN = 0.
010 011	Rajada	Um disparo para transferir todo o bloco. CPU intervalada com as transferências. Ao final do bloco → DMAEN = 0.
100	Simples repetido	Um disparo para cada transferência. DMAEN permanece habilitado.
101	Bloco repetido	Um disparo para transferir todo o bloco. DMAEN permanece habilitado.
110 111	Rajada repetida	Um disparo para transferir todo o bloco. CPU intervalada com as transferências. DMAEN permanece habilitado.

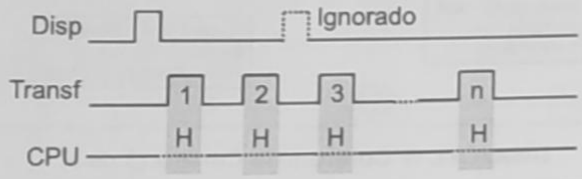
DMAxSZ = quantidade de transferências programada.

MSP430 – DMA - Simples

- Precisa de um disparo para cada transferência.
- CPU entra em Hold por um curto período.

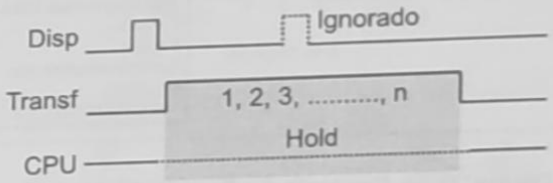
MSP430 – DMA - Rajada

- O primeiro disparo inicia a transferência.
- Só pára quando contador chegar a zero.
- CPU intercalada com as transferências.



MSP430 – DMA - Bloco

- O primeiro disparo inicia a transferência.
- Só pára quando contador chegar a zero.



MSP430 – DMA – Fonte de Disparos

DMACTLx

Trigger	Canal		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG

MSP430 – DMA – Fonte de Disparos

DMACTLx

Trigger	Canal		
	0	1	2
9	Reservado	Reservado	Reservado
10	Reservado	Reservado	Reservado
11	Reservado	Reservado	Reservado
12	Reservado	Reservado	Reservado
13	Reservado	Reservado	Reservado
14	Reservado	Reservado	Reservado
15	Reservado	Reservado	Reservado

MSP430 – DMA – Fonte de Disparos

DMACTLx

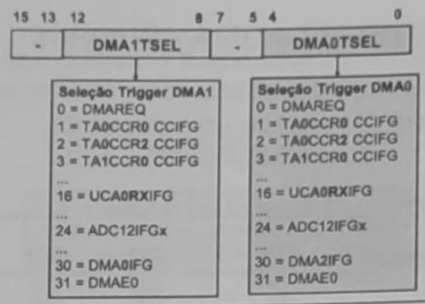
Trigger	Canal		
	0	1	2
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG

MSP430 – DMA – Fonte de Disparos

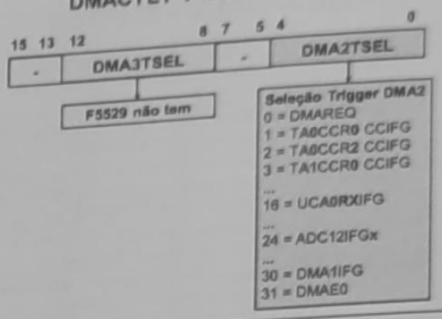
DMACTLx

Trigger	Canal		
	0	1	2
24	ADC12IFGx	ADC12IFGx	ADC12IFGx
25	Reservado	Reservado	Reservado
26	Reservado	Reservado	Reservado
27	USB FNRXD	USB FNRXD	USB FNRXD
28	USB Ready	USB Ready	USB Ready
29	MPY Ready	MPY Ready	MPY Ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

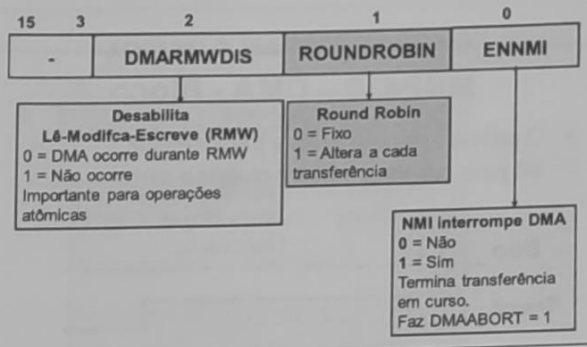
DMACTL0 → Controle 0 do DMA



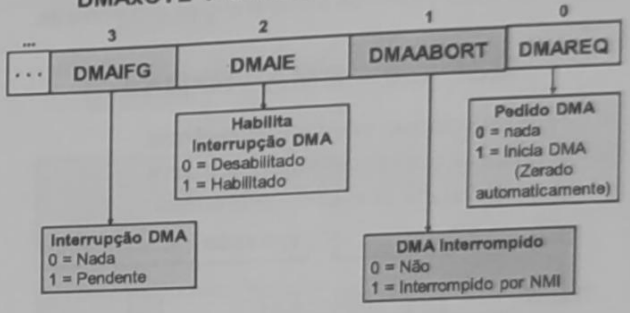
DMACTL1 → Controle 1 do DMA



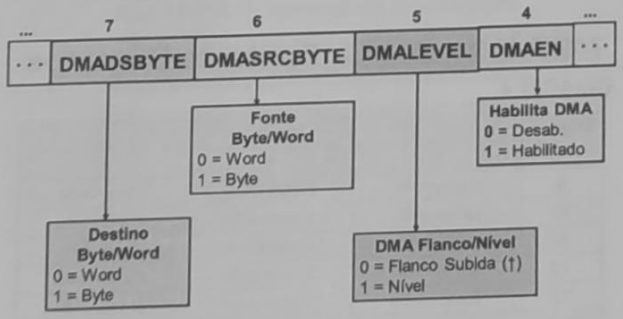
DMACTL4 → Controle 4 do DMA



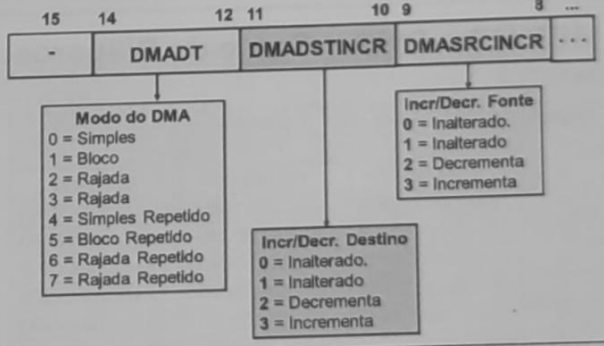
DMAxCTL → Controle do Canal x (1 de 3)



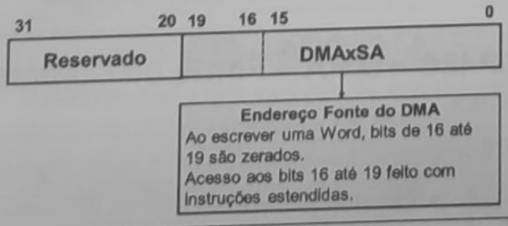
DMAxCTL → Controle do Canal x (2 de 3)



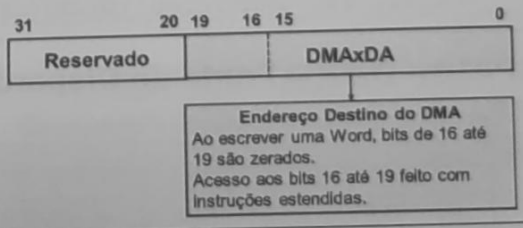
DMAxCTL → Controle do Canal x (3 de 3)



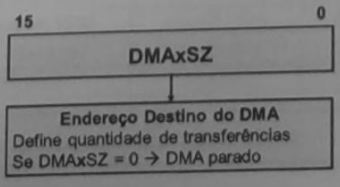
DMAxSA → Endereço Fonte do Canal x



DMAxDA → Endereço Destino do Canal x



DMAxSZ → Quantidade de operações do Canal x



DMAIV → Vetor de Interrupções