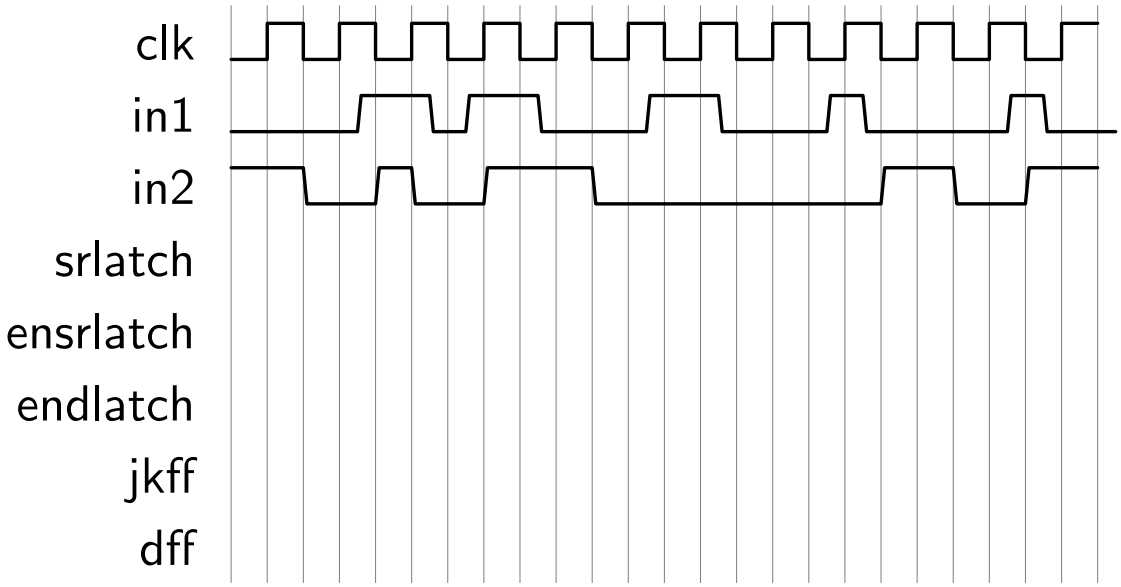
CE/CZ1055 Digital Logic
Tutorial 8: Sequential Logic

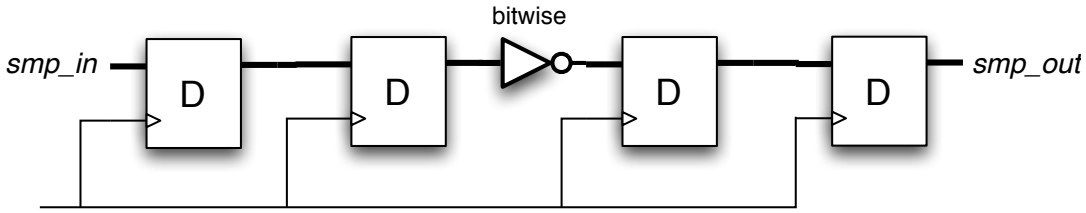
1. The C input in the timing diagram below is connected to the control/enable/clk input of the following circuits:
   - SR-latch (no enable/control)
   - Enabled SR-Latch
   - Enabled D-type latch
   - JK flip-flop
   - D flip-flop

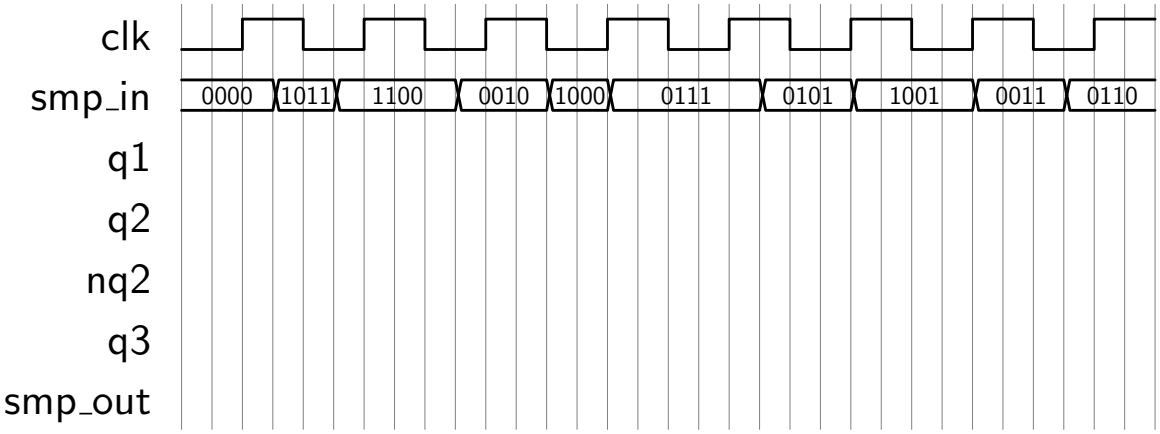
   For the D latch and flip-flop, the in1 input is connected to the D input, and in2 is left disconnected. For the SR-Latches, in1 is connected to the S input and in2 is connected to the R input. For the JK flip-flop, in1 is connected to the J input and in2 is connected to the K input.

   Complete the timing diagram showing the outputs of the four sequential circuits. Indicate metastability/undefined output by shading the relevant area.



2. A bank of 4-bit registers is arranged as per the diagram below, to form a FIFO, with a bitwise inversion in the middle. The input shown in the diagram is applied to the leftmost register. All registers share the same clock. Show a timing diagram for the output at the rightmost register. A bitwise inversion simply inverts each bit of the signal individually. Write down the resulting hexadecimal number sequence at the output





3. Can you deduce the behavior of this circuit? You need to assume some propagation delay through an inverter.