Answers

1 (a) Low-state dc noise immunity = VIL(max) - VOL(max)

Circuit A: 0.9 – 0.4 = 0.5V

Circuit B: 0.7 – 0.3 = 0.4V

Circuit A has better Low-state dc noise immunity.

(b) High-state dc noise immunity = VOH(min) - VIH(min)

Circuit A: 2.2 – 1.6 = 0.6V

Circuit B: 2.5 – 1.8 = 0.7V

Circuit B has better High-state dc noise immunity.

(c) Compare the propagation delays tPHL and tPLH.

Circuit A has much shorter delays than B.

Thus circuit A can operate at higher frequencies than B.

2. The buffer enable input has a bubble drawn. This means it is an active-Low enable input.

When Direction=0, the top buffer is enabled while the bottom buffer is disabled. Data can be transmitted from A to B.

When Direction=1, the top buffer is disabled while the bottom buffer is enabled. Data can be transmitted from B to A.

3. When B=C=1, both Q5 and Q7 turn on, both Q6 and Q8 turn off, Z will go Low. Alternatively, when A=0, Q2 turns on, Q1 turns off, Q3 turns on, Q4 turns off, Z will go Low.

Thus Z = (B’ + C’) A [POS]

Check: when B=0, Q6 turns on, Q5 turns off. When C=0, Q8 turns on, Q7 turns off. If A=1 at the same time, Q1 turns on and Q2 turns off, Q4 turns on and Q3 turns off, Z will go High.

Thus Z = AB’ + AC’ [SOP]