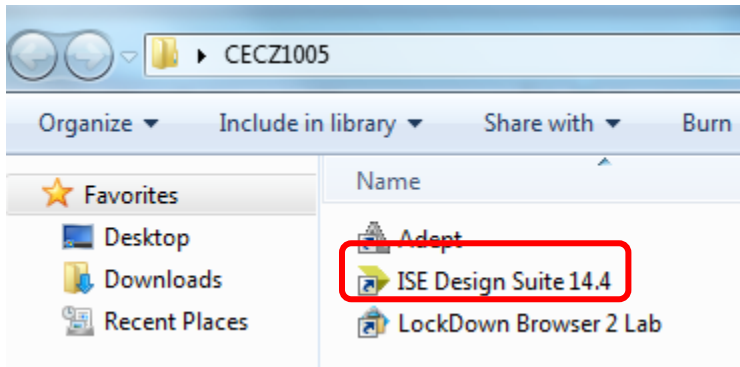
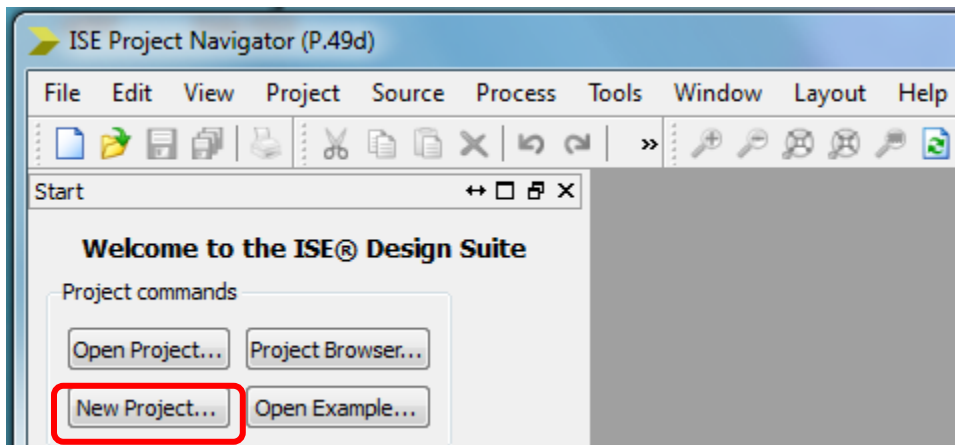


Lab 3 ISE guide

1. Go to CECZ1005 folder. Double click ISE Design Suite 14.4 shortcut



2. Create New Project. Specify project name and working directory.



Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name:	Lab3
Location:	Y:\Lab3
Working Directory:	Y:\
Description:	

Select the type of top-level source for the project

Top-level source type:	HDL
------------------------	-----

3. Select the correct Family, Device and Package.

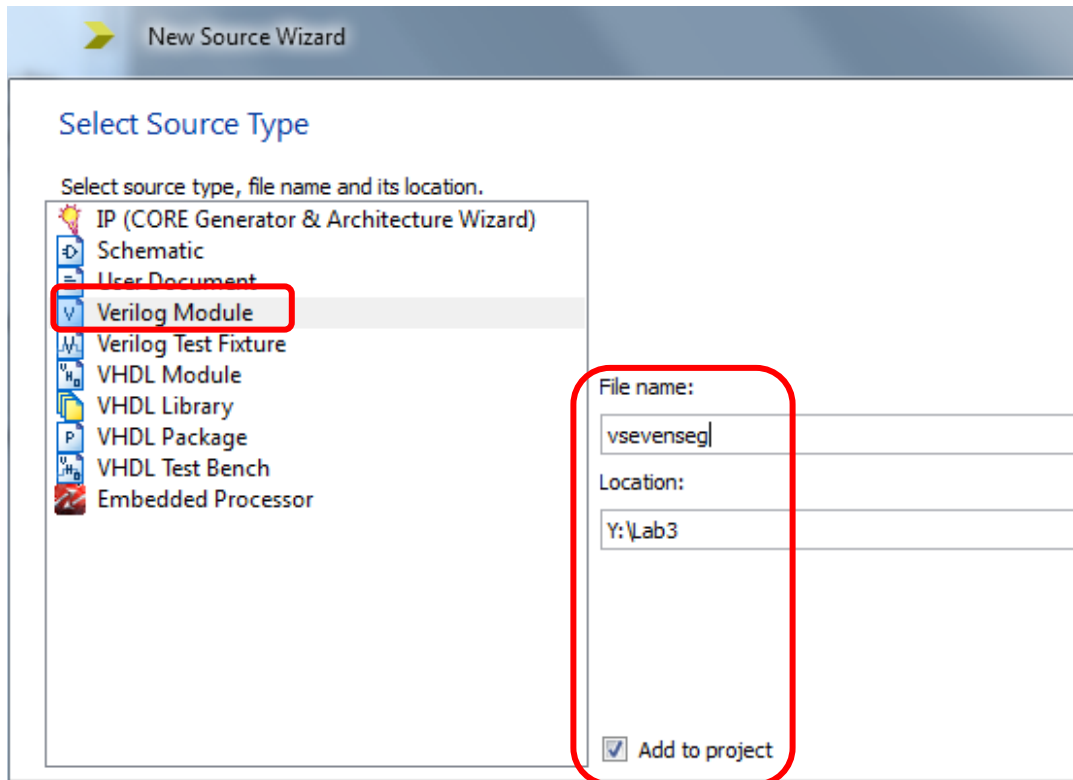
New Project Wizard

Project Settings

Specify device and project properties.
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan6
Device	XC6SLX45
Package	CSG324
Speed	-3
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog

4. Create a new Verilog Module vsevenseg and add it to project



5. Define the inputs and outputs of the vsevenseg circuit

New Source Wizard

Define Module

Specify ports for module.

Module name

Port Name	Direction	Bus	MSB	LSB
x	input	<input checked="" type="checkbox"/>	3	0
seg	output	<input checked="" type="checkbox"/>	6	0
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		

seg is an output

More Info Next Cancel

6. Verilog circuit with inputs and outputs defined

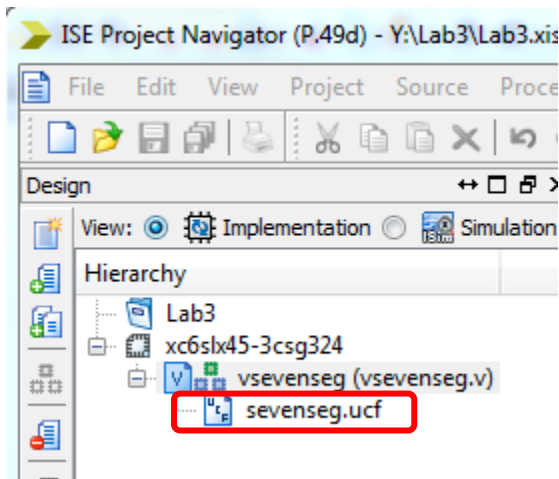
```
1  `timescale 1ns / 1ps
2  ///////////////////////////////////////////////////.
3  // Company:
4  // Engineer:
5  //
6  // Create Date:    10:23:58 02/09/2017
7  // Design Name:
8  // Module Name:    vsevenseg
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////.
21 module vsevenseg(
22     input [3:0] x,
23     output [6:0] seg
24 );
25
26
27 endmodule
28
```

Paste incomplete code from seg.v between lines 25 & 26

Design Summary | vsevenseg.v

Remember to key in the Boolean expressions (in Verilog syntax) for the remaining segments. Otherwise the circuit design is incomplete.

7. After sevenseg.ucf has been added to the project. Double click on it to edit.



Remember to key in the UCF statements for the remaining segments. Otherwise there will be error in the circuit implementation.

8. Check Family, Device and Package. Select vsevenseg.v and double click Generate Programming File

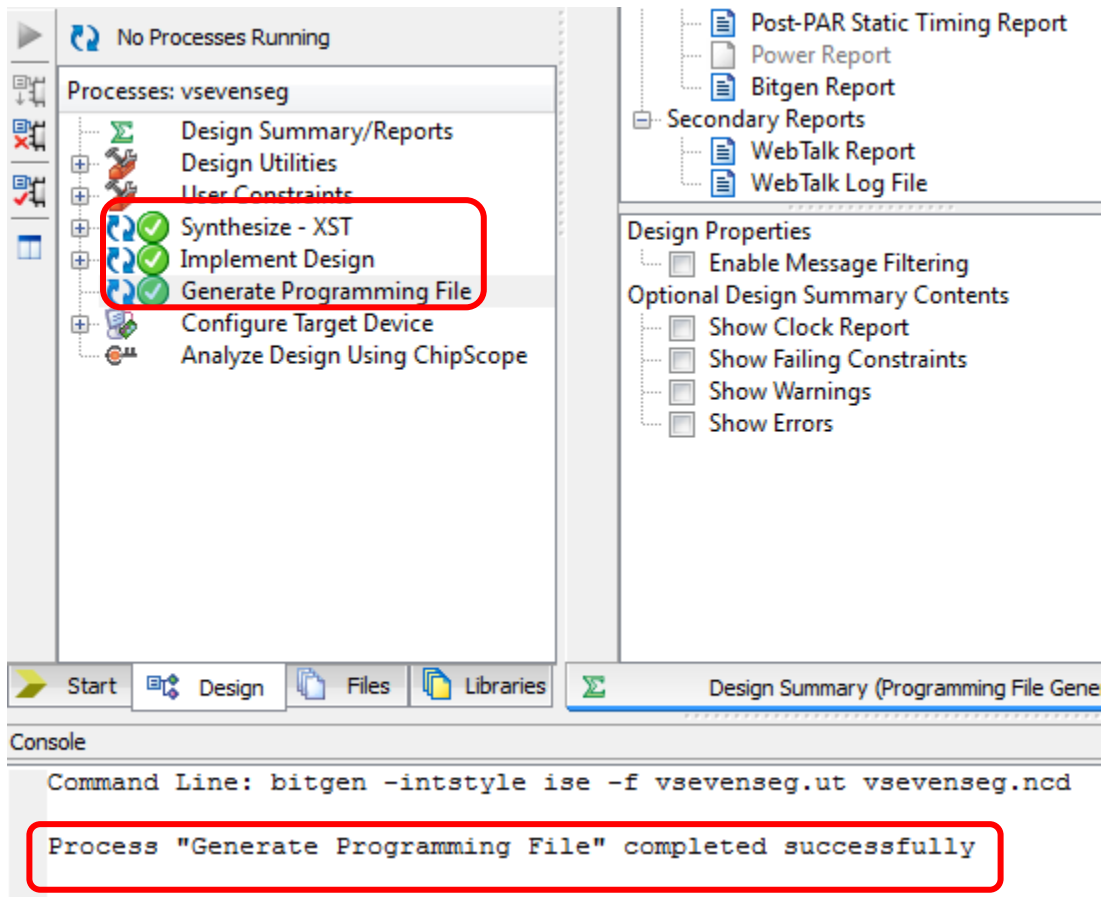
The screenshot shows the ISE Project Navigator window. The top menu bar includes File, Edit, View, Project, Source, Process, Tools, and Window. The Design tab is active, showing a hierarchy of files: Lab3, xc6slx45-3csg324, vsevenseg (vsevenseg.v), and sevensseg.ucf. A red arrow points from a yellow callout box to the xc6slx45-3csg324 file. Another red arrow points from a yellow callout box to the vsevenseg (vsevenseg.v) file. A third red arrow points from a yellow callout box to the 'Generate Programming File' option in the 'Processes: vsevenseg' list. The 'Generate Programming File' option is highlighted with a red rectangle. The 'Processes: vsevenseg' list includes: Design Summary/Reports, Design Utilities, User Constraints, Synthesize - XST, Implement Design, Generate Programming File, Configure Target Device, and Analyze Design Using ChipScope. The right side of the window shows a list of numbers 1 through 30, with some numbers having corresponding text to their right.

Right click to modify if Family-Device-Package is not correctly specified.

Select vsevenseg

Double-click Generate Programming File

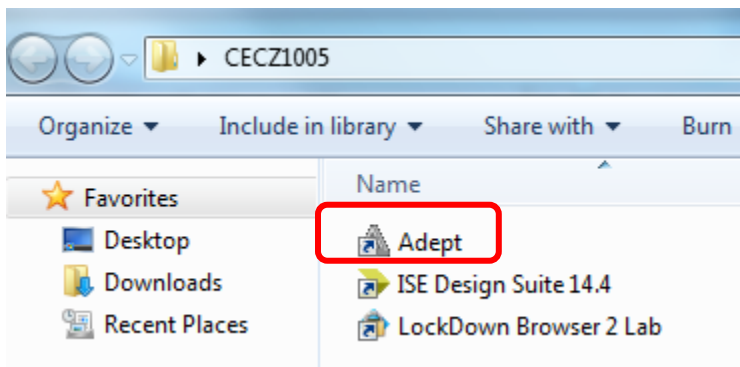
It may take several minutes to complete the bit file generation. Do not program the FPGA if there is error while generating the bit file.



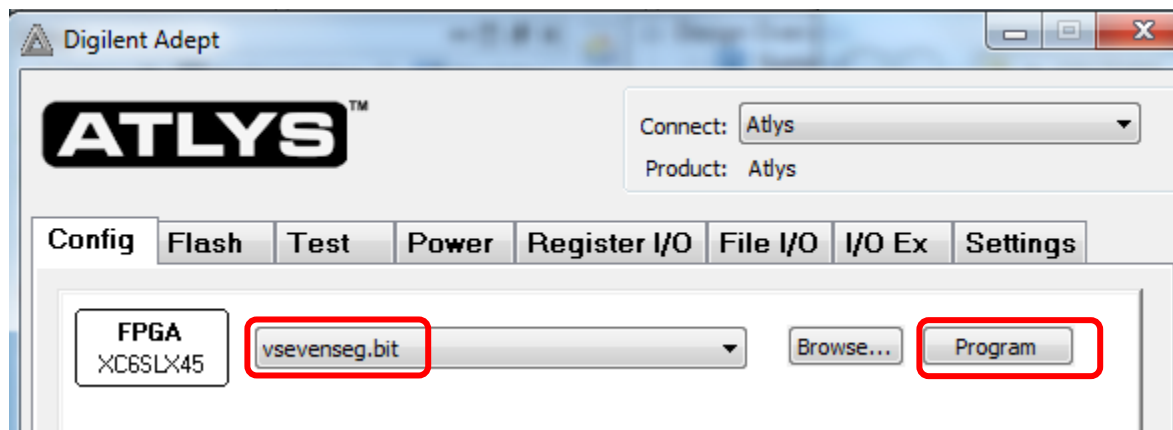
9. Power up the FPGA board before programming (Turn on the power supply main first followed by the switch on board)



10. Double click Adept shortcut icon in CECZ1005 folder



11. Select the correct .bit file and click Program



After programming is completed your circuit on the FPGA is ready for testing.

After you have modified the Verilog file (which specifies the logic circuit design) or the UCF file (which specifies the inputs/outputs on the FPGA) you need to re-generate the bit file (step 8) and re-program the FPGA (step 11) in order to observe the effect of your modification on the circuit behaviour.