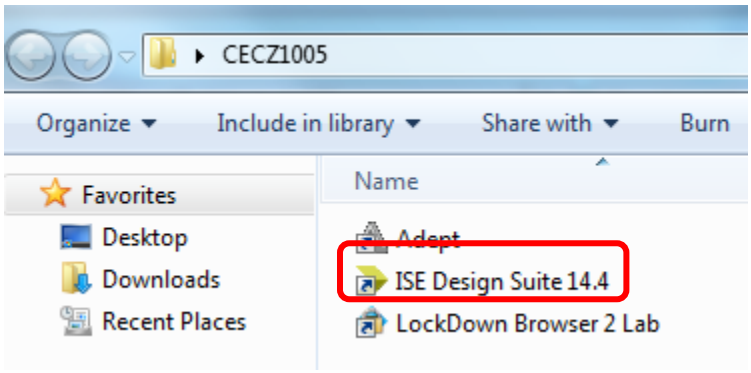
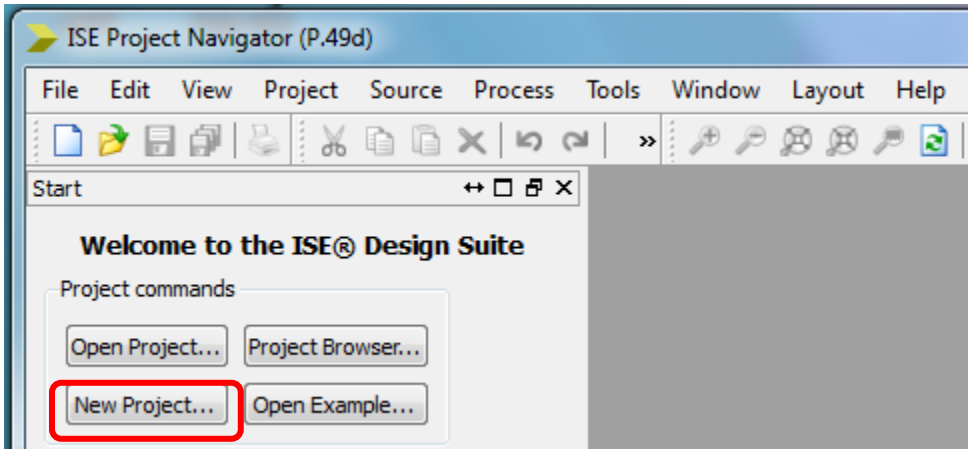
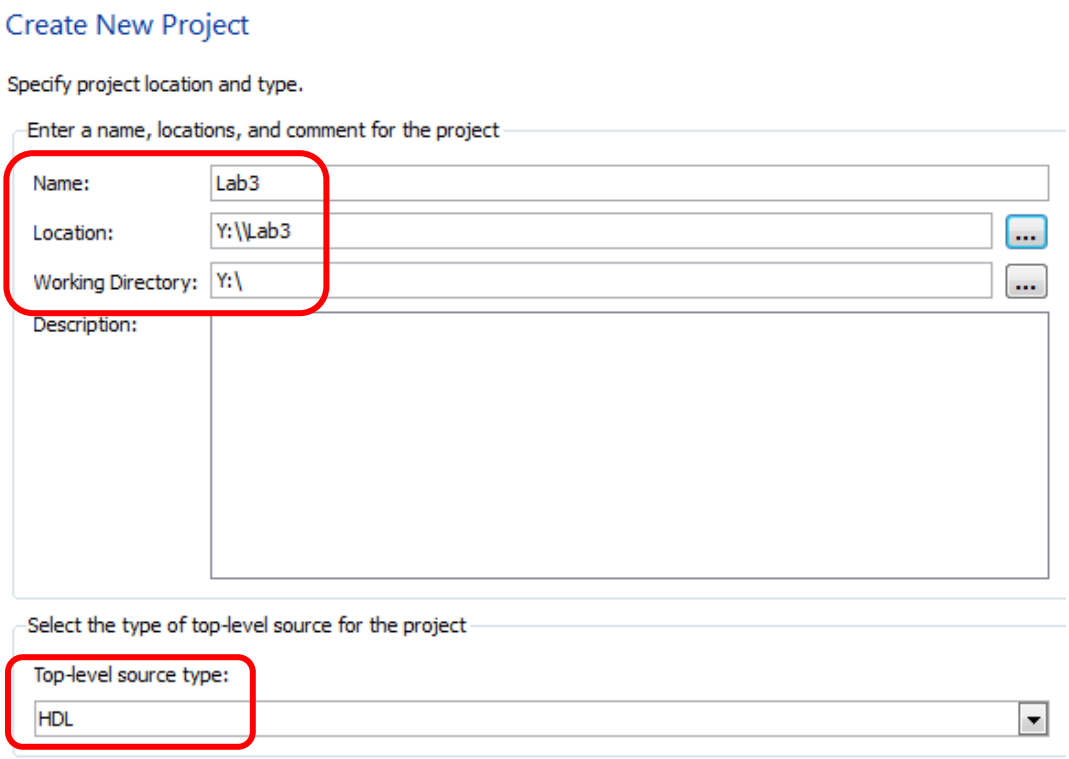
Lab 3 ISE guide

1. **Go to CECZ1005 folder. Double click ISE Design Suite 14.4 shortcut**

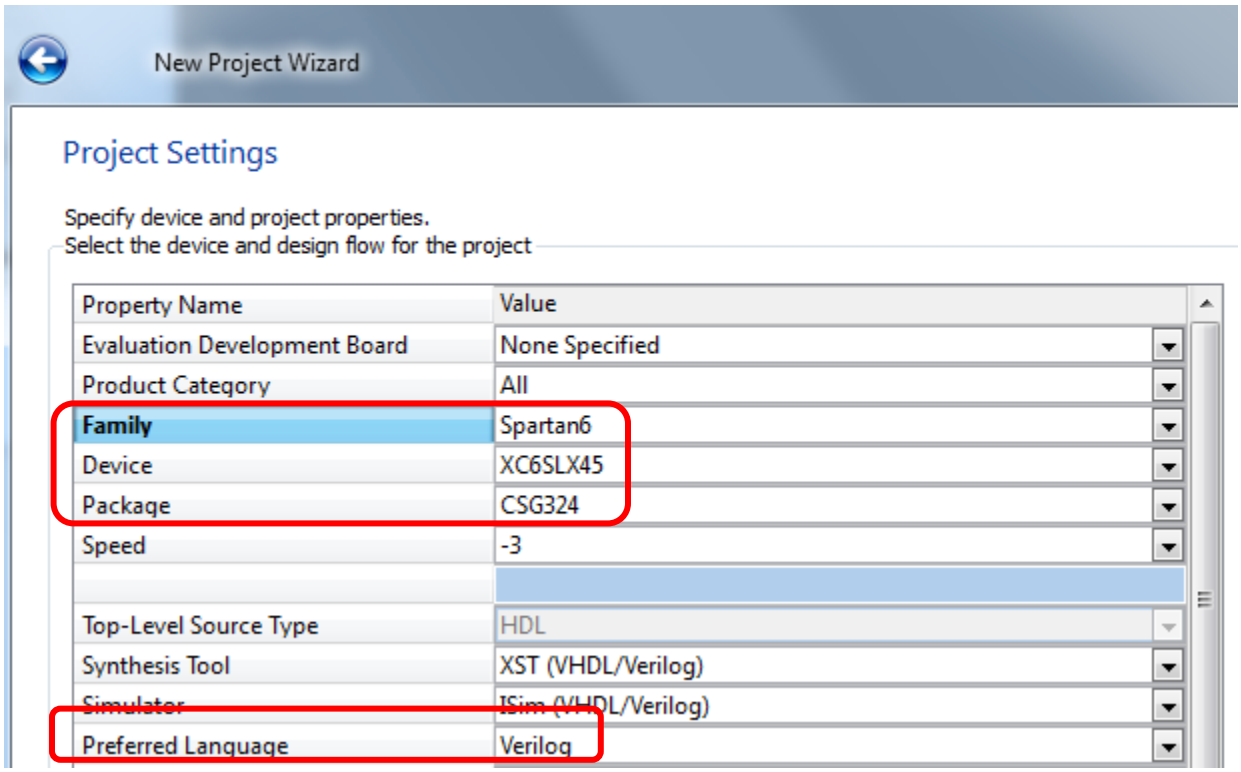


2. **Create New Project. Specify project name and working directory.**

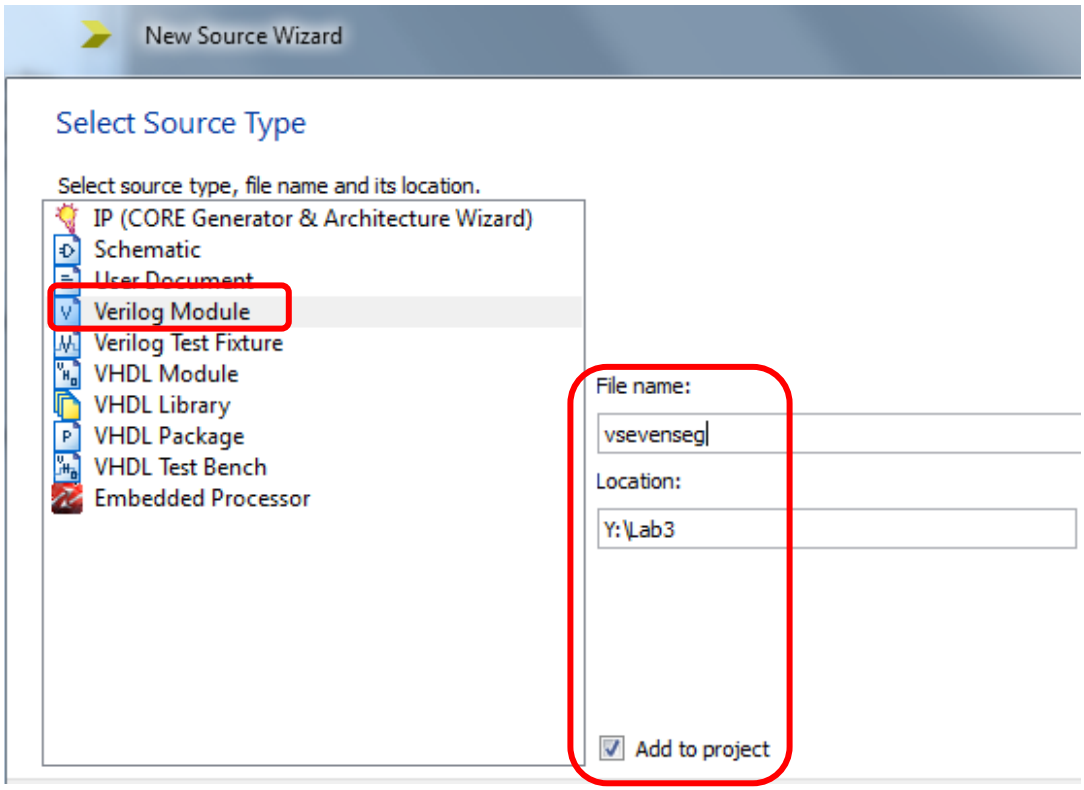




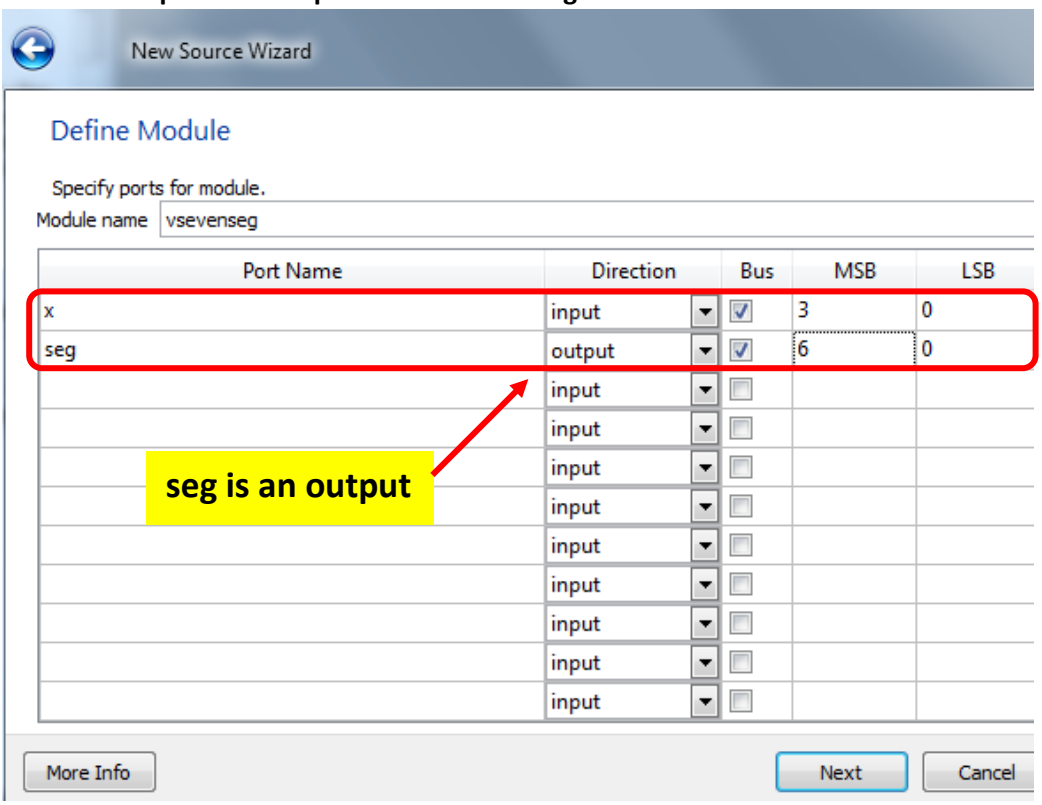
3. **Select the correct Family, Device and Package.**



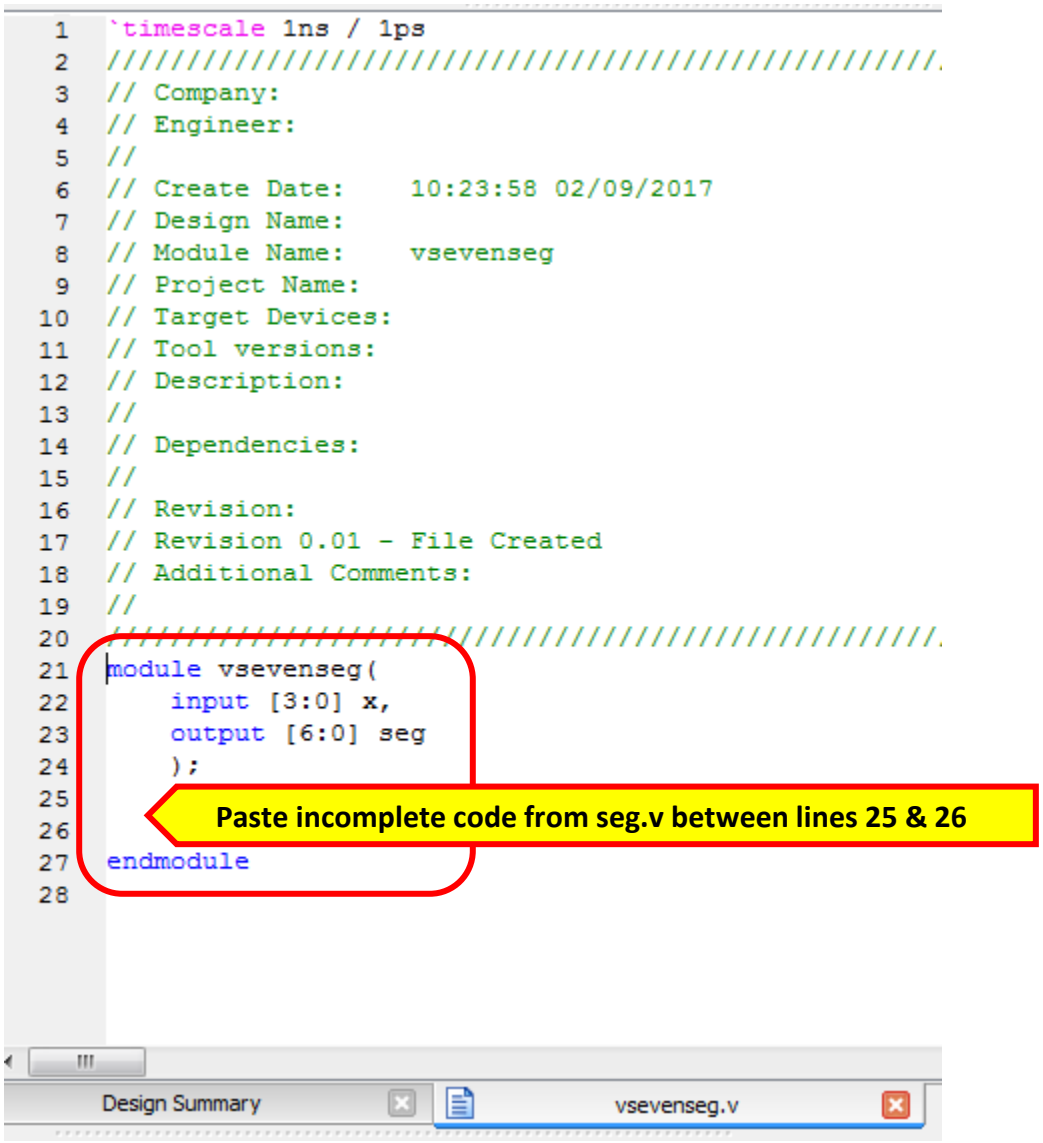
4. **Create a new Verilog Module vsevenseg and add it to project**



5. Define the inputs and outputs of the vsevenseg circuit

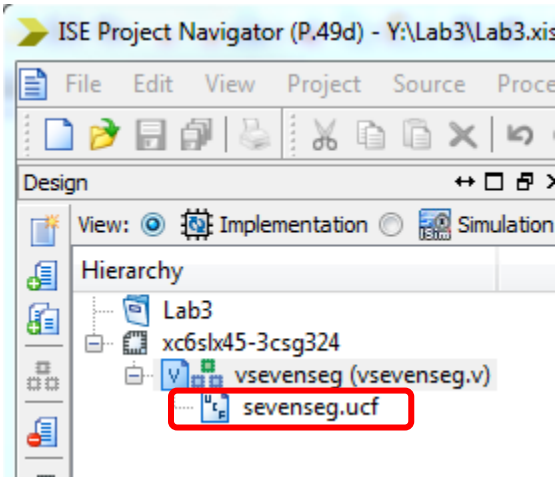


6. **Verilog circuit with inputs and outputs defined**



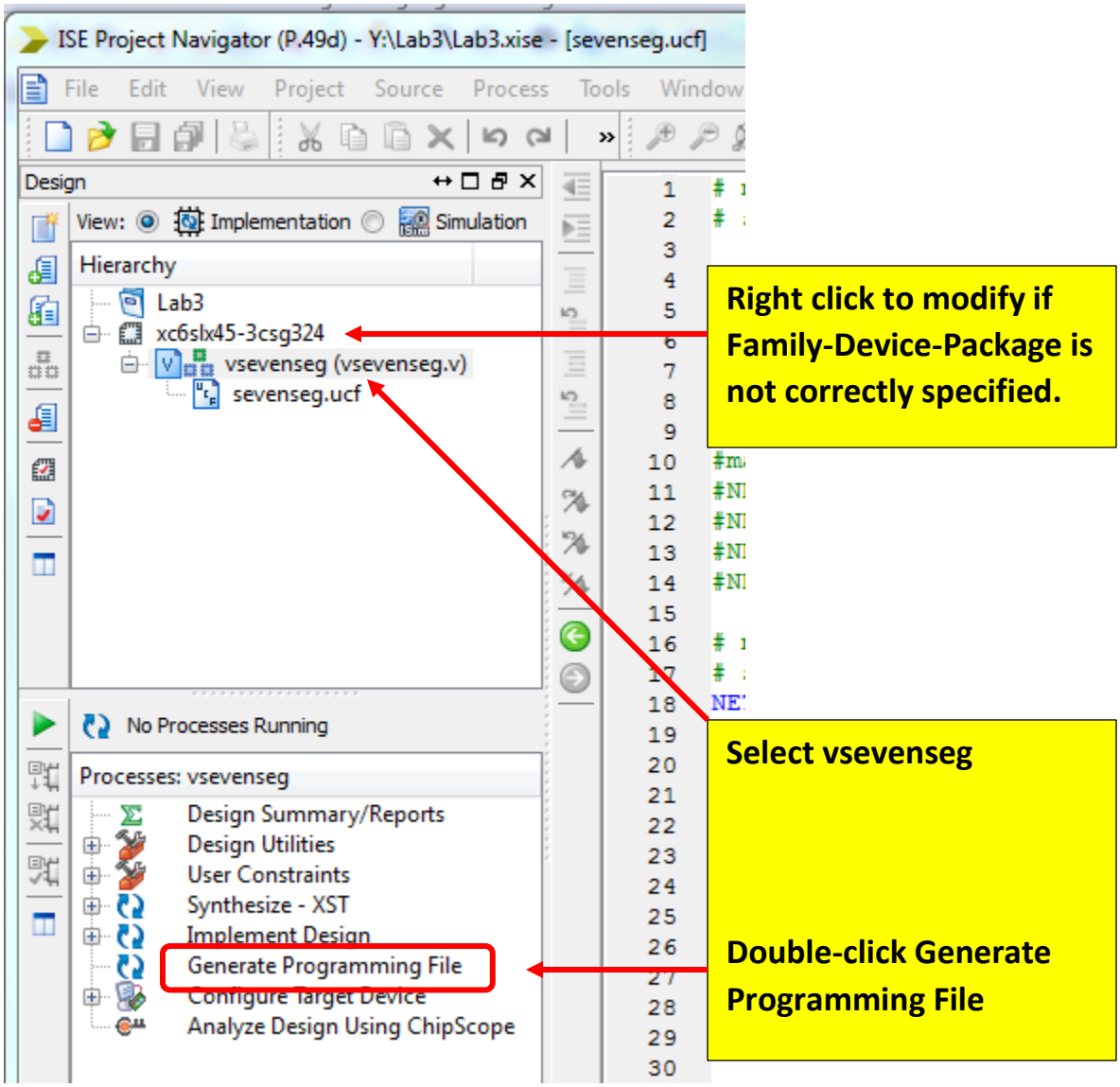
Remember to key in the Boolean expressions (in Verilog syntax) for the remaining segments. Otherwise the circuit design is incomplete.

7. **After sevenseg.ucf has been added to the project. Double click on it to edit.**

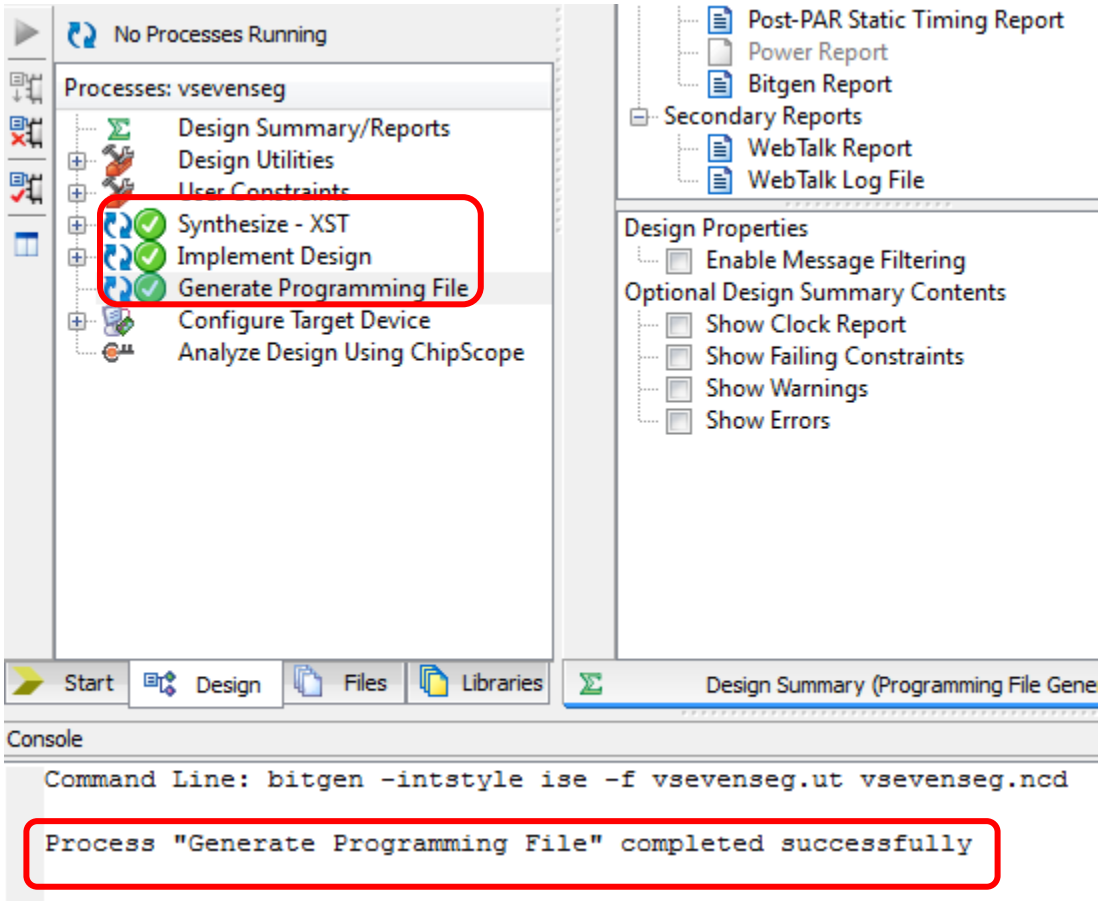


Remember to key in the UCF statements for the remaining segments. Otherwise there will be error in the circuit implementation.

8. **Check Family, Device and Package. Select vsevenseg.v and double click Generate Programming File**

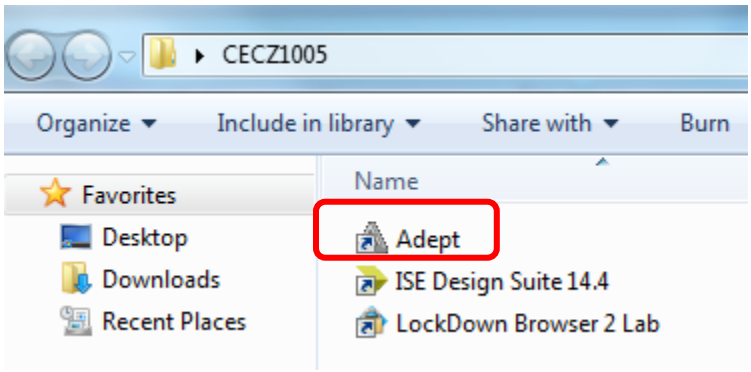


It may take several minutes to complete the bit file generation. Do not program the FPGA if there is error while generating the bit file.

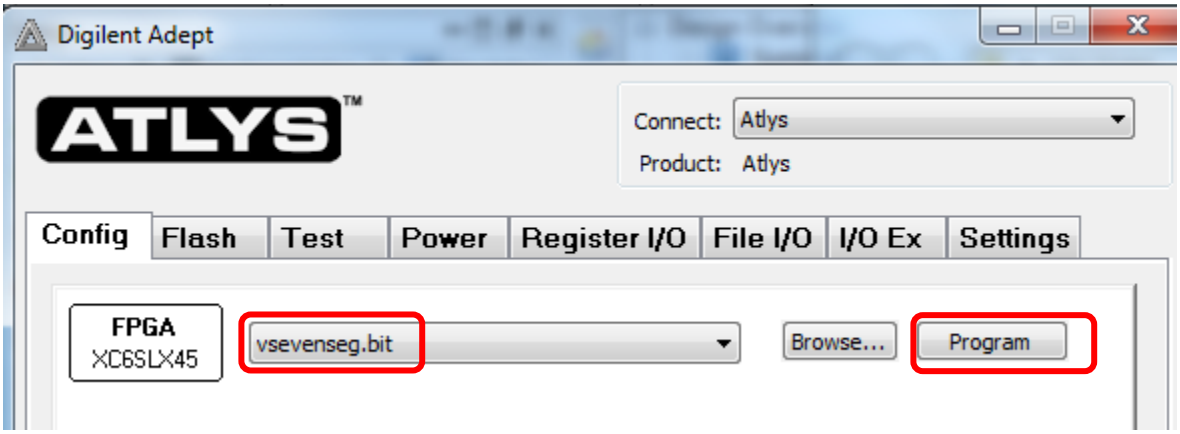


9. **Power up the FPGA board before programming (Turn on the power supply main first followed by the switch on board)**

10. **Double click Adept shortcut icon in CECZ1005 folder**



11. Select the correct .bit file and click Program



After programming is completed your circuit on the FPGA is ready for testing.

After you have modified the Verilog file (which specifies the logic circuit design) or the UCF file (which specifies the inputs/outputs on the FPGA) you need to re-generate the bit file (step 8) and re-program the FPGA (step 11) in order to observe the effect of your modification on the circuit behaviour.