CE/CZ1005 Digital Logic
Tutorial 6: Combinational Logic

Q1. (a) Draw the circuit represented by the following Verilog module. Label the gates and wires.

```
module whatisit (input a, b, c, d, e,
                 output x, y);
    not  n1  (nb, b);
    not  n2  (ne, e);
    and  a1  (w1, a, b);
    and  a2  (w2, nb, c);
    nor  no1 (w3, d, e);
    nand na1 (w4, w2, w3);
    or   o1  (x, w1, w4);
    and  a3  (y, ne, w1);
endmodule
```

(b) Write down a logic expression for each of the outputs.

(c) Rewrite the Verilog module using a single assign statement for each output.

Q2. A traffic light for a toy car track has a 3-bit one-hot vector input, with MSB corresponding to red and the LSB to green. However, the controller delivered with the track has only a 2-bit output for the lights, encoded as: red = “00”, yellow = “01” and green = “10”. The controller outputs “11” when there are no lights active.

Design a Verilog interface (using assign statements) to go between the controller and the lights.

Q3. A digital thermostat has two 8-bit unsigned binary inputs representing the target temperature and the actual temperature in degrees centigrade (°C). The thermostat has two outputs: one to turn a heater on when the actual temperature is 4°C below the target, and one to turn a cooler on when the actual temperature is 4°C above the target

(a) Design a Verilog module, *thermo*, with two 8-bit inputs, Tset and Tact and two 1-bit outputs Hon and Con. Use a parameter statement to specify the 8-bit width.

(b) The module designed in part (a) is instantiated in another module. Write the Verilog statement to instantiate the thermo module with identifier U1 using the same signal names in the upper module.

(c) Part way through the design process, the design team finds out that the temperature sensor and the target set-point both have 12-bit outputs. Describe a simple change to the Verilog statement to instantiate the thermo module so that this will not effect the operation.

Q4. You are required to design a ferry boarding system to direct cars to one of four boarding ramps. The input to the circuit is a 2-bit binary number representing which ramp to use, and a 1-bit signal which is high when all ramps are full. These signals are generated for you (possibly by the human gatekeeper). The circuit has outputs that control four green lights, one above each of the ramps, with only one active at any time, and one red light that indicates that all ramps are full and vehicles should not proceed to join any ramp.

(a) Show a block diagram for the circuit using a single 2-4 decoder and any additional gates. Note: a 2-4 decoder takes a 2-bit binary input and produces a one-hot 4-bit output.

(b) Write a verilog module that instantiates a predefined decoder module with the following declaration:

module dec2to4 (**input** [1:0] a, **input** enable, **output** [3:0] one-hot);