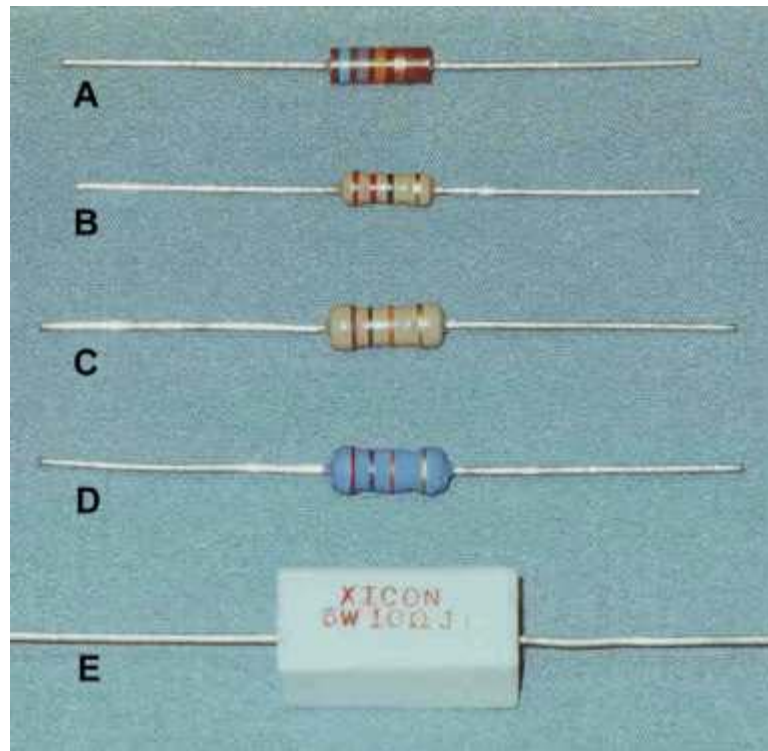
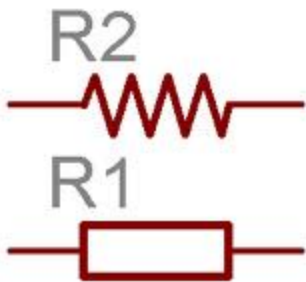


6. Digital Circuits

Integrated digital circuits are

- **made up of a collection of resistors, diodes and transistors**
- **fabricated on a single piece of semiconductor material (e.g. silicon) called substrate - also called die, or chip**

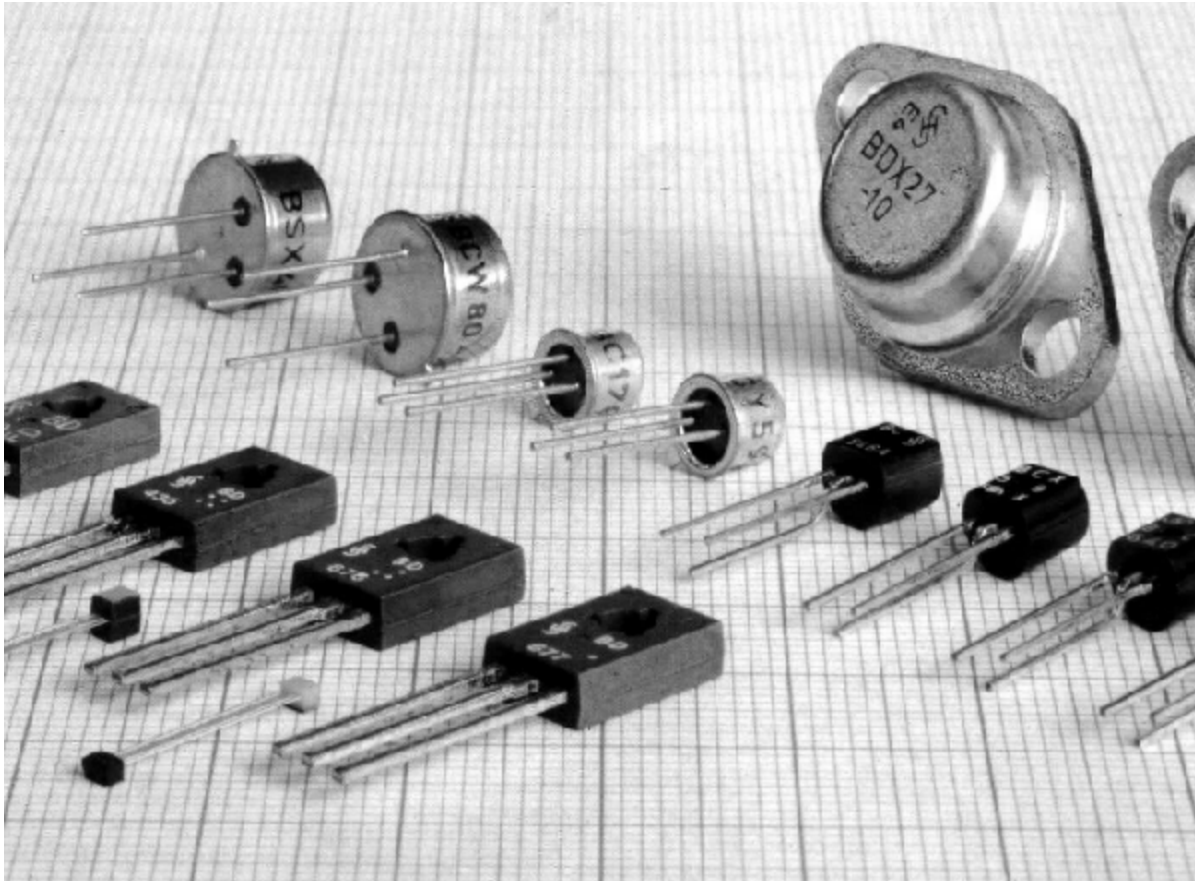
Discrete components: Resistors



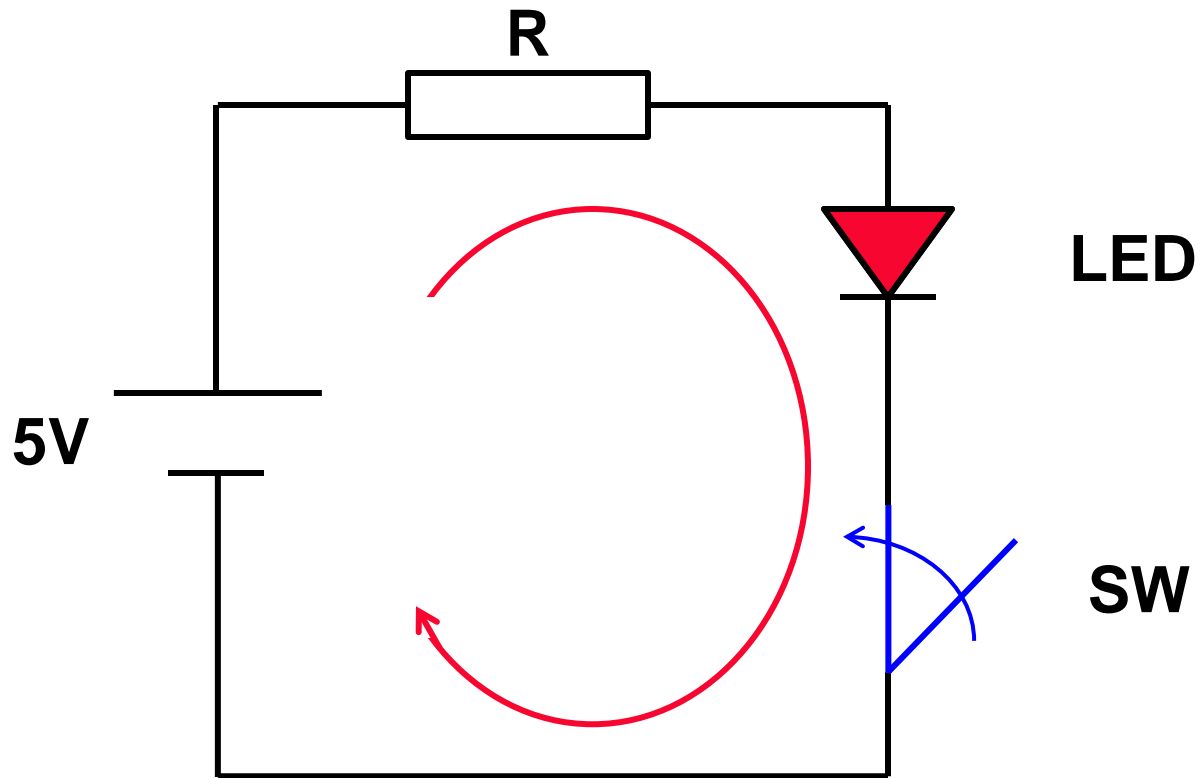
Discrete components: Diodes



Discrete components: transistors



Example of a simple circuit



<i>Technology</i>	<i>State Representing Bit</i>	
	<i>0</i>	<i>1</i>
Pneumatic logic	Fluid at low pressure	Fluid at high pressure
Relay logic	Circuit open	Circuit closed
Complementary metal-oxide semiconductor (CMOS) logic	0–1.5 V	3 .5–5.0 V
Transistor-transistor logic (TTL)	0–0.8 V	2 .0–5.0 V
Dynamic memory	Capacitor discharged	Capacitor charged
Nonvolatile, erasable memory	Electrons trapped	Electrons released
Microprocessor on-chip serial number	Fuse blown	Fuse intact
Polymer memory	Molecule in state A	Molecule in state B
Fiber optics	Light off	Light on
Magnetic disk or tape	Flux direction “north”	Flux direction “south”
Compact disc (CD)	No pit	Pit
Writeable compact disc (CD-R)	Dye in crystalline state	Dye in noncrystalline state

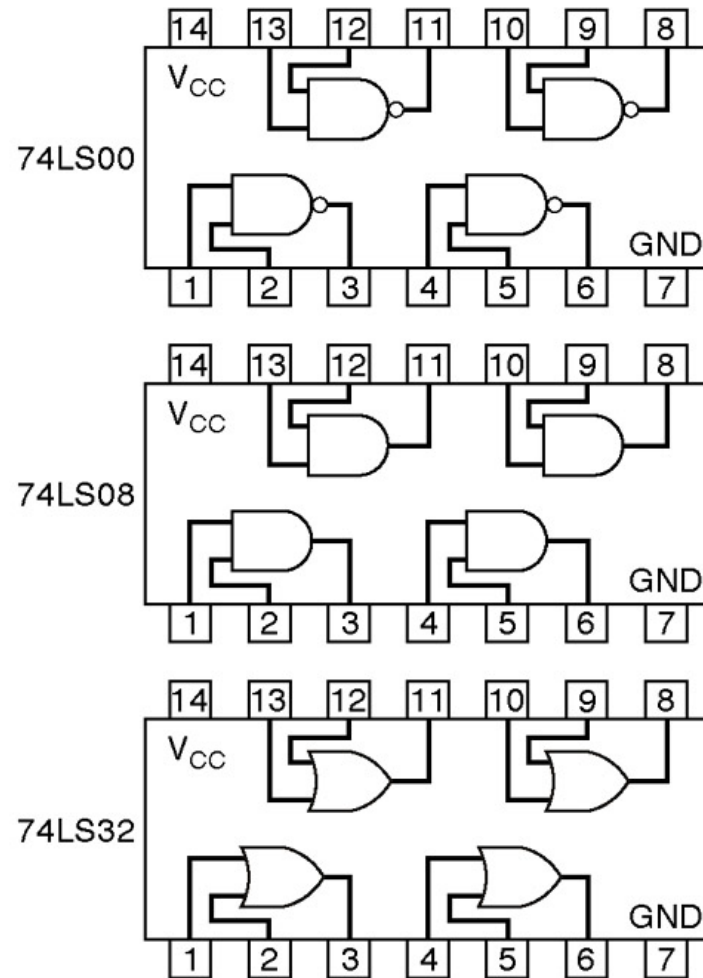
Table 3-1

Physical states representing bits in different logic and memory technologies.

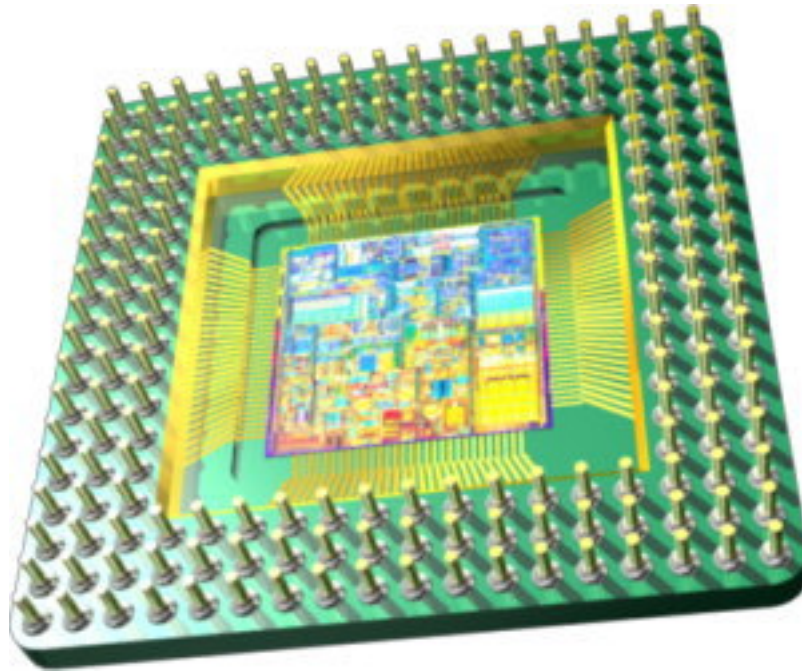
Scale of integration

Complexity	No. of gates
Small-scale (SSI)	< 12
Medium-scale (MSI)	12 - 99
Large-scale (LSI)	100 - 9999
Very large-scale (VLSI)	10,000 – 99,999
Ultra large-scale (ULSI)	100,000 – 999,999
Giga-scale (GSI)	$\geq 1,000,000$

Examples of SSI logic devices



**Example of GSI device:
A microprocessor, MPU, CPU**



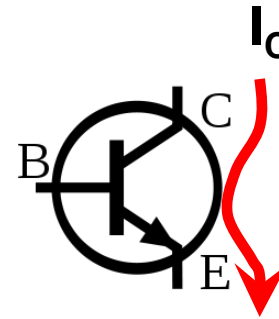
To make logic outputs switch between High and Low (1 and 0), **transistors** are used.

2 broad families:

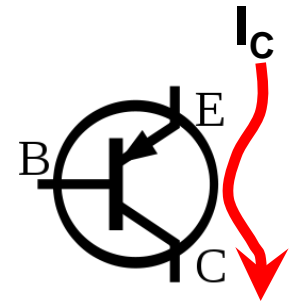
- use bipolar junction transistors
- e.g. **TTL** (transistor-transistor logic) circuits
- use unipolar field-effect transistors
- e.g. **CMOS** (complementary metal-oxide semiconductor) circuits

Bipolar junction transistors (BJT)

- Base, emitter, collector
- With correct voltage at B, current will flow between C and E



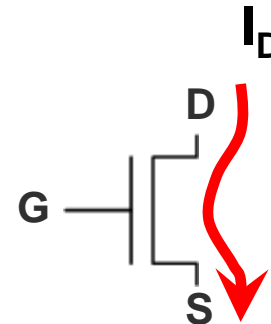
npn



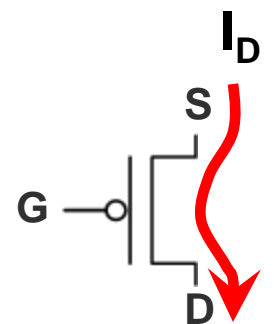
pnp

MOS Field-effect transistors (MOSFET)

- Gate, drain, source
- With correct voltage at G, current will flow between S and D



NMOS



PMOS

TTL family

- **different prefixes**
- **different in electrical characteristics such as power dissipation, delay time, switching speed**
- **do not differ in pin layout or logic function**

- **examples (hex inverters)**

TTL series	Prefix	E.g.
Standard	74	7404
High-speed	74H	74H04
Low-power	74L	74L04
Advanced low-power Schottky	74ALS	74ALS04

CMOS family

- **old series not pin-compatible with TTL**
- **new series pin-compatible with TTL**
- **HCT series is also electrically-compatible with TTL**

examples (quad 2-input NOR)

CMOS series	Prefix	E.g.
old	40/140	4001 14001
metal gate	74C	74C02
high speed	74HC	74HC02
elec. comp with TTL	74HCT	74HCT02

Logic-level Voltage Ranges

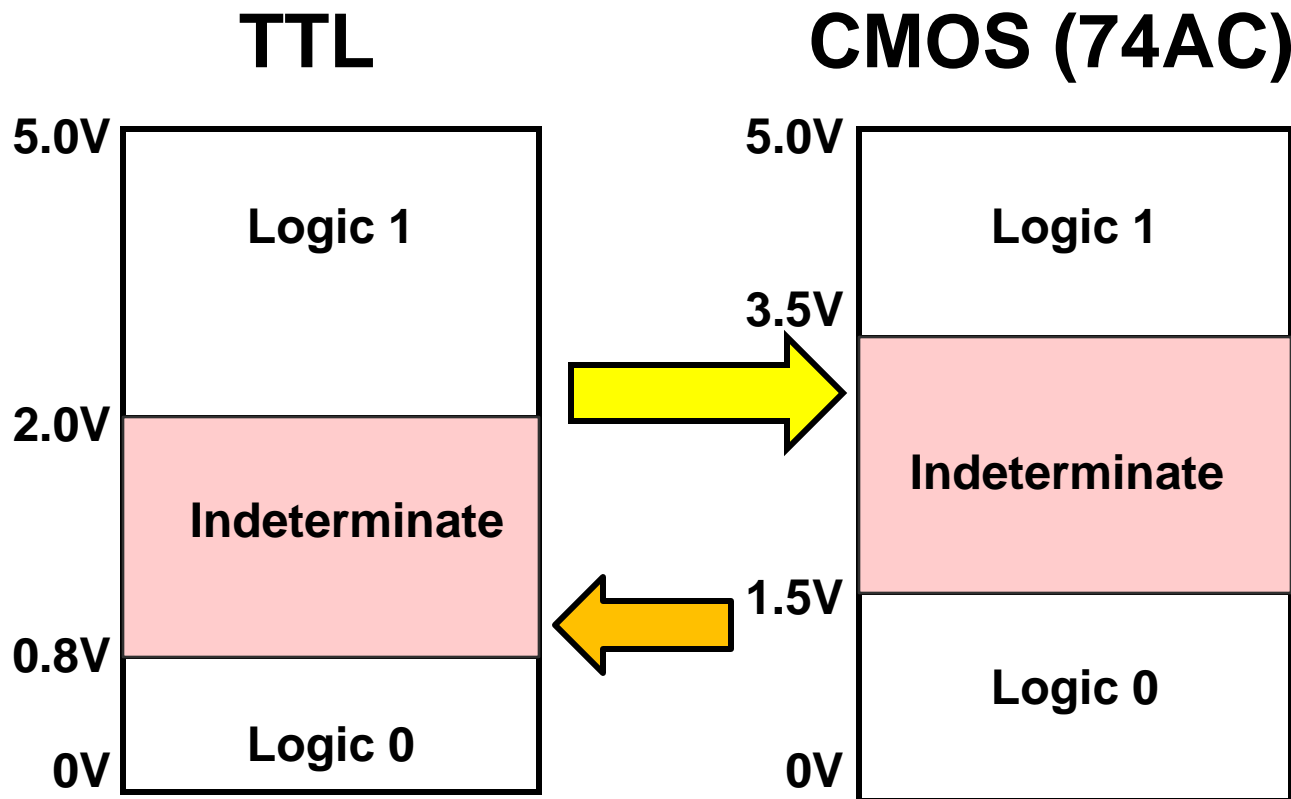
TTL

- V_{CC} nominally +5v

CMOS

- V_{DD} ranges from +3 to +18v
- +5v is most often used when CMOS ICs are used in same circuit with TTL ICs

Incompatible voltage ranges



Unconnected (floating) inputs

TTL

- floating input acts like logic 1
- measures dc level between 1.4 to 1.8 volts
- not recommended due to noise pick-up

CMOS

- disastrous result
- IC may become overheated
- all unused input pins must be connected to V_{DD} , GND, or another input

Active levels

- **Active high: signal performs the named action when it is logic 1**
- **Active low: signal performs the named action when it is logic 0**

Active levels

- E.g. active high signal OPEN is used to open a door when OPEN=1
- What happens when OPEN=0?
- E.g. active low signal UNLOCK* is used to unlock a safe when UNLOCK*=0
- What happens when UNLOCK*=1?

	<i>Active Low</i>	<i>Active High</i>	
	READY-	READY+	
	ERROR.L	ERROR.H	
	ADDR15(L)	ADDR15(H)	
RESET*	RESET*	RESET	RESET
	ENABLE~	ENABLE	
	~GO	GO	
	/RECEIVE	RECEIVE	
	TRANSMIT_L	TRANSMIT	

Table 6-1

Each line shows a different naming convention for active levels.

Asserted and negated

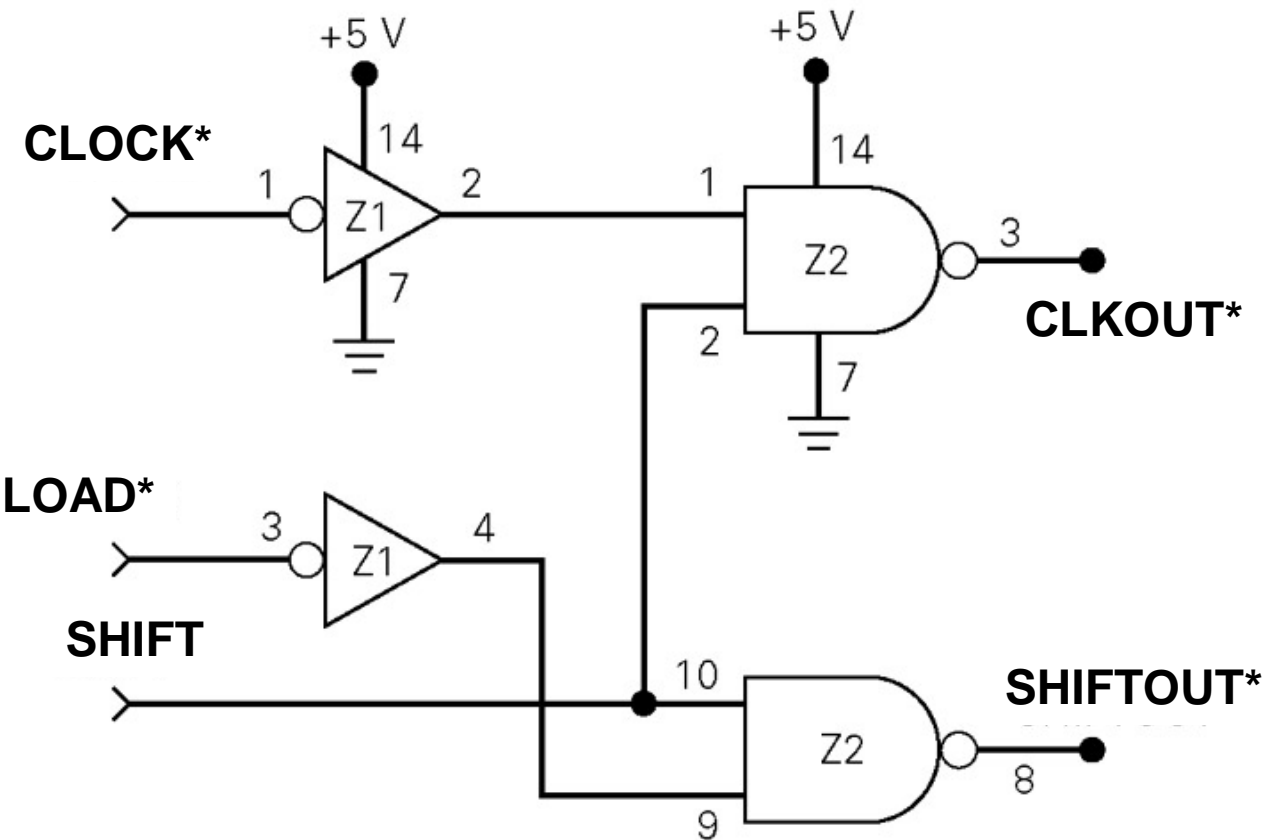
- A logic signal is asserted when it is in its active level
- Otherwise, it is negated

Actual logic level	Active high	Active low
asserted	1	0
negated	0	1

Logic circuit connection diagrams

Fig. 4-32 contains more information than the usual circuit diagram to facilitate circuit connection and troubleshooting

- **pin numbers, IC numbers, component values, signal names and power supply voltages are clearly indicated**
- **conform to bubble-to-bubble design rules**
- **active levels are clearly indicated**



IC	Type
Z1	74HC04 hex inverter
Z2	74HC00 quad nand

Fig. 4-32 Typical logic-circuit connection diagram

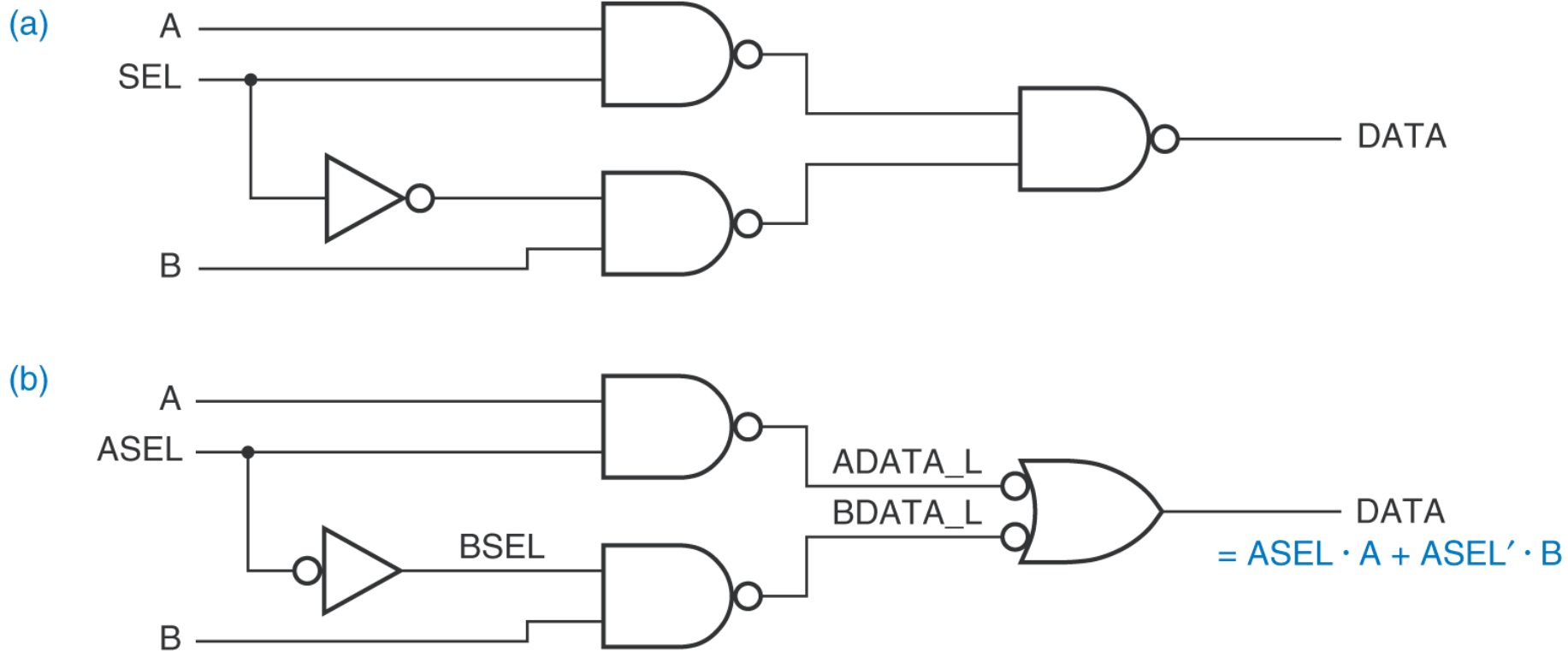


Figure 6-11

A 2-input multiplexer (you're not expected to know what that is yet): (a) cryptic logic diagram; (b) proper logic diagram using active-level designators and alternate logic symbols.

Fig. 6-11 Bubble-to-bubble logic diagram (Wakerly, 4th ed)

Troubleshooting Digital Systems

Read supplementary lab manual

- **Fault detection**
- **Fault isolation**
- **Fault correction**

Internal IC faults

- **malfunction in internal circuitry**
- **short circuit**
- **open circuit**
- **short between two pins**

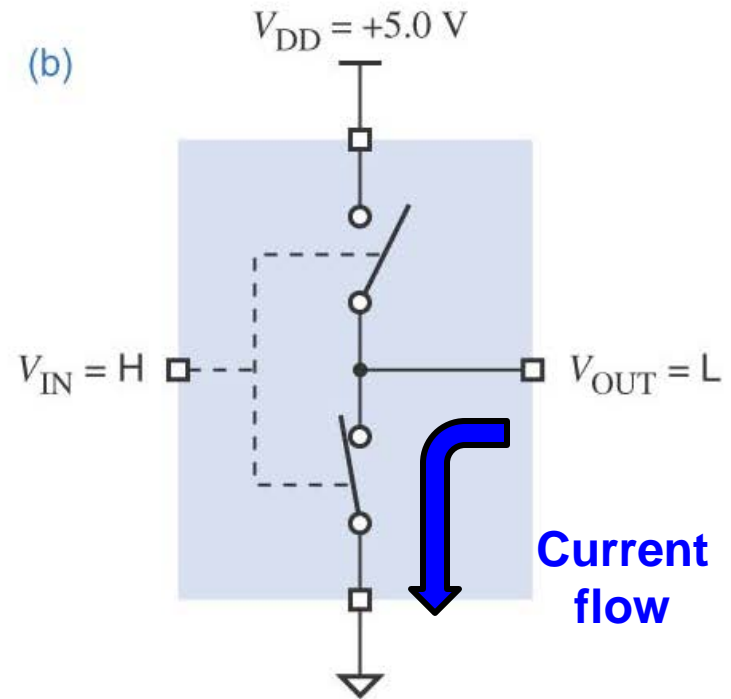
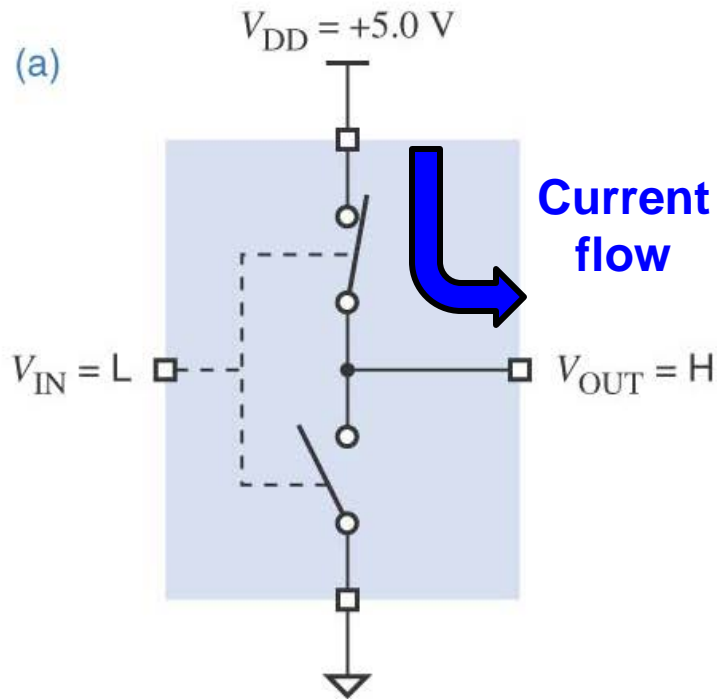
External IC faults

- **open signal line**
- **shorted signal lines**
- **faulty power supply**
- **wrong connection**

NEVER tie any circuit output to:

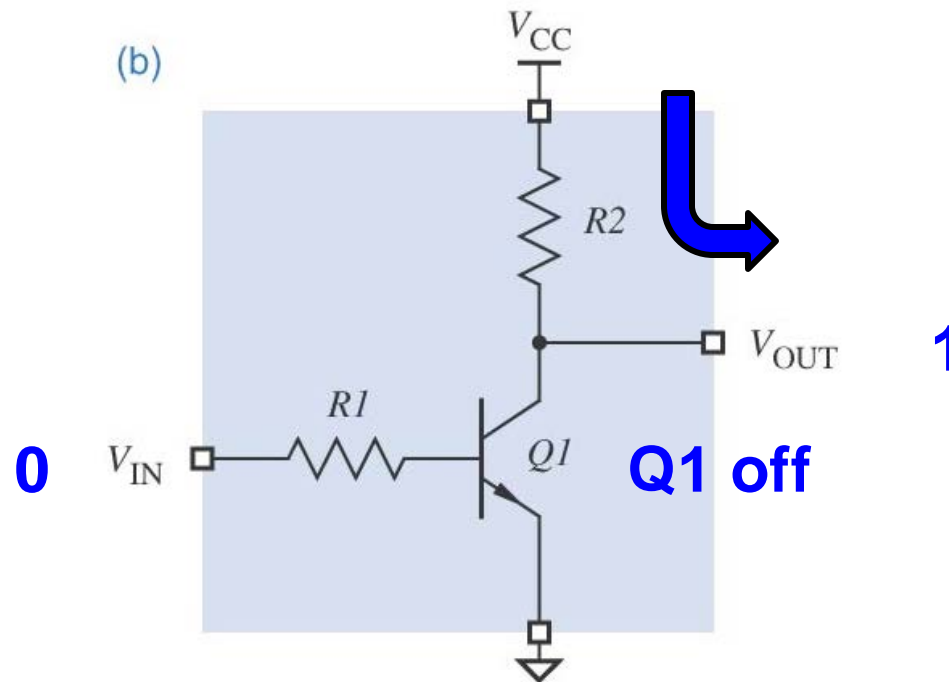
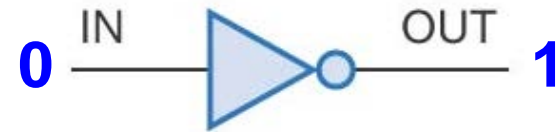
- **another output unless you are very sure**
- **Vcc , GND or any other fixed voltage level**

The transistor as a Switch

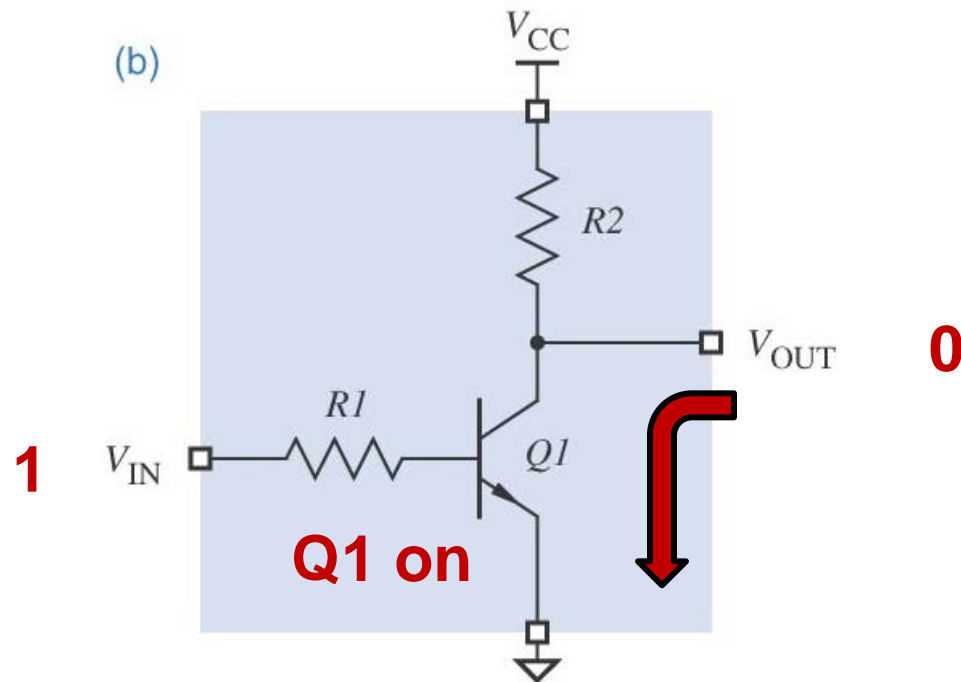
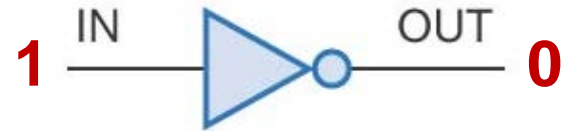


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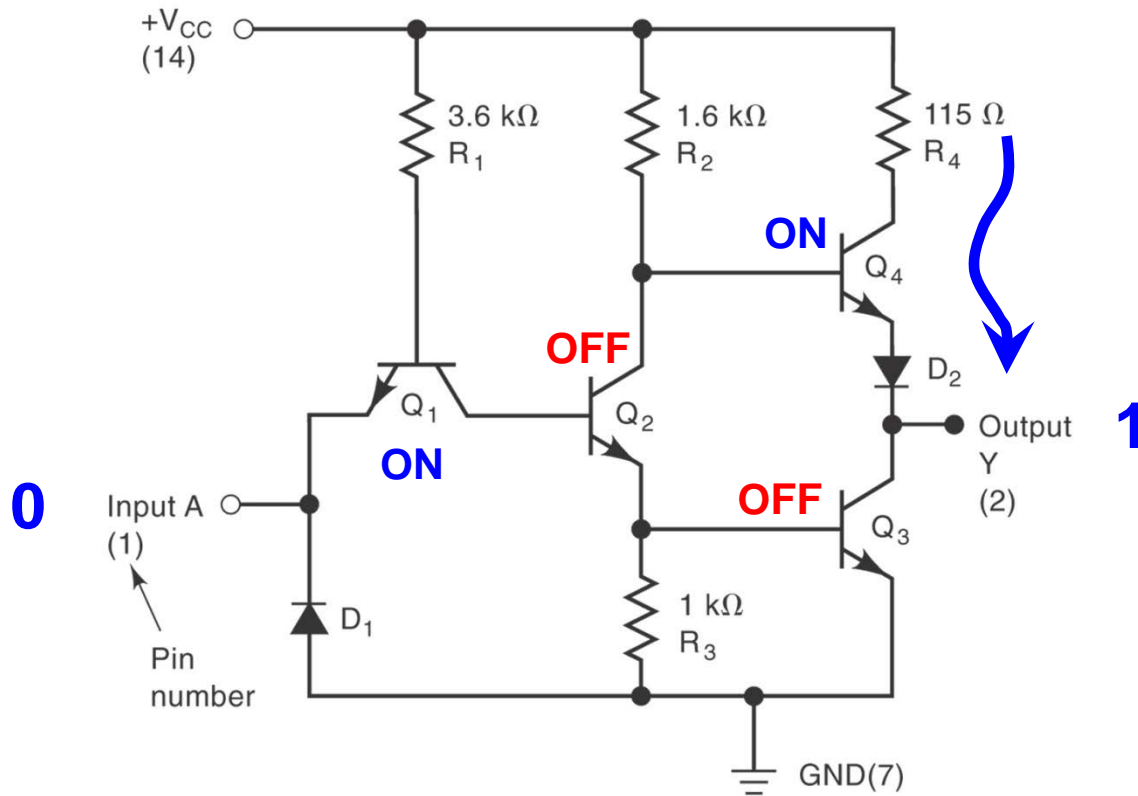
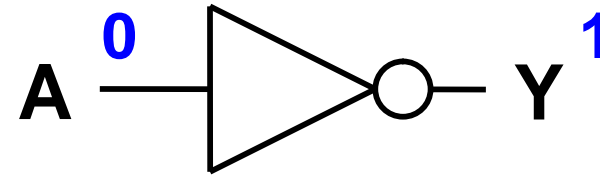
A simple BJT logic inverter



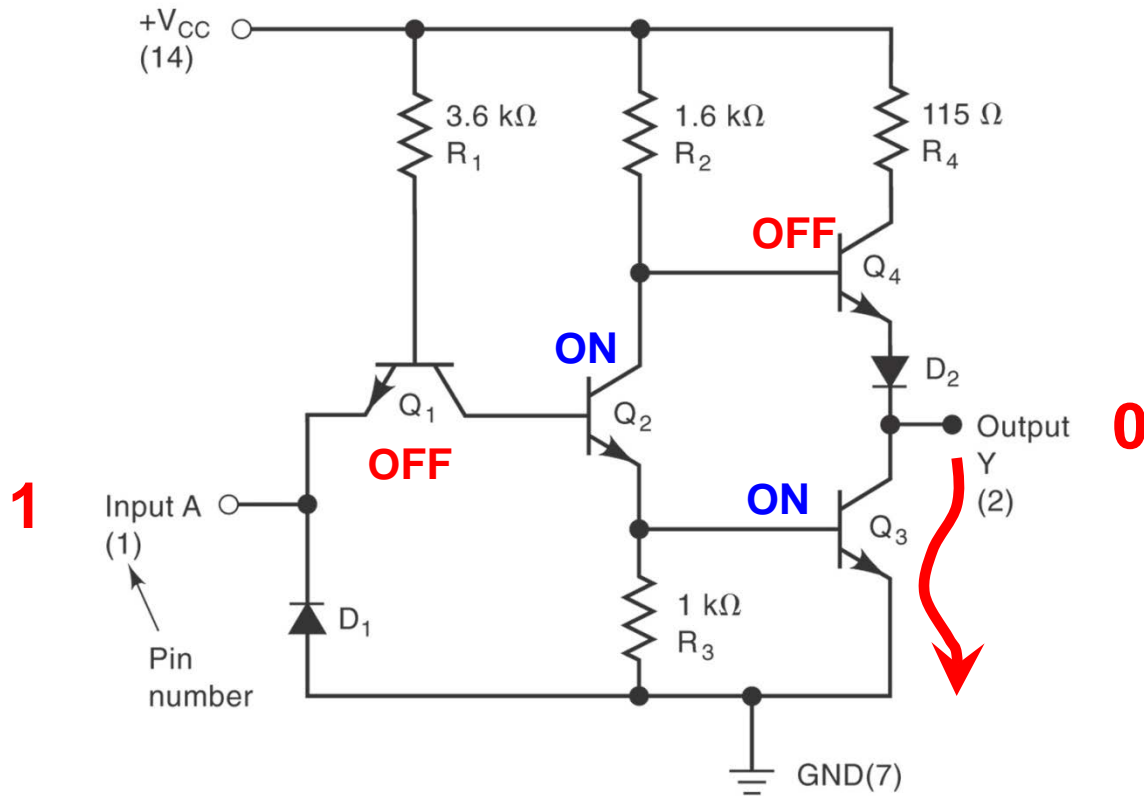
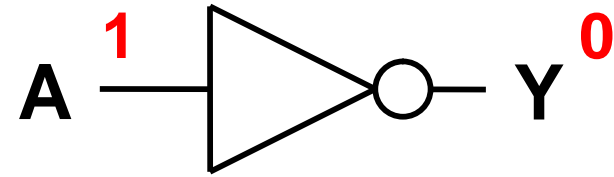
A simple BJT logic inverter



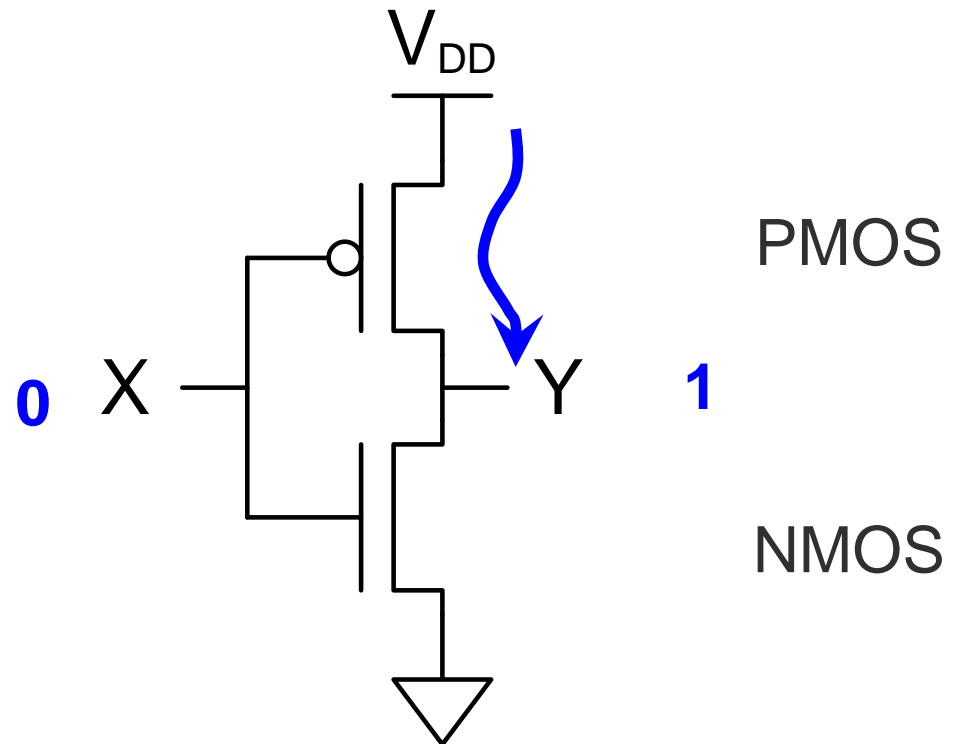
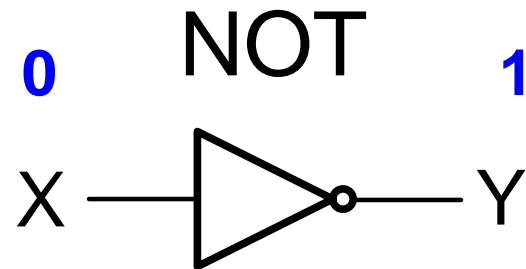
TTL inverter



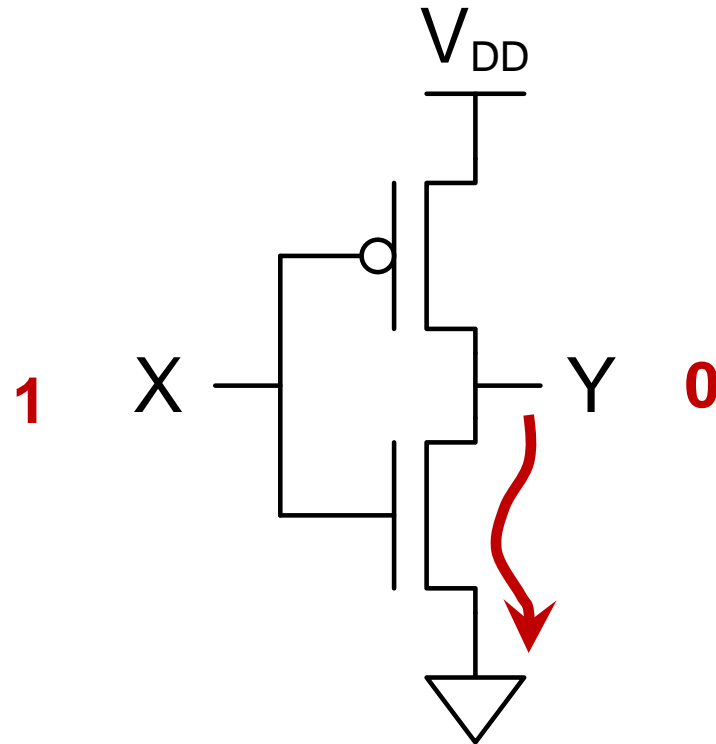
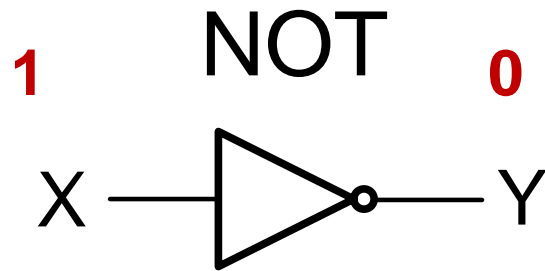
TTL inverter



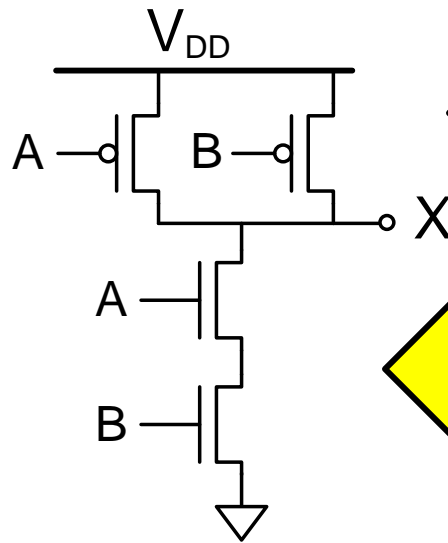
CMOS inverter



CMOS inverter

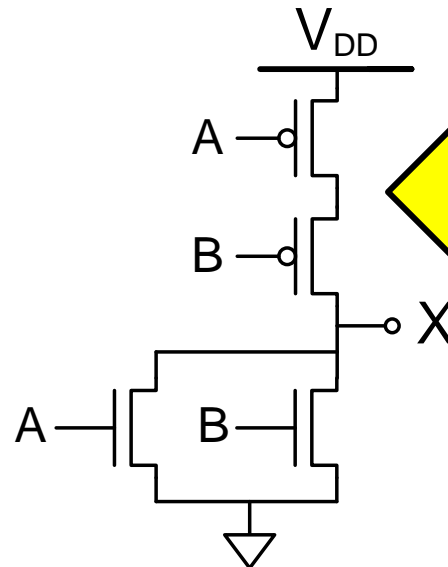


Examples of CMOS logic circuits



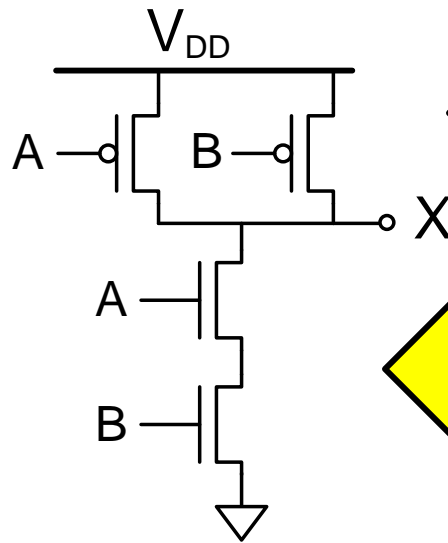
2 transistors in parallel

2 transistors in series



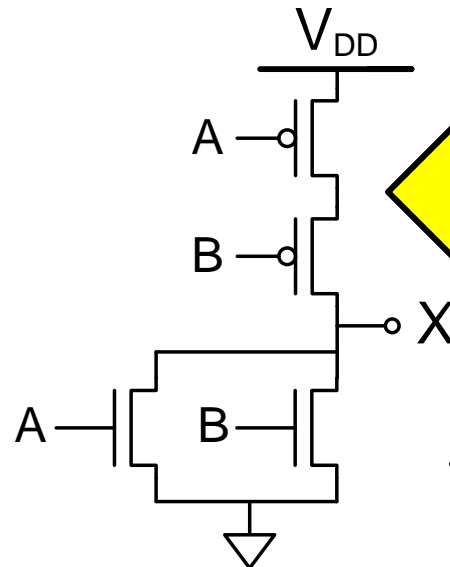
2 transistors in series

2 transistors in parallel



**Either A or B=0
will cause X=1**

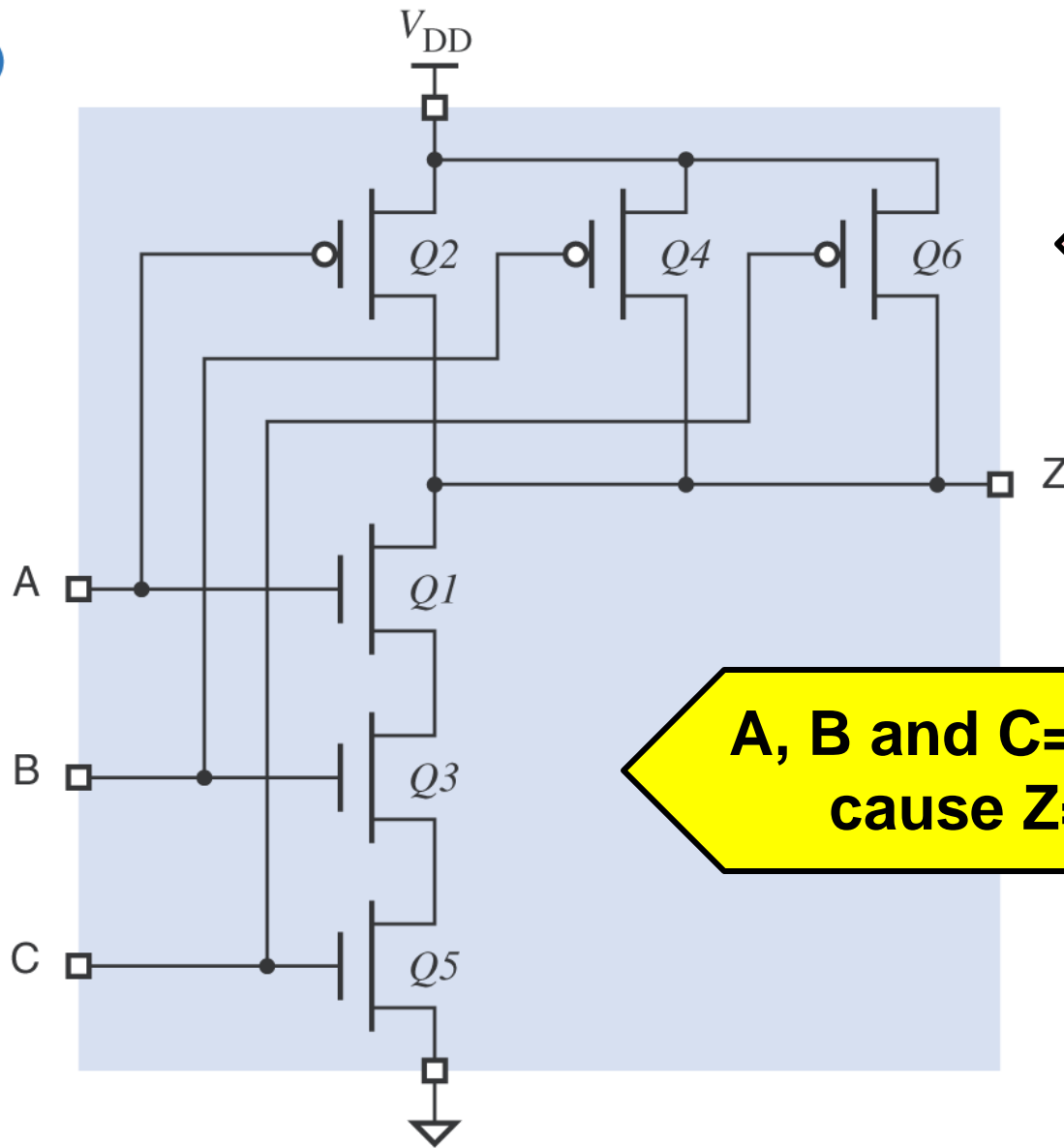
**Both A and B=1
will cause X=0**



**Both A and B=0
will cause X=1**

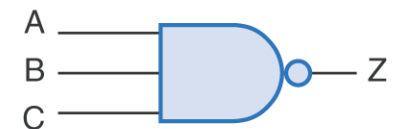
**Either A or B=1
will cause X=0**

(a)

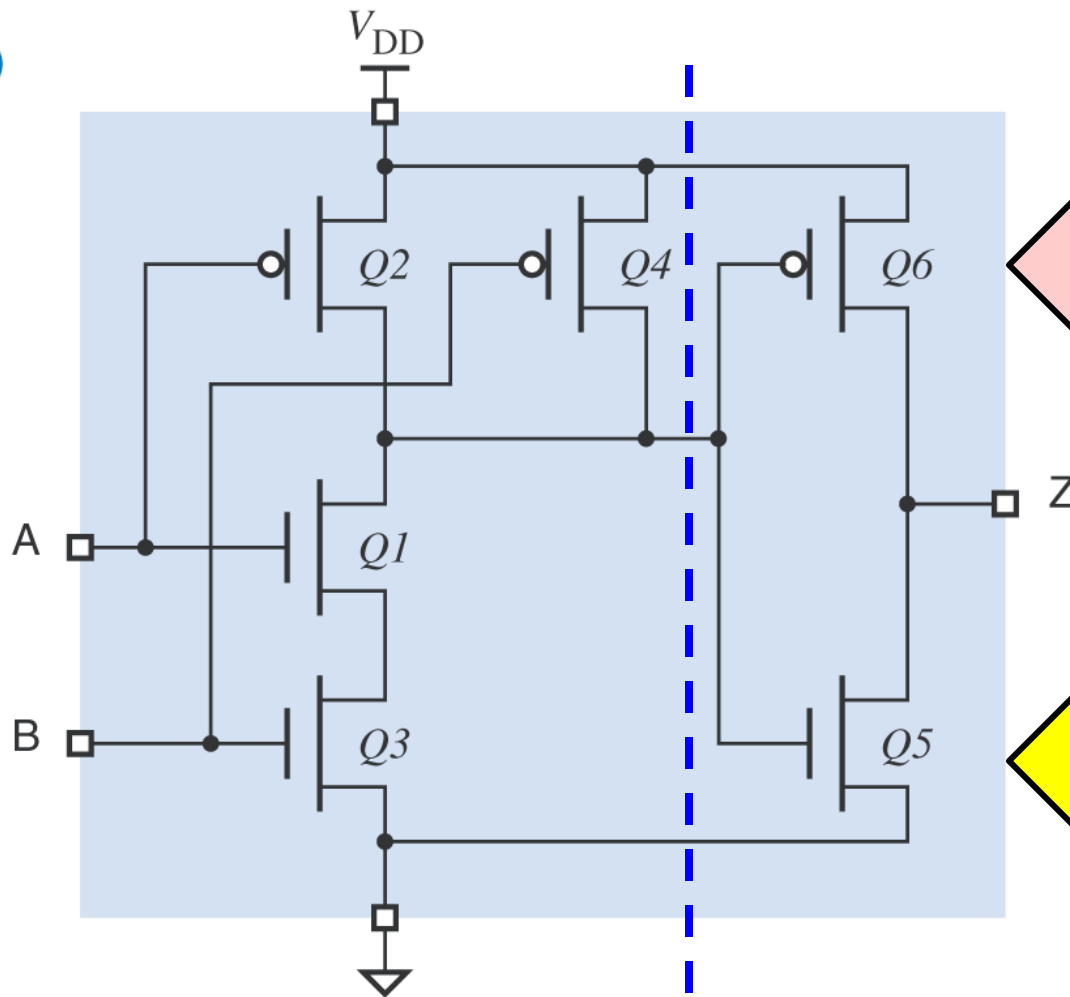


**Either A, B or C=0
will cause Z=1**

**A, B and C=1 will
cause Z=0**



(a)

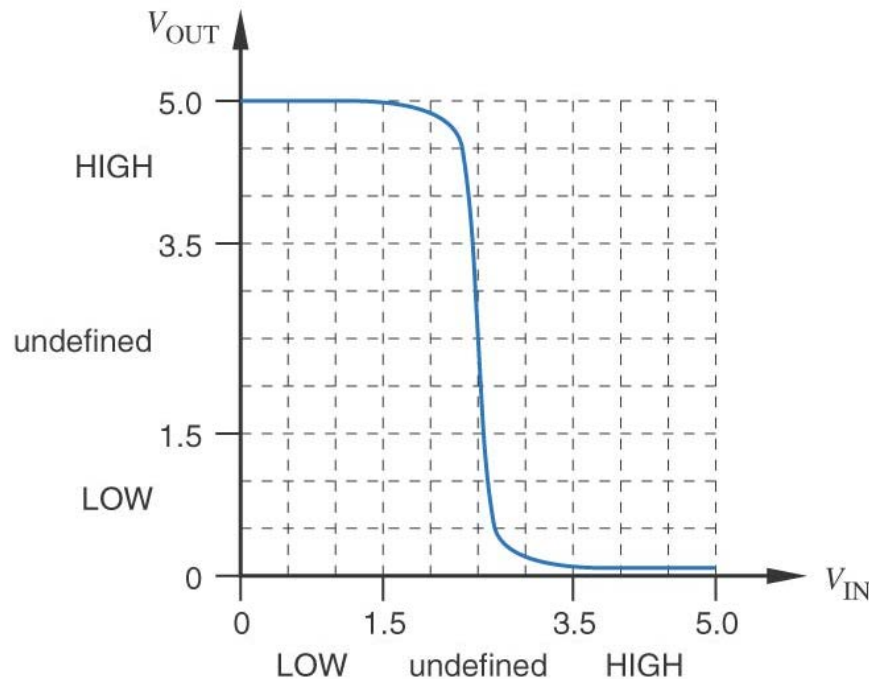


**Either A or B=0
will cause Z=0**

**Both A and B=1
will cause Z=1**



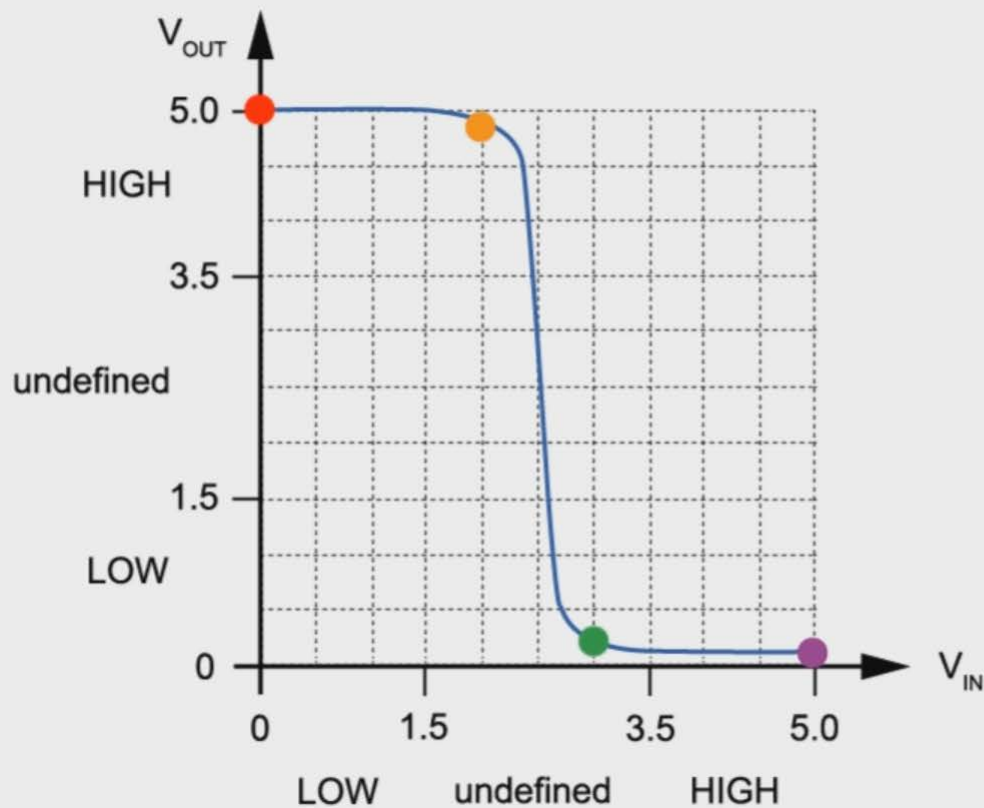
Digital Circuits Characteristics



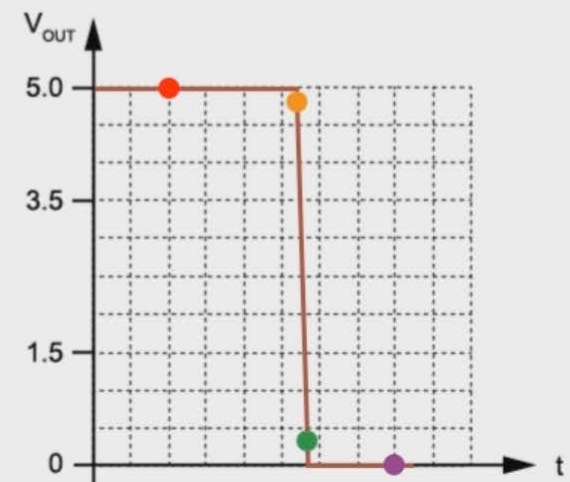
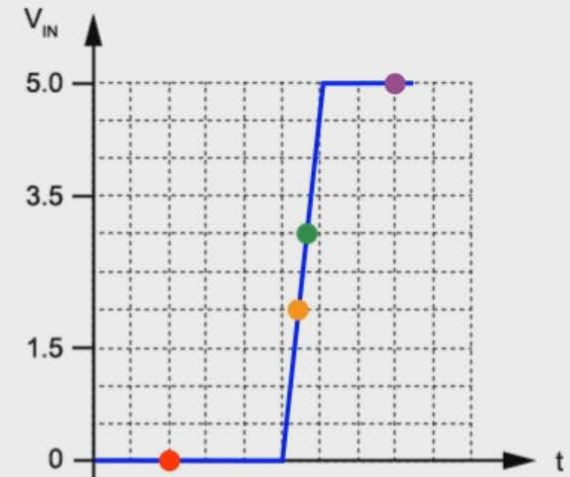
**Not
guaranteed**

Fig. 3-25 Typical input-output transfer characteristic of a CMOS inverter

transfer characteristic:



time-based signals:



Voltage parameters:

V_{OH} (min) - Minimum **output** voltage produced for logic **1**

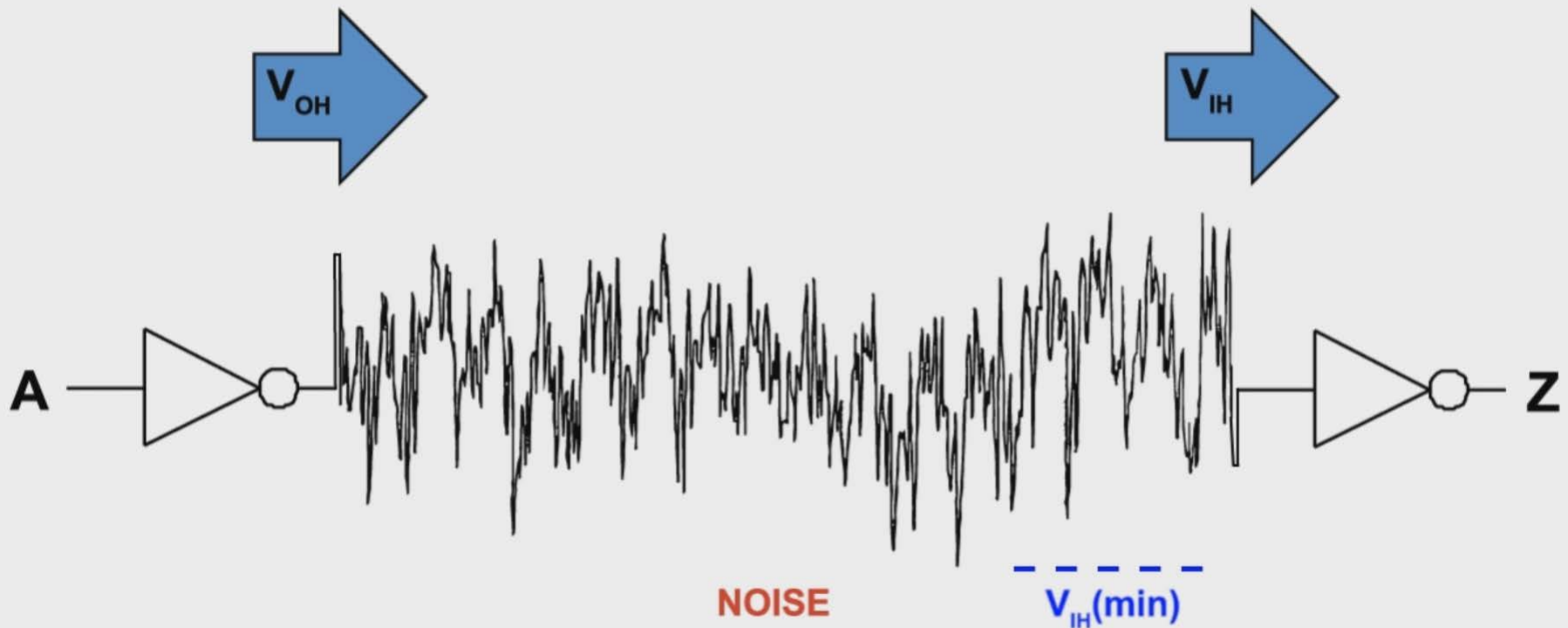
V_{IH} (min) - Minimum **input** voltage to be recognised as logic **1**

V_{IL} (max) - Maximum **input** voltage to be recognised as logic **0**

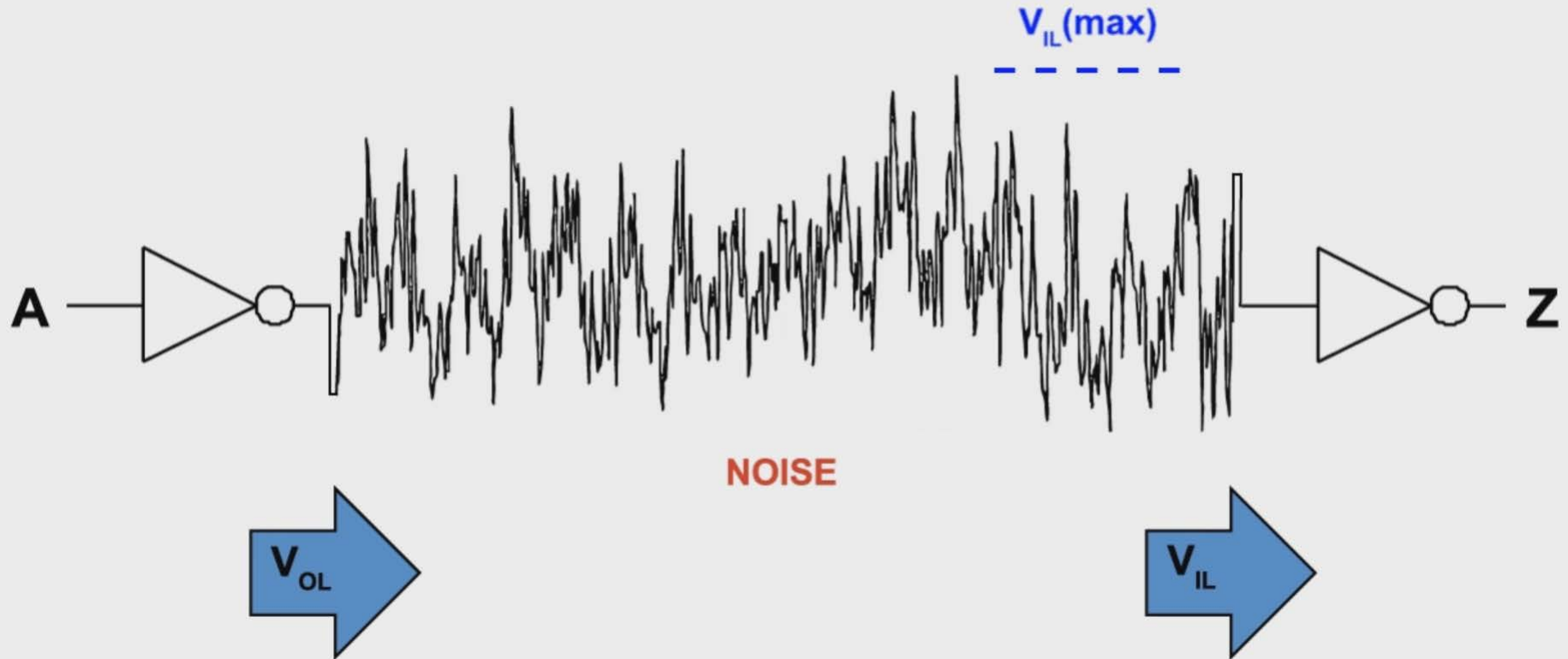
V_{OL} (max) – Maximum **output** voltage produced for logic **0**

Voltage parameters and noise margin:

High-state DC noise margin = $V_{OH(min)} - V_{IH(min)}$

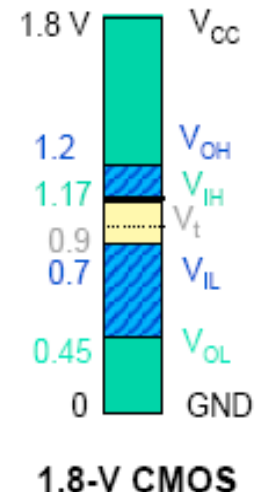
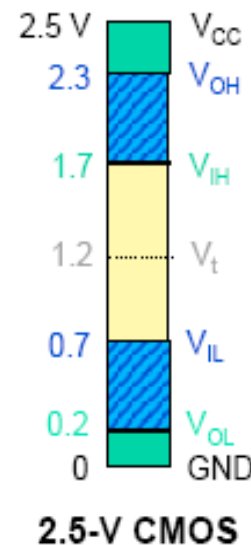
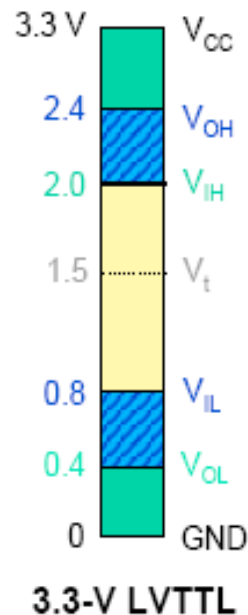
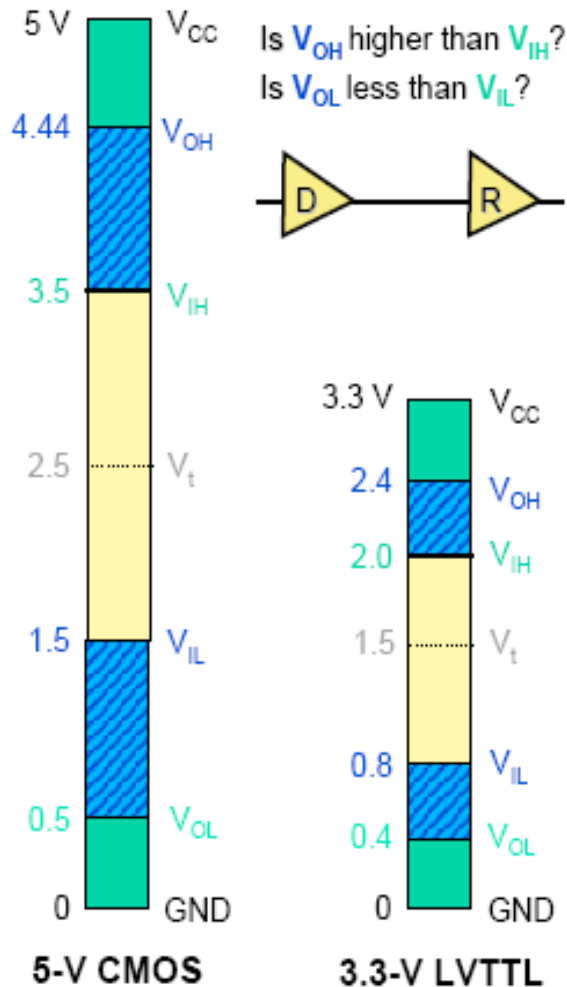
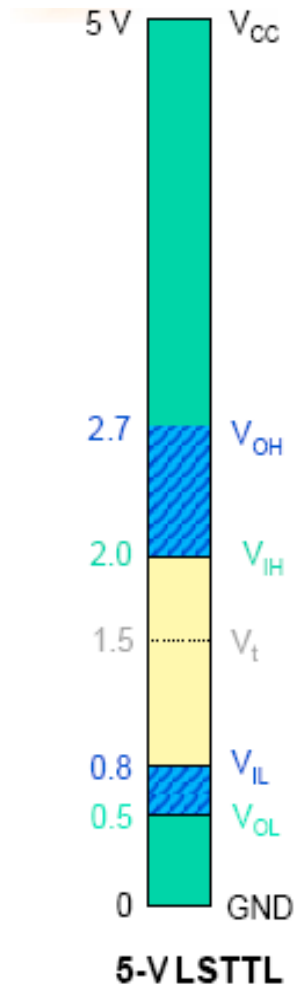


Voltage parameters and noise margin:



Low-state DC noise margin = $V_{IL}(\text{max}) - V_{OL}(\text{max})$

Some typical values



D \ R	5TTL	5CMOS	3LVTTL	2.5CMOS	1.8CMOS
5TTL	Yes	No	Yes *	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes

* Requires V_{IH} Tolerance

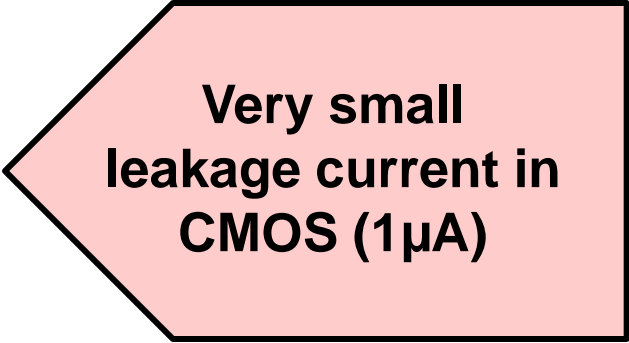
Current parameters

I_{IH} – Maximum current that flows into the **input** at logic **1**

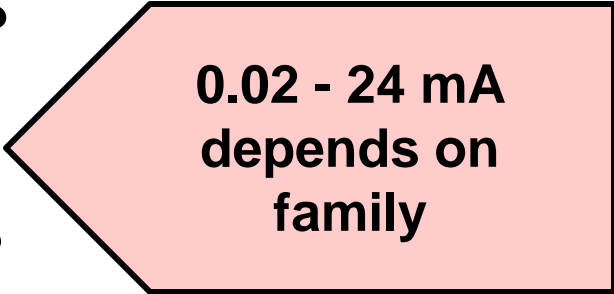
I_{IL} - Maximum current that flows into the **input** at logic **0**

I_{OH} – Maximum current that flows from the **output** at logic **1**

I_{OL} – Maximum current that flows from the **output** at logic **0**



Very small
leakage current in
CMOS ($1\mu\text{A}$)



0.02 - 24 mA
depends on
family

Other characteristics

Fan-out

- specifies the number of standard loads that the output gate can drive
- More loads may reduce DC noise margins and switching speed

Speed

- Time taken for output to switch between 0 and 1

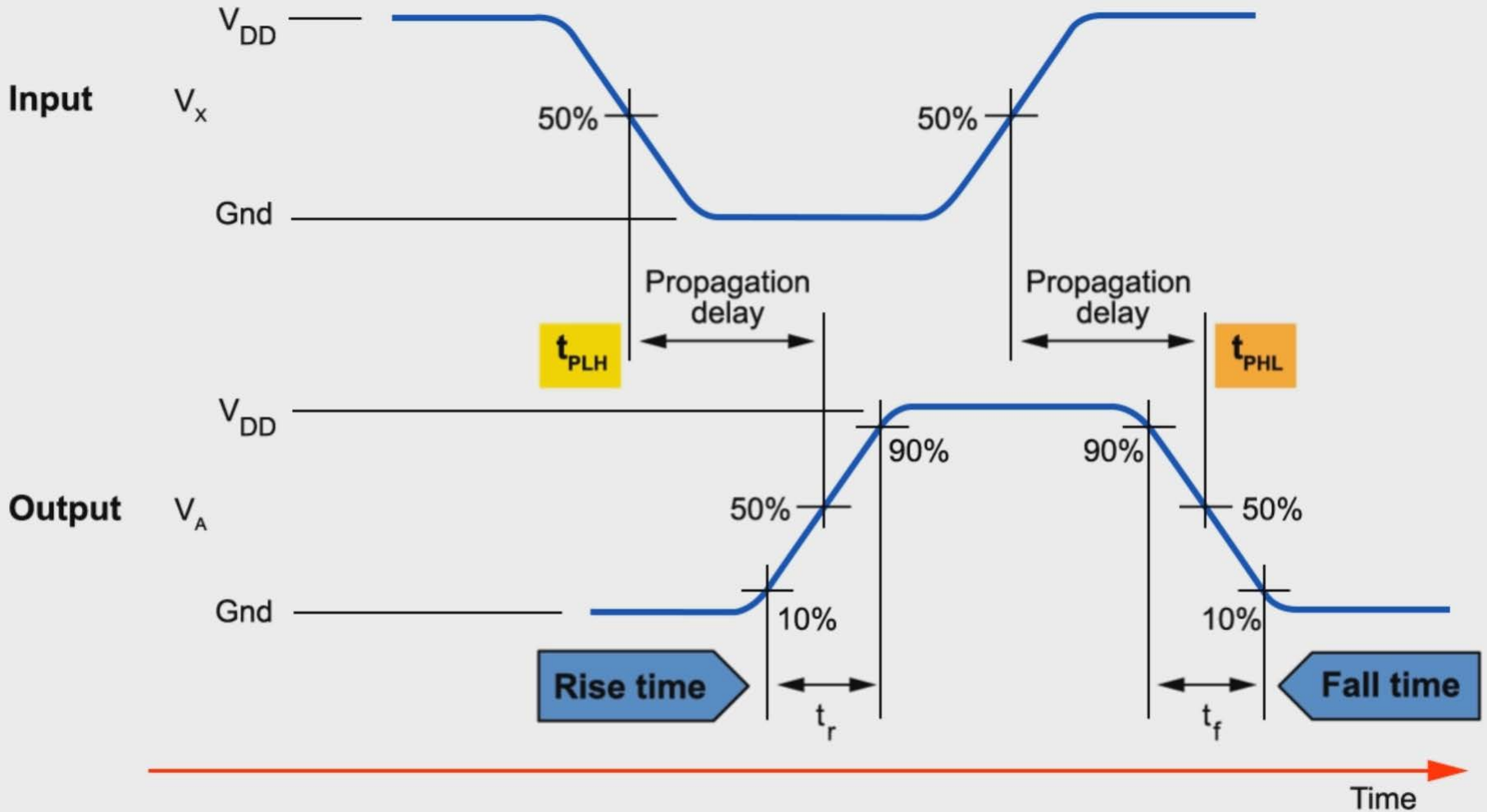
Power dissipation

- power consumed by the gate or device
- For CMOS, most of the power is consumed when output switches between 0 and 1 (dynamic power dissipation)
- $P = C V^2 f$
- Proportional to switching frequency f and square of power supply voltage V
- Static power dissipation (when there is no switching) is usually very small

Propagation delay

- average transition delay time for signal to propagate from input to output
- e.g. 9 – 19 ns for 74HC00
- t_{PD} , or t_{PHL} & t_{PLH}
- t_{PHL} = delay when **output** changes from **High to Low**
- t_{PLH} = delay when **output** changes from **Low to High**

Propagation delay (inverter):



Tristate outputs

3 output states:

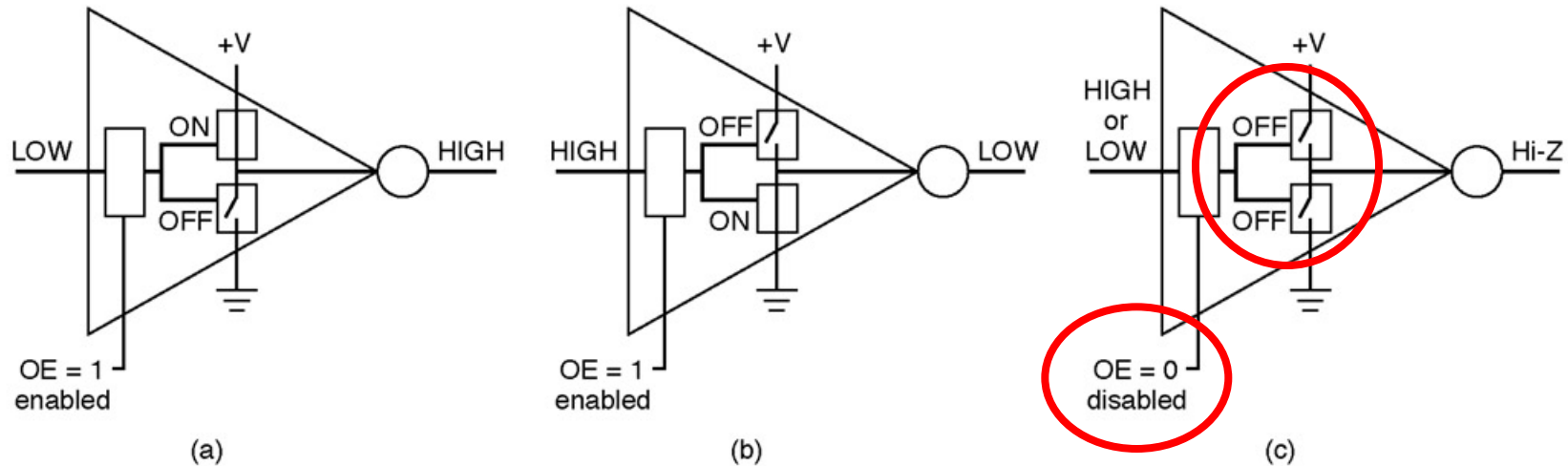
- **logic 0**
- **logic 1**
- **high impedance (Hi-Z)**
 - **neither 0 nor 1**
 - **behaves like an open circuit**

When a device is enabled, output is logic 0 or 1

When device is disabled, output is in Hi-Z

E.g. tristate buffer, tristate inverter

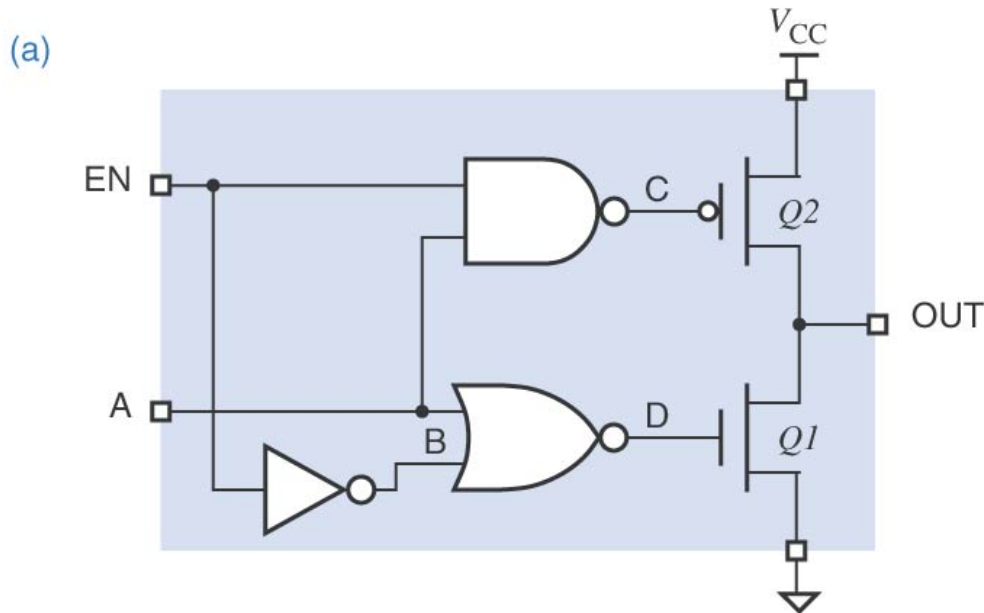
Tristate inverter



(a) & (b): Tristate device behaves as a normal inverter when enabled.

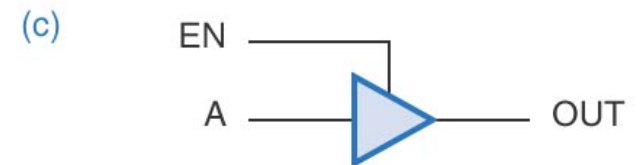
(c): Device output is in high-impedance when disabled.

CMOS Tristate buffer



(b)

EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H



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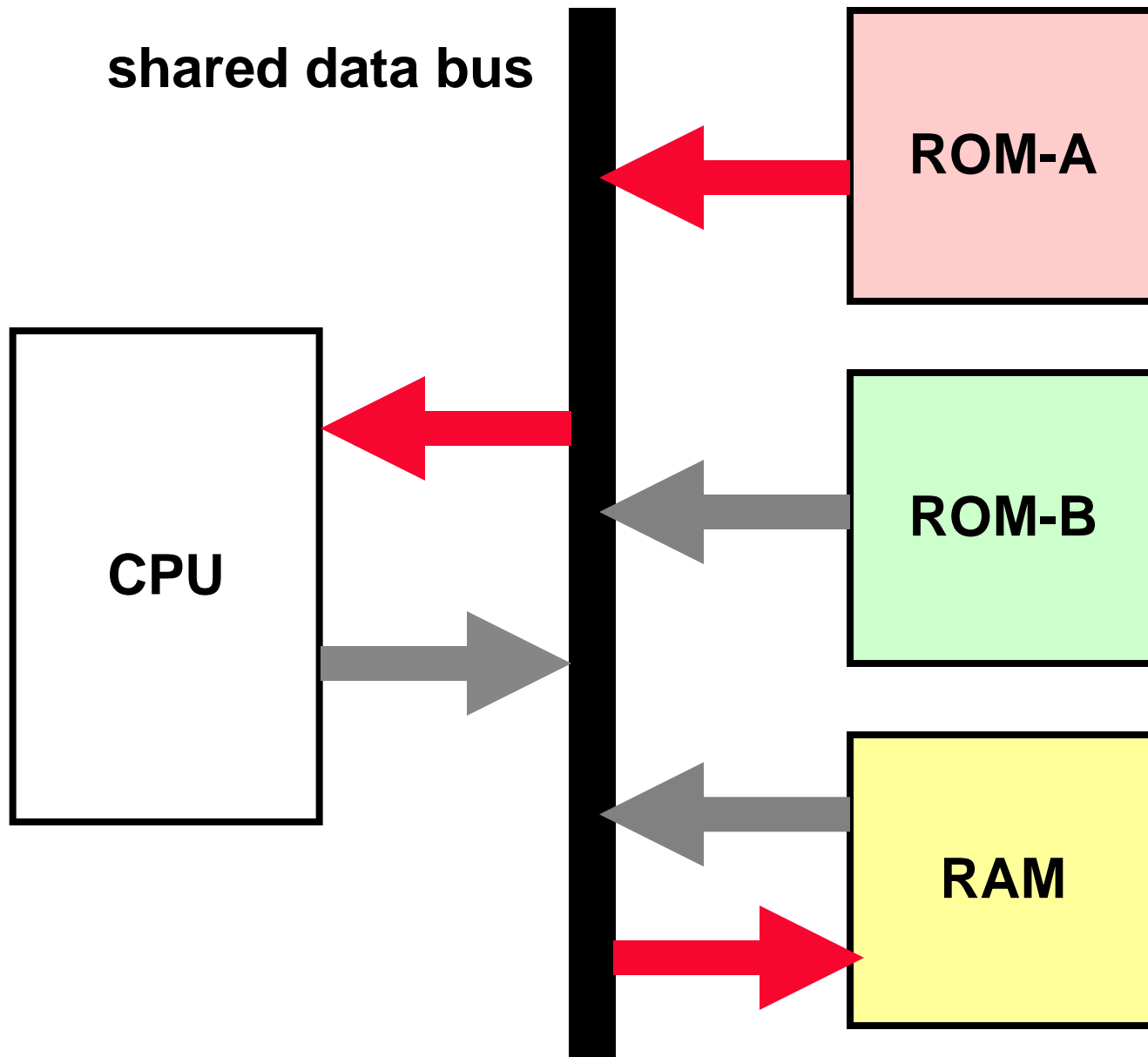
Advantage of using logic devices with tristate outputs

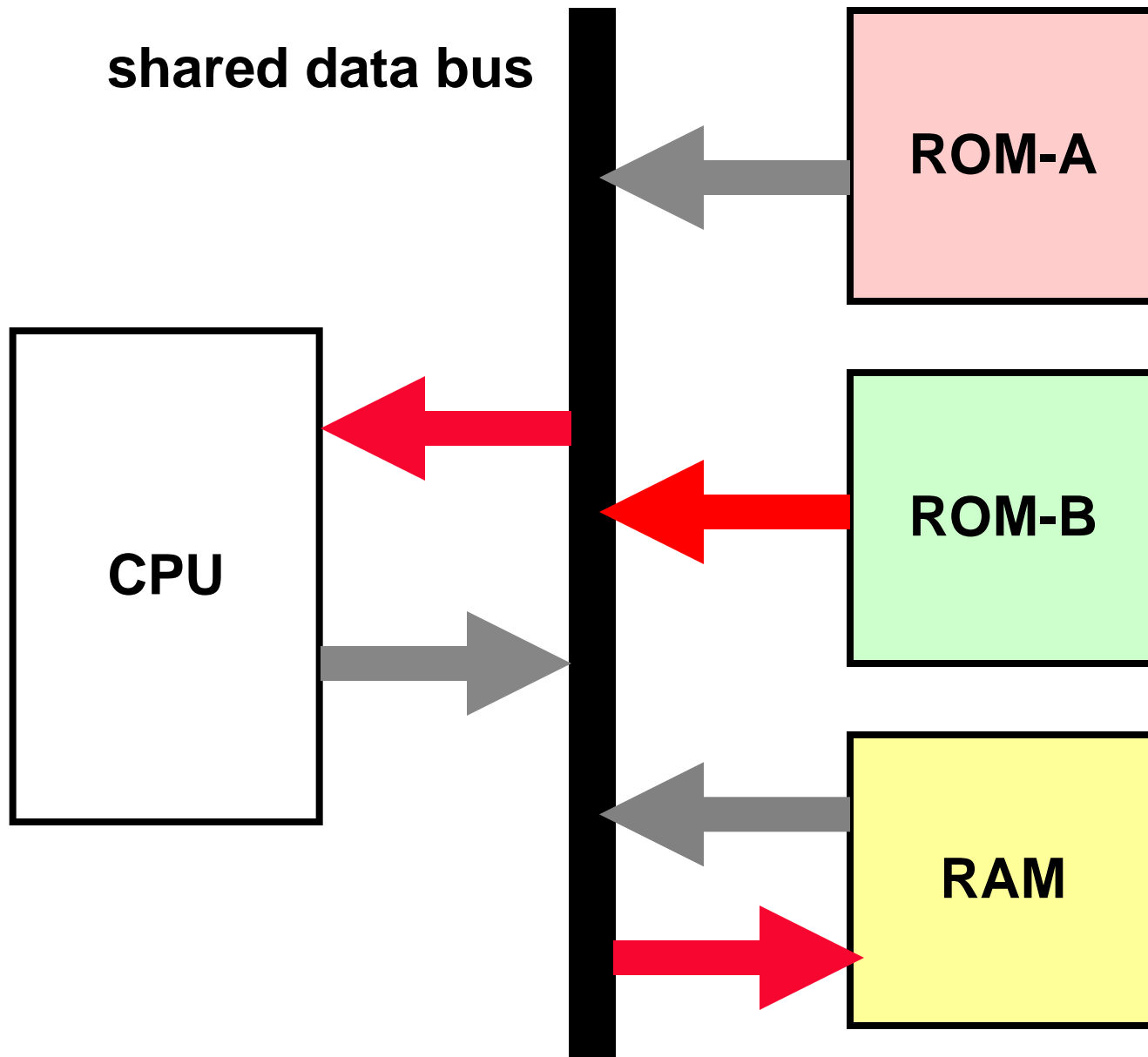
Two or more outputs can be connected together.

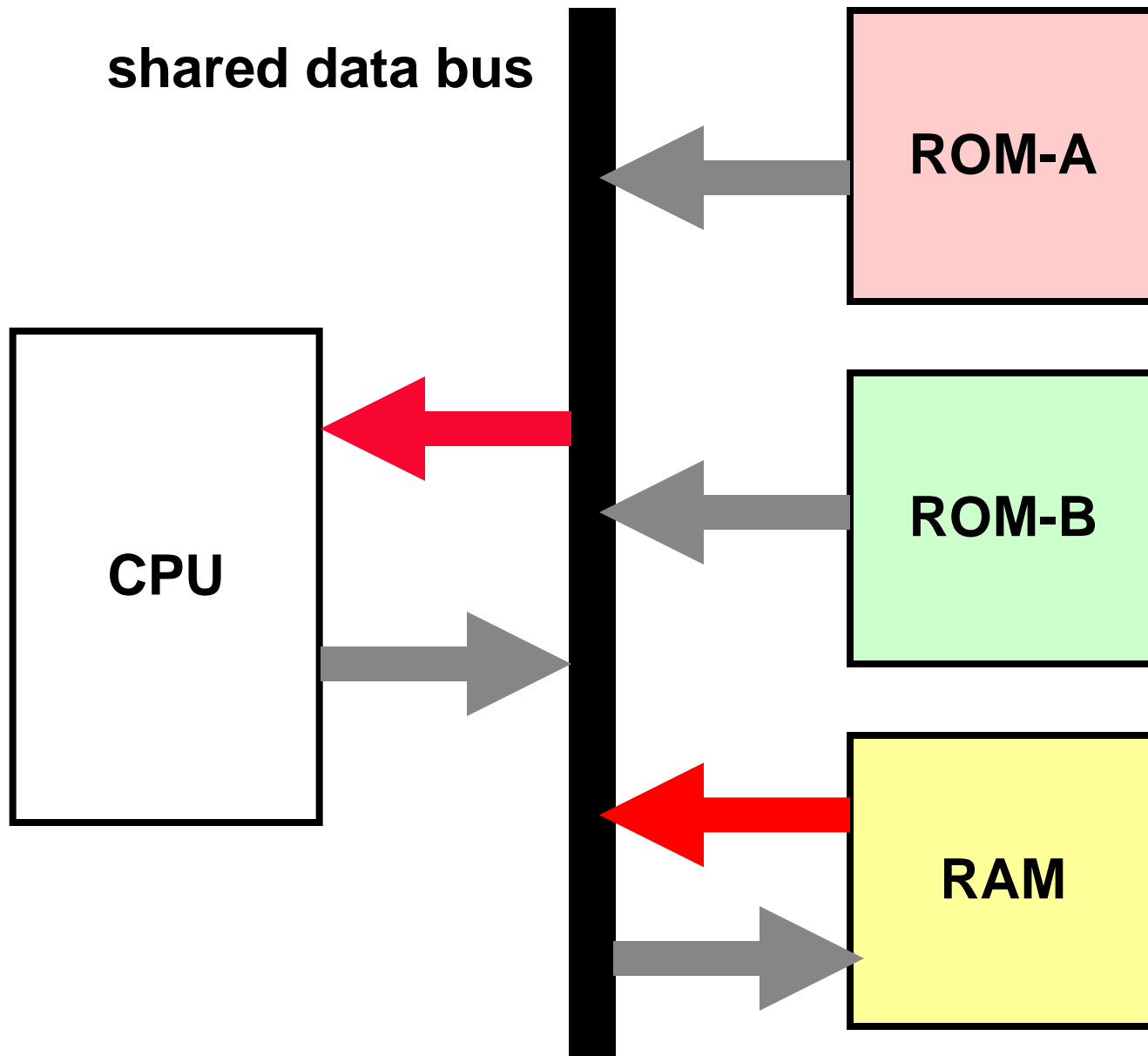
However, at any one time only one (or no) output should be enabled.

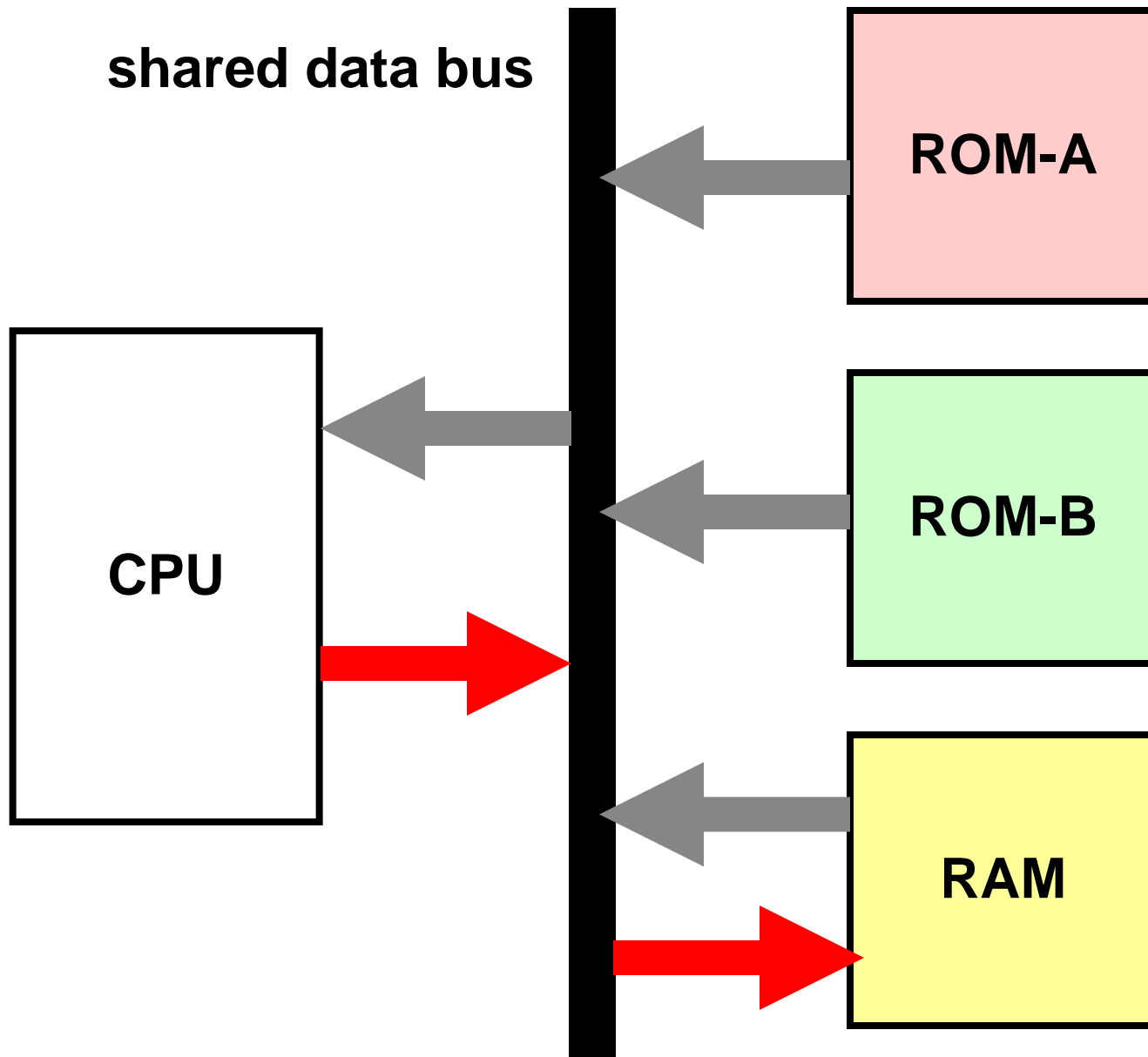
Otherwise, it can lead to bus contention and damage the devices.

Example: memory devices have tristate outputs to share the same data bus.



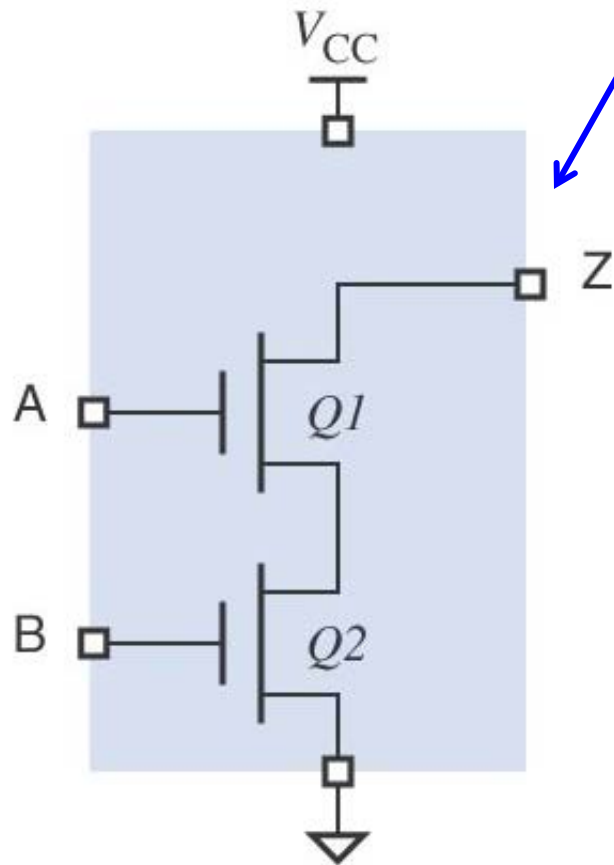






Open-collector/drain output

Need external pull-up resistor to make output=1



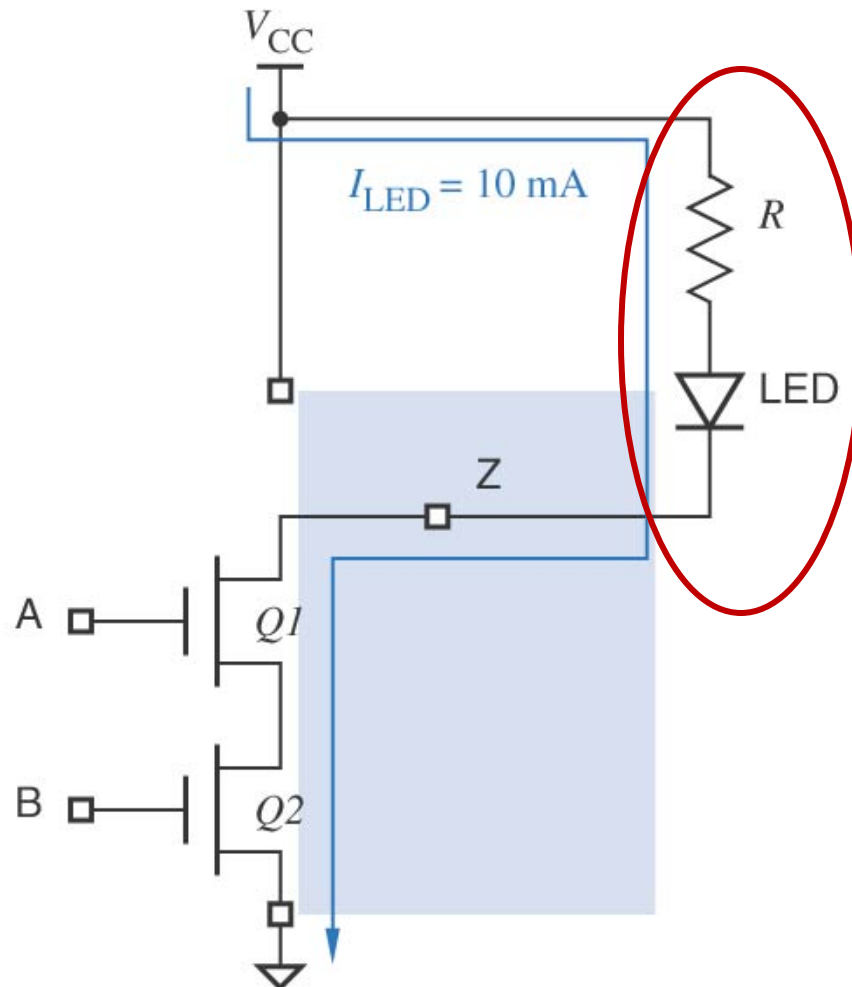
A	B	$Q1$	$Q2$	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

Symbol for open-drain



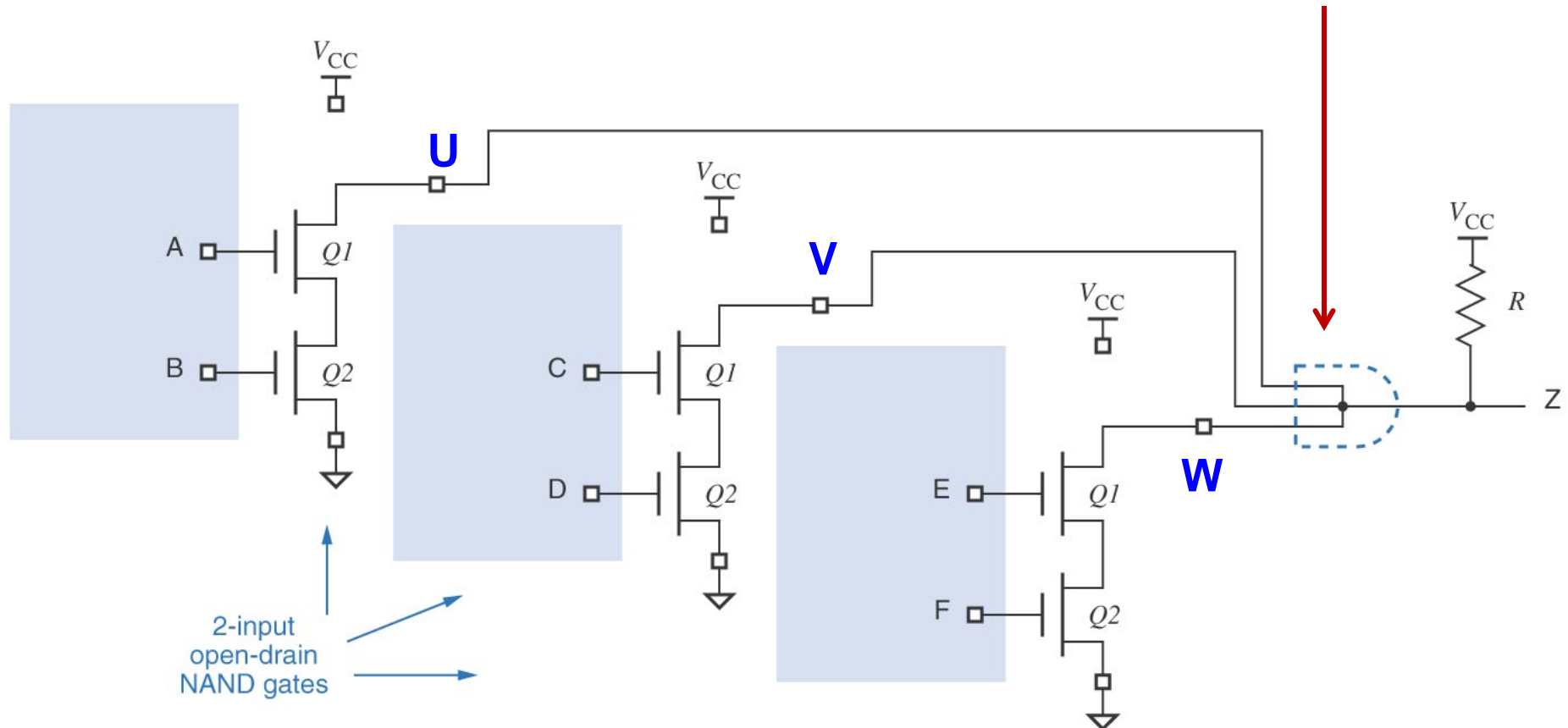
Open-drain output can be used to drive LED

- If $A=B=1$
- Q1 and Q2 ON
- LED ON
- If $A=0$ or $B=0$
- Q1 or Q2 OFF
- LED OFF



Open-drain outputs can be tied together

Form wired-AND logic



Wired-AND logic (in figure on previous page):

- **The common point Z will go low when any one of the NAND outputs, i.e. U, V or W is low**
- **The common point Z will be high only when all of the NAND outputs, i.e. U, V and W are high**

Imagine an elastic band: