

模拟与数字电路实验报告

1. 实验题目：实验 07 FPGA 实验平台及 IP 核使用

2. 实验目的：熟悉 FPGAOL 在线实验平台结构及使用，掌握 FPGA 开发各环节，学会使用 IP 核（知识产权核）




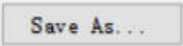
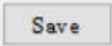


3. 实验平台：Vivado 软件

4. 实验练习：

1). 问题一：对于一个 16*8bit 的 ROM 例化并初始化，接到七段数码管上显示与开关相对应的十六进制数字

根据数码管对应数字二进制表示存入 ROM，例化如下：

Key	Value
memory_initialization_radix	2
memory_initialization_vector	00111111 00000110 01011011 01001111 01100110 ...

verilog 代码如下：

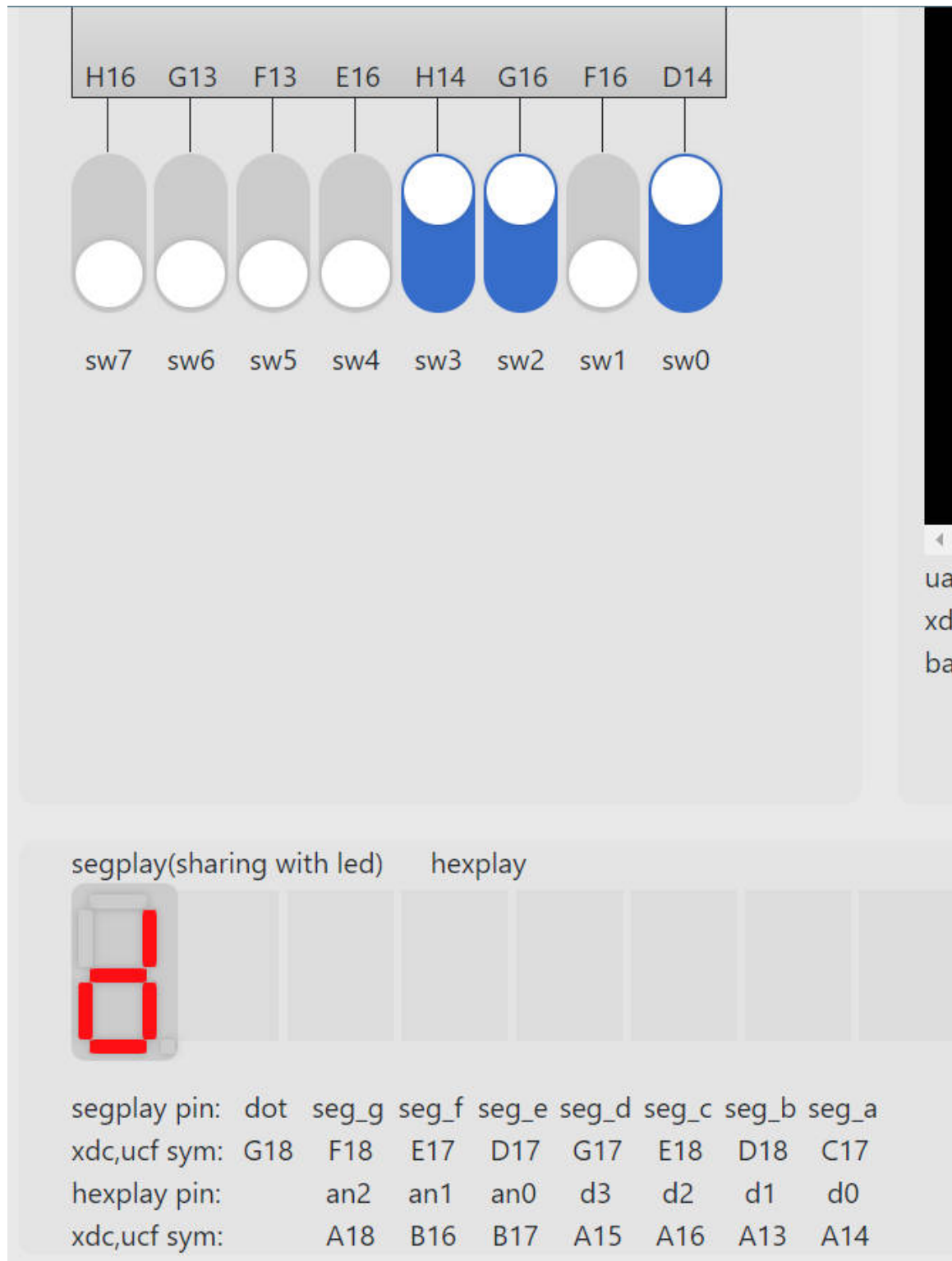
```
1  module problem1(  
2      input  [3:0] sw,  
3      input  clk ,  
4      output [7:0] led  
5  );  
6  dist_mem_gen_0 dist_mem_gen_0(  
7      .a    (sw),  
8      .spo(led)  
9  );  
10 endmodule
```

约束文件如下：

```
1 set_property -dict {PACKAGE_PIN E3 IOSTANDARD LVCMOS33 }  
2 [get_ports { clk }];  
3  
4 set_property -dict {PACKAGE_PIN C17 IOSTANDARD LVCMOS33 }  
5 [get_ports { led [0] }];  
6 set_property -dict {PACKAGE_PIN D18 IOSTANDARD LVCMOS33 }  
7 [get_ports { led [1] }];  
8 set_property -dict {PACKAGE_PIN E18 IOSTANDARD LVCMOS33 }
```

```
9    [get_ports { led [2] }]];
10 set_property -dict {PACKAGE_PIN G17 IOSTANDARD LVCMOS33 }
11    [get_ports { led [3] }]];
12 set_property -dict {PACKAGE_PIN D17 IOSTANDARD LVCMOS33 }
13    [get_ports { led [4] }]];
14 set_property -dict {PACKAGE_PIN E17 IOSTANDARD LVCMOS33 }
15    [get_ports { led [5] }]];
16 set_property -dict {PACKAGE_PIN F18 IOSTANDARD LVCMOS33 }
17    [get_ports { led [6] }]];
18 set_property -dict {PACKAGE_PIN G18 IOSTANDARD LVCMOS33 }
19    [get_ports { led [7] }]];
20
21 set_property -dict {PACKAGE_PIN D14 IOSTANDARD LVCMOS33 }
22    [get_ports { sw [0] }]];
23 set_property -dict {PACKAGE_PIN F16 IOSTANDARD LVCMOS33 }
24    [get_ports { sw [1] }]];
25 set_property -dict {PACKAGE_PIN G16 IOSTANDARD LVCMOS33 }
26    [get_ports { sw [2] }]];
27 set_property -dict {PACKAGE_PIN H14 IOSTANDARD LVCMOS33 }
28    [get_ports { sw [3] }]];
```

效果如下：



2). **问题二：**根据 8 个开关作为输入，十六进制数码管作为输出，采取对数码管扫描的方式，使得在视觉上同时显示在两个数码管上，由于扫描频率不能过快或者过慢，采取 100hz 作为扫描频率；

verilog 代码如下：

```

1  module problem2(
2      input  [7:0] sw,

```

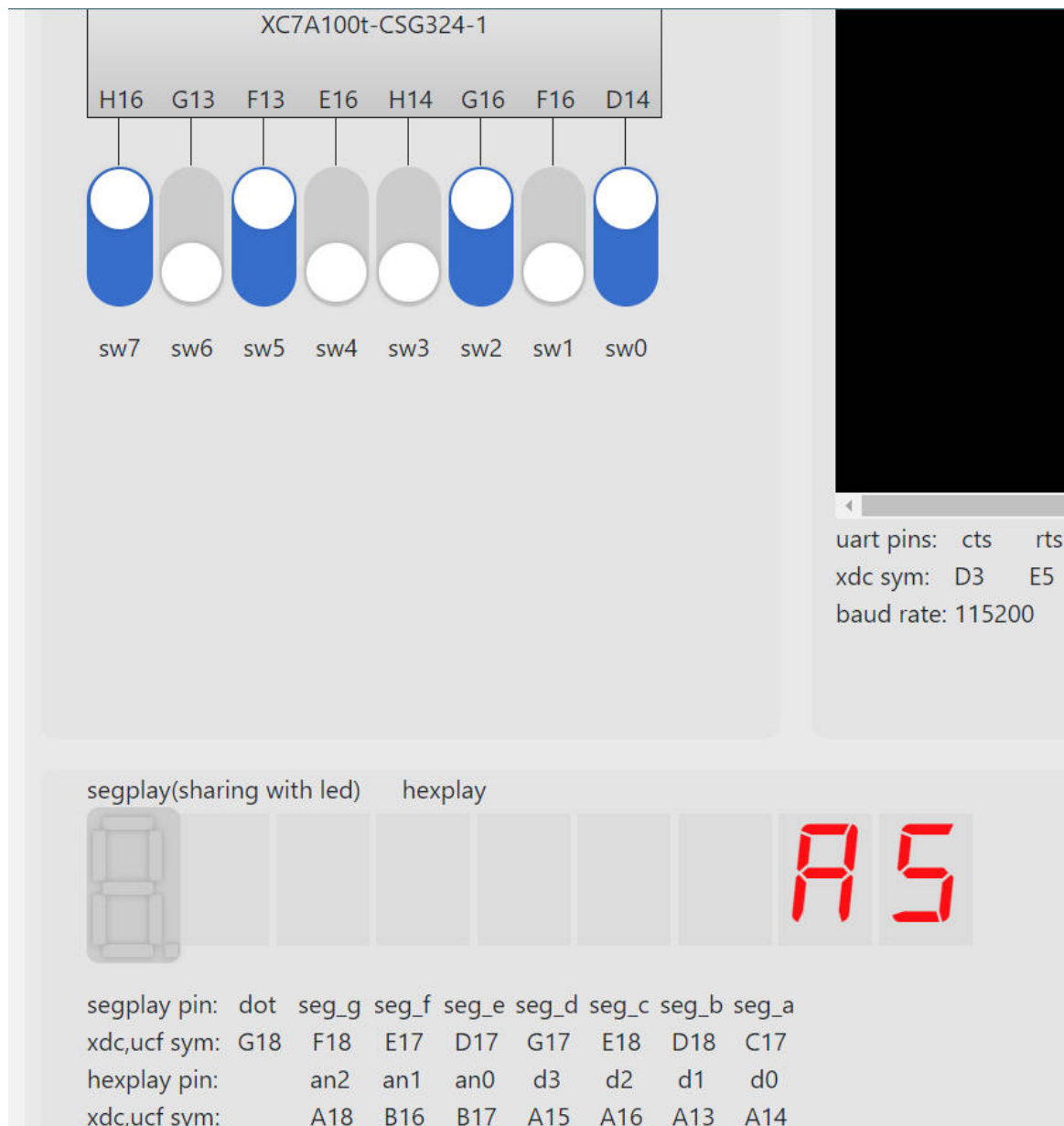
```
3    input clk ,
4    output reg [2:0]AN,
5    output reg [3:0]D
6    );
7    reg [15:0] cnt;
8    always@(posedge clk)
9    begin
10        if(cnt >= 10000)
11            cnt <= 0;
12        else
13            cnt <= cnt + 1;
14    end
15    always@(posedge clk)
16    begin
17        if(cnt == 0)
18            begin
19                if(AN == 3'b000)
20                    AN = 3'b001;
21                else
22                    AN = 3'b000;
23            end
24        end
25        always@(posedge clk)
26        begin
27            if(AN == 3'b000)
28                D <= sw[3:0];
29            else
30                D <= sw[7:4];
31        end
32    endmodule
```

约束文件如下：

```
1 set_property -dict {PACKAGE_PIN E3 IOSTANDARD LVCMOS33 }
2 [get_ports { clk }];
3
4 set_property -dict {PACKAGE_PIN A14 IOSTANDARD LVCMOS33 }
5 [get_ports { D[0] }];
6 set_property -dict {PACKAGE_PIN A13 IOSTANDARD LVCMOS33 }
```

```
7  [get_ports { D[1] }]];
8  set_property -dict {PACKAGE_PIN A16 IOSTANDARD LVCMOS33 }
9  [get_ports { D[2] }]];
10 set_property -dict {PACKAGE_PIN A15 IOSTANDARD LVCMOS33 }
11 [get_ports { D[3] }]];
12 set_property -dict {PACKAGE_PIN B17 IOSTANDARD LVCMOS33 }
13 [get_ports { AN[0] }]];
14 set_property -dict {PACKAGE_PIN B16 IOSTANDARD LVCMOS33 }
15 [get_ports { AN[1] }]];
16 set_property -dict {PACKAGE_PIN A18 IOSTANDARD LVCMOS33 }
17 [get_ports { AN[2] }]];
18
19 set_property -dict {PACKAGE_PIN D14 IOSTANDARD LVCMOS33 }
20 [get_ports { sw[0] }]];
21 set_property -dict {PACKAGE_PIN F16 IOSTANDARD LVCMOS33 }
22 [get_ports { sw[1] }]];
23 set_property -dict {PACKAGE_PIN G16 IOSTANDARD LVCMOS33 }
24 [get_ports { sw[2] }]];
25 set_property -dict {PACKAGE_PIN H14 IOSTANDARD LVCMOS33 }
26 [get_ports { sw[3] }]];
27 set_property -dict {PACKAGE_PIN E16 IOSTANDARD LVCMOS33 }
28 [get_ports { sw[4] }]];
29 set_property -dict {PACKAGE_PIN F13 IOSTANDARD LVCMOS33 }
30 [get_ports { sw[5] }]];
31 set_property -dict {PACKAGE_PIN G13 IOSTANDARD LVCMOS33 }
32 [get_ports { sw[6] }]];
33 set_property -dict {PACKAGE_PIN H16 IOSTANDARD LVCMOS33 }
34 [get_ports { sw[7] }]]];
```

效果如下：



3). **问题三：**利用两个计数器，100hz 用于对数码管扫描，10hz 用于 0.1s 的精确度计时；
verilog 代码如下：

```

1  module problem3(
2      input rst ,
3      input clk ,
4      output reg [3:0] D,
5      output reg [2:0] AN
6      );
7      reg [15:0] sw;
8      reg [31:0] cnt_100;
9      reg [31:0] cnt_10;
10

```

```
11     always@(posedge clk)
12     begin
13         if(cnt_100 >= 1000000)
14             cnt_100 <= 0;
15         else
16             cnt_100 <= cnt_100 + 1;
17     end
18
19     always@(posedge clk)
20     begin
21         if(cnt_100 == 0)
22             begin
23                 if(AN == 3'b011)
24                     AN <= 3'b000;
25                 else
26                     AN <= AN + 3'b001;
27             end
28     end
29
30     always@(posedge clk)
31     begin
32         if(cnt_10 >= 10000000)
33             cnt_10 <= 0;
34         else
35             cnt_10 <= cnt_10 + 1;
36     end
37
38     always@(posedge clk)
39     begin
40         if(cnt_10 == 0)
41             begin
42                 if(rst == 1)
43                     sw = 16'b0001001000110100;
44                 else
45                     sw <= sw + 16'b0000000000000001;
46
47                 if(sw[3:0] == 4'b1010)
```

```
48         begin
49             sw[7:4] <= sw[7:4] + 4'b0001;
50             sw[3:0] <= 4'b0000;
51         end
52         if(sw[7:4] == 4'b1010)
53             begin
54                 sw[11:8] <= sw[11:8] + 4'b0001;
55                 sw[7:4] <= 4'b0000;
56             end
57             if(sw[11:8] == 4'b0110)
58                 begin
59                     sw[15:12] <= sw[15:12] + 4'b0001;
60                     sw[11:8] <= 4'b0000;
61                 end
62                 if(sw[15:12] == 4'b1010)
63                     begin
64                         sw[15:12] <= 4'b0000;
65                     end
66             end
67         end
68
69         always@(posedge clk)
70         begin
71             if(AN == 3'b000)
72                 D <= sw[3:0];
73             else if(AN == 3'b001)
74                 D <= sw[7:4];
75             else if(AN == 3'b010)
76                 D <= sw[11:8];
77             else
78                 D <= sw[15:12];
79         end
80     endmodule
```

约束文件如下：

```
1 set_property -dict {PACKAGE_PIN E3 IOSTANDARD LVCMOS33 }
2 [get_ports { clk }];
3
```



```

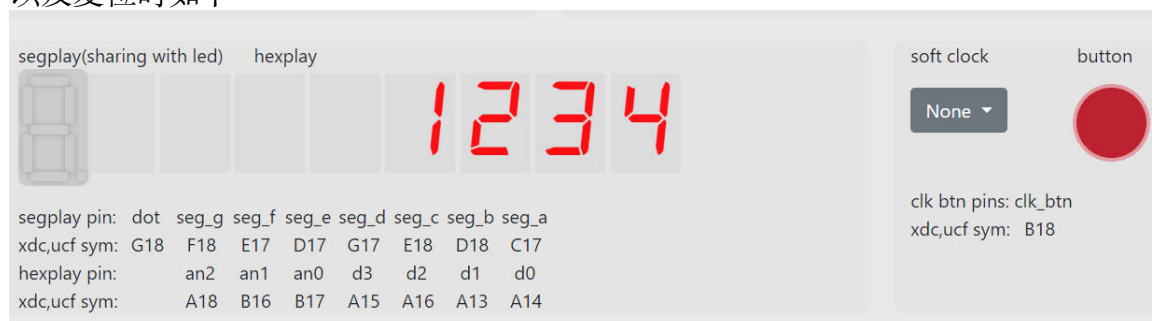
4 set_property -dict {PACKAGE_PIN B18 IOSTANDARD LVCMOS33 }
5 [get_ports { rst }];
6
7 set_property -dict {PACKAGE_PIN A14 IOSTANDARD LVCMOS33 }
8 [get_ports { D[0] }];
9 set_property -dict {PACKAGE_PIN A13 IOSTANDARD LVCMOS33 }
10 [get_ports { D[1] }];
11 set_property -dict {PACKAGE_PIN A16 IOSTANDARD LVCMOS33 }
12 [get_ports { D[2] }];
13 set_property -dict {PACKAGE_PIN A15 IOSTANDARD LVCMOS33 }
14 [get_ports { D[3] }];
15 set_property -dict {PACKAGE_PIN B17 IOSTANDARD LVCMOS33 }
16 [get_ports { AN[0] }];
17 set_property -dict {PACKAGE_PIN B16 IOSTANDARD LVCMOS33 }
18 [get_ports { AN[1] }];
19 set_property -dict {PACKAGE_PIN A18 IOSTANDARD LVCMOS33 }
20 [get_ports { AN[2] }];

```

效果如下：



以及复位时如下：



5. 总结与思考：

- 1). 收获：**通过本次实验对于 FPGA 有了相当了解，同时对于 Vivado 软件的使用有了更为深入的了解，学会 FPGA 开发的各环节以及 IP 核；
- 2). 评价：**实验内容相对而言较难，对于设计以及软件使用难度都有了较大的提升；

3). **建议：**实验内容设置合理，无较大建议；