模拟与数字电路实验报告

1. 实验题目： 实验 07 FPGA 实验平台及 IP 核使用

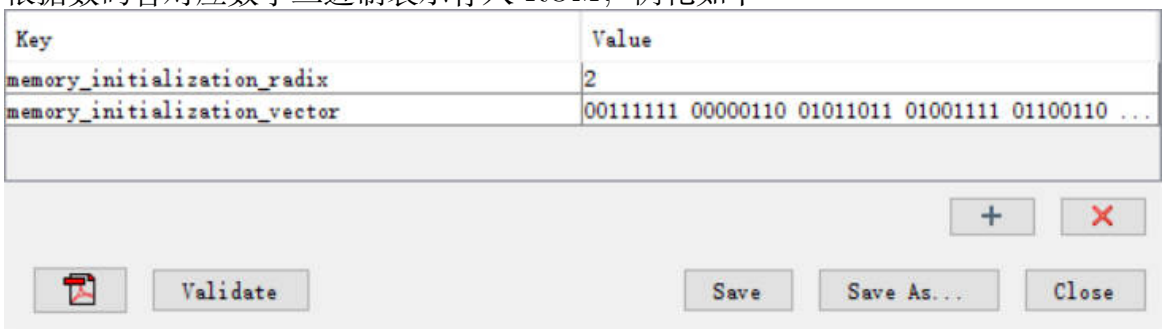
2. 实验目的： 熟悉 FPGAOL 在线实验平台结构及使用，掌握 FPGA 开发各关键环节，学会使用 IP 核（知识产权核）

3. 实验平台： Vivado 软件

4. 实验练习：

1). 问题一： 对于一个 16*8bit 的 ROM 例化并初始化，接到七段数码管上显示与开关相对应的十六进制数字

根据数码管对应数字二进制表示存入 ROM，例化如下：



verilog 代码如下：

```
module problem1(
  input [3:0] sw,
  input clk,
  output [7:0]led
    );
dist_mem_gen_0 dist_mem_gen_0(
  .a  (sw),
  .spo(led)
    );
endmodule
```

约束文件如下：

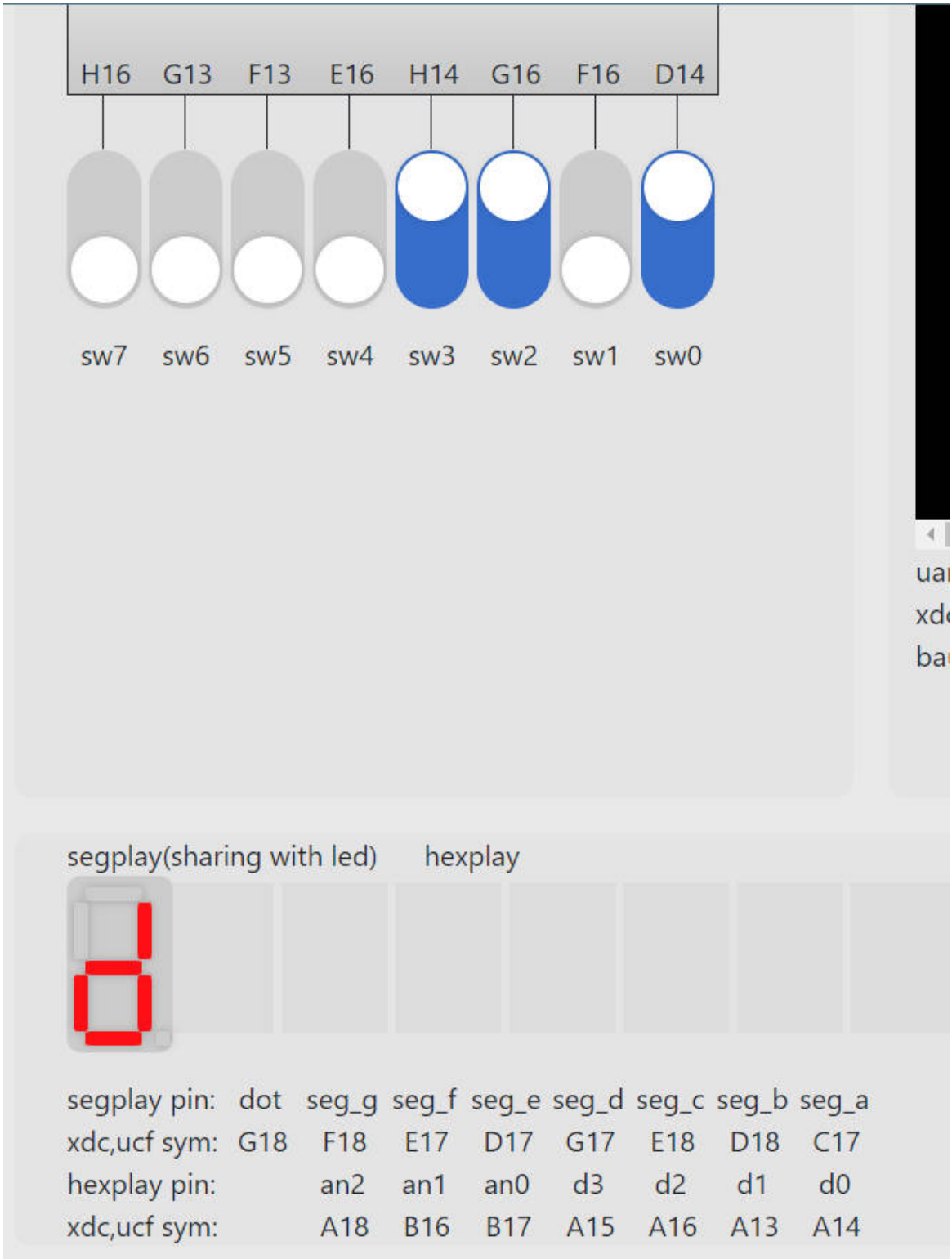
```
set_property  -dict {PACKAGE_PIN E3 IOSTANDARD LVCMOS33 }
  [get_ports { clk }];

set_property -dict {PACKAGE_PIN C17 IOSTANDARD LVCMOS33 }
  [get_ports { led[0] }];
set_property -dict {PACKAGE_PIN D18 IOSTANDARD LVCMOS33 }
  [get_ports { led[1] }];
set_property -dict {PACKAGE_PIN E18 IOSTANDARD LVCMOS33 }
```

```
  [get_ports { led[2] }];
set_property -dict {PACKAGE_PIN G17 IOSTANDARD LVCMOS33 }
  [get_ports { led[3] }];
set_property -dict {PACKAGE_PIN D17 IOSTANDARD LVCMOS33 }
  [get_ports { led[4] }];
set_property -dict {PACKAGE_PIN E17 IOSTANDARD LVCMOS33 }
  [get_ports { led[5] }];
set_property -dict {PACKAGE_PIN F18 IOSTANDARD LVCMOS33 }
  [get_ports { led[6] }];
set_property -dict {PACKAGE_PIN G18 IOSTANDARD LVCMOS33 }
  [get_ports { led[7] }];

set_property -dict {PACKAGE_PIN D14 IOSTANDARD LVCMOS33 }
  [get_ports { sw[0] }];
set_property -dict {PACKAGE_PIN F16 IOSTANDARD LVCMOS33 }
  [get_ports { sw[1] }];
set_property -dict {PACKAGE_PIN G16 IOSTANDARD LVCMOS33 }
  [get_ports { sw[2] }];
set_property -dict {PACKAGE_PIN H14 IOSTANDARD LVCMOS33 }
  [get_ports { sw[3] }];
```

效果如下：



2). 问题二： 根据 8 个开关作为输入，十六进制数码管作为输出，采取对数码管扫描的方式，使得在视觉上同时显示在两个数码管上，由于扫描频率不能过快或者过慢，采取 100hz 作为扫描频率；

verilog 代码如下：

```
1  module problem2(
2    input [7:0]sw,
```

```
    input clk,
    output reg [2:0]AN,
    output reg [3:0]D
        );
    reg [15:0] cnt;
    always@(posedge clk)
    begin
        if(cnt >= 10000)
            cnt <= 0;
         else
            cnt <= cnt + 1;
    end
    always@(posedge clk)
    begin
        if(cnt == 0)
        begin
            if(AN == 3'b000)
                AN = 3'b001;
            else
                AN = 3'b000;
        end
    end
    always@(posedge clk)
    begin
        if(AN == 3'b000)
            D <= sw[3:0];
        else
            D <= sw[7:4];
    end
    endmodule
```

约束文件如下：

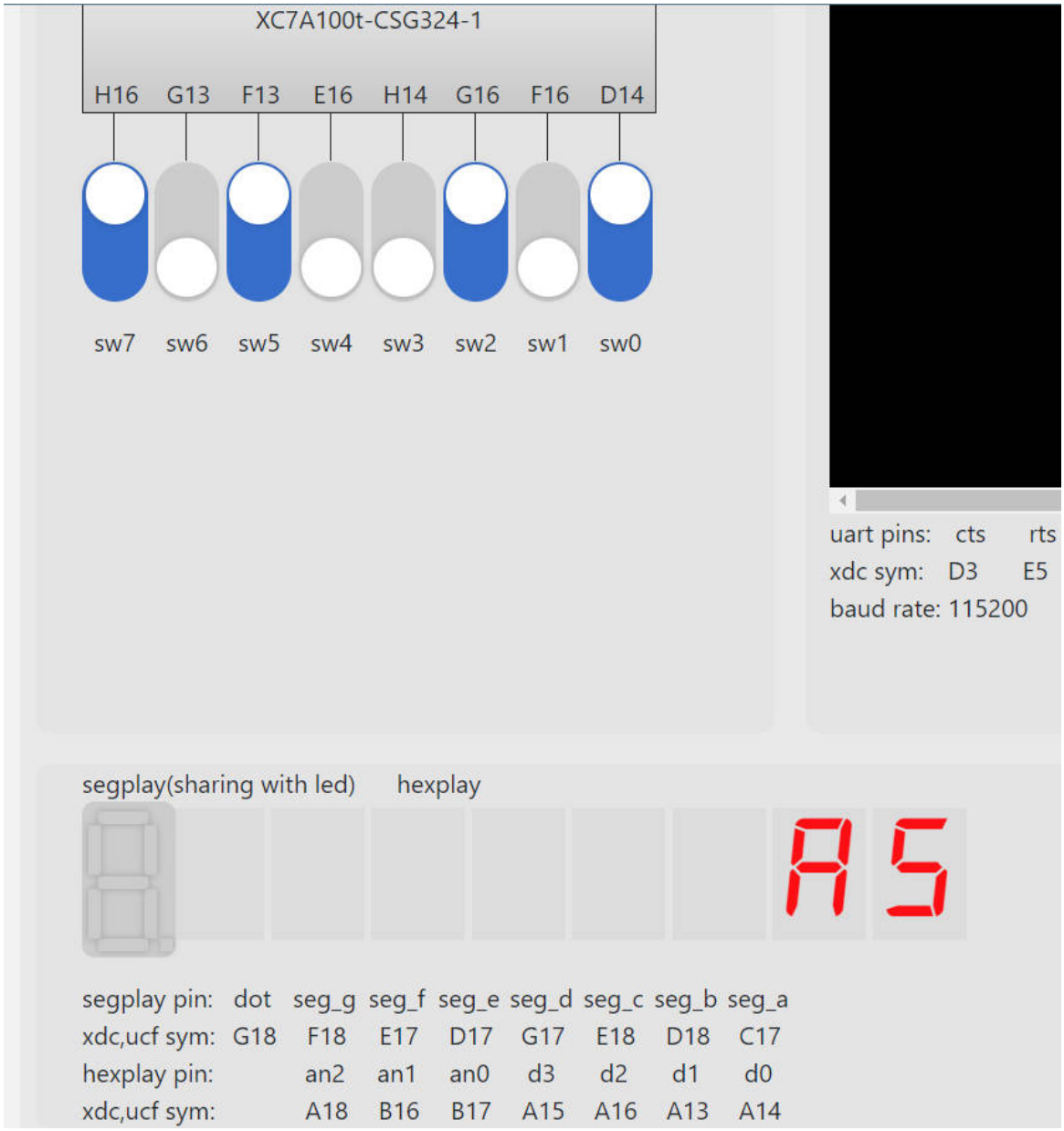
```
set_property -dict {PACKAGE_PIN E3 IOSTANDARD LVCMOS33 }
  [get_ports { clk }];

set_property -dict {PACKAGE_PIN A14 IOSTANDARD LVCMOS33 }
  [get_ports { D[0] }];
set_property -dict {PACKAGE_PIN A13 IOSTANDARD LVCMOS33 }
```

```
  [get_ports { D[1] }];
set_property -dict {PACKAGE_PIN A16 IOSTANDARD LVCMOS33 }
  [get_ports { D[2] }];
set_property -dict {PACKAGE_PIN A15 IOSTANDARD LVCMOS33 }
  [get_ports { D[3] }];
set_property -dict {PACKAGE_PIN B17 IOSTANDARD LVCMOS33 }
  [get_ports { AN[0] }];
set_property -dict {PACKAGE_PIN B16 IOSTANDARD LVCMOS33 }
  [get_ports { AN[1] }];
set_property -dict {PACKAGE_PIN A18 IOSTANDARD LVCMOS33 }
  [get_ports { AN[2] }];

set_property -dict {PACKAGE_PIN D14 IOSTANDARD LVCMOS33 }
  [get_ports { sw[0] }];
set_property -dict {PACKAGE_PIN F16 IOSTANDARD LVCMOS33 }
  [get_ports { sw[1] }];
set_property -dict {PACKAGE_PIN G16 IOSTANDARD LVCMOS33 }
  [get_ports { sw[2] }];
set_property -dict {PACKAGE_PIN H14 IOSTANDARD LVCMOS33 }
  [get_ports { sw[3] }];
set_property -dict {PACKAGE_PIN E16 IOSTANDARD LVCMOS33 }
  [get_ports { sw[4] }];
set_property -dict {PACKAGE_PIN F13 IOSTANDARD LVCMOS33 }
  [get_ports { sw[5] }];
set_property -dict {PACKAGE_PIN G13 IOSTANDARD LVCMOS33 }
  [get_ports { sw[6] }];
set_property -dict {PACKAGE_PIN H16 IOSTANDARD LVCMOS33 }
  [get_ports { sw[7] }];
```

效果如下：



3). 问题三： 利用两个计数器，100hz 用于对数码管扫描，10hz 用于 0.1s 的精确度计时；verilog 代码如下:

```
1  module problem3(
2    input rst,
3    input clk,
4    output reg [3:0] D,
5    output reg [2:0] AN
6        );
7    reg [15:0] sw;
8    reg [31:0] cnt_100;
9    reg [31:0] cnt_10;
10
```

```
    always@(posedge clk)
    begin
        if(cnt_100 >= 1000000)
            cnt_100 <= 0;
         else
            cnt_100 <= cnt_100 + 1;
    end

    always@(posedge clk)
    begin
        if(cnt_100 == 0)
        begin
            if(AN == 3'b011)
                AN <= 3'b000;
            else
                AN <= AN + 3'b001;
        end
    end

    always@(posedge clk)
    begin
        if(cnt_10 >= 10000000)
            cnt_10 <= 0;
         else
            cnt_10 <= cnt_10 + 1;
    end

    always@(posedge clk)
    begin
        if(cnt_10 == 0)
        begin
            if(rst == 1)
                sw = 16'b0001001000110100;
            else
                sw <= sw + 16'b0000000000000001;

            if(sw[3:0] == 4'b1010)
```

```
48              begin
49                  sw[7:4] <= sw[7:4] + 4'b0001;
50                  sw[3:0] <= 4'b0000;
51              end
52              if(sw[7:4] == 4'b1010)
53              begin
54                  sw[11:8] <= sw[11:8] + 4'b0001;
55                  sw[7:4] <= 4'b0000;
56              end
57              if(sw[11:8] == 4'b0110)
58              begin
59                  sw[15:12] <= sw[15:12] + 4'b0001;
60                  sw[11:8] <= 4'b0000;
61              end
62              if(sw[15:12] == 4'b1010)
63              begin
64                  sw[15:12] <= 4'b0000;
65              end
66          end
67      end
68
69      always@(posedge clk)
70      begin
71              if(AN == 3'b000)
72                  D <= sw[3:0];
73              else if(AN == 3'b001)
74                  D <= sw[7:4];
75              else if(AN == 3'b010)
76                  D <= sw[11:8];
77              else
78                  D <= sw[15:12];
79      end
80      endmodule
```

约束文件如下：

```
1 set_property -dict {PACKAGE_PIN E3 IOSTANDARD LVCMOS33 }
2   [get_ports { clk }];
3
```

```
set_property -dict {PACKAGE_PIN B18 IOSTANDARD LVCMOS33 }
  [get_ports { rst }];

set_property -dict {PACKAGE_PIN A14 IOSTANDARD LVCMOS33 }
  [get_ports { D[0] }];
set_property -dict {PACKAGE_PIN A13 IOSTANDARD LVCMOS33 }
  [get_ports { D[1] }];
set_property -dict {PACKAGE_PIN A16 IOSTANDARD LVCMOS33 }
  [get_ports { D[2] }];
set_property -dict {PACKAGE_PIN A15 IOSTANDARD LVCMOS33 }
  [get_ports { D[3] }];
set_property -dict {PACKAGE_PIN B17 IOSTANDARD LVCMOS33 }
  [get_ports { AN[0] }];
set_property -dict {PACKAGE_PIN B16 IOSTANDARD LVCMOS33 }
  [get_ports { AN[1] }];
set_property -dict {PACKAGE_PIN A18 IOSTANDARD LVCMOS33 }
  [get_ports { AN[2] }];
```

效果如下：

以及复位时如下：

5. 总结与思考：

1). 收获： 通过本次实验对于 FPGA 有了相当了解，同时对于 Vivado 软件的使用了有了更为深入的了解，学会 FPGA 开发的各环节以及 IP 核；

2). 评价： 实验内容相对而言较难，对于设计以及软件使用难度都有了较大的提升；

3). 建议：实验内容设置合理，无较大建议；