THE GEORGE WASHINGTON UNIVERSITY
WASHINGTON, DC

DEPARTMENT OF ELECTRICAL & COMUTER ENGINEERING
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New ECE Course for Spring 2017

ECE 6045: Special Topics: Design of Interconnection Networks for Parallel Computer Architectures

Instructor: Dr. Ahmed Louri, louri@gwu.edu, 5580 Science & Engineering Hall
Date and time: Tuesdays: 1:00 PM to 3:30 PM

Course Description and Objectives:
The computing industry is at a critical inflection point, unlike perhaps any since the development of the integrated circuit. While virtually every sector of our society – security, manufacturing, healthcare, financial, education, science, entertainment, and military – has very much become dependent on exponential growth in performance, the end of voltage scaling has made power dissipation (energy per operation times operations per second) the fundamental barrier to scaling computing performance across all platforms: from hand-held, embedded systems, to laptops, to servers, to datacenters. This challenge has forced the microprocessor designers to bet their entire future on parallelism (concurrency) as the only method of improving computing performance. With growing emphasis on parallelism as a means of extracting additional processor performance, the interconnection network connecting processing elements and memory units is becoming pervasive as it provides the adequate communication needs for parallel architectures. These architectures range from multicores where multiple cores (or processors) reside on the same chip and are connected through a Network-on-Chip (NoC), to multiple processors (multiprocessors) and multiple computers (multicomputers) in a system. With technology scaling into the nanoscale, the interconnection network is becoming the most critical factor in the design as it significantly impacts the performance, power consumption, cost, reliability, and scalability of future parallel computing systems.

The course will explore the architecture and design of interconnection networks for multiple domains (multicores, multiprocessors, multicomputers, and datacenters), including architecture topology, routing protocols, flow control, router design, reliability, energy efficiency, scalability, security, modeling and simulation tools, emerging technologies for interconnects (optical, wireless, RF, etc.) and emerging applications (neuromorphic, quantum, approximate computing, etc.). The course is intended to provide graduate students and engineers with an in-depth understanding of the fundamental engineering and design principles of both on-chip (NoC) and off-chip interconnection networks for parallel architectures with emphasis on recent research innovations in these areas.

At the end of the course, students will learn fundamental concepts, design trade-offs, technology factors, and evaluation methods and tools required for understanding and designing modern interconnection networks for parallel computer architectures ranging from mobile systems, to desktops, to servers, to clusters, to large datacenters. Further, students will gain a great understanding of current trends in computing and will be well positioned for successful careers in computer design.