mm-Wave Tunable Colpitts Oscillators Based on FinFETs

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***Abstract*— The characteristics of compact tunable Colpitts oscillators built using FinFET transistor technology are presented. As compared to a conventional single gate MOSFET, the use of common-mode FinFET architecture allows for a more relaxed oscillatory criterion for Colpitts oscillator design, while adaption of independent-mode FinFETs bestows a Colpitts oscillator with a simple and efficient means for tunable performance. The frequency can be tuned to an extent of ∼5% of center frequency without the need of any extra components such as varactors. The effect of supply voltage and FinFET dimensions on the oscillation frequency has also been investigated. The oscillation criterion is relaxed when compared to that of an identical design in single gate MOSFET due to the increase of g_m by a factor of 2 in case of a common-mode FinFET. No separate capacitors are used between the gate and source as part of a conventional Colpitts oscillator: The higher gate-source capacitance of the FinFET is conveniently utilized to substitute the external capacitor thus reducing parasitics and achieving the mm-wave frequency of 65 GHz and 165 GHz. The phase noise of the oscillator is -95 dBc/Hz at 1 MHz offset, for the case of 65 GHz circuit, which deteriorates in higher frequency versions. The compact and tunable characteristics of the proposed oscillator, along with its high frequency potential, make it suitable for applications such as on-chip wireless interconnects required for kilo-core computing that have hard limits on area and power but requires very precise tuning of the carrier.**

I. Introduction

Efficient circuit architectures are possible as we progress with novel semiconductor technologies beyond conventional CMOS devices. In the deca-nano regime, the conventional single-gate MOSFETs have been replaced by 3-D multi-gate devices [1]-[3]. These multi-gate nano-scale transistors can efficiently control the channel from multiple sides of the channel instead of one side as in a single-gate architecture. The ability to alter channel potential by multiple gates (i.e double, triple, surround) provides a relatively easier and robust way to control the channel electrostatics, reducing the short channel effects and leakage concerns considerably. With the multiple gate boundary conditions, efficient tunable analog performance is possible by independently driving FinFET dual gates developed originally for enhancing digital performance via symmetrically-biased (common mode) operation. Moreover, exploration of such analog circuits have become even easier and more practical, with the recent introduction of BSIM-IMG model that has been developed specifically for independent gate (IG) operation. Using the novel BSIM-IMG model, in the present paper we explore one such compact and efficient tunable analog circuit: Colpitts oscillator built using IG FinFETs. The proposed tunable Colpitts oscillators are designed especially for ultra-compact and low-power applications such as found in sensor networks and on- or off-chip wireless communications, where area and power are severely limited and accurate channel tuning and reconfiguration may be necessary.

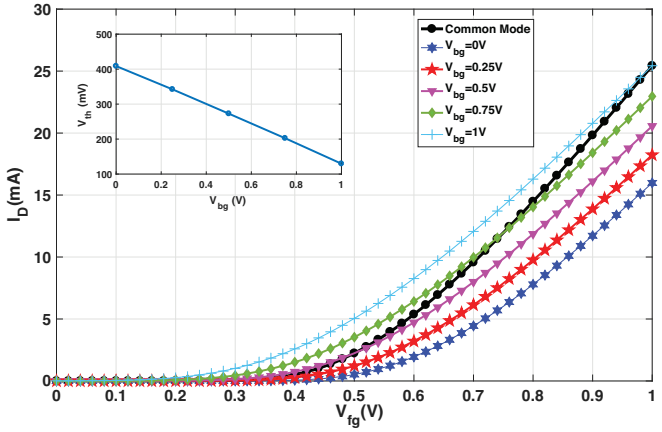

Fig. 1. I_D-V_{fg} characteristics of an n-type Independent ($V_{bg} \neq V_{fg}$) and Common ($V_{bg} = V_{fg}$) Mode DG transistors with BSIM-IMG FinFET. The inset shows the resulting shift in the front gate threshold.

A systematic study of FinFET based oscillator circuits has been achieved herein via BSIM-IMG model that has been developed using surface-potential based approach. The latest version (102.8.0) of the BSIM-IMG models the independent double-gate structure as a four terminal device, containing the source, drain, front and back gates [4]. The two gates are allowed to have different work functions ($\Delta\psi 1$, $\Delta\psi 2$) and dielectric thicknesses (t_{ox1}, t_{ox2}). They can also be biased separately at different voltages [4]. Thus the two gates can be used for alternative purposes in the IG configuration, which is utilized in the Colpitts oscillator investigated herein. The transfer characteristics (I_D-V_{fg}) of an IG-FinFET are shown in Fig. 1, which shows the change in drain current with the front gate voltage for different back gate biases. The common mode characteristic (when the two gates are tied together) has

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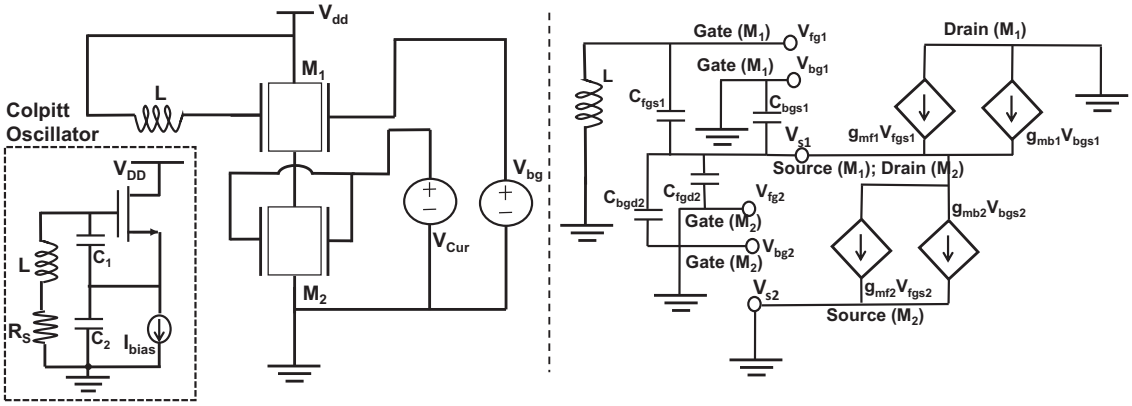

Fig. 2. The Colpitts oscillator designed utilizing the device parasitics and its small signal model.

also been plotted for comparison. Although common-mode provides a higher g_m, it can not be tuned.

Earlier works involving a series of radio frequency transceiver components have been studied in the FinFET technology, and their behaviour have been reported in [5]. As for oscillators reported earlier, the list include relaxation oscillator, cross-coupled LC and quadrature oscillators. The study of the characteristics of the Colpitts oscillator in this paper makes the list more exhaustive and introduces another tunable and compact oscillator architecture for mm-wave circuits. Additionally, a simplified design of Colpitts circuit is accomplished in this paper, thanks to elimination of external capacitors and utilization of FinFET's sizeable gate capacitance to achieve higher operating oscillation frequency. Finally, the use of newly available BSIM-IMG model for oscillator design is another novel aspect of this work, indicating the potential of BSIM-IMG for FinFET-based analog circuit design.

II. Colpitts Oscillator Design

Colpitts oscillator can be designed in all the three topologies: common-source, common-gate and as a source follower. In this paper, we have considered the source-follower topology as depicted in Fig. 2 (Inset) and modified the design with 65, 45 and 32 nm DG-FinFET devices as illustrated along with the small-signal model in Fig. 2. The inductor L along with the series combination of C_1 and C_2 form the parallel resonant tank circuit which determines the frequency of the oscillator given by the following equation:

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{1}{L}\left(\frac{C_1+C_2}{C_1C_2}\right)} \tag{1}$$

In the source-follower topology, the voltage across C_1 provides the positive feedback for oscillation.

To achieve higher operating frequency, one must minimise L, C_1 and C_2. However, as this is attempted, the effective impedance due to the inductor increases while the parasitic capacitance associated with L grows. Hence, the inductor's parasitics establishes an upper limit: Its capacitive effect counteracts the minimization of capacitances of C_1 and C_2 and ultimately affects the oscillation frequency in a way such that there is no significant increase in the oscillation frequency even with decreasing capacitances. Along with the impact on the oscillation frequency it also affects the symmetry of the voltage swing.

To reduce these non-linear effects, C_1 and C_2 are removed from the design. The gate-source capacitance of FinFET, C_{fgs1}, which is inherent to the device, can be used to substitute for C_1. This can be realised as they both represent the same nodes. The capacitor C_2 is essentially the parallel combination of C_{fgd2}, C_{bgd2} and C_{bgs1} in the modified circuit. The effect of C_{fgd2} is only significant as the two back gate capacitances are an order of magnitude less than C_{fgd2}. The calculation of C_{fgs1}, C_{fgd2}, C_{bgs2} and C_{bgd2} are initiated with the implementation of a simple RC circuit and from its time constant the capacitance values are computed. The computed values of the capacitances are given in Table I. Considering the AC/RF analysis initiated in the circuit the L can be connected to drain instead of the source in the modified circuit. The small signal model clarifies this further.

In establishing the frequency criterion of the oscillator, we can observe in comparison to the conventional single gate, the IG-FinFET has a more relaxed oscillatory criterion because of higher g_m. In fact, when the two gates are joined, the oscillator criterion of the common-mode device reduces to

$$g_m > \frac{1}{2}\omega^2 C_{fgs1} C_{fgd2} R_S \tag{2}$$

where, R_S is the resistive loss of the inductor. This is simply because the g_m gets at least doubled and can be verified from the small signal model in Fig. 2. In comparison, in a single-gate source-follower topology the oscillator criterion is given as [6],

$$g_m > \omega^2 C_{fgs1} C_{fgd2} R_S \tag{3}$$

The dimensions of M_2 must be optimized to sink the current from M_1 that determines the g_m to be used for oscillation criterion (Eq.2) and should remain in saturation.

III. Simulation Results

The simulation has been implemented with Cadence Spectre RF and results have been observed for different supply

TABLE I

PARASITIC CAPACITANCES OF M_1 & M_2

Capacitances	Value (fF)
C_{fgs1}	75
C_{fgd2}	130
C_{bgs1}	12
C_{bgd2}	9

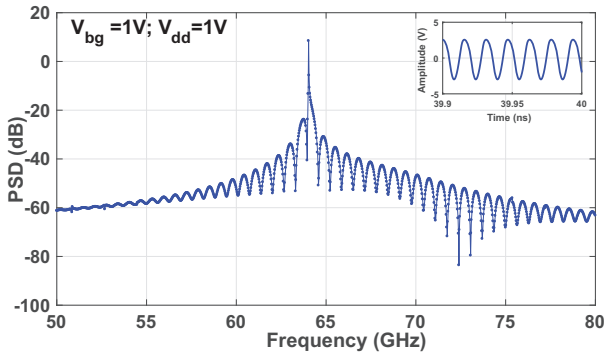

Fig. 3. The PSD of the DG-FinFET oscillator at 60 GHz for a supply of 1 V for a constant back gate bias of 1 V.

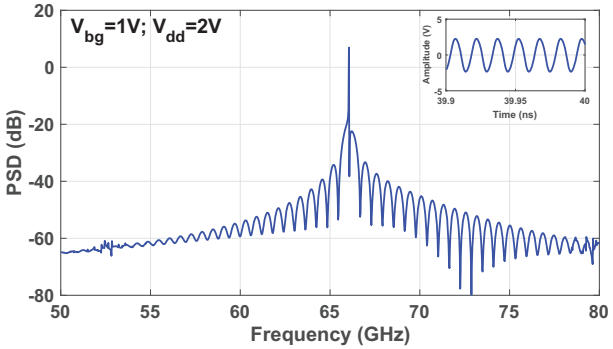

Fig. 4. The PSD of the DG-FinFET oscillator at 60 GHz for a supply of 2 V for a constant back gate bias of 1 V.

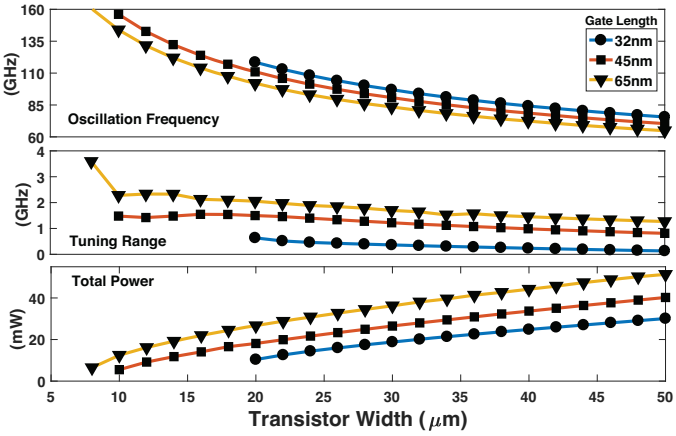

Fig. 5. The dependence of oscillation frequency, tuning range and power dissipation on transistor width (of both M_1 & M_2) of the DG-FinFET oscillator. V_{DD}=1 V in all cases

voltages as well as different back gate biases. The variation in oscillating frequency has been noticed in both the instances. The supply voltage has been varied from 1 V to 2 V and the back gate bias (V_{bg}) ranges from 0 V to 1 V. There is a change in frequency of oscillation from 64 GHz to 67 GHz for increasing values of V_{DD}. The PSD at 1 V and 2 V supply has been plotted and can be observed from the Fig. 3 & Fig. 4. The gate length of both the transistors are kept fixed at 65 nm and the width at 50 μm, if not otherwise stated.

As observed in Fig. 5, the frequency increases with decreasing transistor widths for different gate lengths (top). The gate capacitance increases with increasing widths, which decreases the frequency. The tuning range (middle) and the total power dissipation (bottom) also change with varying widths for all gate lengths studied. Thus it is possible to set the target frequency range using the device dimensions, before fine tuning of oscillator frequency via back gate bias. Clearly, the oscillator frequency up to 160 GHz is possible. Due to threshold voltage decrease, smaller transistors (e.g. L = 32 nm) have a smaller tunable range and lower power dissipation, even though they can reach higher frequencies at the same gate width.

The fine tuning of frequency with the back gate bias for three different supply voltages are illustrated plotted in Fig. 6. Without any change in the V_{bg}, and only changing V_{DD} the circuit shows 2.25-2 GHz difference in oscillation depending on the V_{bg}. So, overall the oscillator can be finely tuned any frequencies ranging between 64.1 to 67.48 GHz.

The variation of output power with different back gate bias at different transistor widths has been illustrated in Fig. 7. Significant variation with back gate bias is observed at the transistor width of 8 μm while at higher widths the back gate bias has no influence on the output power. Thus it is possible, for properly sized transistors, to separately tune the output frequency (via top transistor M_1) while using the lower FinFET (M_2) for amplitude tuning.

The proposed mm-wave oscillator is further modified to work at a maximum frequency of ∼160 GHz (Fig. 8). This has been achieved by reducing the width of the identical transistor to W/L = 8μm/65nm, which in essence reduces the gate-source capacitance. This also allows to reduce the current to 1.6 mA. The oscillation frequency changes between 157.48 GHz to 160.8 GHz (Fig. 9) depending on the bias voltage at V_{DD} = 2 V. At V_{DD} = 2 V and V_{bg} = 0 V, the oscillation frequency is 160.8 GHz and has a voltage swing from 0.5 to -0.5. At V_{bg} = 0.7 V, the oscillation has a frequency of 159.5 GHz and has a voltage swing from 0.56 to -0.56. As the V_{bg} increases beyond 0.7 V, the voltage swing dramatically drops. It has 3.4 GHz tunable bandwidth around 160 GHz with very little distortion on the oscillation signal.

The oscillation has a phase noise around -90.5 dBc/Hz at 1 MHz offset (Fig. 10) at 65 GHz carrier frequency. The phase noise deteriorates as the V_{DD} decreases or V_{bg} increases. The minimum is recorded as -93.3 dBc/Hz at V_{DD} = 1 V and

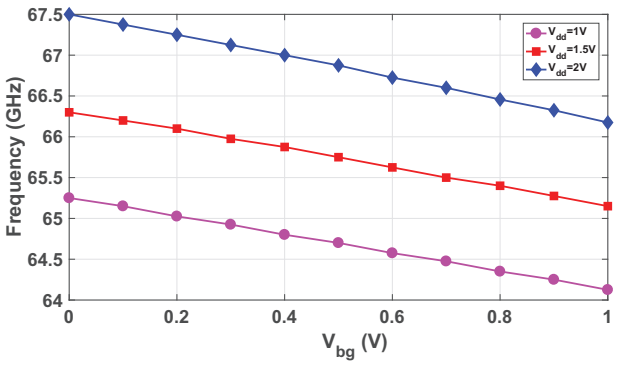

Fig. 6. Variation of oscillation frequency with different back gate bias at three different supply voltages at 60 GHz.

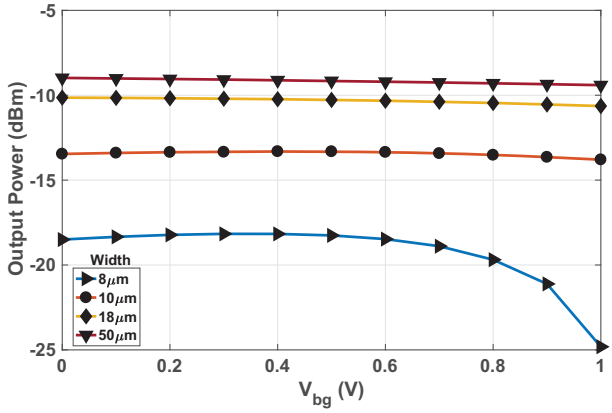

Fig. 7. The output power with different back gate bias for different transistor widths. Significant variation with back gate bias is observed at the transistor width of 8 μm while at higher widths the back gate bias has no influence on the output power.

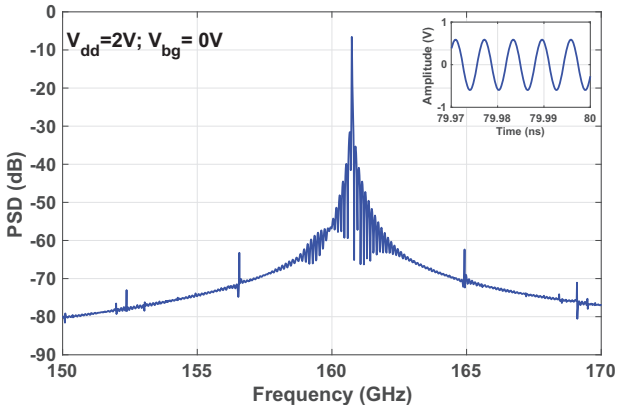

Fig. 8. The PSD of the DG-FinFET oscillator at 160 GHz for a supply of 2 V for a constant back gate bias of 1 V.

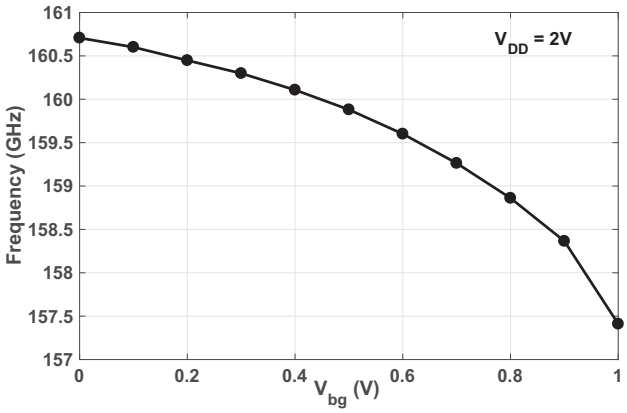

Fig. 9. Variation of oscillation frequency via back-gate bias around 160 GHz.

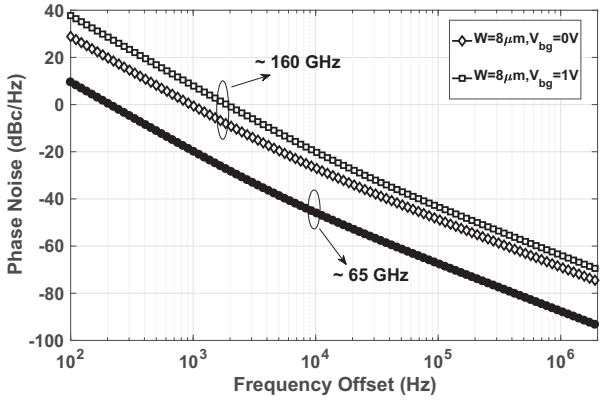

Fig. 10. The phase noise at the center frequency of 60 GHz and 160 GHz.

V_{bg} = 1 V and the maximum is recorded as -88.1 dBc/Hz Hz at V_{DD} =2V and V_{bg} = 0 V. At 160 GHz, the phase noise deteriorates and achieve a value of ∼-70 dBc/Hz. With application intended for on-chip networks (see below) where there is negligible interference of undesired signals and simple OOK modulation is used, the performance of the oscillator at this frequency with a "poor" phase noise can be tolerated. However, improvement of phase noise via additional circuit elements appears to be necessary for phase-critical modulation schemes such as PSK and QAM.

It is important to note that back-gate biasing does not lead to generation of additional high-order terms in the spectrum and cause inefficiency in oscillation performance. As illustrated in Fig. 11, the PSD of the 160 GHz oscillator has significant presence of 2^{nd} and 3^{rd} order harmonics. However, these harmonics remain remarkably similar in magnitude for different back-gate biases. Although generally undesirable, these harmonics can be effectively utilized to achieve higher frequency (eg. twice or thrice of the fundamental) outputs in push-push oscillator designs [7]. The future versions of the proposed Colpitts oscillator will also include such push-push topology with IG FinFETs, so that 500 GHz oscillator could be realized.

IV. Application Example: Wireless On-Chip Networks

Colpitts oscillator proposed here is intended for novel and unique Optical-Wireless NoC (OWN) architecture for kilo-core computing that utilizes both optical and wireless interconnects [8]. Wireless interconnect reduces the hop count between the optically connected clusters, leading to improved

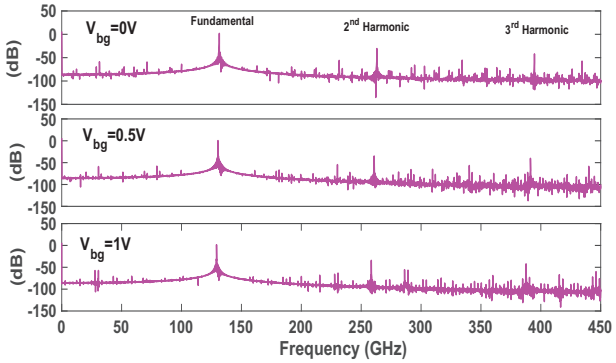

Fig. 11. The PSD of the DG-FinFET oscillator with higher order harmonics highlighted for future design of push-push oscillators to achieve oscillation frequency upto 400 GHz. The width considered here is 12 μm.

performance and more efficient utilization of the finite wireless bandwidth. Our previous results indicate that OWN architecture consumes 30.36% less energy, and improves throughput by 8% over wireless-alone architectures and obtains 35.5% less area than optical-alone architectures [8].

OWN is a tile-based architecture with each tile consisting of four processing cores and their private L1 instruction and data caches, a shared L2 cache and a network interface or router. Each tile is located within a cluster, which consists of 16 such tiles (64 cores), as shown in Figure 12. Four clusters form 256-core OWN architecture, which has an area of about 20 $\times$ 20 mm^2. Intra-cluster communication is implemented using optical interconnects whereas inter-cluster communication is facilitated using 16 wireless links operating within 20 GHz bands, between 50 and 380 GHz. Horizontal (H_n), vertical (V_n) or diagonal (D_n) wireless router pairs (n=1,2,3,4 in Figure 12) utilizing these links enable both neighboring and diagonal inter-cluster communication in the 256-core OWN architecture. Four additional reconfigurable routers (R_n) to be assigned according to the traffic load allow additional flexibility for the OWN interconnect architecture.

In principle, compact, single-inductor tunable yet efficient oscillators are required to implement the OWN architecture, for which the proposed Colpitts oscillators may be used. For instance, the proposed 160 GHz oscillator can serve as a VCO on one of the D1-D4 routers of the OWN architecture, coupled directly to the antenna, thus reducing both area and power associated with power amplifiers. Provided a low-parasitic inductor is available as part of the FinFET back-end process, it would be possible to design and assign different VCOs that can be finely tuned in a given router pair, or directly coupled to monopole antennas also designed by our group for the OWN architecture.

Another useful feature of the proposed Colpitts VCO for the OWN implementation is the presence of higher order harmonics that can be utilized for high-order oscillators. In the *push-push* oscillator configuration that can be designed with two cascode oscillator stages [7], such harmonics combine to result in 2^{nd} and 3^{rd} order harmonic oscillators in a

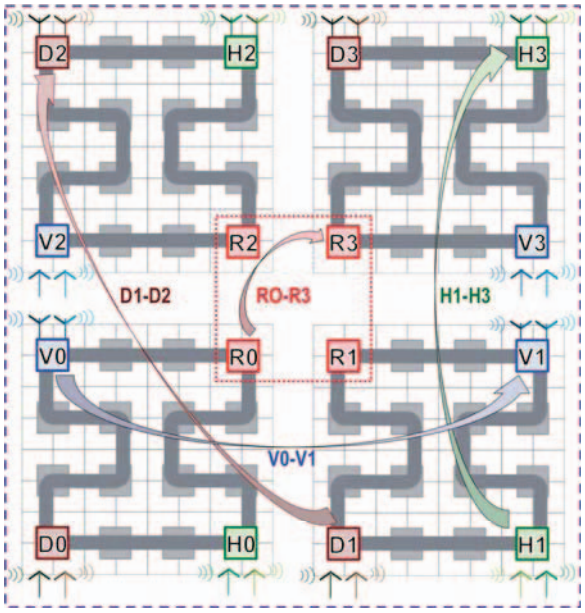

Fig. 12. 256-Core OWN architecture. Routers with same color communicate with each other [8].

relatively efficient and straightforward manner. Since wireless links require carriers up to 400 GHz range, push-push Colpitts oscillators can be a viable option to build also these sub-THz links for OWN, which is currently being developed by our team.

V. Conclusion

This paper showcases the various advantages of the novel BSIM-IMG FinFET model in the design of the compact and efficient Colpitts oscillator circuit in the mm-wave frequency up to 160 GHz. It also presents the oscillator in a new format with circuit modifications that eliminates the use external capacitors in favor of FinFET parasitics, ultimately achieving high frequency operation. The advantage of lenient oscillation criterion has been highlighted for the proposed FinFET Colpitts circuit. In common-mode operation when the two gates are joined, the criterion for oscillation is reduced to half when compared to the single-gate operation. As the two gates operate independently, the back gate bias has been utilized to tune the oscillation frequency. It is shown with rigorous simulation and optimization that independent-gate FinFETs can be used to build tunable sub-THz oscillators in an efficient manner, which is a requirement to build on-chip wireless routers in kilo-core computing. Although the proposed design is not verified experimentally, the use of experimentally tuned BSIM-IMG FinFET model and professional EDA tools provide confidence in the proposed oscillator design.

VI. Acknowledgement

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