Ultra-Compact sub-10nm Logic Circuits Based on Ambipolar SB-FinFETs

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***Abstract*— Novel ultra-compact sub-10nm XOR, NOR and NAND CMOS logic circuits based on ambipolar characteristics of Schottky-Barrier (SB) FinFET devices and gate metal workfunction engineering are introduced. Use of SB source and drain contacts, high-k gate dielectrics and ultra-thin body bestows extreme short-channel immunity to the proposed FinFETs with ambipolar current-voltage characteristics. Thus, the main physical parameter left for practical device design and threshold control is the gate workfunction along with independent-gate drive, which is creatively used in this work to build a novel conjugate (n/p channel) CMOS pass-gate transistor that can function as a two-transistor (2T) XOR gates as opposed to 4 transistor conventional pass-gates. In a similar fashion, gate workfunction engineering can be utilized to design unique ambipolar FinFETs with two independent gates and high thresholds to function as 2T NAND and NOR gates. Functionality of the proposed minimalist logic circuits are verified with Synopsys TCAD simulations, which indicate that optimized gate work-functions lead to CMOS logic circuits as small as 5nm and supply voltage of 0.6V, with a power-delay product at 5×10^{-18}J level.**

I. Introduction

In the last decade of Silicon CMOS engineering, options for reliable and simple device architectures that can deliver required I_{ON}/I_{OFF} current ratios and could be built using the existing material and toolset is rather limited. While intellectually not very rewarding (i.e. no paradigm shift), extension of Moore's law by traditional set of devices and materials in such fashion can be very beneficial financially, and provide additional time for the alternatives to Si CMOS to be fully developed. In the present work, we introduce and explore such an effort to extend conventional CMOS logic via gate workfunction engineering that may be a viable approach to build ultra-compact, relatively simple logic gates down to 5nm scale while also increasing the logic density by way independent-gate control in FinFETs. While standard Silicon CMOS is used for industrial and practical reasons, it should be pointed out on the onset that other ambipolar devices such as nanowire or carbon nanotube channels can also be used to implement transistor architectures presented here. Thus, ultra-high density logic circuit implementations proposed here can be generalized beyond silicon devices. The main device element enabling the proposed circuits is the Schottky-barrier (SB) FinFET that employs metal (typically silicide) source and drain contacts instead of slower and space-charge prone p-n junctions that has become especially problematic as gate dimensions are scaled to 10 nm [1]. Many of significant issues such as poor sub-threshold slope, larger RC parasitics, dopant fluctuations, fabrication challenges as well as incompatibility with novel 1D/2D channel materials (e.g CNT or graphene) can be alleviated with the use SB source and drain contacts which result in ambipolar carrier injection [1], [2]. The type of tunneling carriers, rather than the heavy doping in a p-n junction, determines the characteristics of an ambipolar SB-MOSFET, which suffers from additional series resistance associated with tunneling and reduced ON current, and hence could not quite compete with dominant state-of-the-art FinFET switches in conventional logic performance [2], [3]. In this work, we provide a proof-of-concept simulation analysis of how a unique asymmetric gate workfunction engineering, along with insight into the operation of CMOS transmission (pass) gate pairs can result in a remarkable XOR functionality out of a two-transistor (2T) FinFET cell. The same approach later can be also used to engineer low & high threshold n and p-type FinFET devices key to the 2T NAND and NOR functionality that was originally developed by IBM in 2006 using gate oxide and/or doping engineering [4] which is not feasible in sub-10nm devices. The proposed 2T-XOR gates based on asymmetric SB-FinFETs can in principle lead to substantial gains in logic density and reduction of parasitics

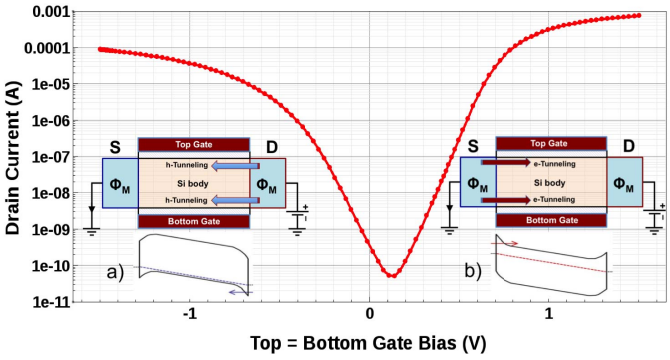

Fig. 1. I_D-V_{fg} schematics an characteristics of an ambipolar FinFET with midgap (4.6eV) source/drain contacts. Note the asymmetry in ON currents as well as minimum current bias. t_{OX}=1nm, ε_{OX}=12, t_{Si}=4nm and $V_{DS} = 0.5$V.

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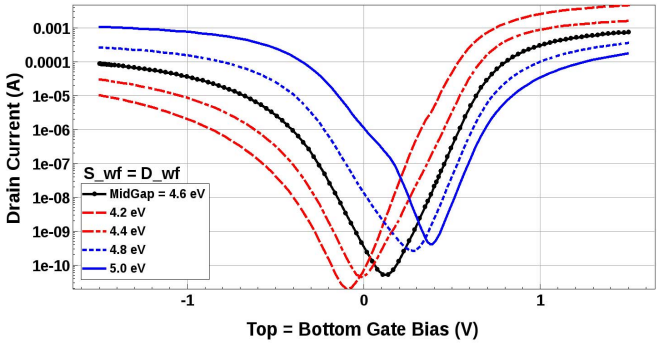


Fig. 2. Balanced ambipolar currents at V_{DS}=0.5V is only possible for S/D work-function of ~4.9eV, i.e. reduction (increase) of hole (electron) barrier, resulting in depletion-mode $V_{tp} > 0$ for hole channels and $min(I_D)$=~0.3V.

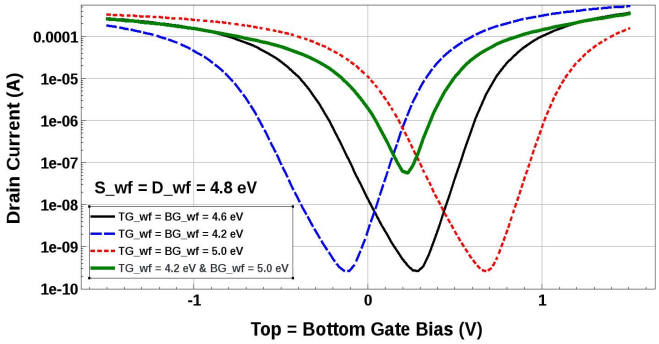
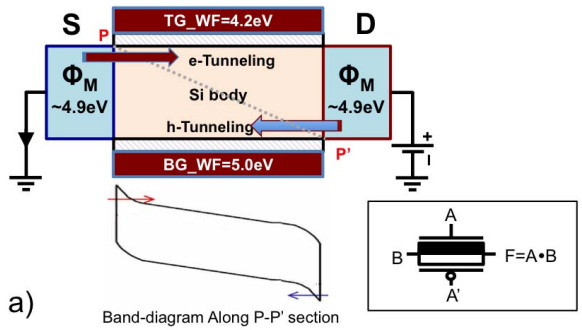


Fig. 3. Setting top & bottom gate work-functions to near band edge values (4.2 & 5.0eV) can provide an inherent 'electro-static bias? for top & bottom channel potentials apt for hole and electron injection, respectively, akin to a CMOS pass-gate.



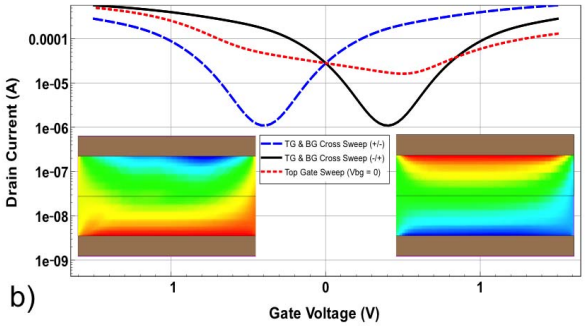


Fig. 4. Proposed SB-FinFET with parameters optimized for conjugate dual channels: a) Bottom gate for hole tunneling/conduction and top gate for electron tunneling/conduction;, b) simulated characteristics of optimized device.

in addition to low power consumption (OFF-current), good potential for scaling down to 5 nm and low-supply (0.5V) operation. It also presents a new route for SB-MOSFETs to offer logic performance in sub-10nm CMOS design.

II. Conjugate Pass-Gates & XOR

Fig.1 introduces the typical structure, operation and characteristics of a generic ambipolar FinFET transistor (t_{ox}=1nm, ε_{ox}=12, t_{Si}=4nm) with SB source/drain contacts. The presence of SB at the contacts 'lifts-up' the potential at the end of the channel that would otherwise slip away from gate control due to depletion fields of S/D junctions, thus improving device scalability. Normally, the two gates are physically one structure and driven together for maximum logic performance (I_{ON}/I_{OFF} ratio). They can create sufficiently thin and low barrier to tunnel only for one end of the channel and one type of carrier. Thus, the inherent 'duality' of the channels cannot be exploited in the same body, and the device can only function either as an n-type or p-type MOSFET at a given gate bias. However, if and when the FinFET gates are built from two different metals (possible, especially in lateral double gate configuration, but not a trivial task), this duality can be present at two separate channels under each gate. This is analogous to pass-gate (or transmission-gate) CMOS pair in parallel n/p-type MOSFETs driven with opposing logic states.

To attain and optimize this conjugate channel operation for logic performance, we illustrate in Fig.2&3 a clear design strategy using the same device parameters above. S/D workfunction is first substantially shifted toward valance band ($\sim 4.90\,eV$) in order to obtain similar ON currents for two channels: This is compulsory as large difference between electrons and holes in terms of effective masses for tunneling (m_e^*=0.2 & m_h^*=0.9) and density of states can result in up to two orders of magnitude difference in ON-currents. Thus, the apparent uneven ambipolar behavior resulting from mid-gap contacts (similar barrier heights) necessitates lowering (raising) barriers in favor of (against) holes (electrons). Next, the top and bottom gates can be 'electrostatically' biased (thresholds lowered) for preferred injection of different type of carriers by choice of different workfunctions (4.2eV vs. 5.0eV). This would place additional demands on device fabrication, especially for standard FinFET case. However, it is well within current level of gate engineering (epitaxial growth or ALD/CVD processes), especially if the lateral double-gate architecture is pursued [3,4]. Nonetheless, the resulting gate-wise asymmetric device is still very much vulnerable to DIBL-related shifts in I-V shifts and imbalances. As a result, it is best to keep $V_{DS} = V_{DD}/2 = 0.5$V throughout this optimization for optimal (balanced) logic switching performance. Thus. it has been possible to design and verify operation of an ambipolar FinFET pass-gate logic switch (see Fig.4) that can be used to build ultra-compact 2T exclusive OR/NOR gates as shown in Fig.5&6.

Fig.5 clearly shows that the optimally designed 10nm

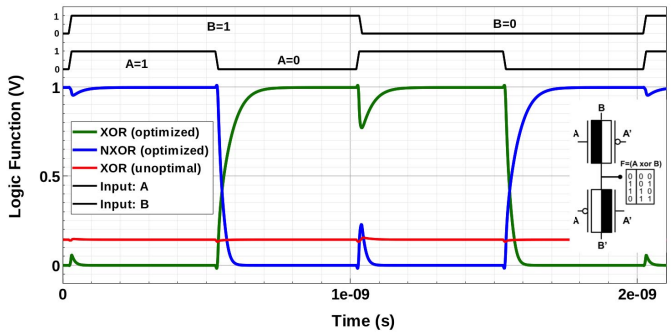


Fig. 5. Verification of ambipolar 2T XOR & XNOR Functions via TCAD simulation.

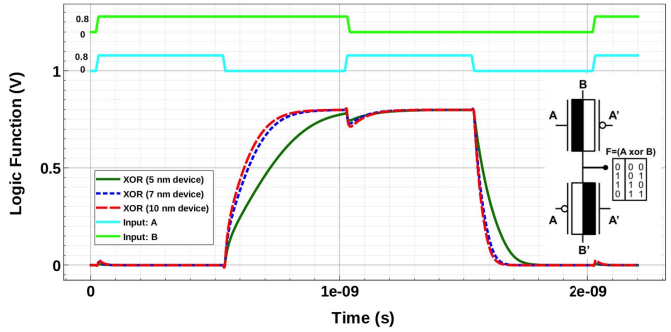


Fig. 6. Simulated 2T XOR functions based 7nm and 5nm versions of the ambipolar FinFETs with $V_d = 0.8$V

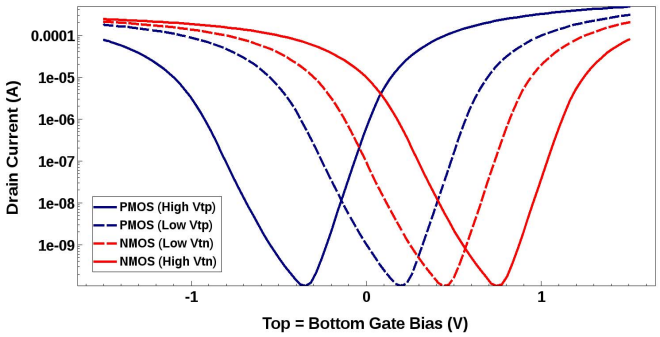


Fig. 7. I-V characteristics of ambipolar FinFETs optimized for low & high threshold FinfETs of both polarity. See text for the corresponding workfunctions

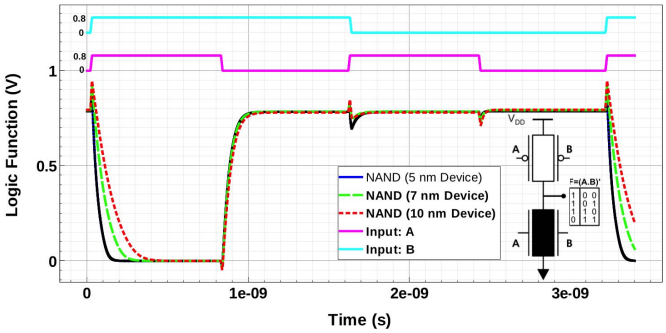


Fig. 8. Verification of ambipolar 2T NAND function via TCAD simulation. NAND operation is confirmed down to 5nm gate length using the same optimized workfunctions

ambipolar FinFET pass-gates result in correctly and evenly switching XOR/XNOR logic gates. Conversely, the un-optimized device (Fig.1) cannot deliver the same output. Moreover, the exact same work-functions applied to $L = 7$nm ($t_{Si} = 3$nm) and $L = 5$nm ($t_{Si} = 2$nm) XOR gates (Fig.6) also operate with nearly similar conviction at $V_{DD} = 0.8$V. More accurate (NEGF) transport models, quantum mechanical corrections and other optimization strategies are currently must be pursued to quantify XOR switching performance.

III. 2T NOR & NAND via Ambipolar FinFET

Gate workfunction engineering can be extended to alter the threshold voltage of a given ambipolar n/p-type SB-FinFET. This should be done with care since arbitrary choice of workfunctions is not only realistic it would also be very demanding for process engineers, even if it was possible to set them arbitrarily. Following the same strategy to optimize device channel thresholds as before, but keeping top/bottom gate workfunctions exactly the same (unlike XOR case), it is possible to obtain low and high V_t devices for both n and p-type SB-FinFETs with relative ease. The resulting $I_D - V_G$ characteristics can be found in Fig.7, which shows four seperate devices, each optimized for a specific function: i) high-V_{tp} pMOS with $\Phi_{tg} = \Phi_{bg} = 4.80$eV; ii) low-$V_{tp}$ pMOS with $\Phi_{tg} = \Phi_{bg} = 5.10$eV; iii) low-$V_{tn}$ nMOS with $\Phi_{tg} = \Phi_{bg} = 4.00$eV; iv) high-$V_{tn}$ nMOS with $\Phi_{tg} = \Phi_{bg} = 4.55$eV. According to the simulated I-V curves, it is obvious that characteristics can be shifted steadily from left to right as the workfunctions are changed from close to mid-gap values (i.e. larger barriers) to band edges (i.e. severely reduced electron or hole barriers), thus creating four distinct FinFETs with high and low thresholds, respectively.

Chiang and co-workers [5] has already shown by simulation that a single high-V_{tn} independent gate FinFET can be utilized as an AND logic pull-down element that only conducts if both gates are biased with logic 1 (V_{DD}) input. This creates an extremely compact 2T NAND gate, that has been shown to reduce both power (40%) and delay (10%), culminating in an absolutely minimal logic gate arrangement. A similar arrangement can be made for p-MOS pull-up network, replacing two series pMOS with a single independent-gate high-V_{tp} SB-FinFET. However, the original work suggested using oxide thickness to adjust for high-Vt, which is impractical and sub-optimal. In the our approach, using the I-V characteristics optimized only by the choice of gate work-functions, it is possible to implement such logic circuits using the above set of sub-10nm SB-FinFETs as shown in Fig.8 and Fig.9.

According to the logic operations in Fig.8 and Fig.9, only a pair of ambipolar SB-FinFETs with low-V_{tp} (empty MOSFET symbol) and high-V_{tn} devices (filled symbol) in series arrangement will work as a NAND logic gate. Similarly, in the opposite arrangement, a NOR logic operation is also confirmed. Moreover, in all cases the logic gates are found to operate correctly with supply voltages as low as 0.6 V and

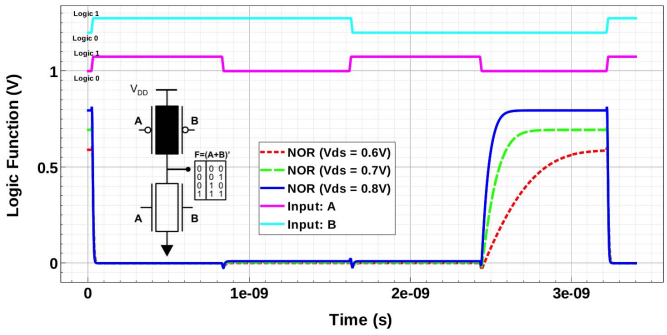


Fig. 9. Verification of ambipolar 2T NOR function via TCAD simulation. NOR operation is confirmed with supply voltages as low as 0.6V

gate lengths as short as 5 nm using the exact same arrangement of workfunctions. In other words, the optimization is valid for a relevant and practical range of devices and operating conditions.

IV. Discussions

It is only fair and necessary to point out that the proposed device concept heavily relies on the capability of building independent gates of FinFETs with four specific workfunctions. Due to the asymmetry of the electron and hole tunneling rates these workfunctions are not symmetrical around mid-gap. Moreover, the drain-induced bias asymmetry (DIBL) at large switch voltage extremes also contribute to the asymmetry of these optimal workfunctions. While introduction of four optimal workfunctions in different gates is indeed a real challenge in manufacturing, it is within the reach of current metal-gate CMOS processes and is easier than integrating entirely new channels or new device architectures, especially in the short term. Clearly, additional simulations with more accurate quantum mechanical corrections and transport model (NEGF) would be necessary to ensure that the proposed device optimizations are indeed accurate and applicable to real cases. Moreover, with more careful choice of tunneling masses it may be possible to further tune the gate workfunctions. It is also helpful to note that there are other recent efforts [6], which explore the gate-function tuning for the independent FinFET for SRAM memory cells, which should give us additional confidence in pursuing the presented optimization and novel gate architectures for logic.

Power-delay product (PDP) of the resulting 5nm NOR and NAND gates (for $V_{DD} = 0.8$V case) are found to be 3.91×10^{-18}J and 5.44×10^{-18}J, as opposed to the earlier XOR gate that has PDP of 5.78×10^{-18}J. While these values are not accurate given the finite parasitics included in the TCAD model ($R_{S,D} = 50$ Ohms and $C_L = 1fF$) and lack of gate tunneling in the present model, they do indicate a very competitive logic performance for the proposed circuits. Similarly, a general assessment of area for the novel XOR, NAND and NOR gates has also been undertaken, based on the recent work of Kim *et al.* [7] and taking into account additional area to route independent gate signals. This preliminary analysis shows that these compact gates can be laid out within $120\lambda^2$ where λ=fin pitch. Thus, depending on the fin pitch for the process employed as well as the M0 contact design rules, we estimate that area increase for the compact gate will be between 1.4 to 2 times as compared to standard (symmetrically driven) FinFET layout. Such an increase is well justified, given the substantial savings in reducing the number of transistors as well as parastics associated with local interconnects. In the next phase of the work, a more accurate, quantitative and comparative analysis of the proposed devices in terms of PDP and layout will be necessary.

V. Conclusion

A novel approach to design and operate ultra-compact XOR, NAND, NOR gates in sub-10nm CMOS was proposed and verified via TCAD simulations. The approach utilizes independent-gate Schottky-barrier FinFETs with specific gate work-functions that can be conveniently utilized unique and compact logic circuits. The first is a two-transistor (2T) XOR circuit based on a hitherto unexplored conjugate dual-channel transistor akin to CMOS pass-gates but having only one pair of S/D contacts and opposing gate workfunctions on two gates. Similarly, novel 2T NAND and NOR gates have also been proposed using high/low threshold devices, utilizing two different workfunctions for n and p type SB-MOSFETs. All gates have been confirmed via standard Synopsys TCAD tools and found to have competitive PDP at 5×10^{-18}J scale, which needs to be studied further with more accurate transport models and parasitics.

VI. Acknowledgement

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