Hardware Programming HWP1

capturing a
FPGA
design with
VHDL

Planning: theory

- First week
  - Introduction digital systems
  - Introduction to FPGAs
  - Structured digital Design
  - Modelling concepts in VHDL
- Second week
  - Introduction VHDL
  - Design verification
  - Code structure and data types
- Third week
  - Combinational versus sequential design
  - Concurrent and sequential code
  - Signals and variables
- Fourth week
  - Components
  - Generics
- Fifth week
  - Designing state machines

Agenda

- **Discussion of previous week**
- Component instantiating
- Generics

Signals versus variables

- **SIGNAL** properties:
  - Can *ONLY* be declared outside a **PROCESS** but can be used within a **PROCESS**
  - Within sequential code the signal is not 'updated immediately' (at the end of the **PROCESS**)
  - Only a *single* assignment is allowed to a signal in the whole code (multiple assignments in **PROCESSES** are fine, but only the last one will be effective!)
- **VARIABLE** properties:
  - Can *ONLY* be declared inside a **PROCESS**
  - Is 'updated immediately' and can be used in the next line of code
  - *Multiple* assignments are not a problem

Agenda

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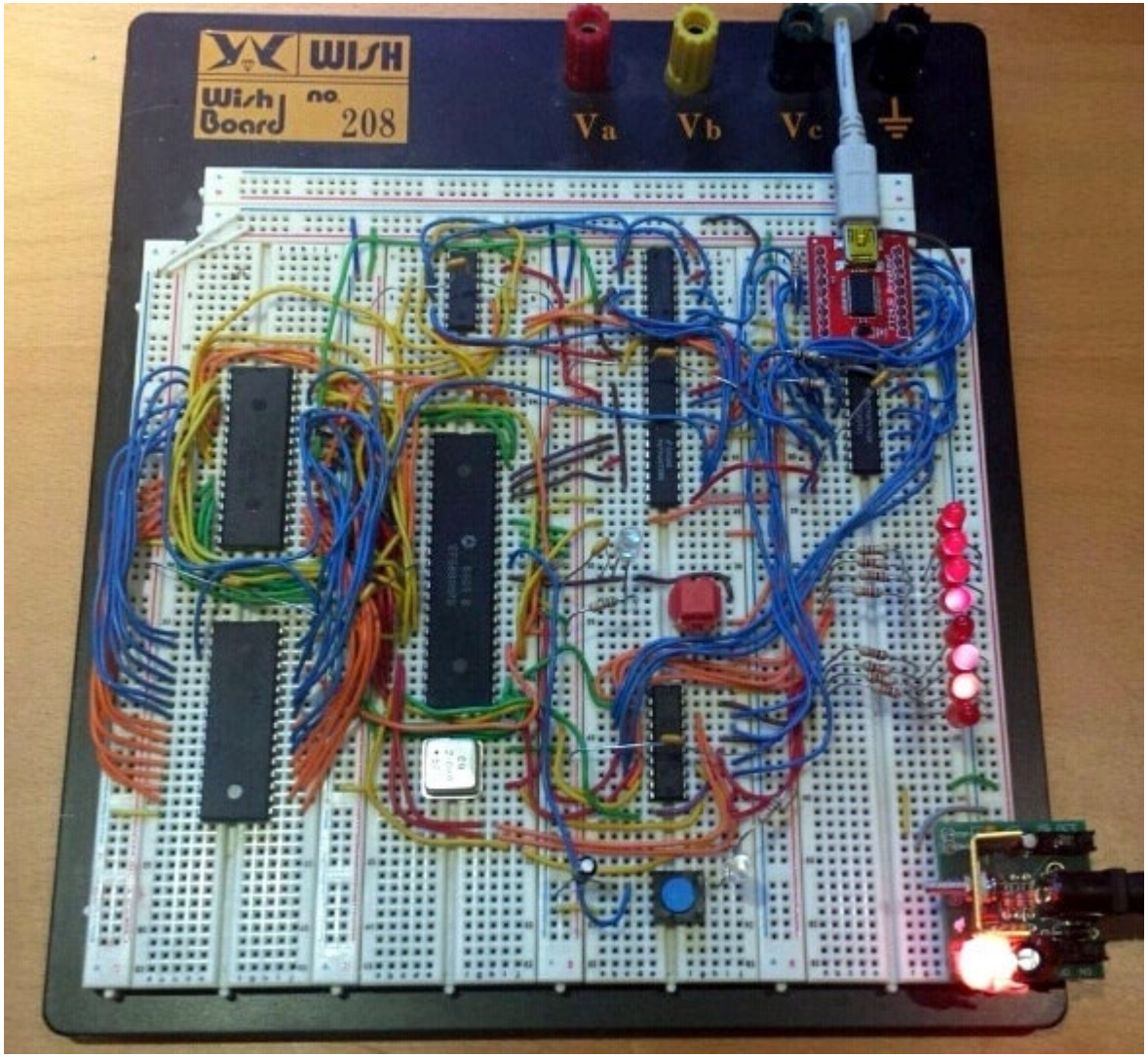
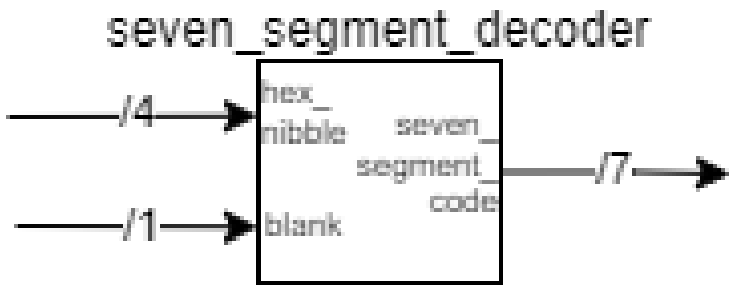
Putting it together

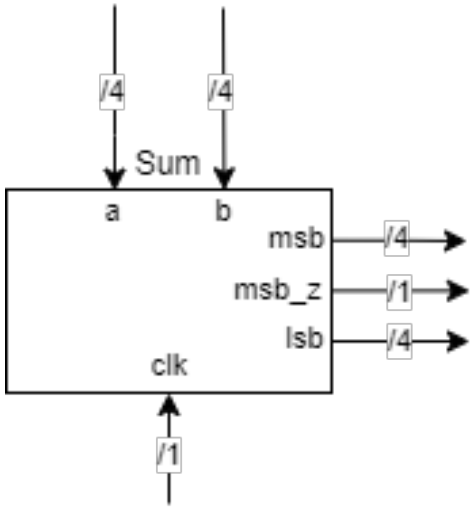


Create (separately) validated components



Entity

Architecture

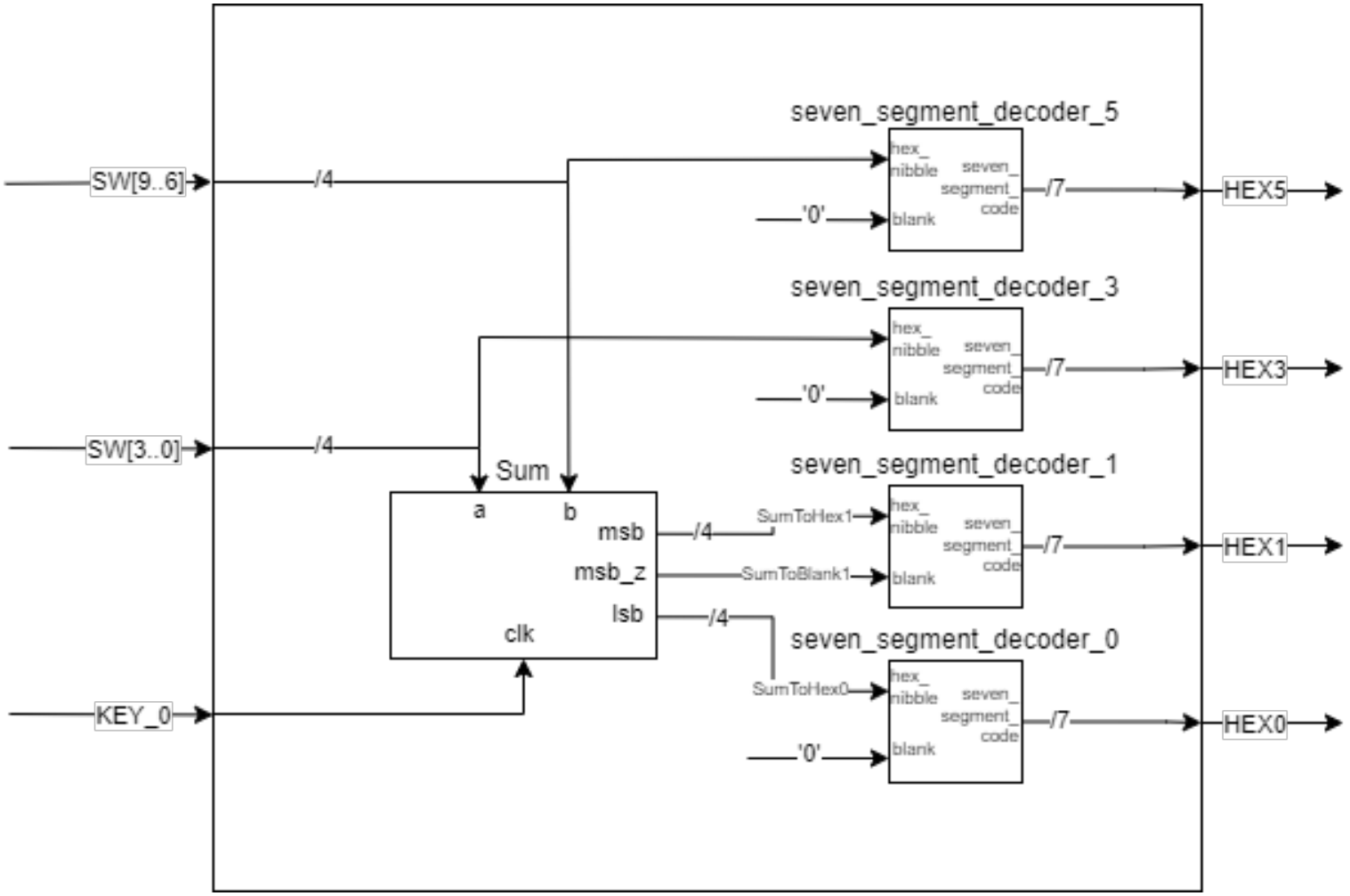


Entity

Architecture

Add components to your top level design

" Top Level Design: multiply_2hexandDisplay.vhd"



Instantiating components

```
begin
    hex5decoder: seven_segment_decoder port map(
        sw => A, blank => '0', hex0 => hex5
    );
    hex3decoder: seven_segment_decoder port map(
        sw => B, blank => '0', hex0 => hex3
    );
    hex1decoder: seven_segment_decoder port map(
        sw => sum_msn, blank => blank_msn, hex0 => hex1
    );
    hex0decoder: seven_segment_decoder port map(
        sw => sum_lsn, blank => '0', hex0 => hex0
    );
```

```
duv : assignment3 port map(
    A => A_tb, B => B_tb, clk => clk_tb, hex0 => hex0_tb, hex1 => hex1_tb, hex3 => hex3_tb, hex5 => hex5_tb
);
```

Agenda

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- Component instantiating
- **Generics**

Generic statements

- Generic values are used for declaring global constants in a component
- What is the use of generics?
- For more information on generics and what else they are capable of, see CH 6.7

Voorbeeld Generics

- With value

```
entity add_compare_cell is
   generic (
      NUM_BITS: natural := 16)
   port (
      a, b: in std_logic_vector(NUM_BITS-1 downto 0);
      comp: out std_logic;
      sum: out std_logic_vector(NUM_BITS downto 0));
end entity;
```

- Without value

```
generic (
   type bus_type;
   BUS_WIDTH: natural := 32;
   LAST_ADDRESS: natural);
```

Summary

- Remember the differences between signals and variables
- Components are pre-validated VHDL library elements used to reduce development time of new products.

- Next week:
  - Chapter 15 (16) “The Case of State Machines