EE575 – Group Project Assignment A
Design of a DC–DC Boost Converter

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January 25, 2026

1 Introduction

This report presents the design calculations and component selection for a DC–DC boost converter as specified in the EE575 Group Project Assignment. The objective is to design an open-loop boost converter operating in continuous conduction mode (CCM) with a rated output power of 30 W. Emphasis is placed on sound engineering justification for the selection of switching frequency, passive components, semiconductor devices, and current limits.

2 Design Specifications

The target specifications provided in the assignment are summarized in Table 1.

Table 1: Design Specifications

Parameter	Specification
Input Voltage (V_{in})	12 V
Output Voltage (V_o)	24 V
Rated Output Power (P_o)	30 W
Operating Mode	CCM
Maximum Output Voltage Ripple	$\leq 2\%$
Switching Frequency (f_s)	100 kHz

3 Duty Cycle Calculation

For an ideal boost converter operating in CCM, the voltage conversion ratio is given by:

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{1}$$

Solving for duty cycle D:

$$D = 1 - \frac{V_{in}}{V_o} = 1 - \frac{12}{24} = 0.5 \tag{2}$$

4 Inductor Design

4.1 Average Inductor Current

Assuming ideal operation:

$$I_{L,avg} = I_{in,avg} = \frac{P_o}{V_{in}} = \frac{30}{12} = 2.5\,\text{A} \tag{3}$$

4.2 Inductor Ripple Current

The peak-to-peak inductor current ripple is given by:

$$\Delta I_L = \frac{V_{in} \cdot D}{L f_s} \tag{4}$$

Choosing a ripple current of approximately 30% of the average inductor current:

$$\Delta I_L = 0.3 \times I_{L,avg} = 0.75\,\text{A} \tag{5}$$

Solving for the inductance:

$$L = \frac{V_{in} \cdot D}{\Delta I_L \cdot f_s} = \frac{12 \times 0.5}{0.75 \times 100 \times 10^3} = 80\,\mu\text{H} \tag{6}$$

A standard inductance value of 82 µH is selected.

4.3 Peak Inductor Current and Current Limit

The peak inductor current is:

$$I_{L,pk} = I_{L,avg} + \frac{\Delta I_L}{2} = 2.5 + 0.375 = 2.875\,\text{A} \tag{7}$$

Applying a design margin of 50% to account for tolerances, transient conditions, and startup:

$$I_{L,limit} = 1.5 \times I_{L,pk} = 4.31\,\text{A} \tag{8}$$

The inductor saturation current rating is therefore chosen to be greater than 4.5 A.

5 Output Capacitor Design

The output capacitor is selected to meet the output voltage ripple requirement of $\leq 2\%$:

$$\Delta V_o \leq 0.02 \times 24 = 0.48\,\text{V} \tag{9}$$

For a boost converter, the output voltage ripple is approximated by:

$$\Delta V_o = \frac{I_o \cdot D}{C \cdot f_s} \tag{10}$$

Where:

$$I_o = \frac{P_o}{V_o} = 1.25\,\text{A} \tag{11}$$

Solving for the capacitance:

$$C = \frac{I_o \cdot D}{\Delta V_o \cdot f_s} = \frac{1.25 \times 0.5}{0.48 \times 100 \times 10^3} \approx 13\,\mu\text{F} \tag{12}$$

To account for ESR effects and to reduce ripple further, a 47 µF electrolytic capacitor in parallel with a 1 µF ceramic capacitor is selected.

6 Semiconductor Device Selection

6.1 MOSFET

The MOSFET must withstand:

- Drain-source voltage $\geq V_o = 24\,\text{V}$
- Peak current $\geq I_{L,limit} = 4.31\,\text{A}$

Including voltage and current margins, a MOSFET rated for at least 60 V and 10 A is selected.

6.2 Diode

The diode must withstand:

- Reverse voltage $\geq V_o$
- Average current $\geq I_o = 1.25\,\text{A}$
- Peak current $\geq I_{L,pk}$

A Schottky diode with a voltage rating of 60 V and current rating of 5 A is selected to minimize conduction losses.

7 Justification of Switching Frequency

A switching frequency of 100 kHz was selected as a compromise between:

- Reduced inductor and capacitor size
- Acceptable switching losses
- Feasible EMI performance for laboratory implementation

At this frequency, the inductor ripple current remains within acceptable limits while maintaining CCM operation at rated load.

8 Conclusion

This report presented the complete design calculations for a 30 W, 12 V to 24 V DC–DC boost converter operating in CCM. Component values and current limits were selected based on worst-case analysis and appropriate safety margins. The designed parameters form the basis for simulation and subsequent hardware implementation.