EE587 Individual Project

Milestone 1

- Write a Verilog module to perform edge detection algorithm (Sobel filter) in behavioral simulation.
- Doesn’t require hardware implementation for Milestone 1.
- Deadline – 13th February, 2026.
- Use a high level language to generate a reference.

Milestone 2

- Implement the design on the Basys3 FPGA board to display the output image through the VGA output.

- Deadline – To be announced.