1.

HEX	Binary	Offset	set	tag	1	2	3	4
0000	0000 0000 0000 0000	0000	000	0000 0000 0	miss	miss	miss	miss
0004	0000 0000 0000 0100	0100	000	0000 0000 0	Hit	Hit	Hit	Hit
000c	0000 0000 0000 1100	1100	000	0000 0000 0	Hit	Hit	hit	Hit
00d0	0000 0000 1101 0000	0000	101	0000 0000 1	Miss	Miss	Miss	Miss
00e0	0000 0000 1110 0000	0000	110	0000 0000 1	Miss	Miss	Miss	Miss
1130	0001 0001 0011 0000	0000	011	0001 0001 0	Miss	Miss	Miss	Miss
0028	0000 0000 0010 1000	1000	010	0000 0000 0	Miss	miss	Miss	Miss
113c	0001 0001 0011 1100	1100	011	0001 0001 0	Hit	Hit	Hit	Hit
2204	0010 0010 0000 0100	0100	000	0010 0010 0	hit	Hit	Hit	Hit
0010	0000 0000 0001 0000	0000	001	0000 0000 0	Miss	Miss	Miss	Miss
0004	0000 0000 0000 0100	0100	000	0000 0000 0	Miss	Hit	Hit	Hit

0040	0000 0000 0100 0000	0000	100	0000 0000 0	Miss	Miss	Miss	Miss
2208	0010 0010 0000 1000	1000	000	0010 0010 0	Miss	Miss	Hit	Hit
0008	0000 0000 0000 1000	1000	000	0000 0000 0	Miss	Miss	Hit	Hit
00a0	0000 0000 1010 0000	0000	010	0000 0000 1	Miss	Miss	Miss	Miss

0004	0000 0000 0000 0100	0100	000	0000 0000 0	Hit	Hit	Hit	Hit
1104	0001 0001 0000 0100	0100	000	0001 0001 0	Miss	Miss	Miss	Miss
000c	0000 0000 0000 1100	1100	000	0000 0000 0	Miss	Hit	Hit	Hit
0084	0000 0000 1000 0100	0100	000	0000 0000 1	Miss	Miss	Miss	Miss
000c	0000 0000 0000 1100	1100	000	0000 0000 0	Miss	Hit	Hit	Hit
3390	0011 0011 1001 0000	0000	001	0011 0011 1	Miss	Miss	Miss	Miss
00b0	0000 0000 1011 0000	0000	011	0000 0000 0	Miss	Miss	Miss	Miss
1100	0001 0001	0000	000	0001 0001 0	miss	miss	hit	hit

	0000 0000							

0028	0000 0000 0010 1000	1000	010	0000 0000 0	hit	Hit	Hit	Hit
0070	0000 0000 0111 0000	0000	111	0000 0000 0	Miss	Miss	Miss	Miss
00d0	0000 0000 1101 0000	0000	101	0000 0000 1	Hit	Miss	Miss	Miss
0008	0000 0000 0000 1000	1000	000	0000 0000 0	Miss	Hit	Hit	Hit
3394	0011 0011 1001 0100	0100	001	0011 0011 1	Hit	Hit	Hit	Hit

2.

Instruction miss cycles = I x 0.02 x 100 = 2 x I
Data miss cycles = I x 0.36 x 0.04 x 100 = 1.44 x I
Total memory stall cycles = 2 x I + 1.44 x I = 3.44 x I
CPI*stall* = 2 + 3.44 = 5.44
CPU time with stalls /CPU time with perfect cache
= I x CPIstall x Clock cycle /I x CPIperfect x Clock cycle
= 5.44 /2
= 2.72

3. (a)
Total words = 64/4 = 16
Number of words left = 16-1 = 15
Tmiss = 2.5 + 50 + (15)(5) + 2.5 = 130ns

(b)
Ts = (0.95)(2.5) + (0.05)(130) = 8.875ns

After modification,
Total words = 128/4 = 32
Number of words left = 32-1 = 31
Tmiss = 2.5 + 50 + (31)(5) + 2.5 = 210ns
Ts = (0.97)(2.5) + (0.03)(210) = 8.725ns
Therefore, average memory access time is reduced.

4.

(1)
Miss Penalty = cache line size * ((clock cycle to send the address to main memory) + (clock cycles to access a 32 bit))
=1 * (1+4)
=5 Clock Cycles

(2)
Cache Line Size = 4 Words
This means when 1 block is accessed, other 3 blocks will be accessed as well

Time Penalty = cache line size * ((clock cycle to send the address to main memory) + (clock cycles to access a 32 bit))
= 4 x(1 + 4)
= 20 Clock Cycles

(3)
Cache Line Size = 4
Number of blocks left = 4 - 1 = 3
Time to access word after initial transfer = 1 Clock Cycle

Initial Transfer = (clock cycle to send the address to main memory) + (clock cycles to access a 32 bit)
= 1 + 4
= 5

Rest Transfer = Number of blocks left x (clock cycles to access a 32 bit)
= 3 x 1
= 3
Miss Penalty = 5 + 3 = 8 Clock Cycles