Project Testing Example for MIPS

Assuming that the first instruction is in address 0, all register values are initially 0, HEY is at address 0000 0000 1111 1111 and at address 0 in the memory the following is present: 1111 1111 1111 1111 0000 0000 0000 0000.

The code segment is as follows:

1-Addi $t0, $0,5	0010 0000 0000 1000 0000 0000 0000 0101
2-Lw $t1, 0($s0)	1000 1110 0000 1001 0000 0000 0000 0000
3-Add $t4, $t2,$t3	0000 0001 0100 1011 0110 0000 0010 0000
4-Or $t7, $t5,$t6	0000 0001 1010 1110 0111 1000 0010 0101
5-sw $s2, 0($s1)	1010 1110 0011 0010 0000 0000 0000 0000
6-beq $t8,$0, HEY	0001 0010 0000 0000 0000 0000 1111 1111

After first clock-cycle: 1

Addi $t0, $0,5 in Fetch stage:

Next PC: 0000 0000 0000 0000 0000 0000 0000 0100
Instruction: 0010 0000 0000 1000 0000 0000 0000 0101

After second clock-cycle: 2

Lw $t1, 0($s0) in Fetch stage:

Next PC: 0000 0000 0000 0000 0000 0000 0000 1000
Instruction: 1000 1110 0000 1001 0000 0000 0000 0000

Addi $t0, $0,5 in Decode stage:

read data 1: 0000 0000 0000 0000 0000 0000 0000 0000
read data 2: 0000 0000 0000 0000 0000 0000 0000 0000
sign-extend: 0000 0000 0000 0000 0000 0000 0000 0101
Next PC: 0000 0000 0000 0000 0000 0000 0000 0100
rt: 01001
rd: don't care
WB controls: MemToReg: 1, RegWrite: 1
MEM controls: MemRead: 0, MemWrite: 0, Branch: 0
EX controls: RegDest: 0, ALUOp: 010, ALUSrc: 1

After third clock-cycle: 3

Add $t4, $t2,$t3 in Fetch stage:

Next PC: 0000 0000 0000 0000 0000 0000 0000 1100
Instruction: 0000 0001 0100 1011 0110 0000 0010 0000

Lw $t1, 0($s0) in Decode stage:

read data 1: 0000 0000 0000 0000 0000 0000 0000 0000

read data 2: 0000 0000 0000 0000 0000 0000 0000 0000
sign-extend: 0000 0000 0000 0000 0000 0000 0000 0000
Next PC: 0000 0000 0000 0000 0000 0000 0000 1000
rt: 01001
rd: don't care
WB controls: MemToReg: 0, RegWrite: 1
MEM controls: MemRead: 1, MemWrite: 0, Branch: 0
EX controls: RegDest: 0, ALUOp: 010, ALUSrc: 1

Addi $t0, $0,5 in Execute stage:

zero flag: 0
branch address: 0000 0000 0000 0000 0000 0000 0001 1000
ALU result/address: 0000 0000 0000 0000 0000 0000 0000 0101
register value to write to memory: 0000 0000 0000 0000 0000 0000 0000 0000
rt/rd register: 01000
WB controls: MemToReg: 1, RegWrite: 1
MEM controls: MemRead: 0, MemWrite: 0, Branch: 0

After 4th clock-cycle: 4

Or $t7, $t5,$t6 in Fetch stage:

Next PC: 0000 0000 0000 0000 0000 0000 0001 0000
Instruction: 0000 0001 1010 1110 0111 1000 0010 0101

Add $t4, $t2,$t3 in Decode stage:

read data 1: 0000 0000 0000 0000 0000 0000 0000 0000
read data 2: 0000 0000 0000 0000 0000 0000 0000 0000
sign-extend: 0000 0000 0000 0000 0110 0000 0010 0000
Next PC: 0000 0000 0000 0000 0000 0000 0000 1100
rt: 01011
rd: 01100
WB controls: MemToReg: 1, RegWrite: 1
MEM controls: MemRead: 0, MemWrite: 0, Branch: 0
EX controls: RegDest: 1, ALUOp: 010, ALUSrc: 0

Lw $t1, 0($s0) in Execute stage:

zero flag: 1
branch address: 0000 0000 0000 0000 0000 0000 0000 1000
ALU result/address: 0000 0000 0000 0000 0000 0000 0000 0000
register value to write to memory: 0000 0000 0000 0000 0000 0000 0000 0000
rt/rd register: 01001
WB controls: MemToReg: 0, RegWrite: 1
MEM controls: MemRead: 1, MemWrite: 0, Branch: 0

Addi $t0, $0,5 in Memory stage:

ALU result: 0000 0000 0000 0000 0000 0000 0000 0101

memory word read: don’t care
rt/rd field: 01000
WB controls: MemToReg: 1, RegWrite: 1

After 5th clock-cycle: 5

sw $s2, 0($s1) in Fetch stage:

Next PC: 0000 0000 0000 0000 0000 0000 001 0100
Instruction: 1010 1110 0011 0010 0000 0000 0000 0000

Or $t7, $t5,$t6 in Decode stage:

read data 1: 0000 0000 0000 0000 0000 0000 0000 0000
read data 2: 0000 0000 0000 0000 0000 0000 0000 0000
sign-extend: 0000 0000 0000 0000 0111 1000 0010 0101
Next PC: 0000 0000 0000 0000 0000 0000 0001 0000
rt: 01110
rd: 01111
WB controls: MemToReg: 1, RegWrite: 1
MEM controls: MemRead: 0, MemWrite: 0, Branch: 0
EX controls: RegDest: 1, ALUOp: 001, ALUSrc: 0

Add $t4, $t2,$t3 in Execute stage:

zero flag: 1
branch address: 0000 0000 0000 0000 0110 0000 0010 1100
ALU result/address: 0000 0000 0000 0000 0000 0000 0000 0000
register value to write to memory: 0000 0000 0000 0000 0000 0000 0000 0000
rt/rd register: 01100
WB controls: MemToReg: 1, RegWrite: 1
MEM controls: MemRead: 0, MemWrite: 0, Branch: 0

Lw $t1, 0($s0) in Memory stage:

ALU result: 0000 0000 0000 0000 0000 0000 0000 0000
memory word read: 1111 1111 1111 1111 0000 0000 0000 0000
rt/rd field: 01001
WB controls: MemToReg: 0, RegWrite: 1

Addi $t0, $0,5 in WB stage

After 6th clock-cycle: 6

beq $t8,$0, HEY in Fetch stage:

Next PC: 0000 0000 0000 0000 0000 0000 001 1000
Instruction: 0001 0010 0000 0000 0000 0000 1111 1111

sw $s2, 0($s1) in Decode stage:

read data 1: 0000 0000 0000 0000 0000 0000 0000 0000
read data 2: 0000 0000 0000 0000 0000 0000 0000 0000
sign-extend: 0000 0000 0000 0000 0000 0000 0000 0000
Next PC: 0000 0000 0000 0000 0000 0000 001 0100
rt: 10010
rd: don't care
WB controls: MemToReg: don't care, RegWrite: 0
MEM controls: MemRead: 0, MemWrite: 1, Branch: 0
EX controls: RegDest: 0, ALUOp: 010, ALUSrc: 1

Or $t7, $t5,$t6 in Execute stage:

zero flag: 1
branch address: 0000 0000 0000 0001 1110 0000 1010 0100
ALU result/address: 0000 0000 0000 0000 0000 0000 0000 0000
register value to write to memory: 0000 0000 0000 0000 0000 0000 0000 0000
rt/rd register: 01111
WB controls: MemToReg: 1, RegWrite: 1
MEM controls: MemRead: 0, MemWrite: 0, Branch: 0

Add $t4, $t2,$t3 in Memory stage:

ALU result: 0000 0000 0000 0000 0000 0000 0000 0000
memory word read: don't care
rt/rd field: 01100
WB controls: MemToReg: 1, RegWrite: 1

Lw $t1, 0($s0) in WB stage

After the 7th clock-cycle: 7

beq $t8,$0, HEY in Decode stage:

read data 1: 0000 0000 0000 0000 0000 0000 0000 0000
read data 2: 0000 0000 0000 0000 0000 0000 0000 0000
sign-extend: 0000 0000 0000 0000 0000 0000 1111 1111
Next PC: 0000 0000 0000 0000 0000 0000 0001 1000
rt: 00000
rd: don't care
WB controls: MemToReg: don't care, RegWrite: 0
MEM controls: MemRead: 0, MemWrite: 0, Branch: 1
EX controls: RegDest: don't care, ALUOp: 110, ALUSrc: 1

sw $s2, 0($s1) in Execute stage:

zero flag: 1
branch address: 0000 0000 0000 0000 0000 0000 001 0100
ALU result/address: 0000 0000 0000 0000 0000 0000 0000 0000
register value to write to memory: 0000 0000 0000 0000 0000 0000 0000 0000

rt/rd register: 10010
WB controls: MemToReg: 0, RegWrite: 0
MEM controls: MemRead: 0, MemWrite: 1, Branch: 0

Or $t7, $t5,$t6 in Memory stage:

ALU result: 0000 0000 0000 0000 0000 0000 0000 0000
memory word read: don't care
rt/rd field: 01111
WB controls: MemToReg: 1, RegWrite: 1

Add $t4, $t2,$t3 in WB stage

After the 8th clock-cycle: 8

beq $t8,$0, HEY in Execute stage:

zero flag: 0
branch address: 0000 0000 0000 0000 0000 0100 0001 0100
ALU result/address: 0000 0000 0000 0000 0000 0000 1111 1111
register value to write to memory: 0000 0000 0000 0000 0000 0000 0000 0000
rt/rd register: 00000
WB controls: MemToReg: don't care, RegWrite: 0
MEM controls: MemRead: 0, MemWrite: 0, Branch: 1

sw $s2, 0($s1) in Memory stage:

ALU result: 0000 0000 0000 0000 0000 0000 0000 0000
memory word read: don't care
rt/rd field: 10010
WB controls: MemToReg: 0, RegWrite: 0

Or $t7, $t5,$t6 in WB stage

After the 9th clock-cycle: 9

beq $t8,$0, HEY in Memory stage:

ALU result: 0000 0000 0000 0000 0000 0000 1111 1111
memory word read: don't care
rt/rd field: 00000
WB controls: MemToReg: don't care, RegWrite: 0

sw $s2, 0($s1) in WB stage

After 10th clock-cycle: 10

beq $t8,$0, HEY in WB stage