

Our code has 4 main entities: Clk_generator, sixty_counter, seven_seg_dec & stopwatch.

Clk_generator: Here we take as input a 50MHz clock and turn into 1 Hz. We first set a new counter variable to 0 and once it reaches 25 million (number of the rising edges that correspond to a 50MHz clock), we set our new clock.

sixty_counter: This entity calculates the number that should be displayed on the screen (from 0 to 59). Firstly, it checks if the reset button is pressed and if so it resets the number back to 0. If the reset button and the pause button are not pressed and the clock is on a rising edge then our number gets incremented by 1. If it hits 59, it automatically is reset to 0.

seven_seg_dec: Given the number that should be displayed on the screen (from 0 to 59) , we output the equivalent representation on the 7 segment display. In the code, we map each number that needs to be represented by lighting up the corresponding LED on the 7 segment display.

StopWatch: This entity outputs 2 vectors each of size 7 and takes as input the clock, reset and pause. It connects all other 3 entities by giving them their corresponding inputs and passing the right output to the other entities. This entity is mandatory for the functionality of the code. For the output of the sixty_counter entity, we don't take it directly, we use the modulus and division operations to take the number and divide it into two numbers to be able to map them on two separate 7 segment displays (using 2 instances of the entity seven_seg_dec).

Below is a table mapping all the pin assignments and a screenshot of the assignments on Quartus.

Node Name	Direction	Location
b[6]	Output	PIN_C17
b[5]	Output	PIN_D17
b[4]	Output	PIN_E16
b[3]	Output	PIN_C16
b[2]	Output	PIN_C15
b[1]	Output	PIN_E15
b[0]	Output	PIN_C14
b1[6]	Output	PIN_B17
b1[5]	Output	PIN_A18
b1[4]	Output	PIN_A17
b1[3]	Output	PIN_B16
b1[2]	Output	PIN_E18
b1[1]	Output	PIN_D18
b1[0]	Output	PIN_C18
Clk	Input	PIN_P11
Pause	Input	PIN_A7
reset	Input	PIN_B8

Groups

Named: *

Node Name	Direction
b[6..0]	Output Group
b[5..0]	Output Group
b[5]	Output
b[4]	Output
b[3]	Output

Tasks

Early Pin Planning

- Early Pin Planning...
- Run I/O Assignment Analysis
- Export Pin Assignments...
- Pin Finder...

Top View - Wire Bond
MAX 10 - 10M50DAF484C6GES

Pin Legend

Symbol	Pin Type
○	User I/O
●	User assigned L...
●	Fitter assigned L...
○	Unbonded pad
○	Reserved pin
○	Other configura...
ⓔ	DEV_OE
ⓔ	DEV_CLR
ⓔ	DIFF_n
ⓔ	DIFF_p
ⓔ	DQ
ⓔ	DQS
ⓔ	DQS8
ⓔ	CLK_n
ⓔ	CLK_p

Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
b[6]	Output	PIN_C17	7	B7_NO	PIN_C17	2.5 V		12mA (default)	2 (default)		
b[5]	Output	PIN_D17	7	B7_NO	PIN_D17	2.5 V		12mA (default)	2 (default)		
b[4]	Output	PIN_E16	7	B7_NO	PIN_E16	2.5 V		12mA (default)	2 (default)		
b[3]	Output	PIN_C16	7	B7_NO	PIN_C16	2.5 V		12mA (default)	2 (default)		
b[2]	Output	PIN_C15	7	B7_NO	PIN_C15	2.5 V		12mA (default)	2 (default)		
b[1]	Output	PIN_E15	7	B7_NO	PIN_E15	2.5 V		12mA (default)	2 (default)		
b[0]	Output	PIN_C14	7	B7_NO	PIN_C14	2.5 V		12mA (default)	2 (default)		
b[5]	Output	PIN_B17	7	B7_NO	PIN_B17	2.5 V		12mA (default)	2 (default)		
b[4]	Output	PIN_A18	7	B7_NO	PIN_A18	2.5 V		12mA (default)	2 (default)		
b[3]	Output	PIN_A17	7	B7_NO	PIN_A17	2.5 V		12mA (default)	2 (default)		
b[2]	Output	PIN_B16	7	B7_NO	PIN_B16	2.5 V		12mA (default)	2 (default)		
b[1]	Output	PIN_E18	6	B6_NO	PIN_E18	2.5 V		12mA (default)	2 (default)		
b[0]	Output	PIN_D18	6	B6_NO	PIN_D18	2.5 V		12mA (default)	2 (default)		
b[1]	Output	PIN_C18	7	B7_NO	PIN_C18	2.5 V		12mA (default)	2 (default)		
clk	Input	PIN_P11	3	B3_NO	PIN_P11	2.5 V		12mA (default)			
pause	Input	PIN_A7	7	B7_NO	PIN_A7	2.5 V		12mA (default)			
reset	Input	PIN_B8	7	B7_NO	PIN_B8	2.5 V		12mA (default)			

0% 00:00:00