2020-08-27 CH 1

Thursday, August 27, 2020 8:32 AM

Student Reflections

- Needs clarification -> The most confusing thing about the chapter was how there are several logic gates that can do the same thing, depending on the inputs. (Jose)
- Talk about MUX and DEMUX chips
- Talk more about N-way / Composite Gates

8WayMux16

Sel[3]

Sel[2]	Sel[1]	Sel[0]	Output
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

- Canonical Representations

Wrap-Up

- Be sure to place code in projects/01 for easier local testing
- How to use github (will be covered more in tomorrow's lab)

NAND -> NOT

NAND Truth Table

A	B	Out	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

NOT Truth Table

In	Out
0	1
1	0