

SI	PECIFICATIONS	
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SAMPLE VERSION	:	
SPECIFICATIONS EDITION	:	
DRAWING NO. (Ver.)	:	
PACKAGING NO. (Ver.)	:	
Cus	stomer Approved	1
		Date: PDWERTIP 2018.09.25 JS RD APPROVED
Approved	Checked	Designer

Approved	Checked	Designer
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- Preliminary specification for design input
- ☐ Specification for sample approval



History of Version

Date	Ver.	Edi.	Description	Page	Design by
01/11/2018	01	001	New Drawing	-	徐明菲
04/13/2018	01	002	New Sample	-	徐明菲
09/17/2018	02	003	Second Drawing (Modify the width of Shading tape on Backlight)	-	徐明菲

Total: 33 Pages



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Note: For detailed information please refer to IC data sheet: NOVATEK - NT7534H-BDT



1. SPECIFICATIONS

1.1 Features

Item	Standard Value
Display Type	128 * 64 Dots
LCD Type	FSTN White, Positive, Transflective, Extended Temp.
Driver Condition	LCD Module: 1/65 Duty, 1/9 Bias
Viewing Direction	6 O'clock
Weight	-
Interface	6800 Serial data input/Parallel data input
Controller / Driver IC	NT7534
50110	THIS PRODUCT CONFORMS THE ROHS OF PTC
ROHS	A

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	67.2 (L) * 48.2 (W) * 5.3 (H)	mm
Viewing Area	61.0 (L) * 31.4 (W)	mm
Active Area	57.58 (L) * 28.78 (W)	mm
Dot Size	0.43 (L) * 0.43 (W)	mm
Dot Pitch	0.45 (L) * 0.45 (W)	mm

Note: For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
Power Supply Voltage	V_{DD}	1	-0.3	+4.0	V
LCD Driver Supply Voltage	V ₀ ,V _{OUT}	1	-0.3	+15.0	V
Input Voltage	V _{IN}	-	-0.3	V _{DD} +0.3	V
Operating Temperature	Тор	-	-20	+70	$^{\circ}\!\mathbb{C}$
Storage Temperature	T _{ST}	-	-30	+80	$^{\circ}\!\mathbb{C}$
Storage Humidity	H _D	Ta < 60 °C	20	90	%RH



1.4 DC Electrical Characteristics

VDD = 3.3V, VSS = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Logic Supply Voltage	V _{DD}	-	3.0	3.3	3.6	V
"H" Input Voltage	VIH	-	0.8V _{DD}	1	V _{DD}	V
"L" Input Voltage	VIL	-	Vss	1	0.2V _{DD}	V
"H" Output Voltage	Vон	-	0.8V _{DD}	1	V _{DD}	V
"L" Output Voltage	Vol	-	V _{DD}	1	0.2V _{DD}	V
Supply Current	I _{DD}	V _{DD} = 3.3V; VOP= 8.2V;	1	1.0	1.5	mA
		-20°C	8.8	9.0	9.2	
LCM Driver Voltage	Vop*1	+25°C	8.0	8.2	8.4	V
		+70°C	7.3	7.5	7.7	

Note: *1. The VOP test point is V0~VSS



1.5 Optical Characteristics

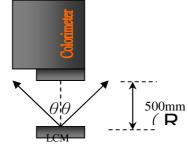
LCD Panel: 1/65 Duty, 1/9 Bias, VLCD = 8.2V, Ta = 25°C

Item		Symbol	Conditions	Min.	Тур.	Max.	Unit	Reference
Posponso Timo	Rise	tr		-	107	161	me	Note 2
Response Time	Fall	tf	-	-	300	450	ms	Note 2
	Тор	θ+		-	40	-		
	Bottom	θ-	C>2.0	-	40	-		Notes 1
Viewing angle range	Left	θL	C <u>></u> 2.0	-	45	-	_	Notes 1
	Right	θR		-	45	-		
Contrast Ratio		CR	θ = 0°	-	9.5	-	-	Note 3
Average Brightness (LCD & B/L) *2		IV		(170)	(260)	-	cd/m ²	
CIE Color Coordinate		Χ	Vf=5V	(0.25)	(0.30)	(0.35)	-	Note 4
(LCD & B/L) *2		Υ		(0.26)	(0.31)	(0.36)	-	
Uniformity *1		∆B		70	-	-	%	

Note 4:

- 1 : △B=B(min) / B(max)*100%
- 2 : Measurement Condition for Optical Characteristics:
 - a: Environment: 25°C±5°C / 60±20%R.H, no wind, dark room below 10 Lux at typical lamp current and typical operating frequency.
 - b : Measurement Distance: $500 \pm 50 \text{ mm}$, $(\theta = 0^{\circ})$
 - c: Equipment: TOPCON BM-7 fast, (field 0.2°), after 10 minutes operation.
 - d: The uncertainty of the C.I.E coordinate measurement ±0.01, Average Brightness ± 4%





Colorimeter=BM-7 fast

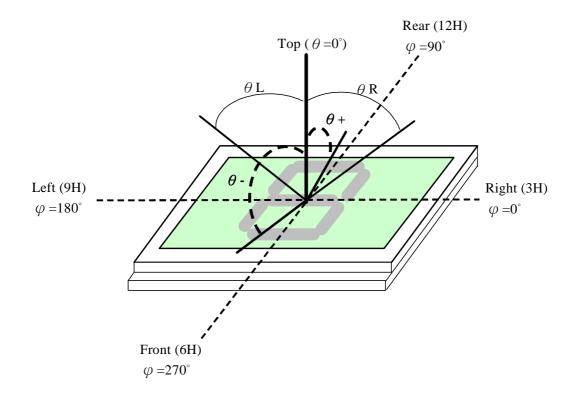
3: This value will be changed while mass production.





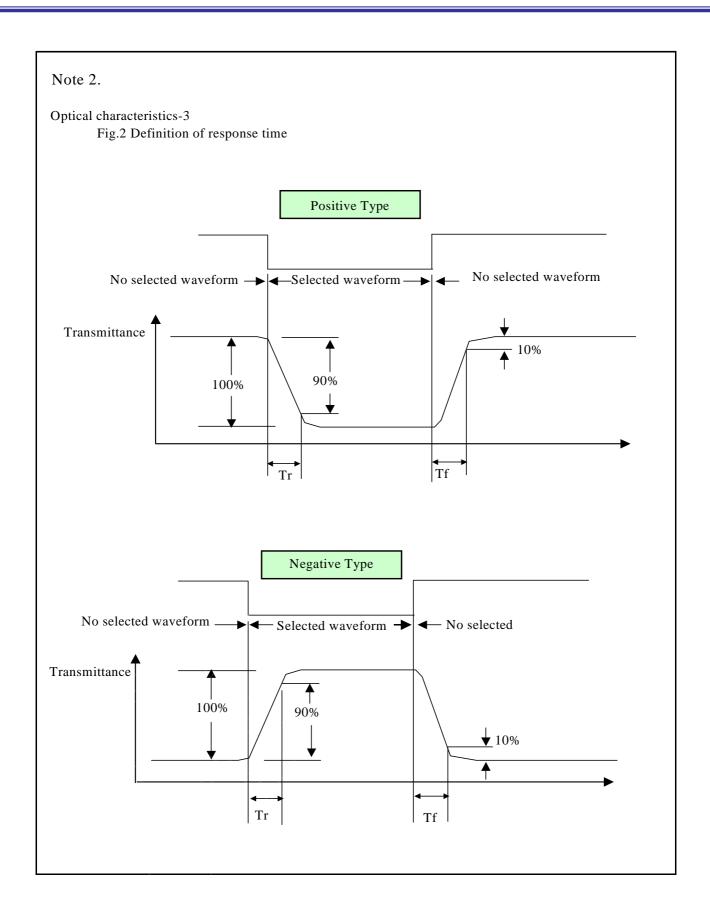
Optical characteristics-2

Viewing angle



Viewing angle







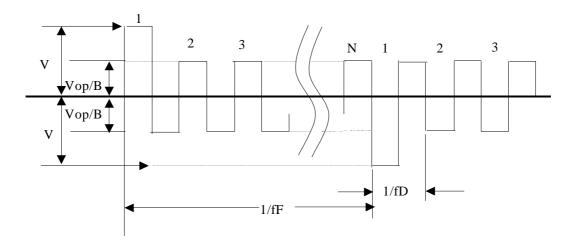
Electrical characteristics-2

※2 Drive waveform

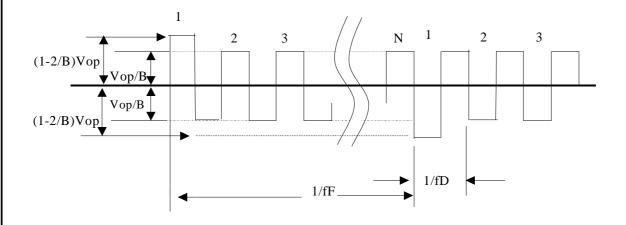
Vop: Drive voltage fF: Frame frequency 1/B: Bias fD: Drive frequency

N: Duty

(1) Selected waveform



(2) Non-Selected wave form

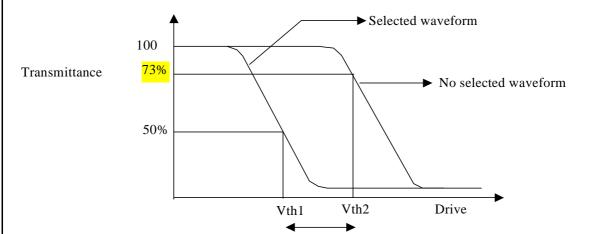


Note:

Frame frequency is defined as follows: Common side supply voltage peak - to - peak /2 = 1 period



Note 3.: Definition of Vth



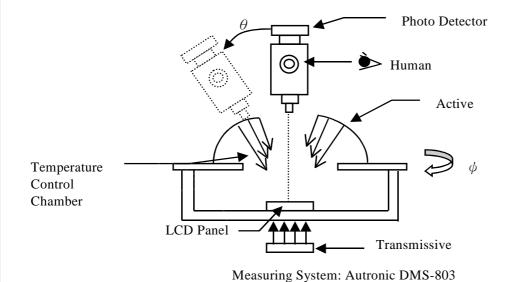
Active voltage range

_	Vth1	Vth2
View direction	10°	40°
Drive waveform	(Selected waveform)	(No selected waveform)
Transmittance	50%	73%

※1 Contrast ratio

= (Brightness in OFF state) / (Brightness in ON state)

Outline of Electro-Optical Characteristics Measuring System





1.6 Backlight Characteristics

Maximum Ratings

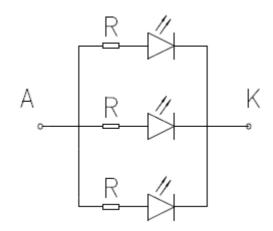
Item	Symbol	Conditions	Min.	Max.	Unit	Remark
Reverse Voltage	IF	Ta=25°C	-	30	mA	Each LED
Forward Current	VR	Ta=25°C	-	5	V	Each LED
Power dissipation	PD	Ta=25°C	-	225	mW	-

Electrical / Optical Characteristics

Ta =25°℃

Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
Forward Voltage	IF		15	30	45	mA
Average Brightness (Without LCD)	IV	VF=5V	1050	1260	-	cd/m ²
CIE Color Coordinate	X		0.26	0.28	0.31	-
(Without LCD)	Υ		0.26	0.28	0.31	-
Color			White			

Circuit Diagram:





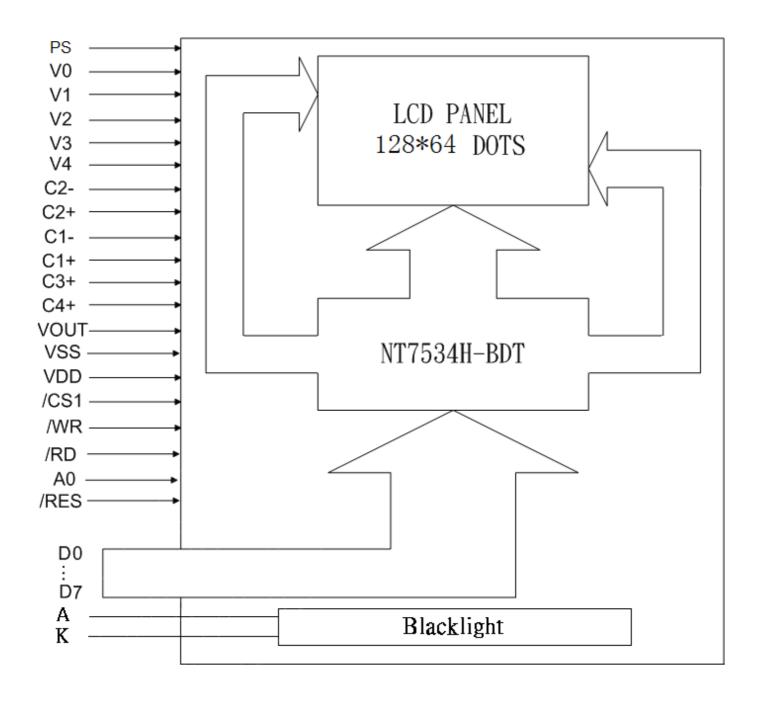
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram





2.2 Interface Pin Description

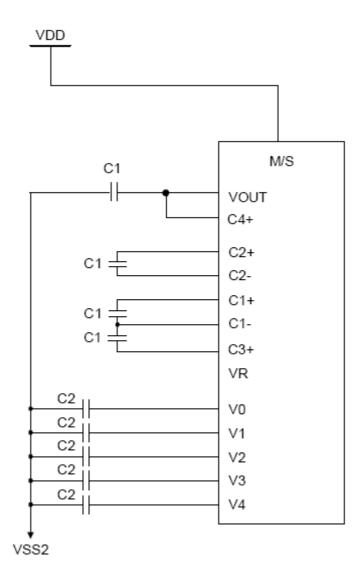
2.2 Inte	rtace Pin	Description
Pin No.	Symbol	Function
1	/CS1	Chip Select signal. Active "L".
2	/RES	When /RES is set to "L", the settings are initialized.
3	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicate that DB0 to DB7 are display data. A0 = "L": Indicates that DB0 to DB7 are control data.
4	/WR(R/W)	When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W = "H": Read When R/W = "L": Write
5	/RD(E)	When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
6	D0	
7	D1	
8	D2	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
9	D3	When the serial interface is selected (P/S="L"), then D7 serves as the serial
10	D4	data input terminal (SI) and D6 serves as the serial clock input terminal (SCL).
11	D5	At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
12	D6(SCL)	which the only scient is inactive, bo to by are set to high impedance.
13	D7(SI)	
14	VDD	Power supply. (+3.3V)
15	VSS	System ground. (0V)
16	VOUT	DC/DC Voltage converter output.
17	C4+	Capacitor 4+ pad for internal DC/DC voltage converter.
18	C3+	Capacitor 3+ pad for internal DC/DC voltage converter.
19	C1-	Capacitor 1- pad for internal DC/DC voltage converter.
20	C1+	Capacitor 1+ pad for internal DC/DC voltage converter.
21	C2+	Capacitor 2+ pad for internal DC/DC voltage converter.
·		



Symbol	Function										
C2-	Capacitor	Capacitor 2- pad for internal DC/DC voltage converter.									
V1	LCD drive	_CD driver supply voltages. The voltage determined by LCD cell is									
V2	impedanc	mpedance-converted by a resistive driver or an operation amplifier for									
V3		application. Voltages should be according to the following relationship:									
V4	When the	When the on-chip operating power circuit is on, the following voltages are									
		oltage selection is performed by the LCD bias set command.									
	LCD bias	V1	V2		V3	V4					
	1/4 bias	3/4*V0	2/4*V0)	2/4*V0	1/4*V0					
\ /O	1/5 bias	4/5*V0	3/5*V0)	2/5*V0	1/5*V0					
VU	1/6 bias	5/6*V0	4/6*V0)	2/6*V0	1/6*V0					
	1/7 bias	6/7*V0	5/7*V0		2/7*V0	1/7*V0					
	1/8 bias	7/8*V0	6/8*V0)	2/8*V0	1/8*V0					
	1/9 bias	8/9*V0	7/9*V0)	2/9*V0	1/9*V0					
	P/S = "H": P/S = "L":	Parallel data in _l Serial data inpu	put t		·						
	P/S	Data/Comma	and	D	ata	Read/Write	Serial Clock				
PS	"H"	A0		D()-D7	/RD,/WR	-				
. 0	"L"	A0		SI	(D7)	Write only	SCL(D6)				
	A0 SI (D7) When P/S /WR (R/W)	Write only SCL = "L", D0 to D5 are fixed to eit	are H		-	-					
	C2- V1 V2 V3	C2- Capacitor V1 LCD drive impedance application V3 V4 When the supplied to Voltage set LCD bias 1/4 bias 1/5 bias 1/6 bias 1/7 bias 1/8 bias 1/9 bias This is the P/S = "H": P/S = "L": \$ The followide P/S "H" "L" A0 D0 to D A0 SI (D7) When P/S /WR (R/W)	C2- Capacitor 2- pad for interval LCD driver supply voltage impedance-converted by application. Voltages shown V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 When the on-chip operation supplied to V1 to V4 by Voltage selection is perful LCD bias V1 1/4 bias 3/4*V0 1/5 bias 4/5*V0 1/6 bias 5/6*V0 1/7 bias 6/7*V0 1/8 bias 7/8*V0 1/9 bias 8/9*V0 This is the parallel data in P/S = "H": Parallel data in P/S = "L": Serial data in put The following applies dependent P/S Data/Commation H" A0 "H" A0 "H" A0 A0 D0 to D7 /RD, /WR - A0 SI (D7) Write only SCL When P/S = "L", D0 to D5	C2- Capacitor 2- pad for internal E V1 LCD driver supply voltages. T impedance-converted by a re application. Voltages should be V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VS When the on-chip operating possible to V1 to V4 by the on Voltage selection is performed LCD bias V1 V2 1/4 bias 3/4*V0 2/4*V0 1/5 bias 4/5*V0 3/5*V0 1/6 bias 5/6*V0 4/6*V0 1/7 bias 6/7*V0 5/7*V0 1/8 bias 7/8*V0 6/8*V0 1/9 bias 8/9*V0 7/9*V0 This is the parallel data input P/S = "H": Parallel data input P/S = "H": Serial data input The following applies depending P/S Data/Command "H" A0 "L" A0 A0 D0 to D7 /RD, /WR - A0 SI (D7) Write only SCL (D6) When P/S = "L", D0 to D5 are H /WR (R/W) are fixed to either "H	C2- Capacitor 2- pad for internal DC/DC V1 LCD driver supply voltages. The voltage impedance-converted by a resistive of application. Voltages should be accorved by a polication. Voltages should be accorved by the voltages application. Voltages should be accorved by the voltage selection is performed by the voltage selection is performed by the LCD bias v1 v2 1/4 bias 3/4*V0 2/4*V0 1/5 bias 4/5*V0 3/5*V0 1/6 bias 5/6*V0 4/6*V0 1/7 bias 6/7*V0 5/7*V0 1/8 bias 7/8*V0 6/8*V0 1/9 bias 8/9*V0 7/9*V0 This is the parallel data input P/S = "H": Parallel data input P/S = "L": Serial data input The following applies depending on the P/S Data/Command Drate P/S Data/	C2- Capacitor 2- pad for internal DC/DC voltage color V1 LCD driver supply voltages. The voltage determined impedance-converted by a resistive driver or a application. Voltages should be according to the V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS When the on-chip operating power circuit is on supplied to V1 to V4 by the on-chip power circuit is on supplied to V1 to V2 V3	C2- Capacitor 2- pad for internal DC/DC voltage converter. V1 LCD driver supply voltages. The voltage determined by LCD impedance-converted by a resistive driver or an operation an application. Voltages should be according to the following relivous V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS When the on-chip operating power circuit is on, the following supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD bias set command LCD bias V1 V2 V3 V4 1/4 bias 3/4*V0 2/4*V0 2/4*V0 1/4*V0 1/5 bias 4/5*V0 3/5*V0 2/5*V0 1/5*V0 1/6 bias 5/6*V0 4/6*V0 2/6*V0 1/6*V0 1/7 bias 6/7*V0 5/7*V0 2/7*V0 1/7*V0 1/8 bias 7/8*V0 6/8*V0 2/8*V0 1/8*V0 1/9 bias 8/9*V0 7/9*V0 2/9*V0 1/9*V0 This is the parallel data input/serial data input switch terminal P/S = "H": Parallel data input P/S = "L": Serial data input The following applies depending on the P/S status: P/S Data/Command Data Read/Write "H" A0 D0-D7 /RD,/WR "L" A0 SI(D7) Write only A0 D0 to D7 /RD, /WR - A0 SI (D7) Write only SCL (D6) When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Operation of the P/S effective of the properties of the propert				



2.2.1 Application Notes



*Value of External Capacitance								
Item	Value							
C1	1.0 - 4.7	uF						
C2	0.1 - 2.2							



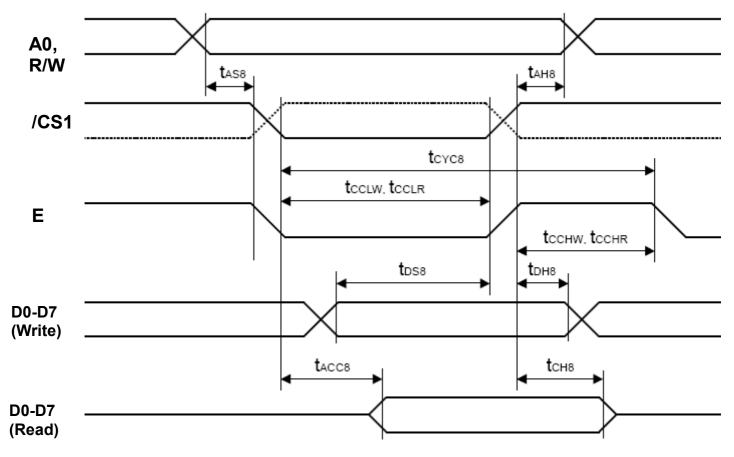
2.2.2 Refer Initial Code

```
void Initial Main(void)
                                     // For NT75451
{
    WriteCOM Main(0xe2);//Software reset
    WriteCOM Main(0xae);//Set Display off
    WriteCOM Main(0x40);//Set start line
    WriteCOM Main(0xa2);//Set 1/9 Bias
    WriteCOM Main(0xa0);//Set ADC
    WriteCOM Main(0xc8);//Set COM direction
    WriteCOM_Main(0xa6);//Set Normal
    WriteCOM Main(0xa4);//Set Normal
    WriteCOM_Main(0x2f);//Set power VC,VR,VF
    WriteCOM Main(0x25);//Set Ra/Rb
    WriteCOM Main(0x81);//Set V0
    WriteCOM Main(16);
    WriteCOM Main(0xf8);//Set BOOSTER RATIO SET
    WriteCOM Main(0x00);//4X
    WriteCOM Main(0xaf);//Set Display ON
}
```

ELSTORE

2.3 Timing Characteristics

For 6800 Series MPU



 $V_{DD} = 3.3 \text{ V}$. Ta = -40 to +85 °C

				V D	D - 3.3 V	$\frac{10}{10} = -40 \text{ to } +85 \text{ °C}$
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Address hold time	t AH8	0	-	-		A0,R/W
Address setup time	t _{AS8}	0	-	-		Αυ,π/νν
System cycle time	tcyc8	240	-	-		-
Control L pulse width (/WR)	tcclw	90	-	-		E
Control L pulse width (/RD)	tcclr	120	-	-		E
Control L pulse width (/WR)	tсснw	100	-	-	ns	E
Control L pulse width (/RD)	tcchr	60	-	-		Е
Data setup time	t _{DS8}	40	-	-		D0D7
Data hold time	t _{DH8}	10	-	-		D0~D7
/RD access time	t _{ACC8}	-	-	140		D0~D7 , CL = 100pf
Output disable time	t _{CH8}	5	-	50		Duadi, CL - 100bi

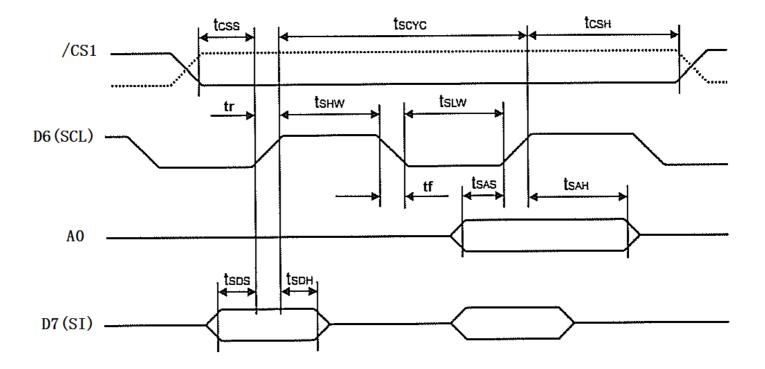


- *1. The input signal rise time and fall time (tr, tf) is specified at 15ns or less.

 (tr + tf) < (tcyc8 tcclw tcchw) for write, (tr + tf) < (tcyc8 tcclr tcchr) for read.
- *2. All timing is specified using 20% and 80% of VDD as the reference.
- *3. tcclw and tcclr are specified as the overlap interval when /CS1 is low (CS2 is high) and E is low.



For Serial Interface



 $V_{DD} = 3.3V$, Ta = -40 to +85 °C

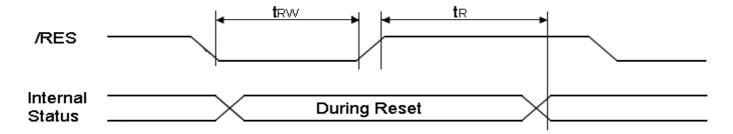
			V UU C	7.0 V , IC	1 10 0	0 00 0
lt a ma	Ciara	Curahal	Condition	Ra	Units	
Item	Signal	Symbol	Condition	Min	Max	Units
Serial clock cycle		tscyc	-	120	-	
Serial clock H pulse width	D6(SCL)	tshw	-	60	-	
Serial clock L pulse width		tslw	-	60	-	
Address setup time	A0	tsas	-	30	-	
Address hold time	AU	tsah	-	20	-	ns
Data setup time	D7(SI)	tsds	-	30	-	
Data hold time	D7(31)	tsdh	-	20	ı	
Chip select setup time	/CS1	tcss	-	20		
Chip select hold time	7031	tсsн	_	40	-	

^{*1.} The input signal rise time and fall time (tr, tf) is specified as 15ns or less.

^{*2.} All timing is specified using 20% and 80% of VDD as the standard.



Reset Timing



 V_{DD} = 3.3V , Ta = -40 to +85 °C

Item	Signal	Symbol	Condition		Rating	Unit	
item	Signal	Symbol	Condition	Min	Тур	Max	Offic
Reset time	-	t R		-	-	1.0	μs
Reset low pulse width	/RES	t _{RW}	_	1.0	-	-	μs



2.4 Display Command

								Code									
Command	Α0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function				
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low				
(2) Display Start Line Set	0	1	0	0	1		Displ	lay Sta	art Ado	Address		Address				40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1		age A			B0h to B8h	Set the display data RAM page in Page Address register				
(4) Column Address Set	0	1	0	0	0	0	1	+	ligher Add	Colum ress	ın	00h to	Set 4 higher bits and 4 lower bits of column address of display data				
(4) Column Address Set	0	1	0	0	0	0	0	L	ower. Add	Colum Iress	in	18h	RAM in register				
(5) Read Status	0	0	1		Sta	itus	•	0	0	0	0	XX	Reads the status information				
(6) Write Display Data	1	1	0				Write	Data			•	XX	Write data in display data RAM				
(7) Read Display Data	1	0	1				Read	Data				XX	Read data from display data RAM				
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0	A0h A1h	Set the display data RAM address SEG output correspondence				
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0	A6h A7h	Normal indication when low, but full indication when high				
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0	A4h A5h	Select normal display (0) or entire display on				
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0	A2h A3h	Sets LCD driving voltage bias ratio				
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write				
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write				
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions				
(15)Common Output Mode Select	0	1	0	1	1	0	0	0	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data				
(16)Power Control Set	0	1	0	0	0	1	0	1	Oper	ation (Status	28h to 2Fh	Select the power circuit operation mode				
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Res	istor F	Ratio	20h to 27h	Select internal resistor ratio Rb/Ra mode				
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h					
Electronic Volume Register Set	0	1	0	*	*		Electr	onic C	ontrol	ontrol ∀alue		хх	Sets the V0 output voltage electronic volume register				
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON				
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	М	ode	ХХ	Sets the flash mode				
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON				
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation				

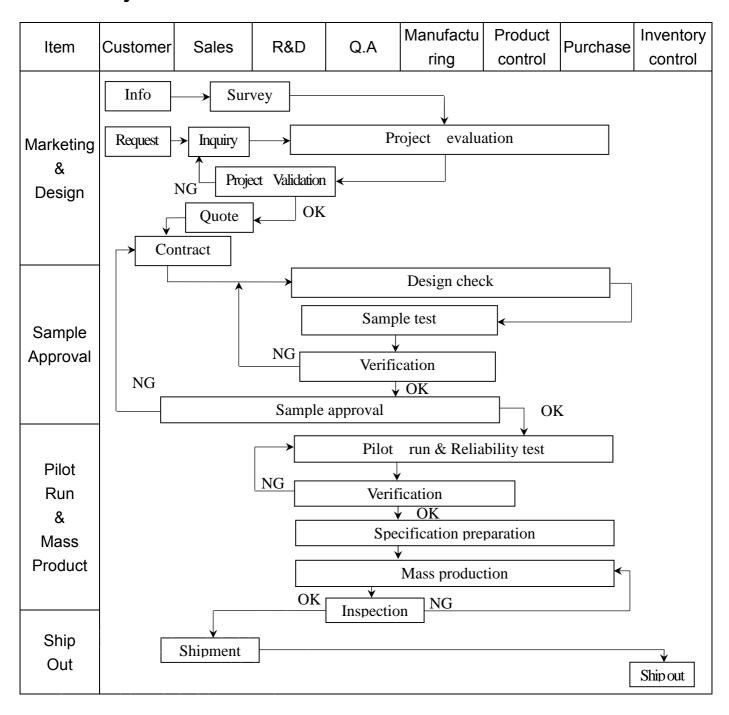


Command		/DD	and.					Code					Fti
Command	Α0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Di	uty Ra	tio		Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bi	as Ra	tio		Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1		Pa	artial S	tart Li	ne		XX	Sets the LCD Number of partial display start line
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*		Num	ber of	Line		xx	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division		xx	Set the Division of DC/DC Clock Frequency		
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

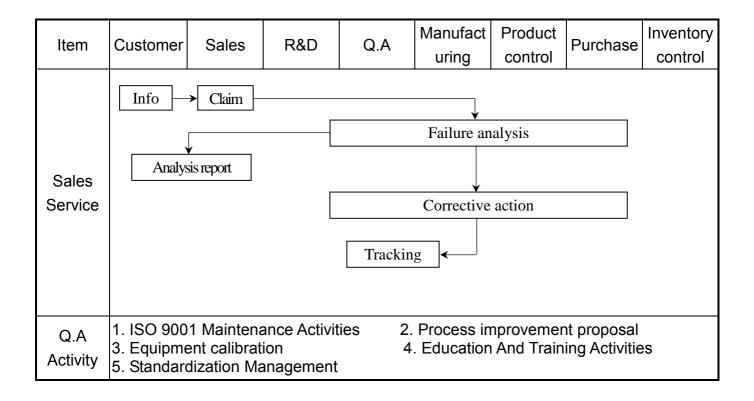


3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart









3.2. Inspection Specification

◆Scope: The document shall be applied to LCD Module for Monotype and Color STN(Ver. B01).

♦Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

◆Equipment : Gauge · MIL-STD · Powertip Tester · Sample

◆Defect Level: Major Defect AQL: 0.4; Minor Defect: AQL: 1.5.

♦OUT Going Defect Level : Sampling .

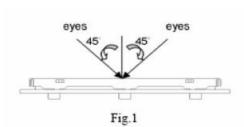
◆Manner of appearance test :

(1). The test be under 20W×2 fluorescent light 'and distance of view must be at 30 cm.

(2). Standard of inspection: (Unit: mm)

(3). The test direction is base on about around 45° of vertical line. (Fig. 1)

(4). Definition of area . (Fig. 2)



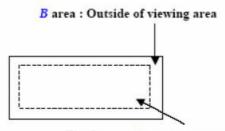


Fig. 2 A area: viewing area

♦ Specification:

NO	Item	Criterion	Level
		1. 1 The part number is inconsistent with work order of Production.	Major
01	Product condition	1. 2 Mixed production types.	Major
		1. 3 Assembled in inverse direction.	Major
02	Quantity	2. 1 The quantity is inconsistent with work order of production.	Major
03	Outline dimension	3. 1 Product dimension and structure must conform to Structure diagram.	Major
		4. 1 Missing line character and icon.	Major
		4, 2 No function or no display.	Major
04	Electrical Testing	4, 3 Output data is error.	Major
		4, 4 LCD viewing angle defect.	Major
		4. 5 Current consumption exceeds product specifications.	Major



NO	Item		C	riteri	on			I	Level	
	Black or white dot \ scratch \ contamination	 5. 1 Round type: 5. 1. 1 display only: • White and black spots on display ≤ 0, 30 mm, no more than 4 white or black spots present. • Densely spaced: NO more than two spots or lines within 3 mm. 								
	Round type	5, 1, 2 Non-o	mension		Acceptance	(O't	v)			
			meter : Φ)		A area	В				
			$\Phi \leq 0.10$		ept no dense					
0.5		0.10 <	$\Phi \leq 0.20$		3	_				
05	─	0.20 <	$\Phi \leq 0.30$	2		Ignore		N	Minor	
	$\Phi = (x+y)/2$	Total quantity			4					
		5. 1. 3 Line type:								
	I in a tame		Dimension		Accep	otano	e (Q'ty)			
	Line type	Length (L)	Width (W)				B area	_		
	✓ / ¥ w		W ≦ (
	· · · · ·	$L \leq 3.0$	0. 05			Ignore				
	L	$L \leq 2.5$	$0.05 < W \le 0.$	075	*					
			W > 0	. 075 As round type						
		Dim	nension		Acceptan	ce (O)'tv)			
		1	eter : Φ)		A area		B area	1		
			$\Phi \leq 0.20$	Accept no dense						
06	Polarizer	0.20 <	$\Phi \leq 0.50$	3			11,	Ainor		
	Bubble	0.50 <	$\Phi \leq 1.00$		2		Ignore			
			$\Phi > 1.00$	0						
		Ψ > 1.00 Total quantity			4					



♦ Speci	ification For Mond	otype and Color	STN:		(Ve	er.B01)
NO	Item		Criterion			Level
110	Item	t: The thicknown to the control of t	of crack Y: 7 ness of crack W: 1 ness of glass a: 1			Level
07	The crack of glass	SP_	Z Z Y (OK)	Y SP [NG]		Minor
			Seal width Z	Y		
		X	Y	Z		
		≦ a	Crack can't enter viewing area	≦1/2 t		
		≦ a	Crack can't exceed the half of SP width.	$1/2 t < Z \leq 2 t$		

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NO	Item		Criterion		Level
		Symbols: X: The length Z: The thickn t: The thickn 7, 1, 2 Corner	ess of crack W ess of glass a :	: The width of crack. : terminal length : LCD side length	
		X	Y	z	
		≦1/5 a	Crack can't enter viewing area	$Z \leq 1/2 t$	
07	The crack of	≤1/5 a	Crack can't exceed the half of SP width.	he $1/2 t < Z \leq 2 t$	
	glass	Rabil of Other States	n over terminal: n electrode pad: X X Y \leq a \leq 1/2 Negle	 	

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♦Specification For Monotype and Color STN:

(Ver. B01)

NO	Item	Criterion	Level
NO	Item	Symbols: X: The length of crack Z: The thickness of crack t: The thickness of glass 7. 2. 2 Non-conductive portion:	Level
07	The crack of glass	$\begin{array}{c cccc} X & Y & Z \\ & \leq 1/3 \text{ a} & \leq W & \leq t \end{array}$	Minor
		 If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications. 7. 2. 3 Glass remain: 	
		V V 7	
		$ \begin{array}{ c c c c } \hline X & Y & Z \\ \hline \leq a & \leq 1/3 \text{ W} & \leq t \\ \hline \end{array} $	



◆Specification For Monotype and Color STN:

(Ver.B01)

NO	Item	Criterion	
08	Backlight elements	8. 1 Backlight can't work normally.	Major
		8. 2 Backlight doesn't light or color is wrong.	Major
		8. 3 Illumination source flickers when lit.	Major
09	General appearance	9. 1 Pin type must match type in specification sheet.	Major
		9. 2 No short circuits in components on PCB or FPC.	Major
		9. 3 Product packaging must the same as specified on packaging specification sheet.	Minor
		9. 4 The folding and peeled off in polarizer are not acceptable.	Minor
		9. 5 The PCB or FPC between B/L assembled distance (PCB or FPC) is ≤1.5 mm.	Minor



4. RELIABILITY TEST

4.1 Reliability Test Condition

(Ver.B01)

NO.	TEST ITEM	TEST CONDITION				
1	High Temperature Storage Test	Keep in +80 ±2°C 240 hrs Surrounding temperature, then storage at normal condition 4hrs.				
2	Low Temperature	Keep in -30 ±2°C 240 hrs				
	Storage Test High Temperature /	Surrounding temperature, then storage at normal condition 4hrs. Keep in +60 °C /90% R.H duration for 240 hrs				
3	High Humidity Storage Test	Surrounding temperature, then storage at normal condition 4hrs. (Excluding the polarizer)				
				→ +80°C → +		
4	Temperature Cycling	(30 mins) (5			(5 mins) →	
	Storage Test	20 Cycle Surrounding temperature, then storage at normal condition 4hrs.				
			tnen sto			n 4nrs.
		Apply 2 KV with 5 times		Contact Discharge: Apply 250 V with 5 times		
		Apply 2 KV with 5 times Discharge for each polarity +/-		discharge for each polarity +/-		
		1. Temperature ambiance : $15^{\circ}\text{C} \sim 35^{\circ}\text{C}$				
5	ESD Test	2. Humidity relative: 30%~60%				
		3. Energy Storage Capacitance(Cs+Cd): 150pF±10%				
		4. Discharge Resistance(Rd): 330Ω±10% 5. Discharge mode of expertion:				
		5. Discharge, mode of operation : Single Discharge (time between successive discharges at least 1 sec)				
		(Tolerance if the output voltage indication: ±5%)				
		1. Sine wave 10~55 Hz frequency (1 min/sweep)				
6	Vibration Test	2. The amplitude of vibration :1.5 mm				
	(Packaged)	3. Each direction (X \ Y \ Z) duration for 2 Hrs				
		Packing Weig	ght (Kg)	Drop Heig	ght (cm)	
		0 ~ 4	5.4	122	2	
7	Drop Test	45.4 ~ 9	0.8	76)	
	(Packaged)	90.8 ~ 4	454	61		
		0ver 4!	54	46)	
		Drop Direction: **1 corner / 3 edges / 6 sides each 1 time				



5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

- 5.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

5.2 HANDLING

- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module, be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands, this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is 320±10°C and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM.
- 5.2.10 Caution!(LCM products with Capacitive Touch Panel)
 Strong EMI-sources such as switch-mode power supplies (SMPS) can lead to touch malfunction (e.g. ghost-touches).
 Therefore, the touch needs to be thoroughly tested inside the target application.

5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is 25° C $\pm 5^{\circ}$ C and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush, shake, or jolt the module.

5.4 TERMS OF WARRANTY

5.4.1 Applicable warrant period

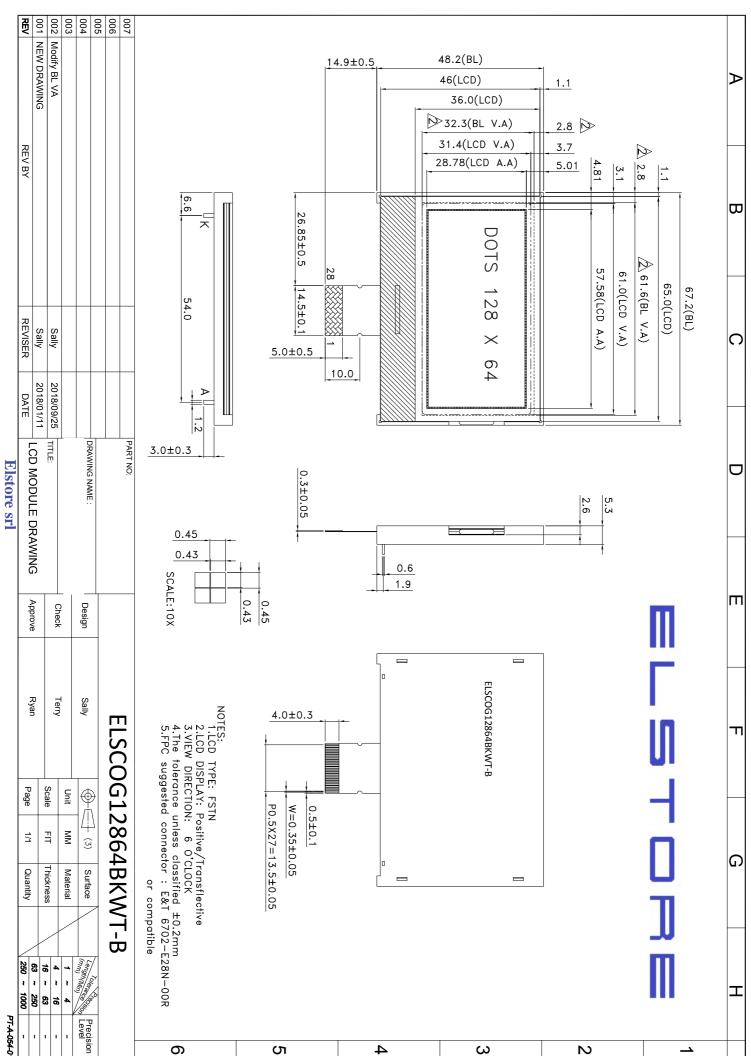
The period is within thirteen months since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in



nuclear power control equipment, aerospace equipment, fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.



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