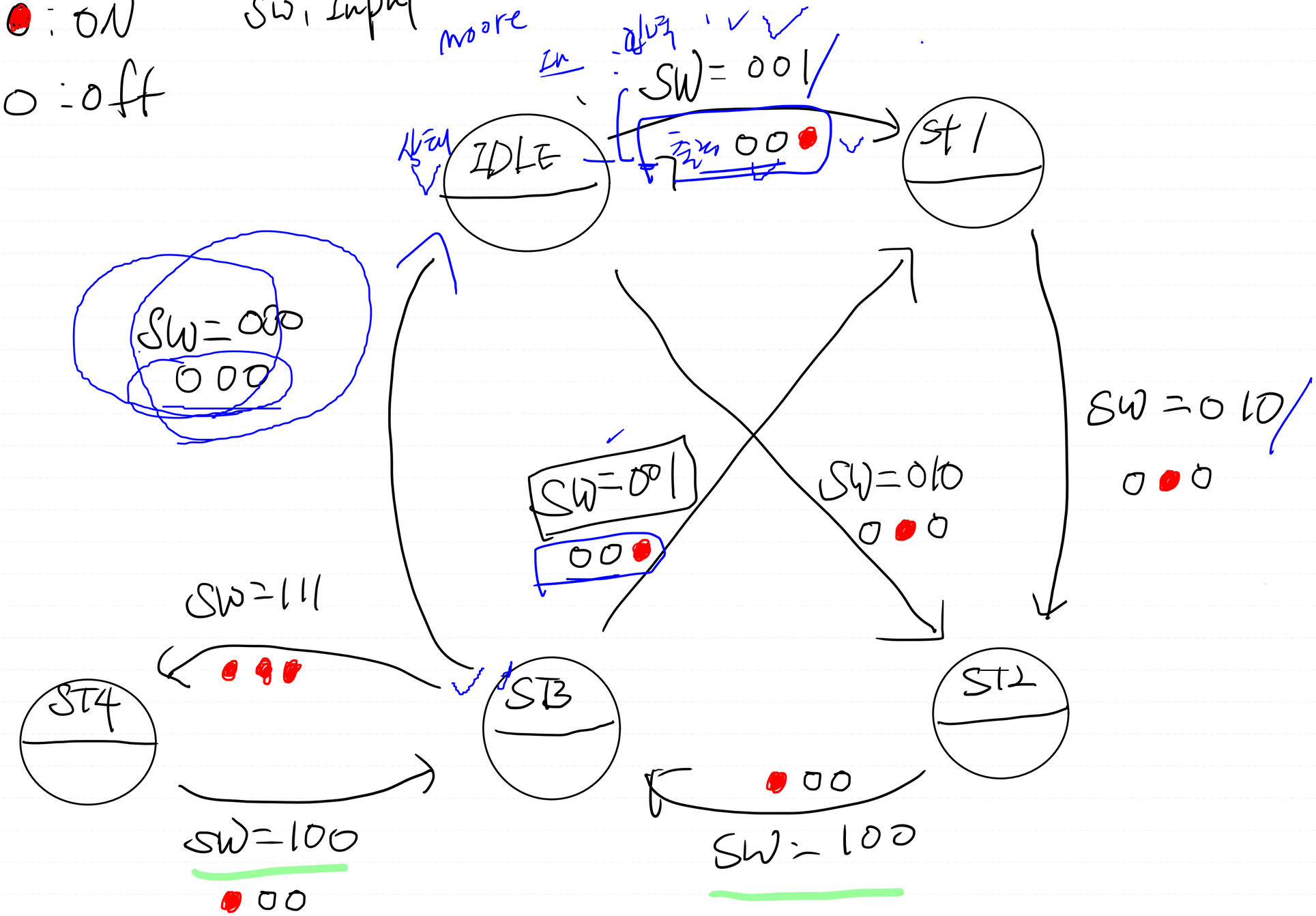
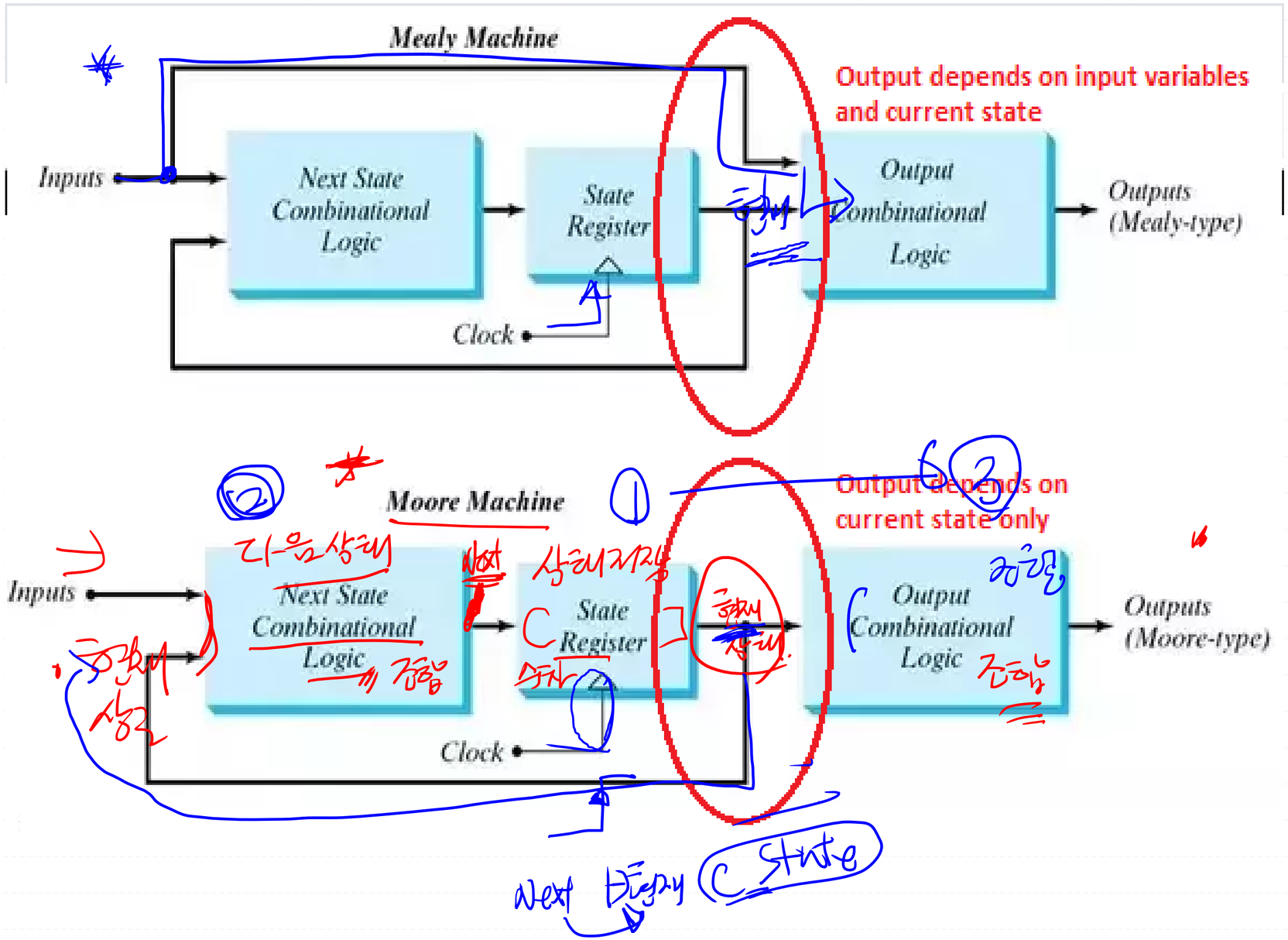
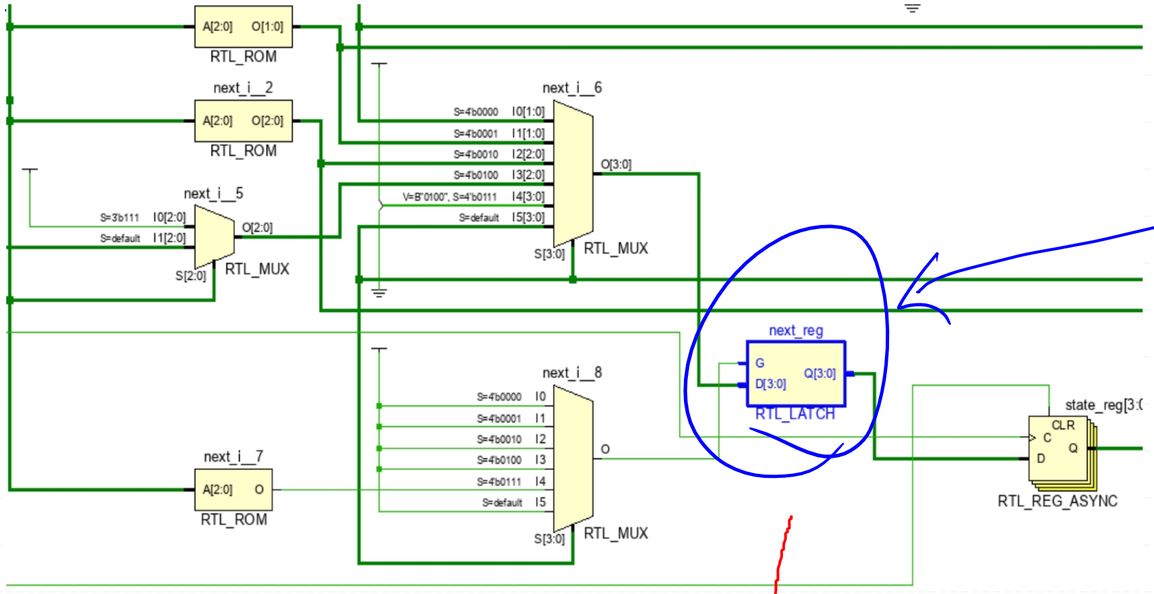
LED ● : ON

LED ○ : off

SW : Input



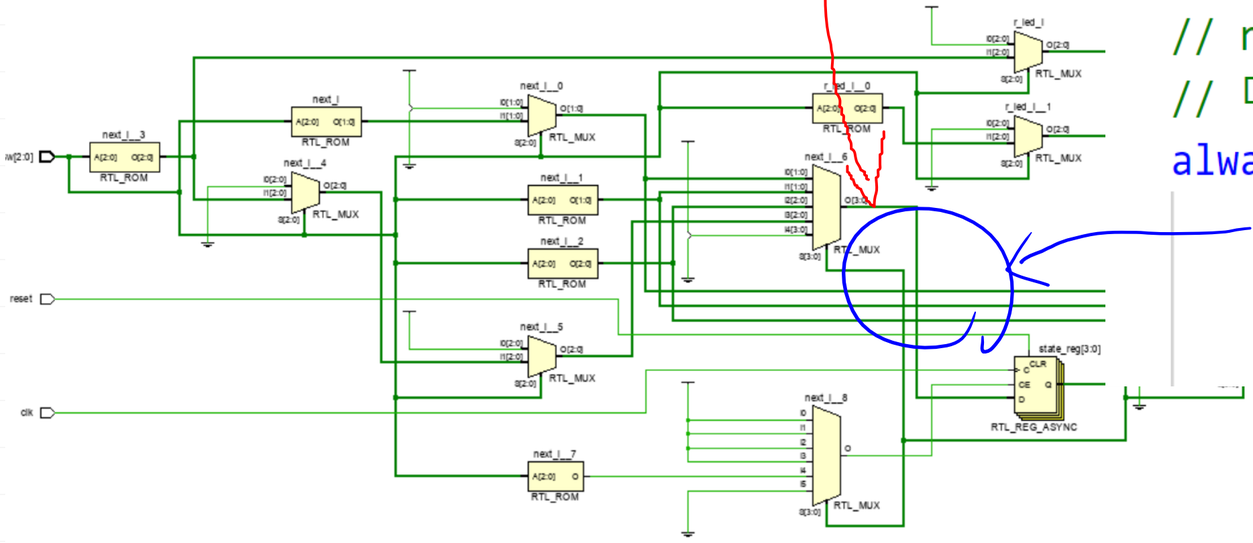

Mealy Machine
Inputs
Next State Combinational Logic
State Register
Clock
Output Combinational Logic
Outputs (Mealy-type)
Output depends on input variables and current state
Moore Machine
Inputs
Next State Combinational Logic
State Register
Clock
Output Combinational Logic
Outputs (Moore-type)
Output depends on current state only



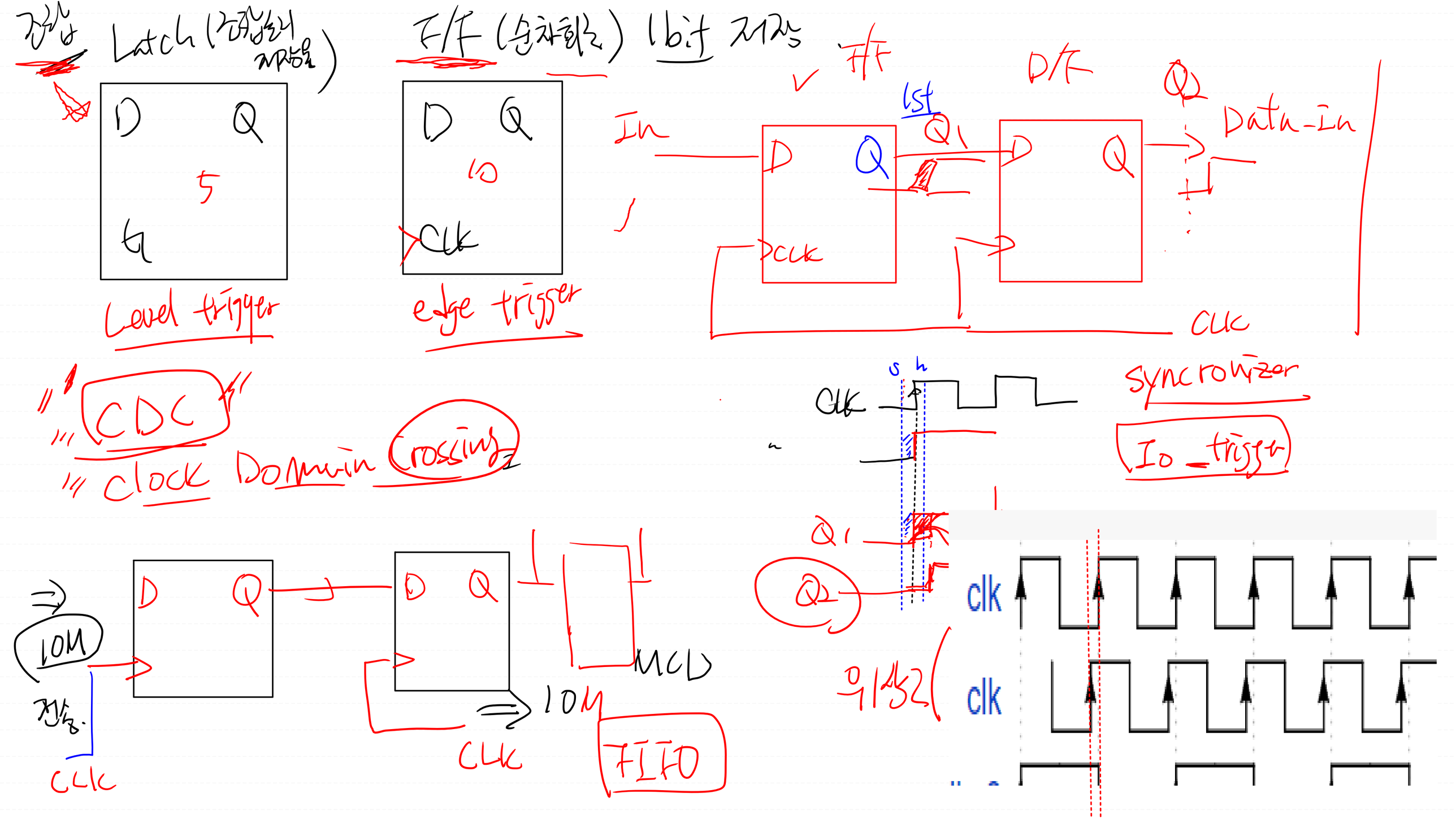

```
// next combinational logic
// 다음 상태로 가기위한 로직.
always @(*) begin
    //next = state;     // 초기값
      case (state)  // 현재상태.
          IDLE: begin
```

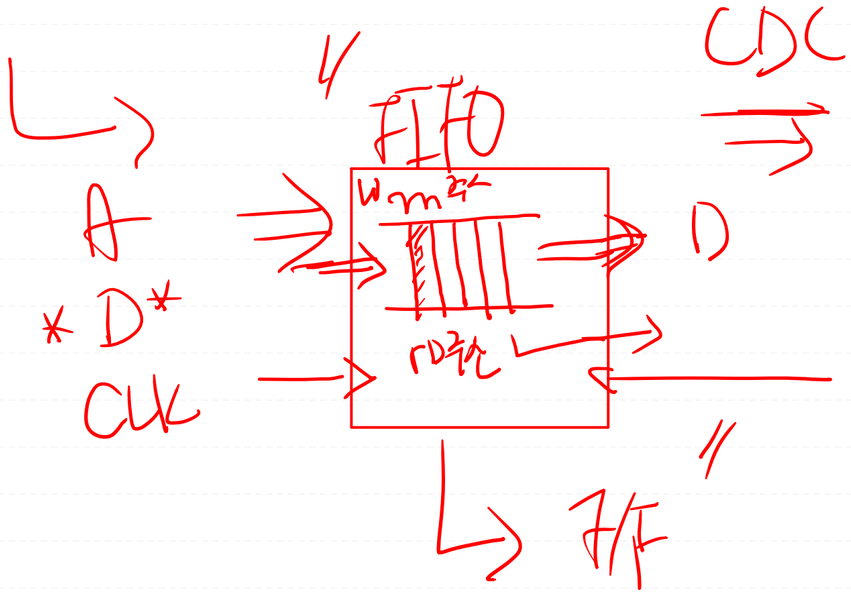
case default 필수

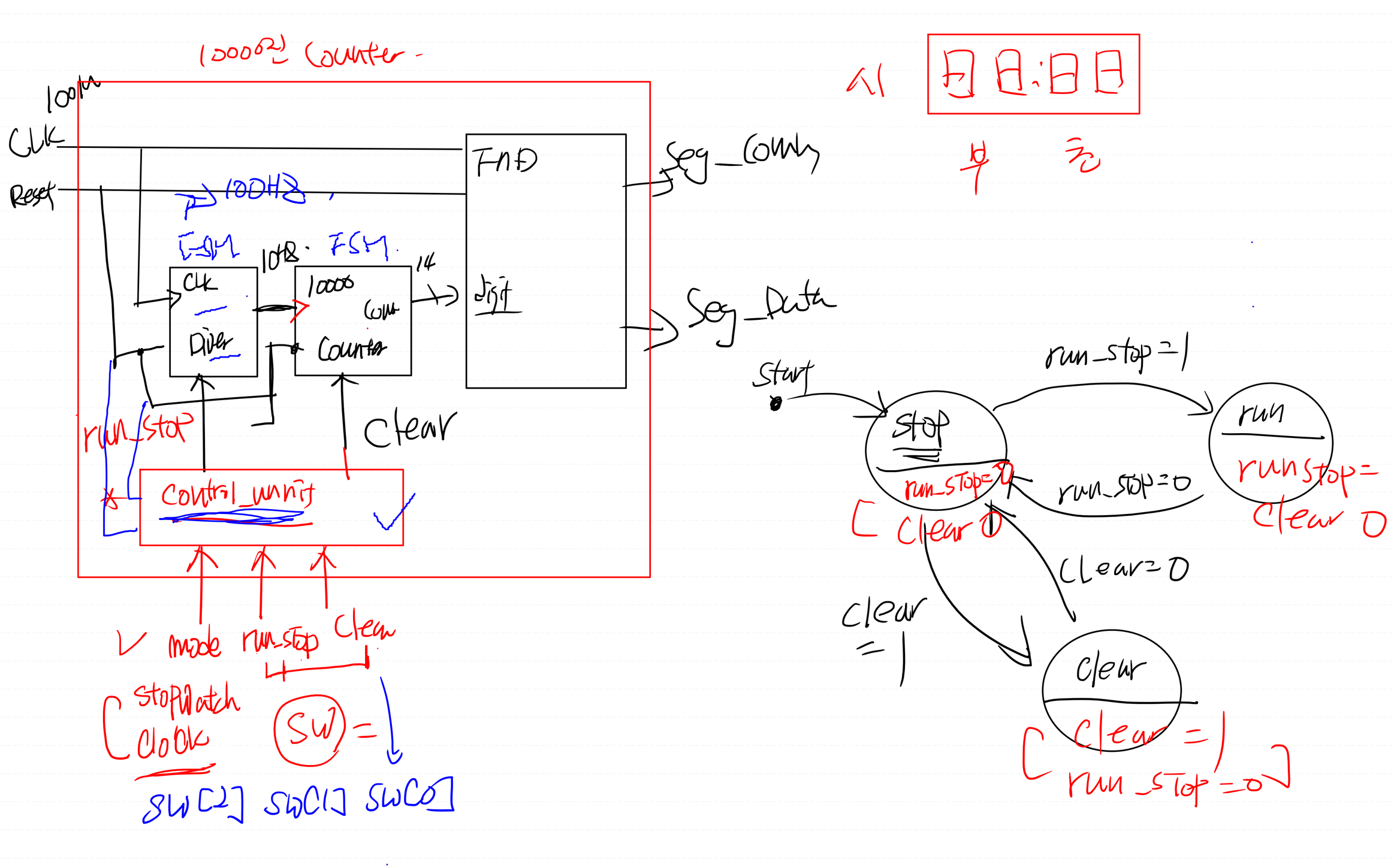
강제로 always(*) 초기값 설정.




```
// next combinational logic
// 다음 상태로 가기위한 로직.
always @(*) begin
    next = state;     // 초기값
      case (state)  // 현재상태.
          IDLE: begin
```

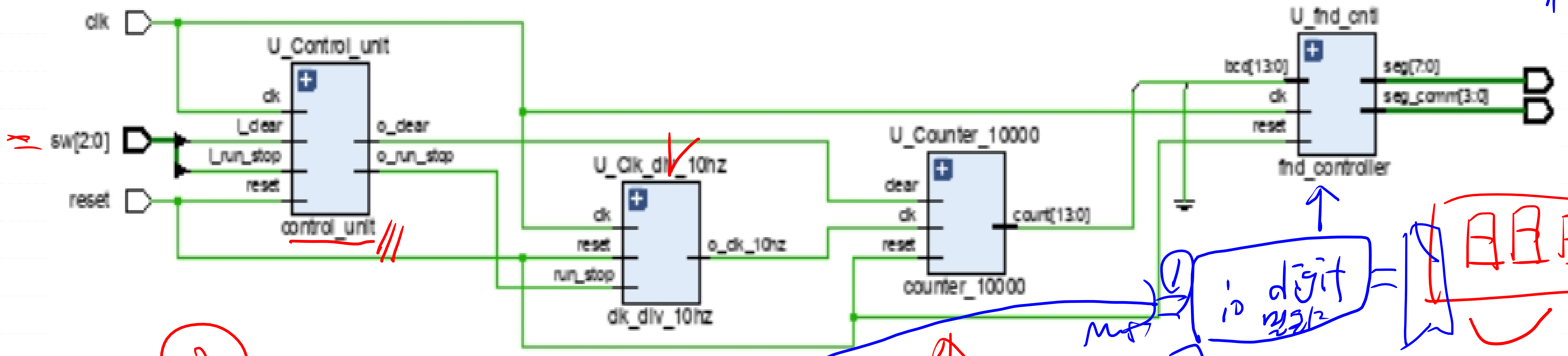

Latch (래치)
D
Q
G
Level trigger
F/F (플립플롭) 1bit 저장
D
Q
CLK
edge trigger
FF
D/F
In
1st
Q1
Q
Data-in
CLK
CDC
Clock Domain crossing
S
h
CLK
Synchronizer
IO trigger
Q1
Q2
D
Q
10M
전송.
CLK
MCU
10M
CLK
FIFO
clk
clk


FIFO
CDC
A
D
CLK
D
FF


100MHz
Clk
Reset
FND
Seg_comm
Seg_Data
100Hz
FSM
10ms FSM
clk
Div
10000
Counter
14
digit
clear
run_stop
control_unit
mode
run_stop
clear
stopWatch
clock
SW
SW[2] SW[1] SW[0]
start
stop
run_stop=0
run_stop=1
run
runstop=1
clear 0
clear=0
clear
=1
clear
clear=1
run_stop=0

① 10000진 Couter

③ Clock



60진 ②

초
분
시

sec msec

시간 분

sw[3]

② Stopwatch

· 1/100초 10msec

· 0~59 초

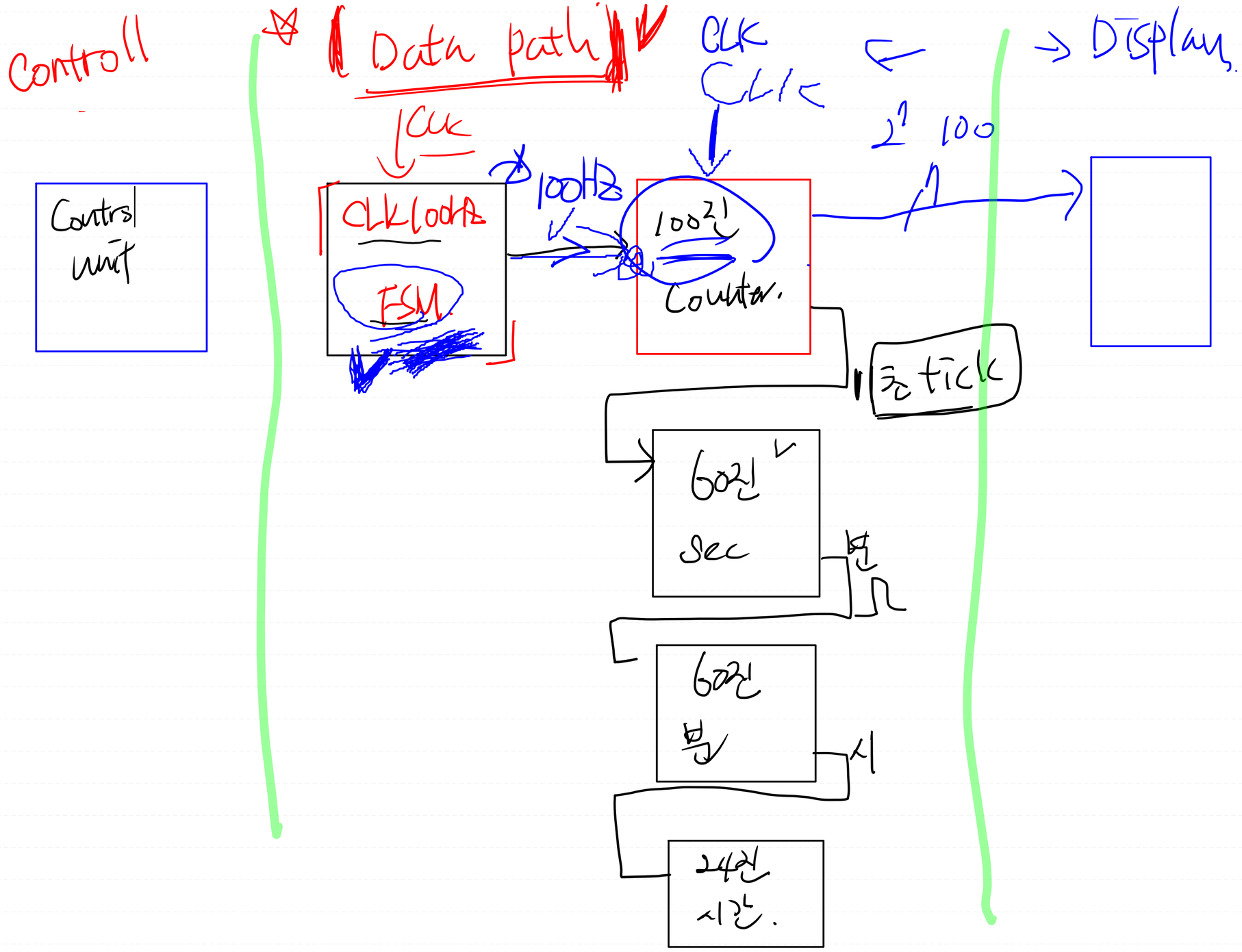
· 0~59 분

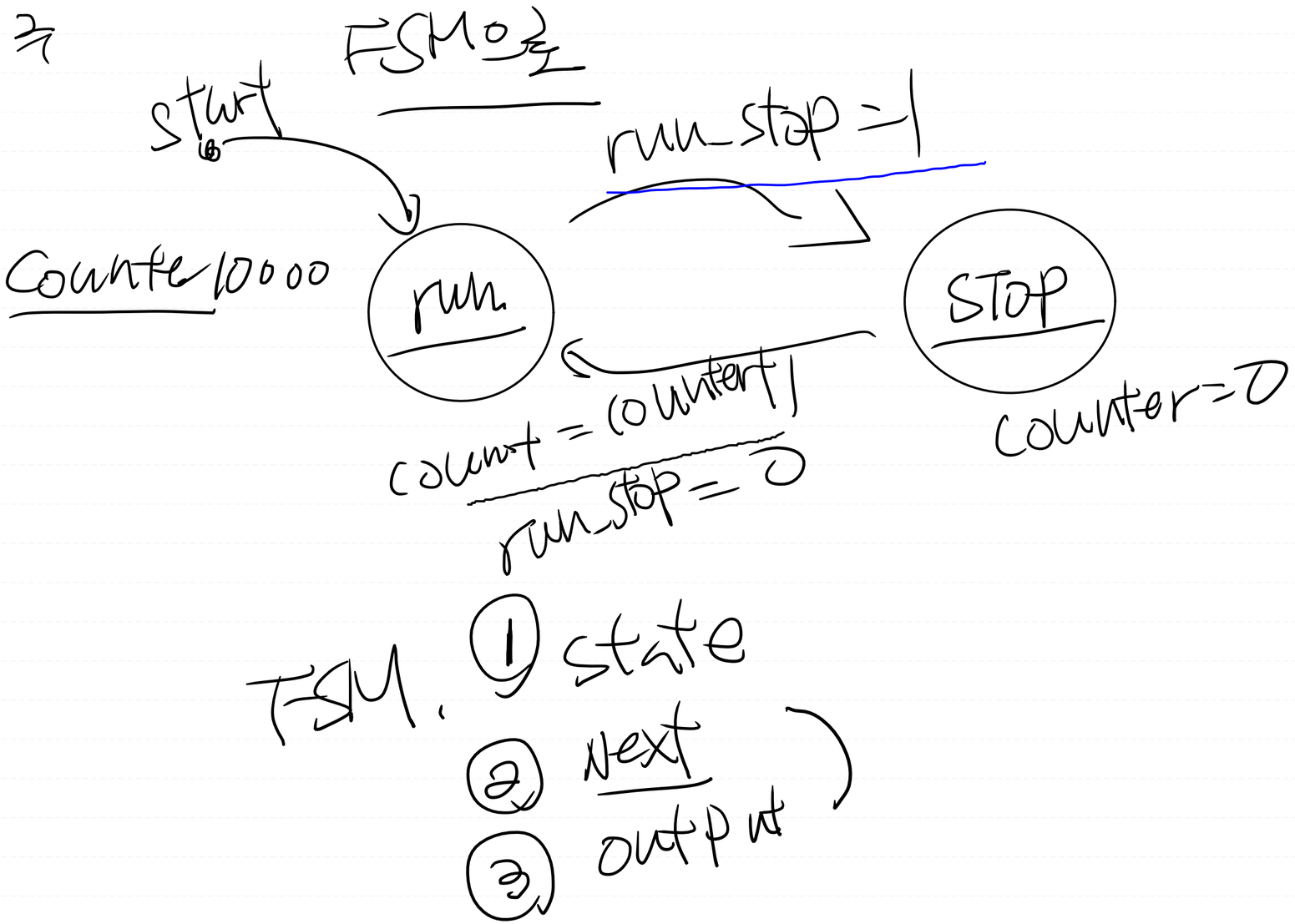
· 0~23 시.

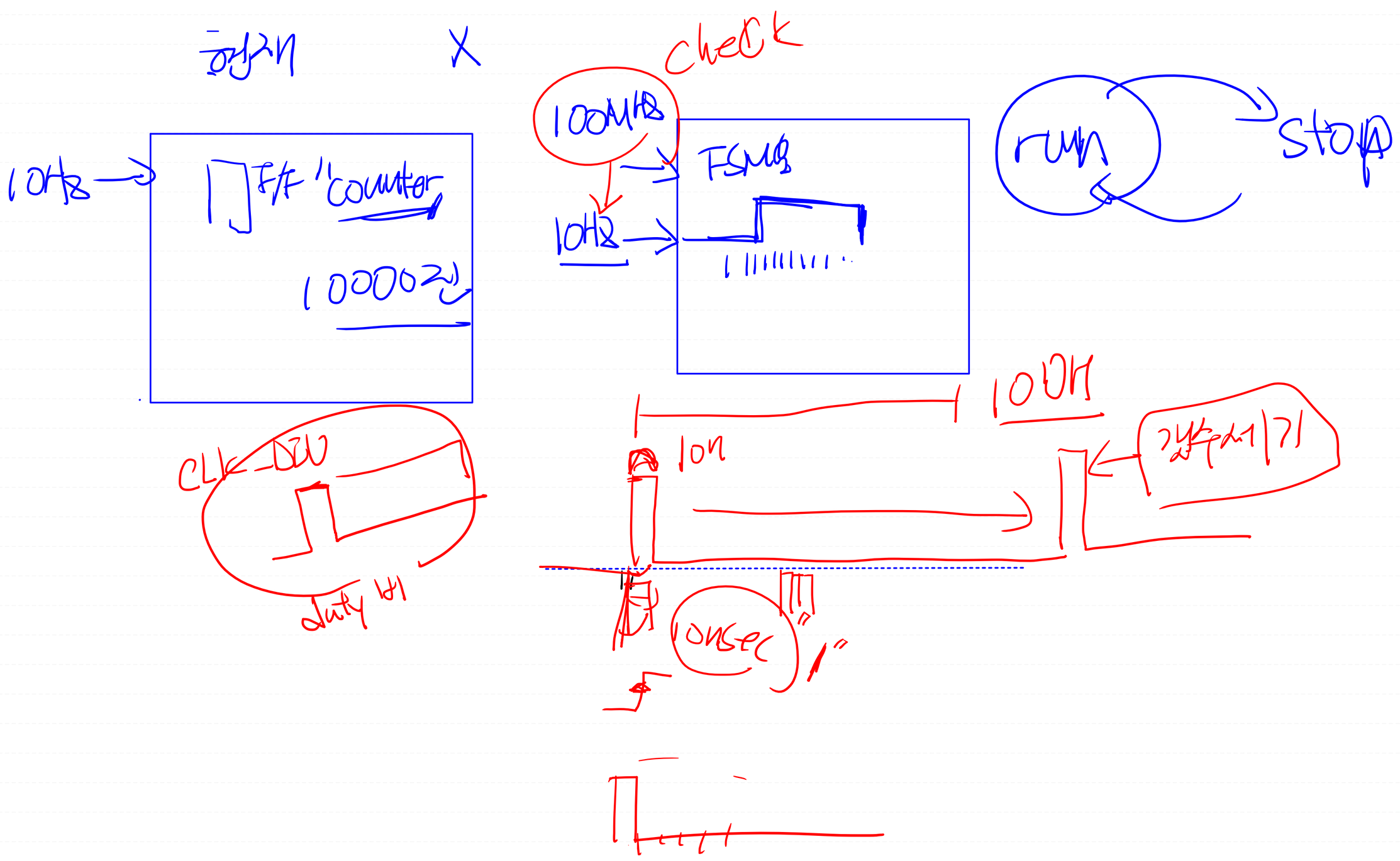
clk_div_10hz

FSM 100hz

FSM


Controll
Data path
CLK
Display
Contrs unit
CLK 100Hz
FSM
100Hz
100진 Counter
1? 100
5ms tick
60진 sec
60진 분
24진 시간.


FSM의 종류
start
run_stop=1
Counter 10000
run
STOP
count = counter-1
run_stop=0
counter=0
FSM. ① state
② next
③ output


check
100MHz
10Hz
FSM
run
stop
10Hz
F/F
counter
100002진
CLK
DIV
duty 비
10cm
1cm
10nsec

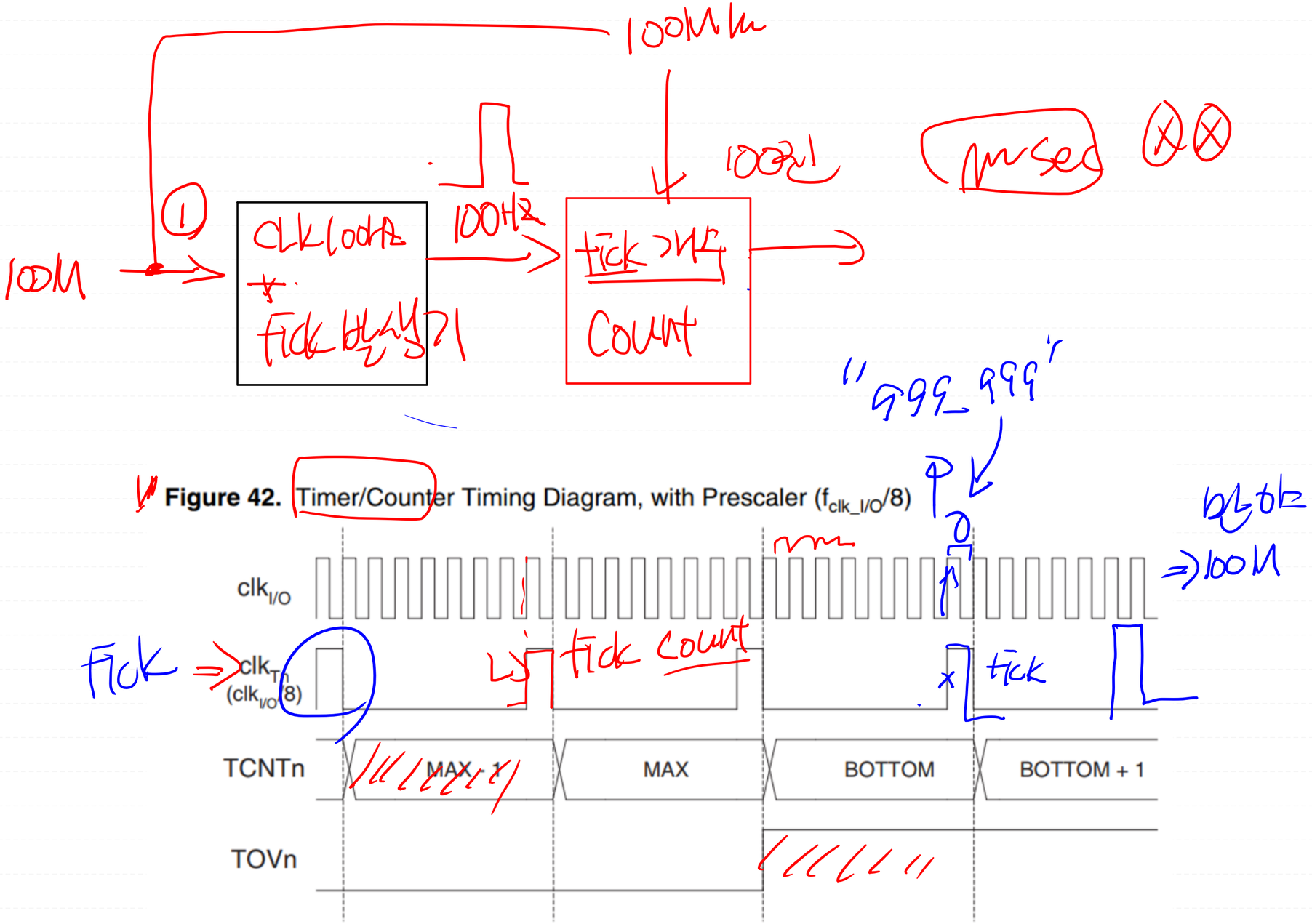


Figure 42. Timer/Counter Timing Diagram, with Prescaler ($f_{clk\_I/O}/8$)

H/W

교재 348 page.

연습하기 Test bench 결과