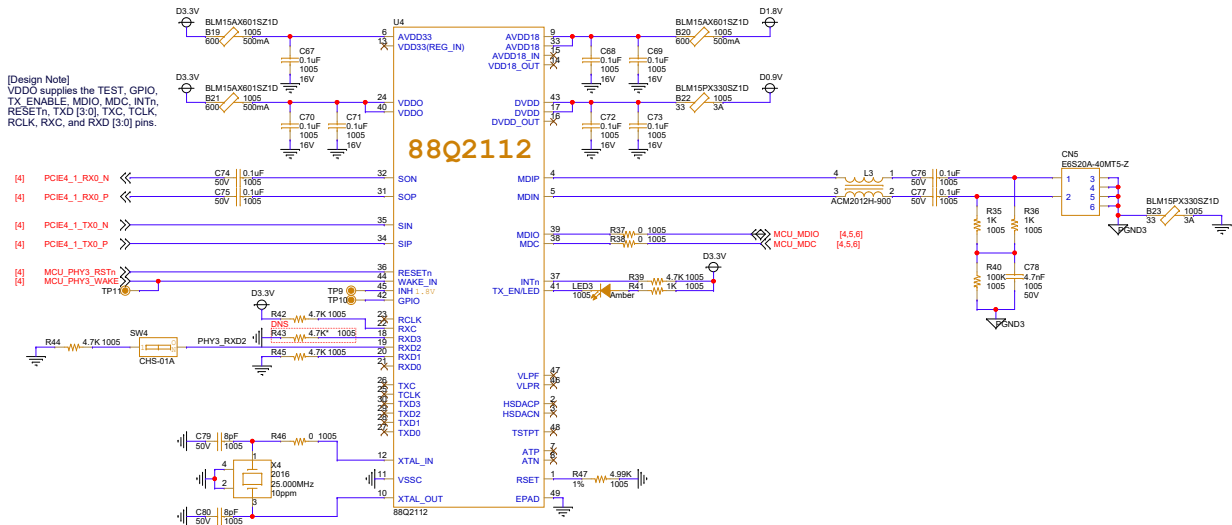


[Design Note]
Hardware Configuration
RXC=1
-> SGMII

PHYAD =010
GPIO=open -> PHYAD[2]=0
RXD[1]=0 -> PHYAD[1]=1
RXD[0]=open -> PHYAD[0]=0

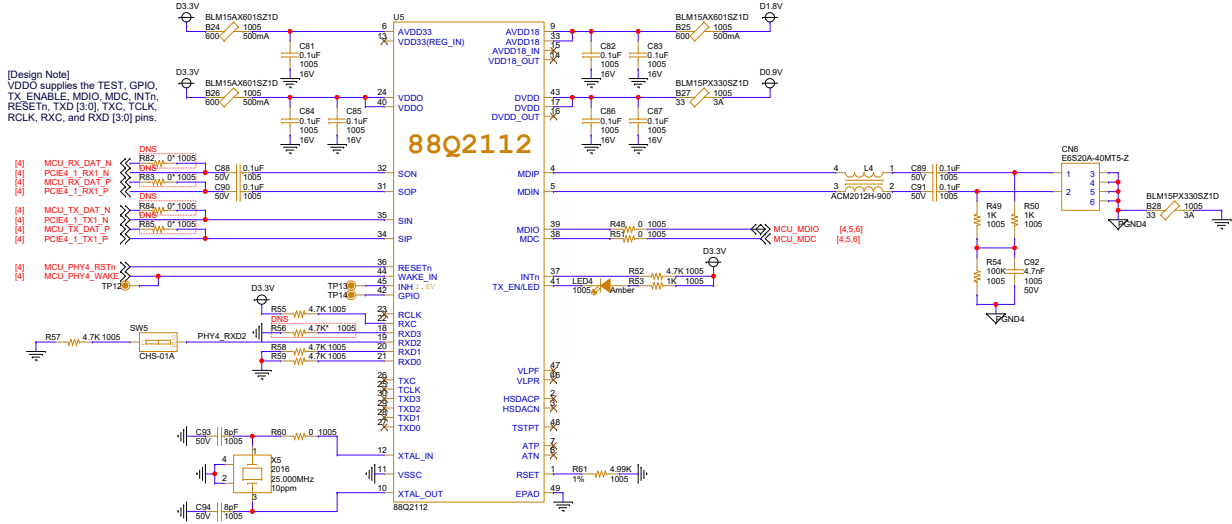
RXD[3:2] (RXD[3]=1, fixed)
10 = 1000BASE-T1, Master
11 = 1000BASE-T1, Slave

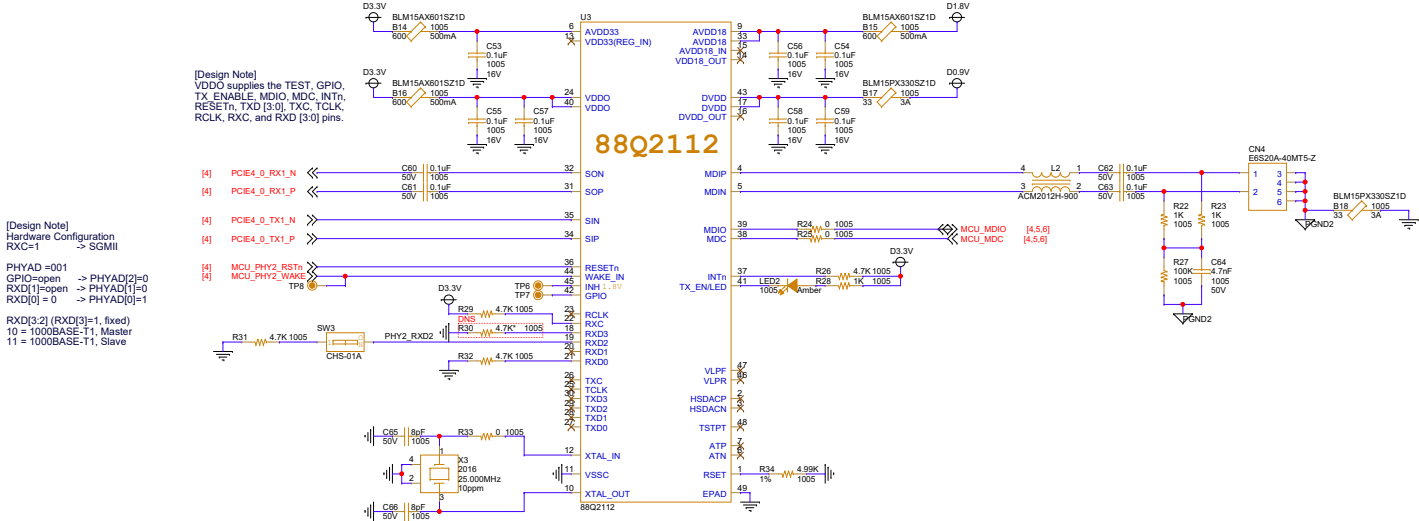
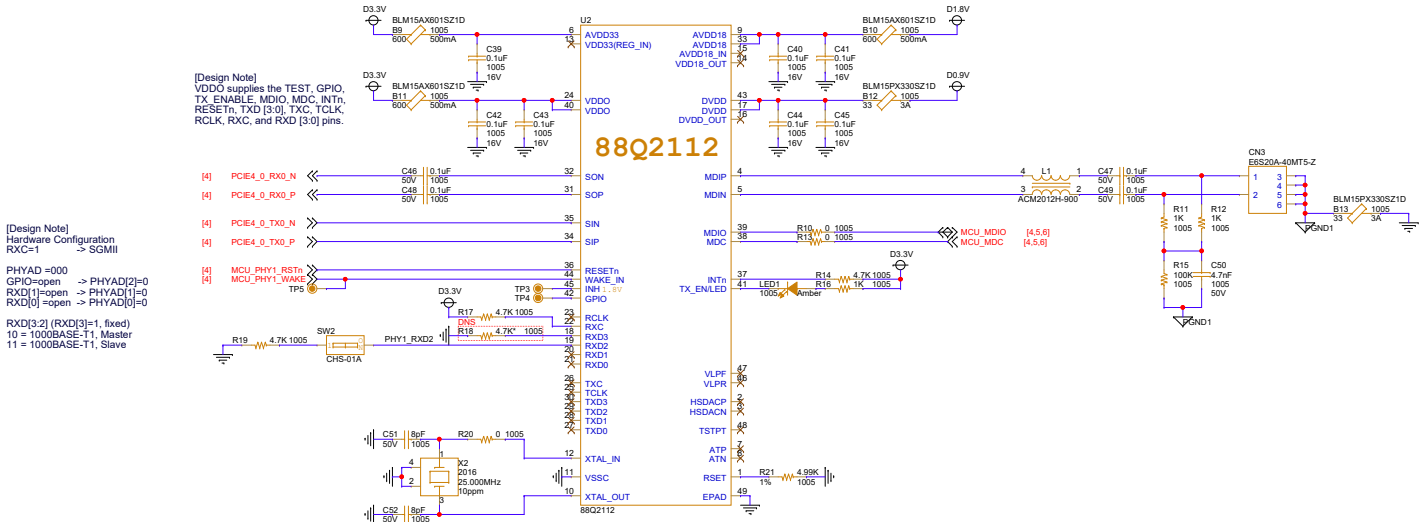


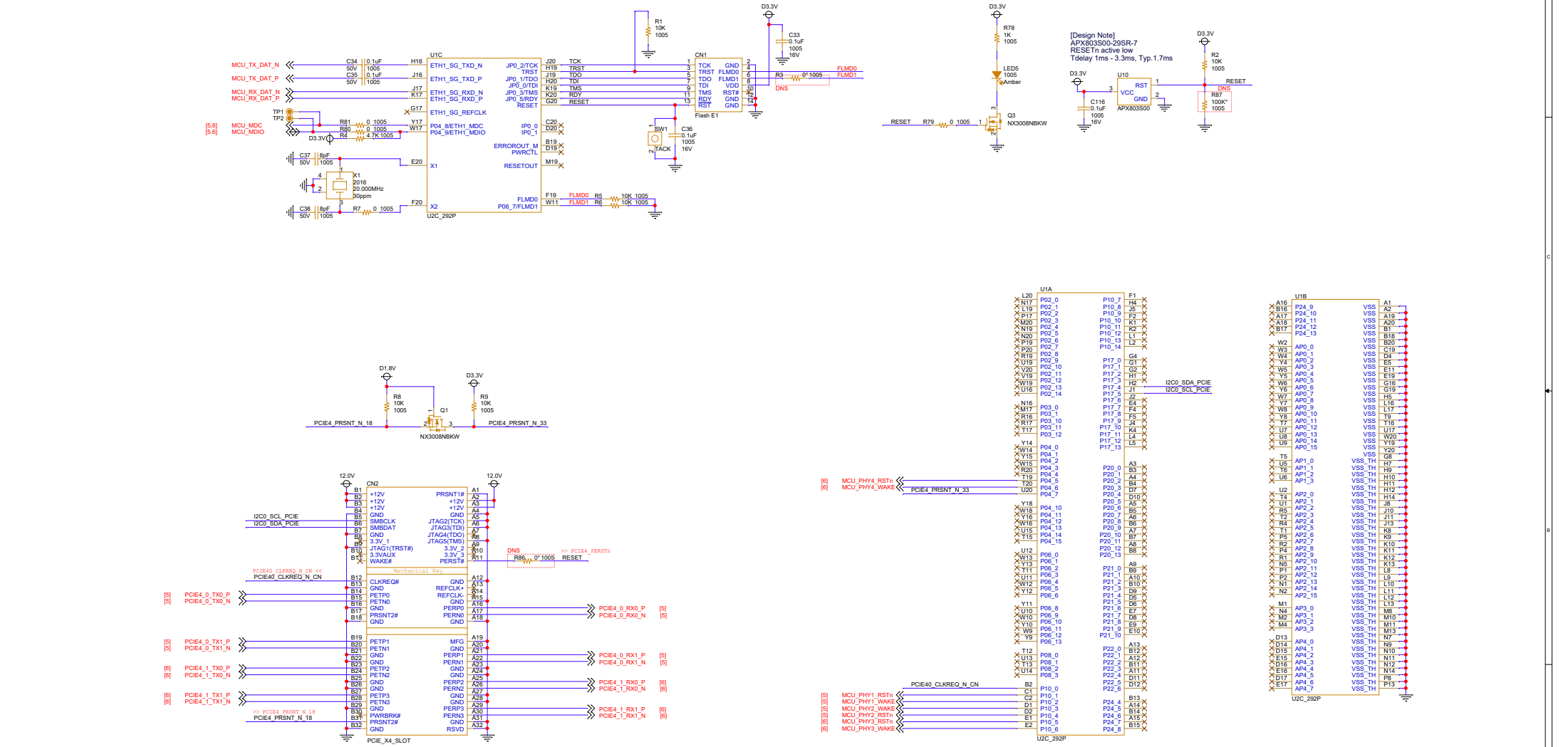
[Design Note]
Hardware Configuration
RXC=1
-> SGMII

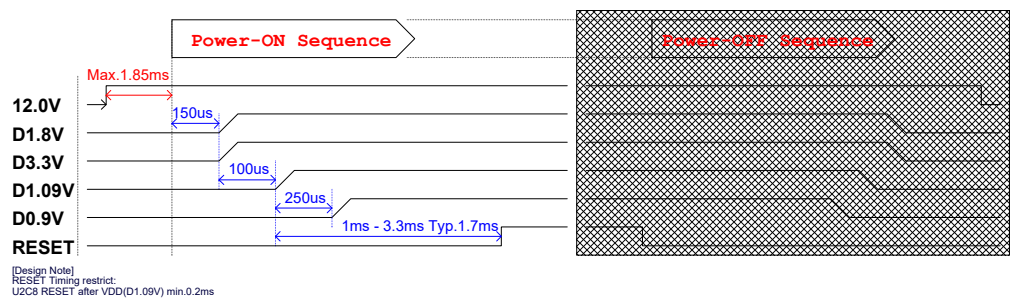
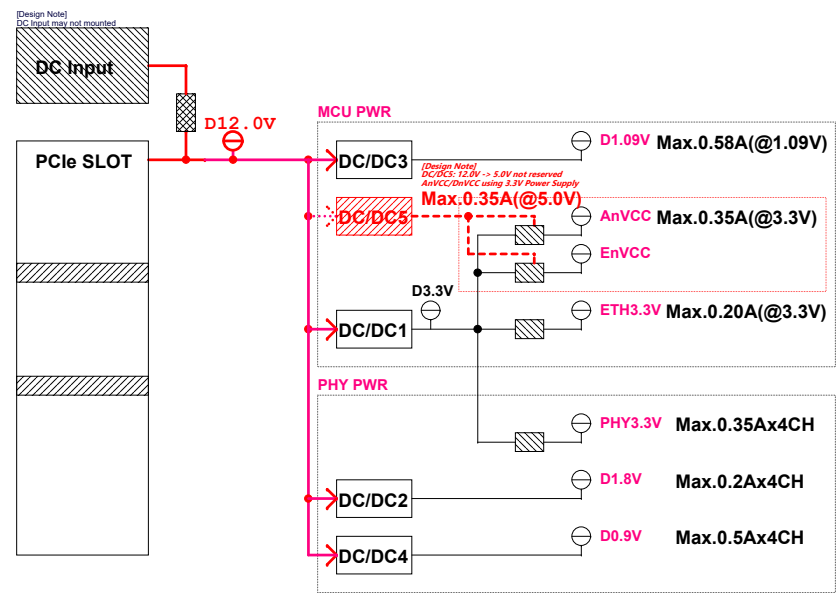
PHYAD =011
GPIO=open -> PHYAD[2]=0
RXD[1]= 0 -> PHYAD[1]=1
RXD[0]= 0 -> PHYAD[0]=1

RXD[3:2] (RXD[3]=1, fixed)
10 = 1000BASE-T1, Master
11 = 1000BASE-T1, Slave









Preliminary

X5H PCIE4.0 SLOT ETH EX-Board

R7F702600AFABB-C

Rev.0.01

Preliminary

P01: TITLE
P02: POWER TREE
P03: U2C8_292P_PWR
P04: U2C8_292P_FUN
P05: SGMII_PHY1/2
P06: SGMII_PHY3/4
P07: PWR_INPUT