88Q2110/88Q2112

Automotive 100/1000BASE-T1 Transceiver

Datasheet

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PRODUCT OVERVIEW

The Marvell® 88Q2110/88Q2112 device is a single-pair Ethernet physical layer transceiver (PHY) that supports operation over unshielded twisted pair (UTP). The transceiver implements the Ethernet physical layer portion of 100/1000BASE-T1 as defined by IEEE 802.3bw and the IEEE 802.3bp standard, including auto-negotiation, link-synchronization, and OAM features. It is manufactured using a standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on a single balanced twisted pair.

The device family supports reduced pin count GMII (RGMII) and SGMII for direct connection to a MAC/switch port. SGMII operates at 1.25 Gbps over a single differential pair, reducing power and number of I/Os used on the MAC interface.

The device integrates media dependent interface (MDI) termination resistors into the PHY. This resistor integration simplifies board layout and reduces board cost by reducing the number of external components.

The device has a linear regulator to generate all required voltages. The device can run off a single 3.3V supply. The device supports 1.8V, 2.5V, and 3.3V LVCMOS I/O standards.

The device incorporates the Marvell Advanced Virtual Cable Tester® (VCT) feature, which uses time domain reflectometry (TDR) technology for the remote identification of potential cable malfunctions, reducing equipment returns and service calls. Using VCT, the device will also detect cable opens, shorts, or any impedance mismatch in the cable and report the distance to the fault accurately within one meter.

The device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a data rate of either 100 Mbps or 1 Gbps. The device achieves robust performance and exceeds automotive electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

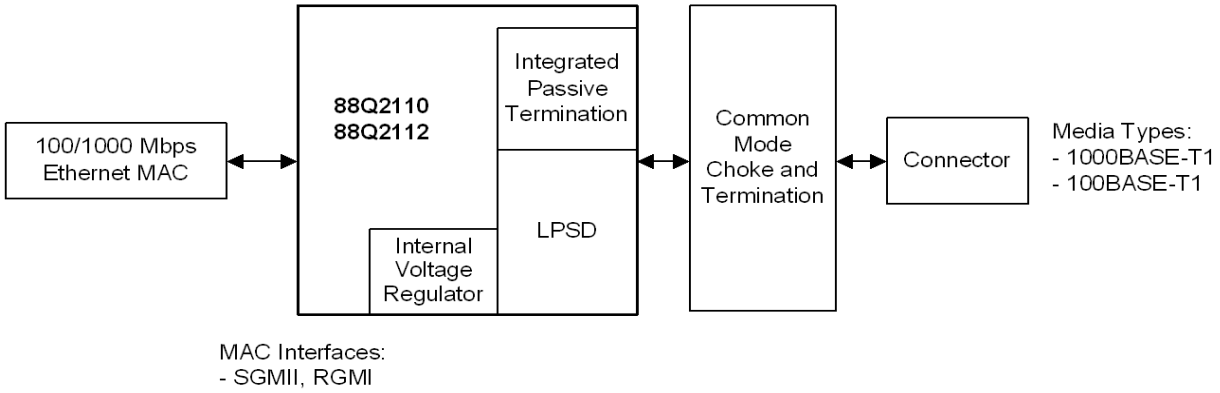
The 88Q2110 device is compatible to the footprint of the 88Q1010 100BASE-T1 Ethernet PHY transceiver.

Features

- Interfaces
  - 1000BASE-T1, IEEE 802.3bp-compliant
  - 100BASE-T1, IEEE 802.3bw-compliant
  - RGMII interface
    1.8V/2.5V/3.3V MAC interface I/Os
  - MDC/MDIO management interface
- Multiple operating modes
  - RGMII to copper
  - SGMII to copper
- Four RGMII timing modes including integrated delays which eliminates the need for adding trace delays on the PCB
- Supports LVCMOS I/O standards on the RGMII interface
- Supports Energy Efficient Ethernet (EEE)
- Integrated MDI interface termination resistors which eliminate passive components
- Integrated voltage regulators
- Loopback modes for diagnostics
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic polarity correction
- Supports both IEEE 802.3bp-compliant Auto-Negotiation mode and Link Synchronization mode
- Software programmable LED modes
- Supports Synchronous Ethernet (SyncE)
- Supports 802.1AS – precision time protocol (PTP)
- Supports 1-step PTP
- CRC checker, packet counter
- Packet generation
- Advanced VCT for cable diagnostics
- Ultra-low power
- Low power signal detect (LPSD) with energy detect <50 µA

- Auto-calibration for MAC interface outputs
- Supports single 3.3V supply when using an internal regulator
- I/O pads can be supplied with 1.8V, 2.5V, or 3.3V for all packages
- AEC-Q100 Automotive Standard compliant
- Supports Automotive Grade 2
- 40-pin QFN, 6 mm × 6 mm (88Q2110)
- 48-pin QFN, 7 mm × 7 mm (88Q2112)
- Integrated temperature sensor

Figure 1: MAC Interface to Copper Device Application



Features	88Q2110	88Q2112
RGMII to copper	Yes	Yes
SGMII to copper	No	Yes
100BASE-T1	Yes	Yes
1000BASE-T1	Yes	Yes
I/O Voltage (VDDO)	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V
Package	40-pin QFN	48-pin QFN

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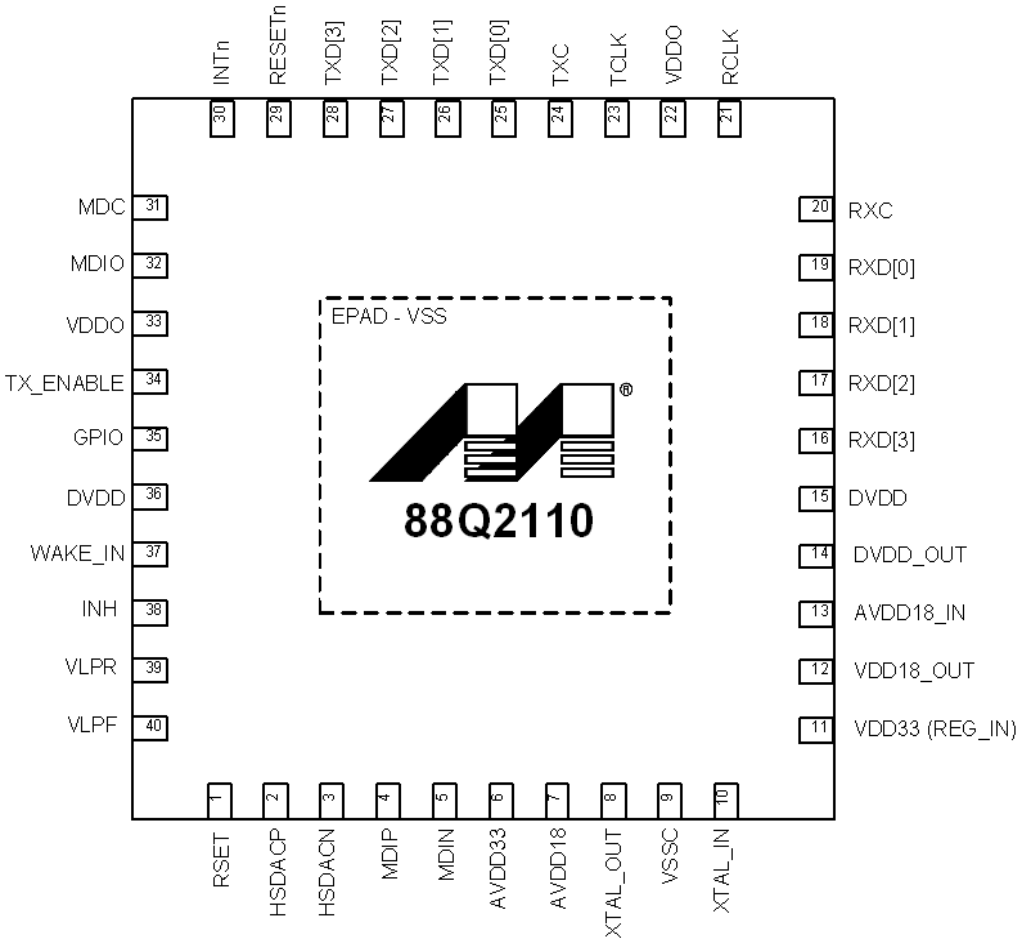
1 Signal Description

1.1 Pinout

1.1.1 88Q2110 Device 40-pin Package

The 88Q2110 device is a 100/1000BASE-T1 Ethernet transceiver.

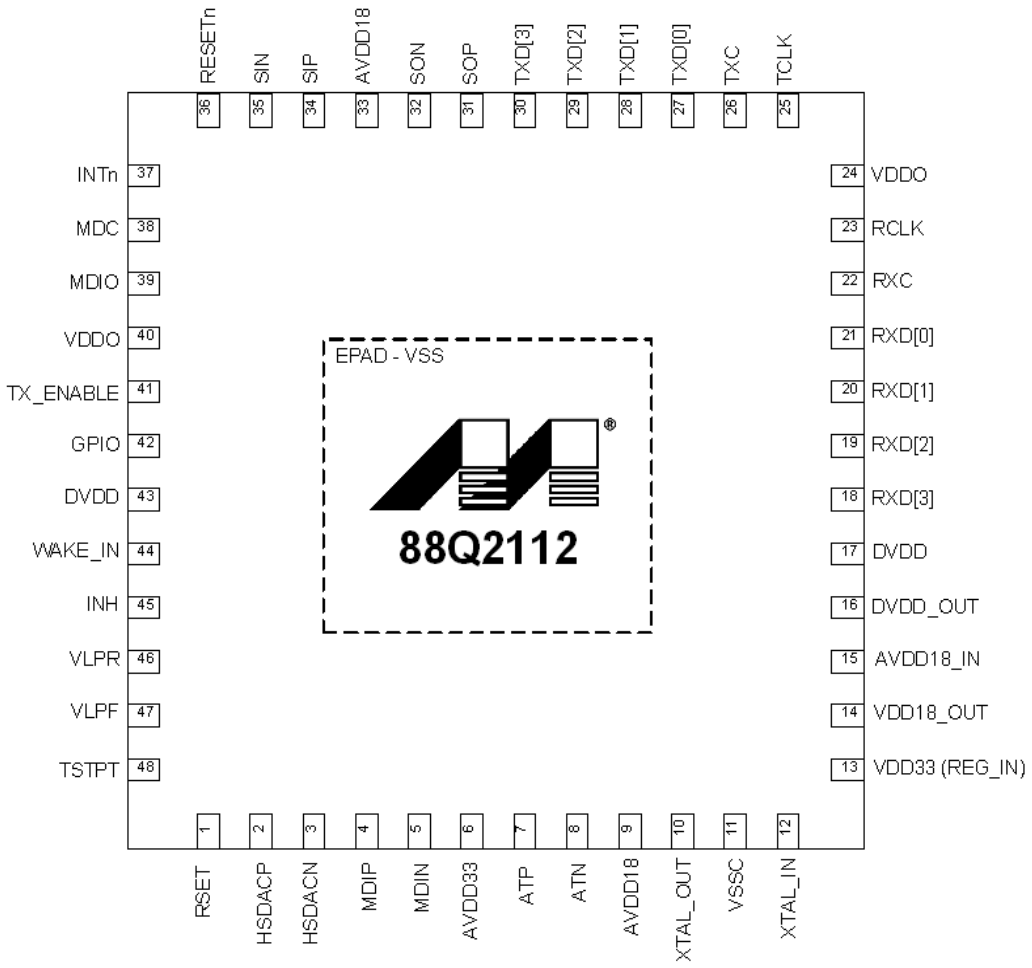
Figure 2: 88Q2110 Device 40-pin RGMII Package (Top View)



1.1.2 88Q2112 Device 48-pin Package

The 88Q2112 device is a 100/1000BASE-T1 Ethernet transceiver.

Figure 3: 88Q2112 Device 48-pin RGMII/SGMII Package (Top View)



1.2 Pin Descriptions

Table 1: Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.2.1 Media Dependent Interface

Table 2: Media Dependent Interface

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
5 4	5 4	MDIN MDIP	I/O	Media Dependent Interface. In 100/1000BASE-T1, MDIN/P are used for transmit and receive.

1.2.2 Host Interfaces

The host interfaces support 100BASE-T1 and 1000BASE-T1 modes of operation.

Table 3: Host Interfaces

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
23	25	TCLK	I	When RGMII is used, this pin is an input. • 100BASE-T1 mode: This pin should be driven with a 25 MHz clock with ±50 ppm tolerance. • 1000BASE-T1 mode: This pin should be driven with a 125 MHz clock with ±50 ppm tolerance.
24	26	TXC	I	When RGMII is used, this pin's signal must be presented according to the RGMII timing mode requirements.
28 27 26 25	30 29 28 27	TXD [3] TXD [2] TXD [1] TXD [0]	I	When RGMII is used, the signal for these pins must be presented according to the RGMII timing mode requirements. • 100BASE-T1 mode: Data is presented for sampling with the rising edge of TCLK only. • 1000BASE-T1 mode: Data is presented for sampling with both edges of TCLK.
21	23	RCLK	O	When RGMII is used, this pin is an output. • 100BASE-T1 mode: This pin is an output that drives out a 25 MHz clock with ±50 ppm tolerance. • 1000BASE-T1 mode: This pin is an output that drives out a 125 MHz clock with ±50 ppm tolerance.
20	22	RXC	O	When RGMII is used, this pin's signal must be presented according to the RGMII timing mode requirements.
16 17 18 19	18 19 20 21	RXD [3] RXD [2] RXD [1] RXD [0]	O	When RGMII is used, the signal for these pins must be presented according to the RGMII timing mode requirements. • 100BASE-T1 mode: Data is presented for sampling with the rising edge of RCLK only. • 1000BASE-T1 mode: Data is presented for sampling with both edges of RCLK.
--	32	SON	A, O	SGMII Transmit Data. 1.25 GBaud output. Negative.
--	31	SOP	A, O	SGMII Transmit Data. 1.25 GBaud output. Positive.
--	35	SIN	A, I	SGMII Receive Data. 1.25 GBaud input. Negative.
--	34	SIP	A, I	SGMII Receive Data. 1.25 GBaud input. Positive.

1.2.3 Management Interface

Table 4: Management Interface

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
31	38	MDC	I	Management Interface Clock. This pin is MDC. A continuous clock stream is not required for MDC; however, the maximum frequency allowed is 12.5 MHz. Management Interface Data
32	39	MDIO	I/O	Management Interface Data. This pin is MDIO and requires a pull-up resistor with a resistance from 1.5 kΩ to 10 kΩ.

1.2.4 TX_ENABLE/GPIO/Interrupt Interface

Table 5: TX_ENABLE/GPIO/Interrupt Interface

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
34	41	TX_ENABLE	I/O	Tx Enable/GPIO/LED. This pin is an input by default and used to implement a feature that allows blocking Tx packets. For details, see Section 2.3.3, Tx Disable Feature. This pin can still be used as an GPIO/LED.
35	42	GPIO	I/O	GPIO/LED Output/SyncE Recovered Clock Output.
30	37	INTn	O, D	Interrupt Output.

1.2.5 Clock/Configuration/Reset/I/O

Table 6: Clock/Configuration/Reset/I/O

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
10	12	XTAL_IN	I	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference or oscillator input. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin should be AC coupled with a 0.1 nF capacitor. **NOTE:** The XTAL_IN pin is not 2.5V/3.3V tolerant. For information on how to convert a 2.5V/3.3V clock source to a 1.8V clock, see the *Oscillator Level Shifting Application Note* (MV-S301630-00).
8	10	XTAL_OUT	O	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected to a crystal, it should be connected to ground through a 0.1 nF ceramic capacitor.
9	11	VSSC	I	XTAL ground.
29	36	RESETn	I	Hardware reset, active-low. 0 = Reset 1 = Normal operation

1.2.6 Control and Reference

Table 7: Control and Reference

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
1	1	RSET	I	Constant Voltage Reference. For this pin, an external 4.99 kΩ 1% resistor connection to VSS is required.

1.2.7 Test

Table 8: Test

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
3 2	3 2	HSDACN HSDACP	A, O	Test Pins. These pins must be left floating.
--	48	TSTPT	A, O	DC Test Point. This pin must be left floating.
--	8	ATN	A, O	Test Pin. This pin must be left floating
--	7	ATP	A, O	Test Pin. This pin must be left floating.

1.2.8 Power, Ground, and Internal Regulators

Table 9: Power, Ground, and Internal Regulators

88Q2110 Pin #	88Q2112 Pin #	Pin Name	Pin Type	Description
7	9 33	AVDD18	Power	Analog Supply – 1.8V[1]. AVDD18 can be supplied externally with 1.8V or via the 1.8V internal regulator.
6	6	AVDD33	Power	Analog Supply – 3.3V.
11	13	VDD33 (REG_IN)	Power	Analog Supply for the Internal Regulator – 3.3V. If the internal regulator is not used, then this pin must be left floating (No Connect). **CAUTION:** If the internal regulator is not used, then this pin must be left floating. Connecting this pin to either another power supply or to ground will damage the device.
13	15	AVDD18_IN	Power	Power Regulator Input – 1.8V. AVDD18_IN is supply input for internal DVDD regulator.
12	14	VDD18_OUT	Power	Regulator Output – 1.8V. If the internal regulator is used, then this pin must be connected to the 1.8V power plane that is connected to AVDD18. If the external supply is used, this pin must be left floating (No Connect).
14	16	DVDD_OUT	Power	Regulator Output – 0.9V. If the internal regulator is used, then this pin must be connected to the 0.9V power plane that is connected to DVDD. If the external supply is used, then this pin must be left floating (No Connect).
22 33	24 40	VDDO	Power	3.3V or 2.5V or 1.8V Digital I/O Supply[2]. If VDDO is 2.5V or 3.3V, then it must be supplied externally. If VDDO is 1.8V, then the 1.8V regulator output can be used to supply this or it may be supplied externally.
15 36	17 43	DVDD	Power	Digital Core Supply – 0.9V. DVDD can be supplied externally with 0.9V or via the 0.9V internal regulator.
EPAD	EPAD	VSS	GND	Ground to Device. Both the 40-pin and the 48-pin QFN package have an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. For the exact location and dimensions of the E-PAD, see Section 6, Package Mechanical Dimensions, on page 212.

1. AVDD18 supplies the XTAL_IN and XTAL_OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, INTn, TX_ENABLE, GPIO, TEST, and the host interface pins.

Note

If an application requires an internal/external mixed supply, then refer to Figure 20, Supply and Regulator Connection Options.

- 1.8V external, DVDD internal
  - VDD33 is supplied from external 3.3V.
  - VDD18_OUT is not connected to AVDD18_IN and AVDD18, but it is still required to bypass the capacitors.
  - AVDD18 and AVDD18_IN are supplied from external 1.8V.
  - DVDD_OUT is connected to DVDD.
- DVDD external, 1.8V internal
  - VDD33 is supplied from external 3.3V.
  - VDD18_OUT is connect to AVDD18_IN and AVDD18.
  - DVDD_OUT is not connected to DVDD, but it is still required to bypass the capacitors.
  - DVDD is supplied from external 0.9V.

1.2.9 Low Power Signal Detect (LPSD)

Table 10: Low Power Signal Detect

88Q2110P in #	88Q2112P in #	Pin Name	Pin Type	Description
38	45	INH	A	This is the output to control enable of the external regulator. This pin should be left floating when LPSD is not used.
39	46	VLPR	A	This is the regulated supply derived from battery. This supplies the energy detect sensing circuit and the INH I/O.
40	47	VLPF	A	Connect to the external battery circuit. Refer to Figure 10, LPSD Block Diagram, on page 41. This pin should be left floating when LPSD is not used.
37	44	WAKE_IN	A, I	This is used for local wake-up. This pin should be left floating when LPSD is not used.

1.3 Pin Assignment List — Alphabetical by Signal Name

1.3.1 88Q2110 40-pin QFN Pin Assignment List

Table 11: 88Q2110 40-pin QFN Pin Assignment List — Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
7	AVDD18	17	RXD [2]
13	AVDD18_IN	16	RXD [3]
6	AVDD33	23	TCLK
15	DVDD	34	TX_ENABLE
36	DVDD	24	TXC
14	DVDD_OUT	25	TXD [0]
35	GPIO	26	TXD [1]
3	HSDACN	27	TXD [2]
2	HSDACP	28	TXD [3]
38	INH	12	VDD18_OUT
30	INTn	11	VDD33 (REG_IN)
31	MDC	22	VDDO
5	MDIN	33	VDDO
32	MDIO	40	VLPF
4	MDIP	39	VLPR
21	RCLK	E-PAD	VSS
29	RESETn	9	VSSC
1	RSET	37	WAKE_IN
20	RXC	10	XTAL_IN
19	RXD [0]	8	XTAL_OUT
18	RXD [1]		

1.3.2 88Q2112 48-pin QFN Pin Assignment List

Table 12: 88Q2112 48-pin QFN pin Assignment List — Alphabetical by Signal Name

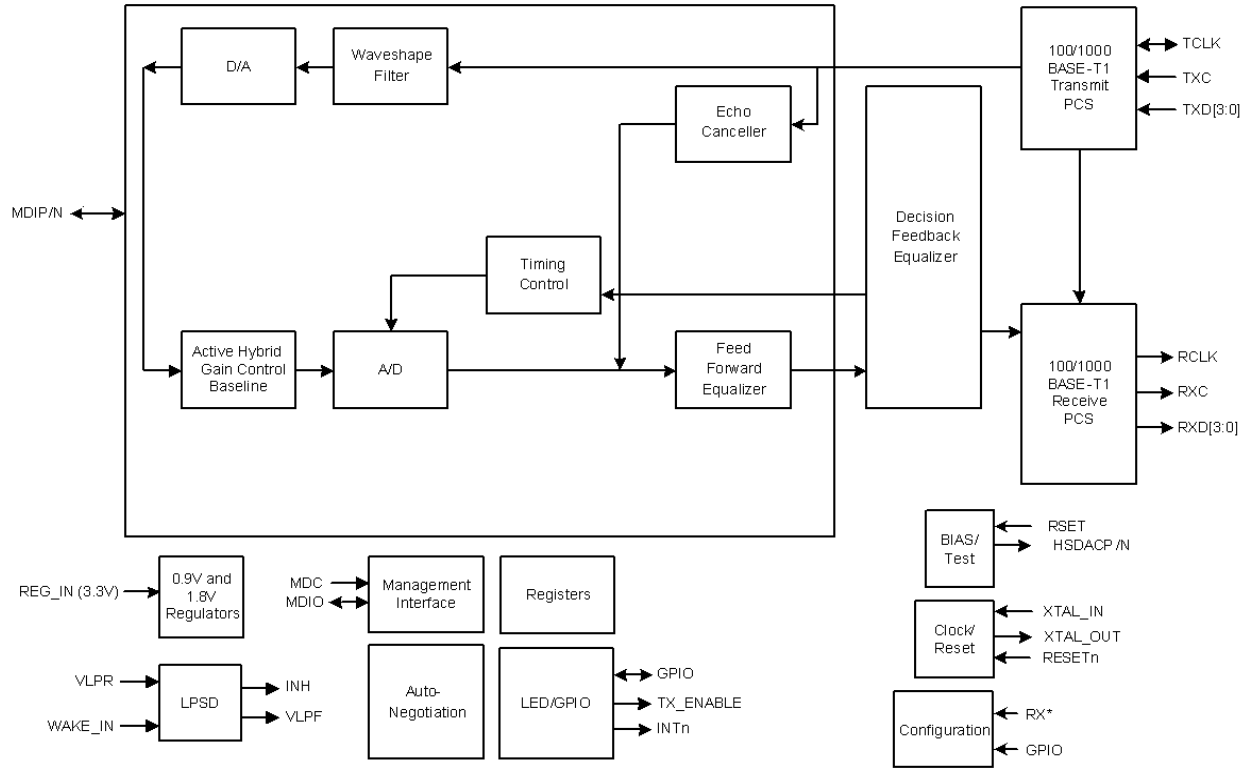
Pin #	Pin Name	Pin #	Pin Name
8	ATN	18	RXD [3]
7	ATP	35	SIN
9	AVDD18	34	SIP
33	AVDD18	32	SON
15	AVDD18_IN	31	SOP
6	AVDD33	25	TCLK
17	DVDD	26	TXC
43	DVDD	27	TXD [0]
16	DVDD_OUT	28	TXD [1]
42	GPIO	29	TXD [2]
3	HSDACN	30	TXD [3]
2	HSDACP	41	TX_ENABLE
45	INH	48	TSTPT
37	INTn	47	VLPF
38	MDC	46	VLPR
5	MDIN	13	VDD33 (REG_IN)
39	MDIO	24	VDDO
4	MDIP	40	VDDO
23	RCLK	14	VDDO18_OUT
36	RESETn	EPAD	VSS
22	RXC	11	VSSC
1	RSET	44	WAKE_IN
21	RXD [0]	12	XTAL_IN
20	RXD [1]	10	XTAL_OUT
19	RXD [2]		

2 PHY Functional Specifications

The device is a 100/1000BASE-T1 Ethernet transceiver. Figure 4 shows the functional block diagram of the devices.

Note Refer to the Product Overview for a list of features supported by the devices.

Figure 4: Device Functional Block Diagram



2.1 System Interfaces

The device has two system interfaces: SGMII and RGMII. They are available in two different package options:

- 88Q2110– 40-pin option with only RGMII interface
- 88Q2112– 48-pin option with both SGMII and RGMII interface

Two RGMII modes can be configured to select the data/clock timing relation. The default of registers 31.8001.15:14 will be set by the strapped value of the configuration pin as defined in Table 25; the delay of TCLK and RCLK is based on the value set in this register. For optimal design flexibility, the delay of TCLK and RCLK can also be controlled by reprogramming register 31.8001.15:14. For a detailed timing requirement for all modes, see Section 5.7, MAC Interface Timing, on page 206.

Table 13: Modes

Mode	Description	31.8001.15:14
RGMII (mode1)	TCLK (input) transitions at the same time as TXD/TXC. RCLK (output) transitions when RXD/RXC is stable. TCLK and RCLK are 25 MHz or 125 MHz. This is a DDR interface.	01
RGMII (mode2)	TCLK (input) transitions when TXD/TXC is stable. RCLK (output) transitions when RXD/RXC is stable. TCLK and RCLK are 25 MHz or 125 MHz. This is a DDR interface.	11

2.2 Copper Media Interface

The copper interface consists of the MDIP/N pins that connect to the physical media for 100/1000BASE-T1 mode of operation.

The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the connector. The resistors must be very accurate to meet the strict IEEE return loss requirements. Typically, ±1% accuracy resistors are used on the board. These additional components between the PHY and the connector complicates board layout. Integrating the resistors has many advantages, including component cost savings, better in-circuit test (ICT) yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements.

2.2.1 Transmit Side Network Interface

2.2.1.1 Multi-mode Tx Digital-to-Analog Converter

The device incorporates a transmit DAC to generate filtered 3-level pulse amplitude modulation (PAM3) symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement.

2.2.1.2 Slew Rate Control and Waveshaping

In 100/1000BASE-T1 mode, slew rate control is used to minimize high-frequency EMI.

2.2.2 Encoder

2.2.2.1 100/1000BASE-T1

In 100/1000BASE-T1 mode, the transmit data nibbles are organized into groups of three bits. These 3-bit symbols are scrambled and encoded into two PAM3 symbols. This prevents link partners from outputting the same sequence during idle, which helps to reduce EMI.

2.2.3 Receive Side Network Interface

2.2.3.1 Analog-to-Digital Converter

The device incorporates an advanced high-speed ADC on the receive channel. Higher resolution ADC results in better SNR, and lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power-supply noise rejection, and low metastability error rate.

2.2.3.2 Analog Active Hybrid

The device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to be coupled to and share the twisted pair cable, which reduces the cost of the overall system.

2.2.3.3 Digital Echo Canceller

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The device employs a fully developed digital echo canceller to adjust for echo impairments from more than 15 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.2.3.4 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from the ADC output and uses a combination of feed-forward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise ratio (SNR).

2.2.3.5 Digital Phase-Locked Loop

In 100/1000BASE-T1 mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty resolving receive symbols due to unreliable synchronization; this results in higher bit error rates. In the device, an advanced digital phase-locked loop (DPLL) is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own which maximizes the achievable SNR.

2.2.3.6 Link Monitor

The link monitor is responsible for determining if a link is established with a link partner. In 100/1000BASE-T1 mode, link is established by scrambled idles.

2.2.4 Decoder

2.2.4.1 100/1000BASE-T1

In 100/1000BASE-T1 mode, the receive idle stream is analyzed so that the scrambler seed and the polarity of the pair can be accounted for. When calibrated, the PAM3 symbols are converted to 2-bit symbols, which are then descrambled and sent to the host side. If the descrambler loses lock due to excessive Reed-Solomon uncorrectable errors in 1000BASE-T1 or high CRC mismatch count in 100BASE-T1 mode, then the link is brought down and calibration is restarted.

2.3 MAC Interfaces

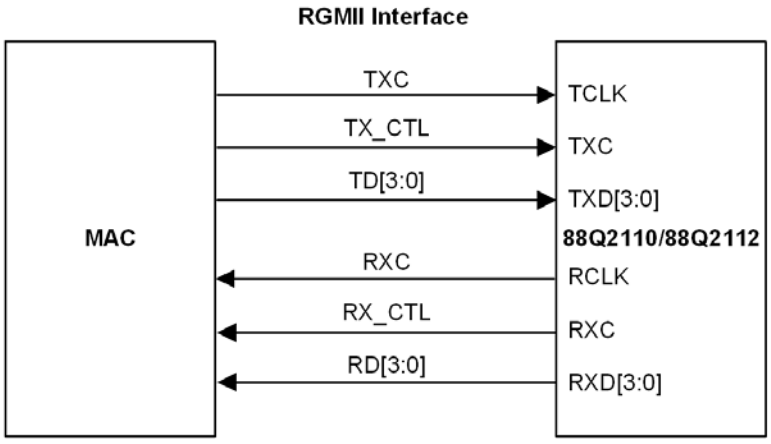
2.3.1 RGMII Interface

The device supports an RGMII interface. Four RGMII timing modes with different receive clock to data timing and transmit clock to data timing can be programmed by setting register 31.8001.15:14. For timing details, see Section 5.7.2, RGMII Delay Timing for Different RGMII Modes, on page 207.

Table 14: RGMII Signal Mapping

Device Pin Name	RGMII Specification Pin Name	Description
TCLK	TXC	25/125 MHz transmit clock with ±50 ppm tolerance.
TXC	TX_CTL	Transmit Control Signals. TX_EN is encoded on the rising edge of TCLK. TX_ER XOR'ed with TX_EN is encoded on the falling edge of TCLK.
TXD [3:0]	TD [3:0]	For 100BASE-T1 mode, TXD [3:0] are synchronous with the rising edge of TCLK. For 1000BASE-T1 mode, TXD [3:0] are synchronous with the rising and falling edge of TCLK.
RCLK	RXC	25/125 MHz receive clock derived from the received data stream.
RXC	RX_CTL	Receive Control Signals. RX_DV is encoded on the rising edge of RCLK. RX_ER XOR'ed with RX_DV is encoded on the falling edge of RCLK.
RXD [3:0]	RD [3:0]	For 100BASE-T1 mode, RXD [3:0] are synchronous with the rising edge of RCLK. For 1000BASE-T1 mode, RXD [3:0] are synchronous with the rising and falling edge of RCLK.

Figure 5: RGMII Signal Diagram



2.3.2 SGMII Interface

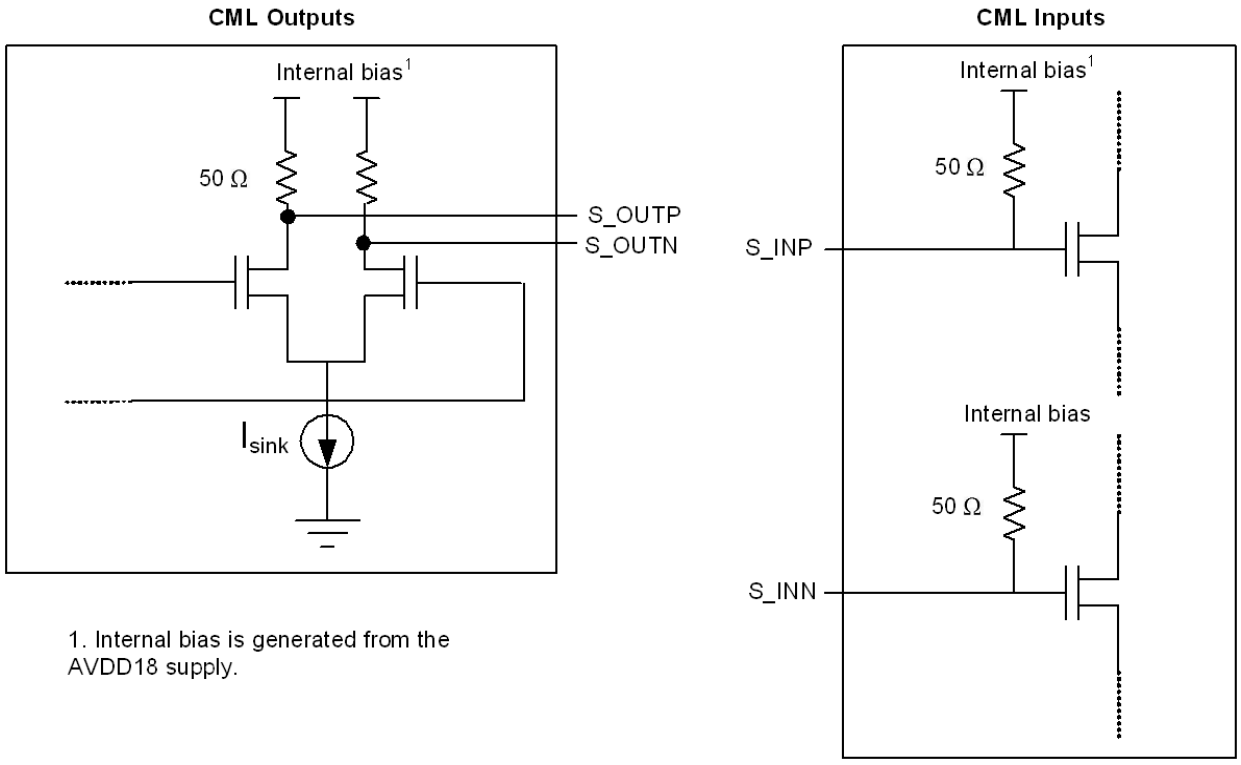
The device supports the SGMII specification revision 1.8, except for the carrier extension block that must be carried out in software. This interface supports 100BASE-T1 and 1000BASE-T1 modes of operation.

2.3.2.1 1.25 GHz SERDES Interface

The 1.25 GHz SERDES interface can be configured as an SGMII to be hooked up to a MAC.

The input and output buffers of the 1.25 GHz SERDES interface are internally terminated by 50Ω impedance. No external terminations are required. The output swing can be adjusted by programming register 4.801A.2:0. The 1.25 GHz SERDES I/Os are current mode logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os.

Figure 6: CML I/Os



1. Internal bias is generated from the AVDD18 supply.

2.3.2.2 SGMII Speed and Link

Two registers are available to determine whether the SGMII achieved link and sync. Status Register 4.8011.5 indicates that the SERDES locked onto the incoming KDKDKD… sequence. Register 4.8011.10 indicates whether a link is established on the SERDES. If SGMII Auto-Negotiation is disabled, then register 4.8011.10 has the same meaning as register 4.8011.5. If SGMII Auto-Negotiation is enabled, then register 4.8011.10 indicates whether SGMII Auto-Negotiation successfully established the link.

2.3.2.3 SGMII TRR Blocking

When the SGMII receives a packet with odd number of bytes, a single symbol of carrier extension will be passed on and transmitted onto 1000BASE-T1. This carrier extension may cause problems with full-duplex MACs that incorrectly handle the carrier extension symbols. When register 4.8010.13 is set to 1, all carrier extend and carrier extend with error symbols received by the SGMII will be converted to idle symbols when operating in full duplex. Carrier extend and carrier extend with error symbols will not be blocked when operating in half duplex or if register 4.8010.13 is set to 0. Symbol errors will continue to be propagated regardless of the setting of register 4.8010.13.

2.3.3 Tx Disable Feature

The device supports a Tx Disable feature (TX_ENABLE pin). If the pin input is LOW, then Tx packets will be stopped after link up, but Rx packets are still received normally. The link will stay up and only idles will be sent out the Tx media side. There is an internal pull-up, which will disable this feature if the pin is left floating. A HIGH value from the pull-up or if driven externally will allow packets to flow by default.

To disable this feature completely and use this pin for LED or GPIO functions, write register 3.8000.3 = 0. This will change the pin to an output and the link status will light up the LED without additional programming. For the register description, see Table 63, Reset and Control Register, on page 91.

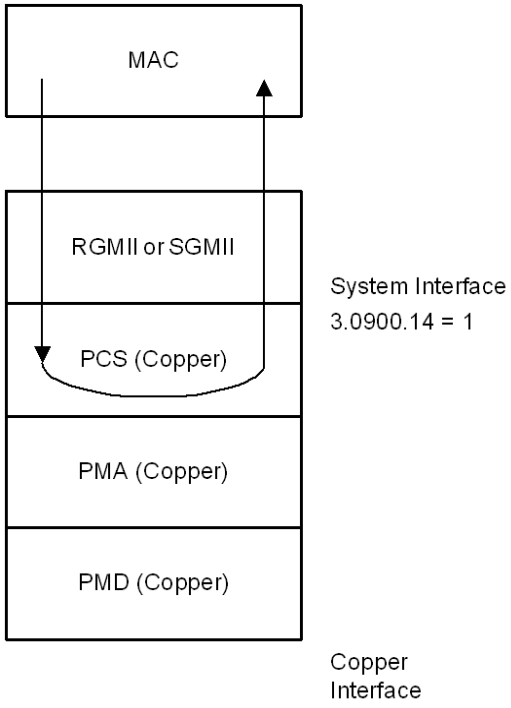
2.4 Loopback

The device implements various different loopback paths.

2.4.1 System Interface Loopback

The functionality, timing, and signal integrity of the system interface can be tested by placing the device in system interface loopback mode. This can be accomplished by setting register 3.0900.14 = 1.

Figure 7: MAC Interface Loopback Diagram — Copper Media Interface

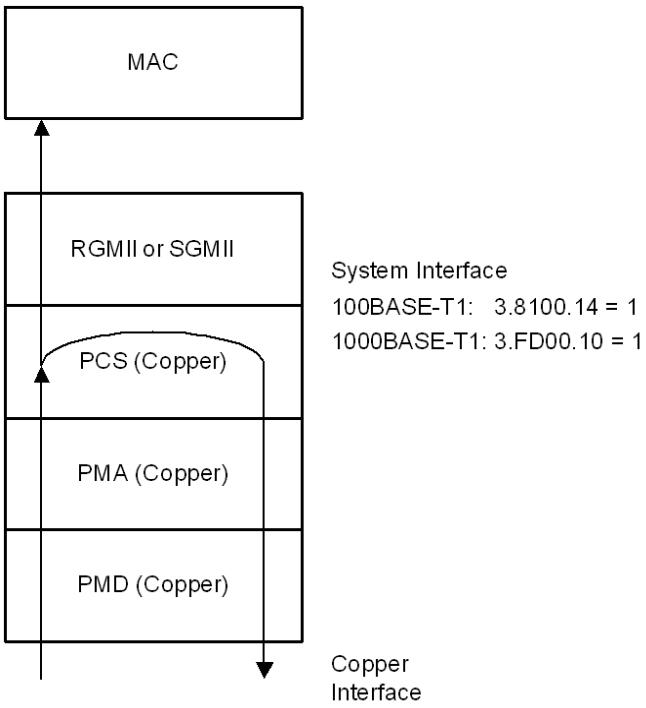


2.4.2 Line Loopback

Line loopback allows a link partner to send frames into the device to test the transmit and receive data path. Frames from a link partner received by the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish a link to another PHY link partner. When the link is established, the line loopback mode can be enabled. In 100BASE-T1 mode, register 3.8100.14 = 1 enables the line loopback on the copper interface; in 1000BASE-T1 mode, it is register 3.FD00.10 = 1.

Figure 8: Copper Line Loopback Data Path

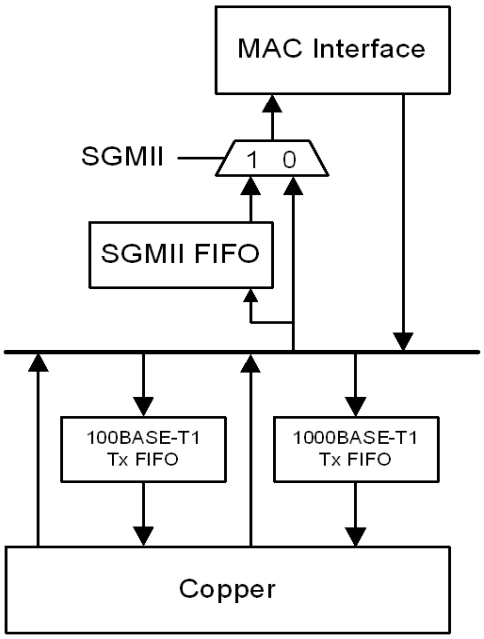


2.5 Synchronizing FIFO

The device has transmit synchronizing FIFOs to reconcile frequency differences between the clocks of the MAC interface and the media side. There are three FIFOs on the paths of the copper and SGMII, as shown in Figure 9. The depth of the FIFOs can be independently programmed by programming register bits 3.8210.15:14 (for 100BASE-T1) or register bits 4.8010.15:14 (for SGMII FIFO) and 3.FD20.1:0 (for 1000BASE-T1). The default Tx FIFO depth setting for all three FIFOs is 01.

The FIFO depths can be increased in length to support longer frames. The device can handle jumbo frame sizes up to 25 KB with up to ±100 ppm clock jitter for SGMII. The deeper the FIFO depth is, the higher the latency will be.

Figure 9: FIFO Locations



The SGMII FIFO status bits can generate interrupt on the register bit 4.8013.7 with an enable bit in 4.8012.7. The 100BASE-T1 FIFO status can generate an interrupt on the register bit 3.8213.7 with an enable bit in 3.8212.7. The 1000BASE-T1 FIFO status for either underflow or overflow are reported in 3.0008.11.

2.6 Resets

In addition to the hardware reset pin (RESETn), there are several software reset bits as summarized in Table 15.

The copper circuit is reset via any of the registers 1.0900.15, 3.0900.15, or 7.0200.15. The SGMII circuit is reset via register 4.8000.15. The RGMII circuit is reset via register 3.8000.15. The reset in one circuit does not directly affect another circuit.

All reset registers except RGMII are self-clear.

Table 15: Reset Control Bits

Reset Register	Register Effect	Functional Block
1.0900.15	Software Reset for Registers in Device 1	Copper
3.0900.15	Software Reset for Registers in Device 3	Copper
3.8000.15	Software Reset for Registers in Device 3	RGMII
7.0200.15	Software Reset for Registers in Device 7	Copper
4.8000.15	Software Reset for Registers in Device 4	SGMII

2.7 Power Management

The device supports several advanced power management modes that conserve power.

2.7.1 Low Power Modes

The following two low power modes are supported in the device:

- IEEE Compliance Power Down mode
- Low Power Signal Detect

2.7.1.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 1.0900.11 or 3.0000.11. In this mode, the PHY does not respond to any system interface (that is, RGMII/SGMII) signals except the MDC/MDIO. It also does not respond to any activity on the copper media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 1.0900.11 and 3.0000.11= 0.

The automatic PHY power management can be overridden by setting the power down control bits. These bits have priority over the PHY power management in that the circuit can not be powered up by the power management when its associated power down bit is set to 1. When a circuit is power back up by setting the bit to 0, a software reset is also automatically sent to the corresponding circuit.

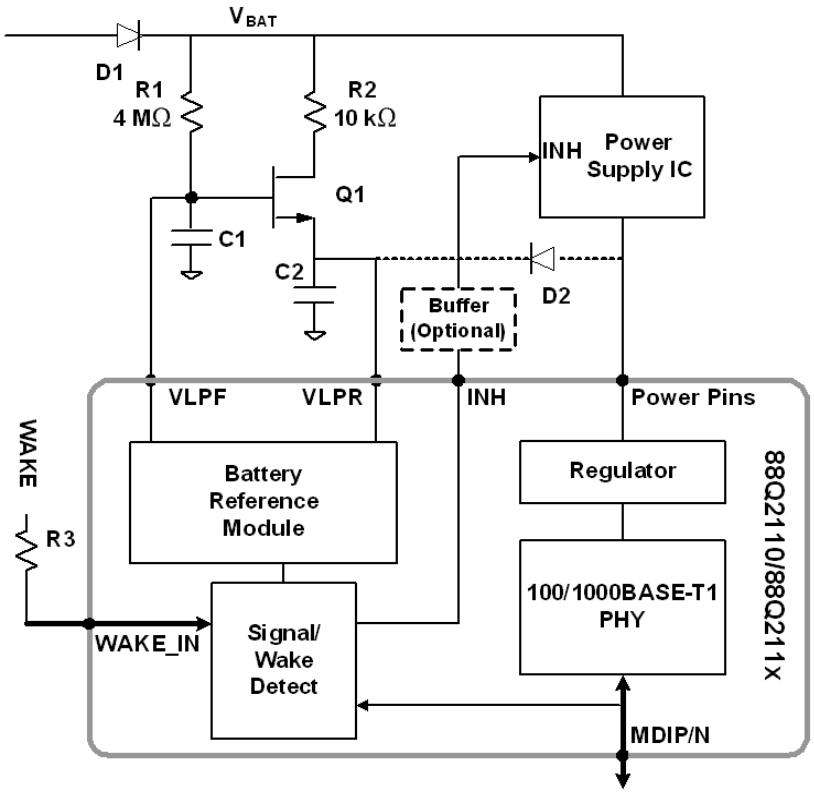
Table 16: Power Down Control Bits

Reset Register	Register Effect
1.0900.11	Copper Power Down
3.0000.11	Copper Power Down

2.7.1.2 Low Power Signal Detect Mode

The device can operate in a low power sleep mode with minimal standby current from the battery voltage with the main supply shut off. During this mode, the device can continuously monitor for line activity (remote wake) or a pulse at the WAKE_IN pin to trigger device wake up. The Low Power Signal Detect is enabled by default.

Figure 10: LPSD Block Diagram



Recommended components:

Q1: 2N7002 (NFET)

D2: Optional. Only if need to support active device with no battery voltage.

C1/C2: 1 nF

R3: 50 kΩ

Electrical Characteristics

Table 17: LPSD Electrical Characteristics

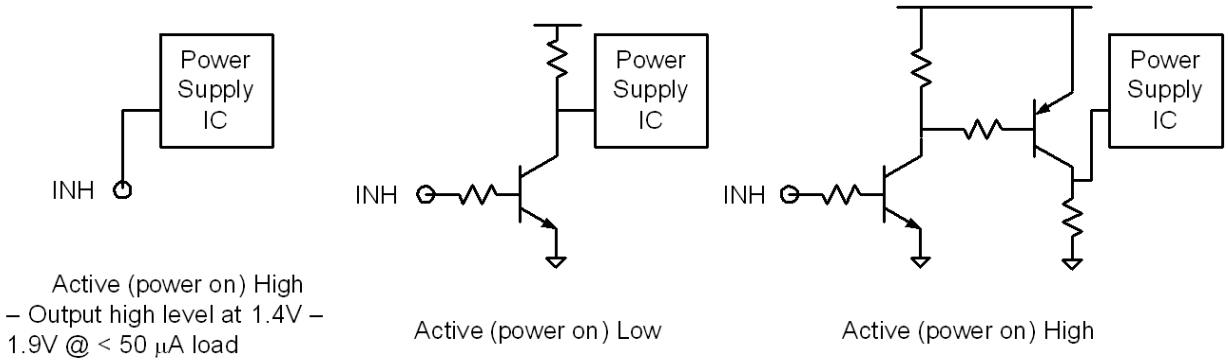
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BAT}	Battery Voltage	–	6	12	28	V
$I_{STANDBY}$	Standby Current	Battery voltage = 12V	–	–	50	µA
$T_{MDI,LAT}$	Latency from MDI Signals to INH Assertion	Normal link	–	–	20	µs
$T_{WAKE,PW}$	WAKE_IN Pin Pulse Width to Wake-up	–	10[1]	–	–	µs
I_{INH}	INH Pin Source Current	–	–	–	50	µA
V_{INH}	INH Pin Output High Voltage	–	1.4	–	1.9	V

1. = Default value.

Application Notes

- WAKE bus voltage
  a) If WAKE bus is running on 3.3V supply, then WAKE bus direct hooks up to WAKE_IN pin is OK.
  b) If WAKE bus is running on battery supply, then an external series 50 kΩ resistor is required to drive WAKE_IN pin.
- INH output
  Power supply IC EN/INH pin can be driven by 88Q2110/88Q2112 INH pin in typical cases. For higher voltage and current requirements, external buffer may be added.
  a) If Power Supply IC EN input VIH <1.4V and load current <50 μA, then INH pin can directly connect to Power Supply IC.
  b) Otherwise, external buffer components are required.
  For example configurations, see Figure 11.
  c) If an on-chip regulator not used, then INH output must control EN input of all power supply ICs that power the device.

Figure 11: INH Output Example Configurations



- Wake-up application scenarios – the following four cases of wake-up schemes can be supported:
  - Case 1: Local wake-up and remote wake-up.
    WAKE_IN from host controller. 3.3V or VBAT level can be accepted.
    For VLPR, VLPF, and INH, see Figure 10, LPSD Block Diagram, on page 41.
  - Case 2: No local wake-up. Remote wake-up support.
    WAKE_IN = VSS. For VLPR, VLPF, and INH, see Figure 10.
    Or use case 1 configuration, but use registers to program.
  - Case 3: Local wake-up only. No remote wake-up.
    Use case 1 configuration. Use register program to disable remote wake-up.
  - Case 4: No local wake-up. No remote wake-up.
    WAKE_IN = VSS or NC. VLPR, VLPF, and INH = NC.

2.8 Auto-Negotiation

The optional Auto-Negotiation is based on Clause 98 of the IEEE 802.3 specification. It is used to negotiate speed and master/slave.

Auto-Negotiation is disabled by default, it can be enabled via register 7.0200.12. When Auto-Negotiation is disabled, the speed defaults to strapped value on RXD [3] pin. When Auto-Negotiation is enabled, the abilities that are advertised can be changed via registers 7.0202 to 7.0204. Changes to these registers do not take effect unless one of the following occurs:

- There is a software reset (1.0900.15, 3.0000.15, or 7.0200.15).
- A Restart Auto-Negotiation is asserted (7.0200.9).
- There is a transition from power down to power up (1.0900.11 or 3.0000.11).
- The Auto-Negotiation Enable bit toggles (7.0200.12).
- The copper link goes down.

Registers 7.0202 to 7.0204 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. So, a write to registers 7.0202 to 7.0204 has no affect when the PHY begins to transmit differential Manchester encoding (DME) pages. This guarantees that sequences of DME pages transmitted are consistent with one another.

If additional next pages are not required, then the next page bit (7.0202.15) can be set to 0 (default) and no further action is required by the user. When a link partner indicates a next page will be sent, where 7.020B.15 = 1, a null next page (IEEE 802.3 Annex 98C) is automatically generated and sent back to the link partner. If next pages are required, then the user can set register 7.0202.15 to 1. Additional next pages can be transmitted and received via registers 7.0208 to 7.020A and 7.021B to 7.021D, respectively.

When the PHY completes Auto-Negotiation, it updates the various status in registers 7.0201 and 7.0205 to 7.0207.

2.9 Advanced Virtual Cable Tester

The device's Advanced VCT feature uses time domain reflectometry (TDR) to determine the quality of the cables, shorts, cable impedance mismatch, bad connectors, and termination mismatch. The device transmits a signal of known amplitude (+1V) down the single pair of an attached cable. It will conduct the cable diagnostic test on MDIP/MDIN. The transmitted signal will continue down the cable until it reflects off of a cable imperfection.

2.9.1 VCT Configuration

The VCT test is configured by setting the following register bits:

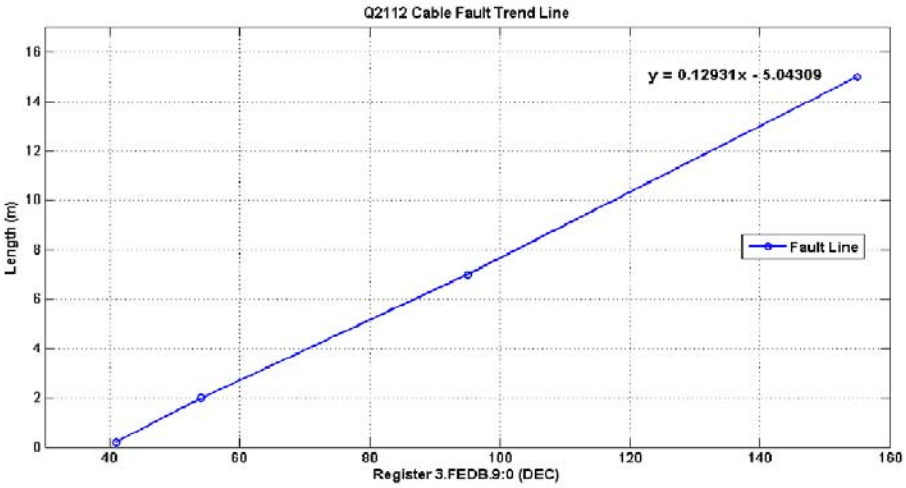
- VCT Startup Routine
  - Register 3.FEC9 bit 7 to 1 (Ignore wire activity).
  - Register 3.FEC3 bit 13 to 1 (Fix incoming ADC sign bit).
  - Register 3.FEC4 = 0x0F20 (Adjust threshold).
  - Register 3.FEC7 = 0x1219 (Adjust threshold).
  - Register 3.FEC3 bit 14 to 1 (Enable TDR function, Self-clear Register).
- Reading Results
  - Read register 3.FEDB [10] set to 1 when VCT data is ready.
  - Read register 3.FEDB [9:0] VCT distance.
  - Read register 3.FEDC [7] Polarity.
  - Read register 3.FEDC [6:0] VCT Amplitude.
- Cable Status
  - Polarity = 1, amplitude equal to 0, cable is terminated.
  - Polarity = 1, amplitude not equal to 0, cable is open.
  - Polarity = 0, amplitude not equal to 0, cable is short.

Finally, the VCT test is initiated by setting register 3.FEC3 bit 14 to 1. Register 3.FEDB bit 10 will be set to 1 indicating that the TDR test is over and the results in the registers are valid. Each time the VCT test is enabled, the results seen on the single channel are reported in register 3.FEDB bits [9:0], which indicate the distance of the peak.

2.9.2 Maximum Peak

The Maximum Peak method is used for TDR testing. For this method, the maximum peak above a certain threshold is reported. Pulses are sent out. Register 3.FEDB bits 9:0 reports the distance of the peak. The distance can be converted using the trend line in Figure 12. The equation used for conversion is y = 0.12931x-5.04309; plug the value of 3.FEDB bits 9:0 converted to decimal into the equation to get the distance in meters.

Figure 12: TDR Trend Line



Register 3.FEDC bits 6:0 report the reflected amplitude, bit 7 reports whether the reflected amplitude was positive or negative. When bits 7:0 of 3.FEDC return a value of 0x80, it means there was no peak detected above the threshold. If bits 7:0 return a value of 0x00, then the test failed. If 3.FEDC bit 7 is 1, then the cable is open, other if 3.FEDC bit 7 is 0, indicating that the cable is shorted.

2.9.3 Pulse Amplitude and Pulse Width

The transmitted pulse amplitude and pulse width can be adjusted via register 3.FEC3 bits 11 to 7 and register 3.FEC3 bits 1 to 0, respectively. These bits should be set to full amplitude and full pulse width.

2.10 Packet Generator and Packet Checker

2.10.1 CRC Error Counter and Frame Counter

The cyclic redundancy check (CRC) counter and packet counters that are normally found in MACs are available in the device. The error counter and packet counter features are enabled through register writes, and each counter is stored in eight register bits.

To enable the packet counter in two different write commands, first enable the counter 3.FD07.0 and then start the count sequence via 3.FD07.2.

To read the CRC counter and packet counter, read register 3.FD08:

- 3.FD08.7:0 (Frame count is stored in these bits)
- 3.FD08.15:8 (CRC error count is stored in these bits)

The CRC counter and packet counter do not clear on a read command. To clear the counters, write register 3.FD07. 3 = 1 (this bit is a self-clear bit). Disabling the counters by writing register 3.FD07.2 = 0 will also reset the counters.

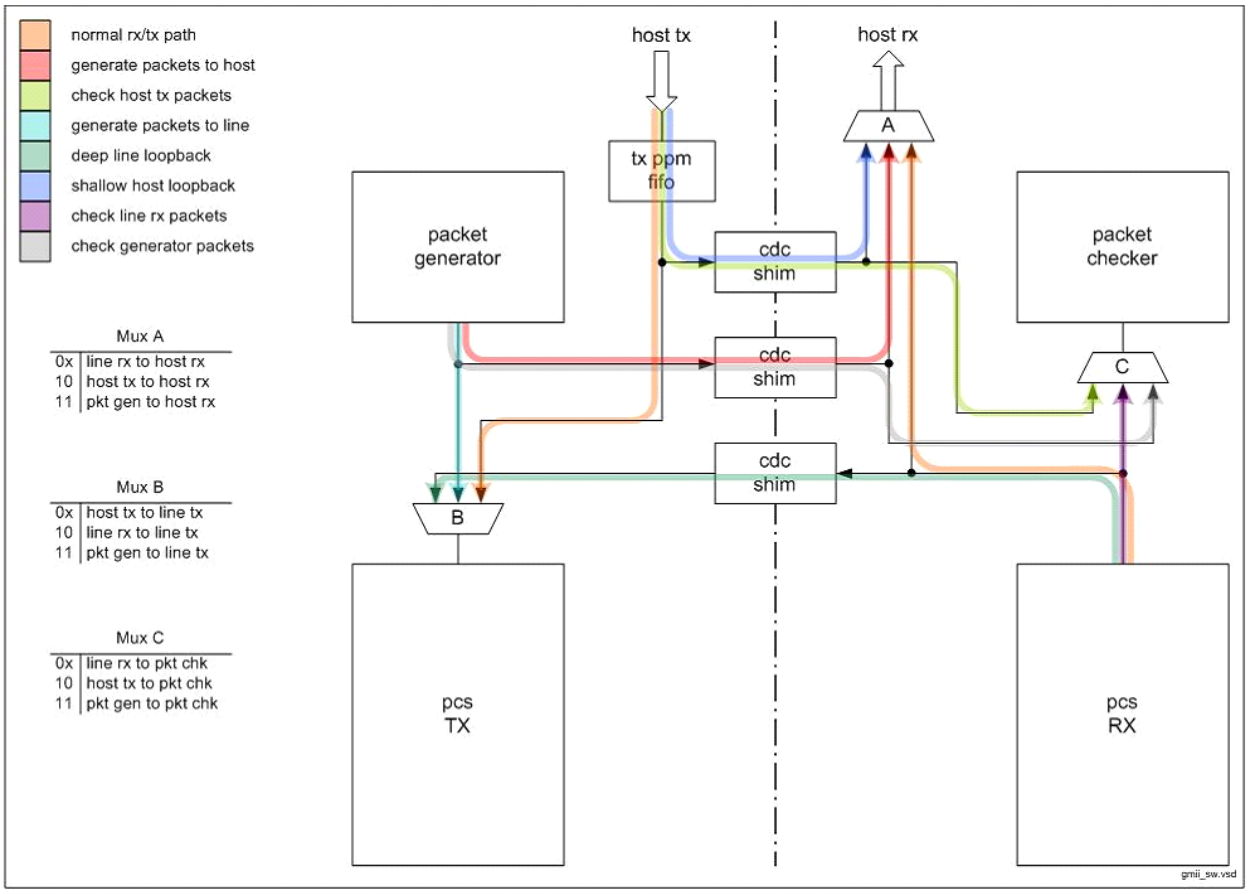
2.10.2 GMII Data Steering

The copper unit in the device includes a data steering module that allows packet generator and checker to be connected to multiple sources or destinations. The same module is also used to perform data loopback operation.

There are three sources for line data output: host GMII input, internal packet generation, and line data input also known as deep line loopback. Similarly, there are three sources for host GMII output: line data input, internal packet generation, and host GMII input also known as shallow host loopback. In addition, there is an internal packet checker as described in Section 2.10.1, which has three sources: host GMII input, internal packet generation, and line data input. Each of these selections can be independently controlled. The controls of these multiplexers must be set up for packet generator and checker before enabling the blocks. The register controls are located in 3.FD00.12:6.

A MAC loopback path should be implemented, where the output of the FIFO is looped back to the GMII Rx. Register 3.0900.14 will overwrite the multiplexer that controls this loopback path.

Figure 13: Data Steering around GMII Interface



2.10.3 Packet Generator

The device contains a very simple packet generator. Write to register 3.FD04.3 to enable the packet generator.

When enabled, fixed length packets of 64 or 1518 bytes (including CRC) will be transmitted, separated by 12 bytes of inter-packet gap (IPG).The preamble length will be 8 bytes. The payload of the packet is either a fixed 5A, A5, 5A, A5, or pseudo-random pattern. A correct IEEE CRC is appended to the end of the packet. An error packet can also be generated.

The registers are as follows:

- 3.FD04.2 Payload Type
  - 0 = Pseudo-random
  - 1 = Fixed 5A, A5, 5A, A5, and so on
- 3.FD04.1 Packet Length
  - 0 = 64 bytes
  - 1 = 1518 bytes
- 3.FD04.0 Error Packet
  - 0 = Good CRC
  - 1 = Symbol error and corrupt CRC

- 3.FD04.15:8 Packet Burst Size
  - 0x00 = Continuous
  - 0x01 to 0xFF = Burst 1 to 255 packets

2.11 Automatic Polarity Detection and Correction

The device automatically corrects polarity errors on the receive pairs in 1000BASE-T1 mode.

On the receive side, receive polarity inversion are automatically corrected based on the sequence of idle symbols. When the descrambler is locked, the symbol lock is found and the polarity is also locked based on the incoming data. The polarity becomes unlocked only when the receiver loses lock.

If 1000BASE-T1 link is established, then register 1.0900.2 records the real-time status of the polarity.

1.0900.1 Polarity (real time)

- 1 = Reversed
- 0 = Normal

When configured as a slave in 100BASE-T1 mode, the device has the capability to automatically detect an correct the polarity on the receive side when a polarity swap is observed. When a polarity flip is observed, it will also invert the polarity on the transmit side.

The feature is disabled by default can be enabled by programming register 3.8100.9 to 1.

If 100BASE-T1 link is established and automatic polarity detection and correction is enabled, the register 3.8109.1 records the real-time status of the polarity.

3.8109.1 Polarity (real time)

- 1 = Reversed
- 0 = Normal

2.12 DME Pages Exchange Complete with No Link

Auto-Negotiation uses the DME scheme. Sometimes when the link does not come up, it is difficult to determine whether the failure is due to incomplete DME exchanges or the 1000BASE-T1 link is unable to come up.

Register 7.8001.15 is a sticky bit that gets set to 1 whenever the Auto-Negotiation exchange is completed, but master/slave does not resolve or a link cannot be established. When the bit is set, it can be cleared only by reading the register.

This bit will not be set if the DME pages exchange is not completed or if link is established.

2.13 GPIO

The GPIO and TX_ENABLE pins can be used for GPIO functionality. Registers 3.8010 to 3.8015 control the operation of the GPIO/TX_ENABLE pins. Registers 3.8013.3 and 3.8014.3 are used to program the TX_ENABLE pin for GPIO functionality. To use the TX_ENABLE pin for a GPIO function, 3.8013.3 should be 0, while 3.8104.3 should be written to 1. Register bits 3.8013.0 and 3.8013.1 control the direction of these pins. When they are programmed to 0, these pins are used as input pins. Otherwise, these are used as output pins.

When the GPIO/TX_ENABLE pins are in input mode, the register bits 3.8012.1:0 can be used to read the state of these pins. 3.8012.1 indicates the state of the TX_ENABLE pin and 3.8012.0 indicates the state of the GPIO pin. In input mode, an interrupt can also be generated depending on the value of the GPIO/TX_ENABLE pins. Registers 3.8014.10:8 and 3.8014.2:0 can be used to select when an interrupt should be generated. The interrupt status is stored in register 3.8011.1:0.

When the GPIO/TX_ENABLE pins are configured in output mode, register bits 3.8012.1:0 are used to drive the state of these pins. The value written to the 3.8012.1 register bit will be driven on the TX_ENABLE pin and the value written to the 3.8012.0 register bit will be driven on the GPIO pin. By default, the GPIO pin is programmed to be used for LED functionality.

2.14 LED

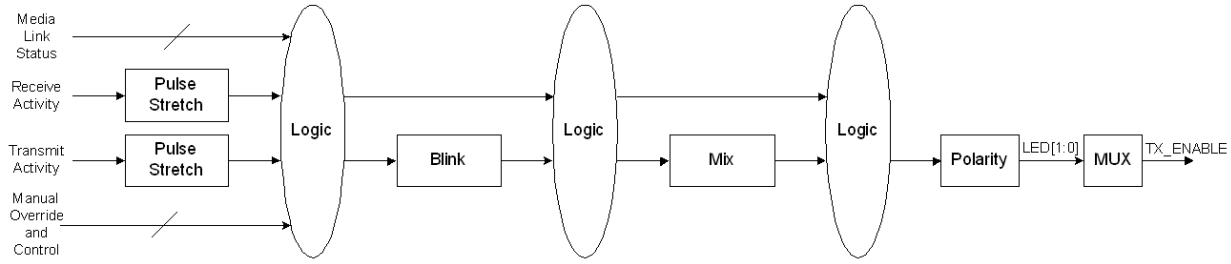
The TX_ENABLE and GPIO pins can be used to drive LED functionality. Registers 3.8013 to 3.8018 control the operation of the LEDs and by default, the GPIO pin is programmed for LED functionality. Registers 3.8014.7 and 3.8014.3 are used to configure internal bus LED [1:0] as shown in the diagram with the LED function and register bit 3.8013.3 is used to select which of the two LED signals of LED [1:0] are to be multiplexed onto the single TX_ENABLE pin. This arrangement of the LED will invalidate certain LED modes.

In general, 3.8016.7:4 controls the LED functionality for the GPIO pin and 3.8016.3:0 controls the LED functionality for the TX_ENABLE pin. These are referred to as single LED modes.

However, there are some LED modes where the GPIO and TX_ENABLE pins operate as a unit. These are entered when 3.8016.3:2 is set to 11. These are referred to as dual LED modes. In dual LED modes, register 3.8016.7:4 has no meaning when 3.8016.3:2 are set to 11.

Figure 14 shows the general chaining of function for the LEDs. The various functions are described in the following sections.

Figure 14: LED Chain

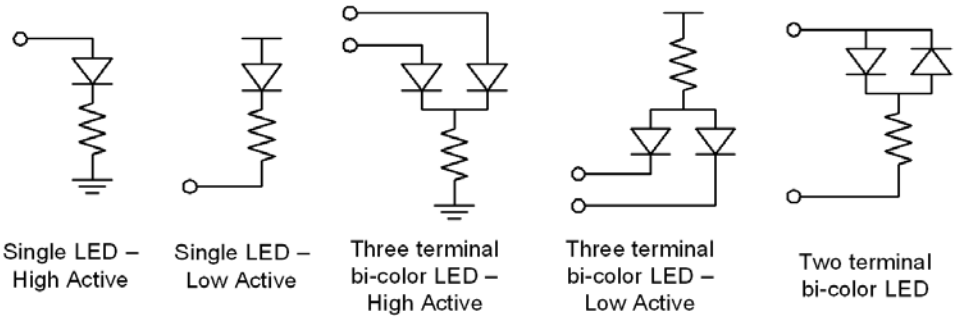


2.14.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 15. For optimal design flexibility, registers 3.8017.3:2 and 3.8017.1:0 specify the output polarity for the LEDs. The lower bit of each pair specifies the On (active) state of the LED, either high or low. The upper bit of each pair specifies whether the Off (inactive) state of the LED should be driven to the opposite level of the On state or Hi-Z.

For the register description, see Table 167, LED [1:0] Polarity Control Register, on page 133.

Figure 15: Various LED Hookup Configurations



2.14.2 Pulse Stretching and Blinking

Register 3.8018.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require a blinking state instead of a solid On state. Register 3.8018.10:8 specifies the blink rate. The pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

The stretched/blinked output will then be mixed if required (for details, see Section 2.14.3) and then inverted/Hi-Z according to the polarity described in Section 2.14.1.

For the register descriptions, see Table 168, LED Timer Control Register, on page 134.

2.14.3 Bi-Color LED Mixing

In the dual LED modes, mixing function allows the two colors of the LED to be mixed to form a third color. Register 3.8017.15:12 controls the amount to mix in the GPIO pin. Register 3.8017.10:8 controls the amount to mix in the TX_ENABLE pin. Mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

There are two types of bi-color LEDs: a three-terminal type and a two-terminal type. For example, the third and fourth LED block from the left in Figure 15 illustrate three-terminal types and the block on the far right is the two-terminal type. In the three-terminal type, both LEDs can be turned on at the same time. So the sum of the percentage specified by 3.8017.15:12 and 3.8017.10:8 can exceed 100%. However, in the two-terminal type, the sum should never exceed 100% since only one LED can be turned on at any given time.

Mixing only applies when register 3.8016.3:0 is set to 11xx. There is no mixing in single LED modes.

For the register descriptions, see Table 166, Function Control Register, on page 132 and Table 167, LED [1:0] Polarity Control Register, on page 133.

2.14.4 Modes of Operation

The TX_ENABLE pins relay some modes of the PHY so that these modes can be displayed by the LEDs. Most of the single LED modes are self-explanatory from the register map. The non-obvious modes are covered in this section.

For the description of the related registers, see Table 166, Function Control Register, on page 132 and Table 168, LED Timer Control Register, on page 134.

2.14.4.1 Compound LED Modes

Compound LED modes are defined in Table 18.

Table 18: Compound LED Status

Compound Mode	Description
Activity	Transmit Activity OR Receive Activity

2.14.4.2 Speed Blink

When 3.8016.3:0 is set to 0010, the TX_ENABLE pin assumes the following behavior.

The TX_ENABLE pin outputs the sequence shown in Table 19, depending on the status of the link. The sequence consists of eight segments. If a 100 Mbps link is established, then the TX_ENABLE pin outputs 2 pulses and no link 0 pulses. The sequence repeats over and over again indefinitely.

The odd numbered segment pulse duration is specified in register 3.8018.1:0. The even numbered pulse duration is specified in register 38018.3:2.

Table 19: Speed Blinking Sequence

Segment	1000 Mbps	No Link	Duration
1	On	Off	3.8018.1:0
2	Off	Off	3.8018.3:2
3	On	Off	3.8018.1:0
4	Off	Off	3.8018.3:2
5	Off	Off	3.8018.1:0
6	Off	Off	3.8018.3:2
7	Off	Off	3.8018.1:0
8	Off	Off	3.8018.3:2

Table 20: Speed Blink

Register	Pin	Definition
3.8018.3:2	Pulse Period for Even Segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
3.8018.1:0	Pulse Period for Odd Segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

2.14.4.3 Manual Override

When registers 3.8016.7:6 and 3.8016.3:2 are set to 10, the LEDs are manually forced. Registers 3.8016.5:4 and 3.8016.1:0 select whether the LEDs are on, off, Hi-Z, or blink.

If bi-color LEDs are used, then the manual override will select only one of the two colors. To get the third color, mixing MODE 1 and MODE 2 should be used (Section 2.14.4.4).

2.14.4.4 MODE 1, MODE 2, MODE 3, and MODE 4

MODE 1 through 4 are dual LED modes. These are used to mix to a third color using bi-color LEDs.

When 3.8016.3:0 is set to 11xx, then one of the four modes are enabled:

- MODE 1 – Solid mixed color.
  Mixing is discussed in Section 2.14.3.
- MODE 2 – Blinking mixed color.
  Mixing is discussed in Section 2.14.3 and blinking is discussed in Section 2.14.2.
- MODE 3 – Behavior according to Table 21.
- MODE 4 – Behavior according to Table 22.

Table 21: MODE 3 Behavior

Status	GPIO	TX_ENABLE
100 Mbps Link – No Activity	Solid Mix	Solid Mix
100 Mbps Link – Activity	Blink Mix	Blink Mix
No Link	Off	Off

Table 22: MODE 4 Behavior

Status	GPIO	TX_ENABLE
100 Mbps Link – No Activity	Solid On	Off
100 Mbps Link – Activity	Blink	Off
No Link	Off	Off

2.15 Synchronous Ethernet (SyncE) Clock

The GPIO pin can output a 125 MHz SyncE clock that can be used to clock other digital logic. This clock should not be used as an input to devices that require a higher quality clock.

Register 3.8004.0 is used to enable/disable the SyncE clock output on the GPIO pin. When 3.8004.0 is 1, the GPIO pin is used to output the SyncE clock. When 3.8004.0 is 0, the GPIO pin is used for GPIO/LED functionality. The default value of 3.8004.0 is 0 on power on, reset, or hardware reset.

2.15.1 Hardware Reset State

When hardware reset is asserted, the SyncE clock will not be output.

2.16 Interrupt

An interrupt function is brought out to the chip's INTn pin. Register 3.8018.11 selects the polarity of the interrupt signal when it is active, where 3.8018.11 = 1 means it is active low and 3.8018.11 = 0 means it is active high. Register 3.8013.11 = 1 disables the tri-state on the INTn pin allowing an interrupt to be routed to the pin.

The registers 3.8010 and 3.8011 are interrupt enabled and function for 1000BASE-T1 and other modes of operation. For a specific interrupt, refer to the following registers:

- Register 3.8112/3.8113: Interrupt enabled and function for specific 100BASE-T1 operations
- Register 3.8213/3.8214: Interrupt enabled and function for 100BASE-T1 MAC
- Register 4.8012/4.8013: Interrupt enabled and function for specific SGMII media

Registers 3.8010 and 3.8011 also contain the Interrupt Enable and the Interrupt Status registers for the GPIO pins (GPIO/LED).

There are force bits, polarity bits and tri-state control for the INTn pin. See Table 23 and Table 24.

Table 23: Interrupt Enable Bits

Register	Function
3.8018.15	Force interrupt.
3.8018.11	Set polarity.
3.8013.11	0 = The tri-state is enabled (This is the default state where the interrupt pin configured as an input). 1 = The tri-state is disabled (This setting is only for A0 or later).
3.8013.9	1 = Output is driven LOW for active interrupt and tri-stated when inactive.
3.8013.8	1 = Output is driven HIGH for active interrupt and tri-stated when inactive.

Table 24: Control Bit Interrupts

Register/Combination	Function
3.8013.9=1 and 3.8018.11=1	Output is driven LOW for active interrupt and tri-stated when inactive.
3.8013.9=0, 3.8013.8=1, and 3.8018.11=0	Output is driven HIGH for active interrupt and tri-stated when inactive.
3.8013.9=0, 3.8013.8=0, and 3.8018.11=1	Output is driven LOW for active interrupt and HIGH for inactive.
3.8013.9=0, 3.8013.8=0, and 3.8018.11=0	Output is driven HIGH for active interrupt and LOW for inactive.

2.17 Automatic and Manual Impedance Calibration

2.17.1 MAC Interface Calibration Circuit

Auto-calibration is available for the RGMII MAC interface I/Os. The PHY operates the automatic calibration circuit with a 47.3Ω impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the automatic calibration through register writes. Individual N-type metal-oxide semiconductor (NMOS) and P-type metal-oxide semiconductor (PMOS) output transistors can be controlled.

Manual NMOS and PMOS settings are available if the automatic calibration is not required. If the printed circuit board (PCB) traces are different from 47.3Ω, then the output impedance of the MAC interface I/O buffers can be programmed to match the trace impedance. Users can adjust the NMOS and PMOS driver output strengths to perfectly match the transmission line impedance and eliminate reflections completely.

For the description of the related register, see Table 180, RGMII Output Impedance Control Register, on page 139.

2.17.2 Changing Auto Calibration Targets

The PHY runs the automatic calibration circuit with a 47.3Ω impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes.

To change the auto calibration targets:

1. Write to register 31.8000.2:0 with the target impedance.
2. Write to register 31.8000.15 = 1 to restart the auto-calibration with the new target.

2.17.3 Manual Settings to the Calibration Registers

To use manual calibration, write to the following registers:

Write to register 31.8000.11:8 = b'PPPP and register 31.8000.7:4 = b'NNNN to adjust the PMOS and NMOS fingers accordingly, where

- PPPP is the 4-bit value for the PMOS strength.
- NNNN is the 4-bit value for the NMOS strength.

PPPP or NNNN will depend on the PCB used. A value of 1111 enables all the fingers for maximum drive strength and for minimum impedance. A value of 0000 turns all fingers off for minimum drive strength and maximum impedance. For an assessment of the auto-calibration required on a particular PCB, the RGMII pins at the destination can be monitored and depending on the signal integrity on the PCB, the auto-calibration values can be changed accordingly. For example, if the automatic calibration has a 47.3Ω target and the RGMII trace impedance on the board is 60Ω, then by monitoring the RCLK pin at the destination reflections can be noticed. This is shown in Figure 16. Through manual calibration, the reflections can be eliminated as shown in Figure 17.

Figure 16: Signal Reflections Using the 50Ω Setting, 60Ω Line

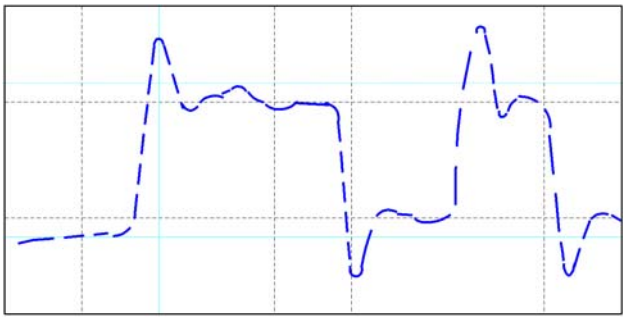
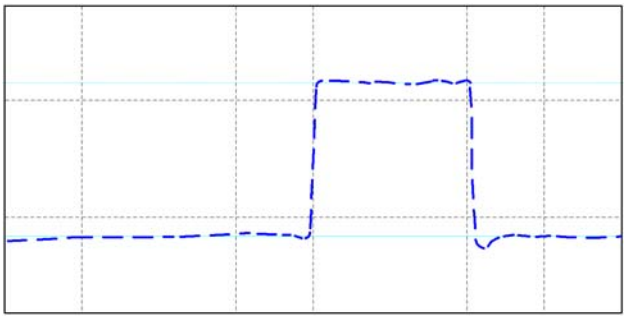


Figure 17: Clean Signal after Manual Calibration of the 60Ω Line



2.18 Configuring the 88Q2110/88Q2112

The device can be configured in two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

The master/slave configuration settings can be overwritten by software. RGMII/SGMII mode settings can also be overwritten by software, but PHYAD configuration settings cannot be overwritten.

2.18.1 Hardware Configuration

The RXC, RXD [3:0], and GPIO pins are used as configuration pins. When RESETn is low, GPIO, RXC, and RXD [3:0] are set as inputs and the internal pull ups are activated. If an external pull-down resistor is attached to the pin, then the input will be low; otherwise the input will be high. GPIO, RXC, and RXD [3:0] are sampled on the de-assertion of RESETn. After sampling is completed, the internal pull ups are disabled and the pins are set to outputs.

Table 25 shows how the sampled values are used.

Table 25: Sampled Values

Pin Name	88Q2110	88Q2112
GPIO	PHYAD [2]	PHYAD [2]
RXD [1]	PHYAD [1]	PHYAD [1]
RXD [0]	PHYAD [0]	PHYAD [0]
RXD [3] RXD [2]	RXD [3:2] 00 = 100BASE-T1, Master 01 = 100BASE-T1, Slave 10 = 1000BASE-T1, Master 11 = 1000BASE-T1, Slave	RXD [3:2] 00 = 100BASE-T1, Master 01 = 100BASE-T1, Slave 10 = 1000BASE-T1, Master 11 = 1000BASE-T1, Slave
RXC	0 = RGMII Delay Tx and Rx clock 1 = RGMII Delay Rx clock	0 = RGMII Delay Tx and Rx clock 1 = SGMII

Master/slave configuration can be overwritten by register bit 7.0202.12.

The RXD [0], RXD [1], and GPIO pins are used to configure PHYAD [0], PHYAD [1], and PHYAD [2], respectively. For a PHYAD of 0, these pins should be left floating. To configure a 1 on the PHYAD [0]/PHYAD [1]/PHYAD [2] bits, the corresponding RXD/GPIO pins must have a pull-down resistor (4.7 kΩ) added to them externally. The mapping is shown in Table 26.

Table 26: {GPIO, RXD [1:0]} to PHYAD [2:0] Mapping for Configuration (Sheet 1 of 2)

GPIO Pin	RXD [1] Pin	RXD [0] Pin	PHYAD [2:0] Value
Unconnected	Unconnected	Unconnected	000
Unconnected	Unconnected	4.7 kΩ Pull-Down Resistor	001
Unconnected	4.7 kΩ Pull-Down Resistor	Unconnected	010
Unconnected	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	011
4.7 kΩ Pull-Down Resistor	Unconnected	Unconnected	100
4.7 kΩ Pull-Down Resistor	Unconnected	4.7 kΩ Pull-Down Resistor	101

Table 26: {GPIO, RXD [1:0]} to PHYAD [2:0] Mapping for Configuration (Sheet 2 of 2)

GPIO Pin	RXD [1] Pin	RXD [0] Pin	PHYAD [2:0] Value
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	Unconnected	110
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	111

2.18.2 Software Configuration — Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u Clause 45 MDIO protocol. MDC is the management data clock input and it can run from DC to a maximum rate of 12.5 MHz. At high MDIO fanouts, the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bidirectional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ that pulls the MDIO high during the idle and turnaround phases of read and write operations.

Bits 1 and 0 of the PHY address are configured during the hardware reset sequence. PHY address bits [4:2] are set to 000 internally in the device. For detailed configuration information, see Section 2.18.

2.18.2.1 Clause 45 Register Access

Typical read and write operations on the management interface are shown in Figure 18 and Figure 19. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in Section 3, General Registers, on page 83.

Figure 18: Typical MDC/MDIO Read Operation

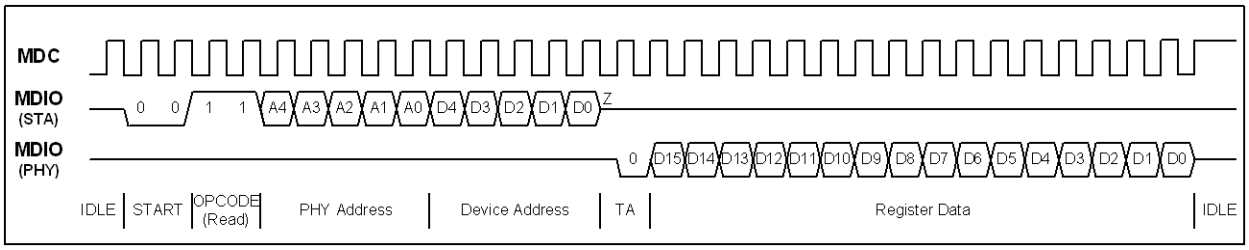
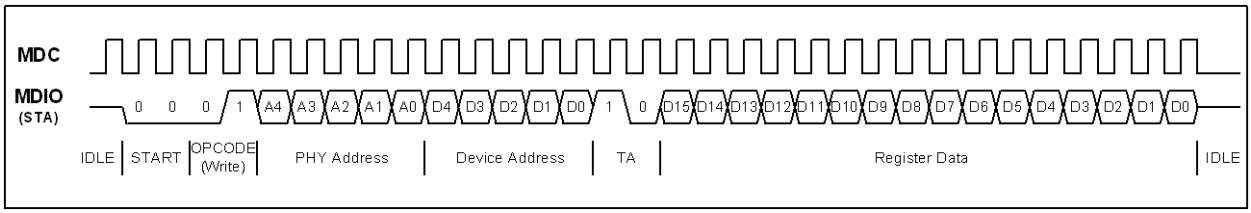


Figure 19: Typical MDC/MDIO Write Operation



The MDIO interface frame structure is compatible with the one defined in Clause 22 such that the two management interfaces can coexist on the same MDIO bus.

The extensions for Clause 45 MDIO indirect register accesses are specified in Table 27.

Table 27: Extensions for Management Frame Format for Indirect Access

Frame	PRE	ST	OP	PHYAD	DEVADR	TA	ADDRESS/DATA	Idle
Address	1...1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1...1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

The MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read-increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined.

Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

2.18.2.2 Clause 22 MDIO Register Access Method

The 88Q2110/88Q2112 supports Clause 22 MDIO manageable devices (MMD) extension registers to access Clause 45 MMD registers, using register 13 and 14 as specified in the IEEE Annex 22D.

Table 28: XMDIO MMD Control Register
Device 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0	0	11 = Data, post increments on writes only 10 = Data, post increment on reads and writes 01 = Data, no post increment 00 = Address
13:5	Reserved	RO	0	0	Reserved
4:0	DEVAD	R/W	0	0	Device Address

Table 29: XMDIO MMD Address Data Register
Device 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0	0	If 13.15:14 = 00, then MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register.

2.18.2.3 Preamble Suppression

The device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.19 Temperature Sensor

The device features an internal temperature sensor. The sensor reports the die temperature and is updated approximately once per second.

The temperature is obtained by reading the value in register 3.8043.7:0 and performing conversion functions as described in Table 30.

Table 30: Temperature Sensor

Register	Function	Setting	Mode	HW Rst	SW Rst
3.8043.7:0	Temperature Value	Temperature in °C = 3.8043.7:0 - 75, that is, for 100°C, the value is 1010_1111.	RO	xx	xx

To detect the high-temperature condition, the INTn pin must be asserted. Also, register bits 3.FE16.8 and 3.8010.11 must be enabled to allow the interrupt condition to propagate to the INTn pin.

2.20 Regulators and Power Supplies

The 88Q2110/88Q2112 devices have built-in regulators to support single rail operation from a 3.3V source. These internal regulators generate 1.8V and 0.9V. The integrated regulators greatly reduce the PCB BOM cost. If regulators are not used, then an external 1.8V and 0.9V supply are needed. The following tables list the valid combinations of regulator usage.

The VDDO supply can operate at 1.8V/2.5V/3.3V supplies.

Note

- If VDDO is tied to either 1.8V or 2.5V, then the I/Os are not 3.3V tolerant.
- AVDD18 is tied to 1.8V, so the XTAL_IN pin is not 2.5V/3.3V tolerant.

Table 31: Power Supply Options — Integrated Regulator (REG_IN)

Functional Description	AVDD33	AVDDC18/ AVDD18	DVDD	Setup
Supply Source	3.3V	1.8V from Internal Regulator	0.9V from Internal Regulator	Single 3.3V external supply Internal regulator enabled

Table 32: Power Supply Options — External Supplies

Functional Description	AVDD33	AVDDC18/ AVDD18	DVDD	Setup
Supply Source	3.3V	1.8V from External	0.9V from External	3.3V, 1.8V, and 0.9V external supplies Internal regulator disabled.

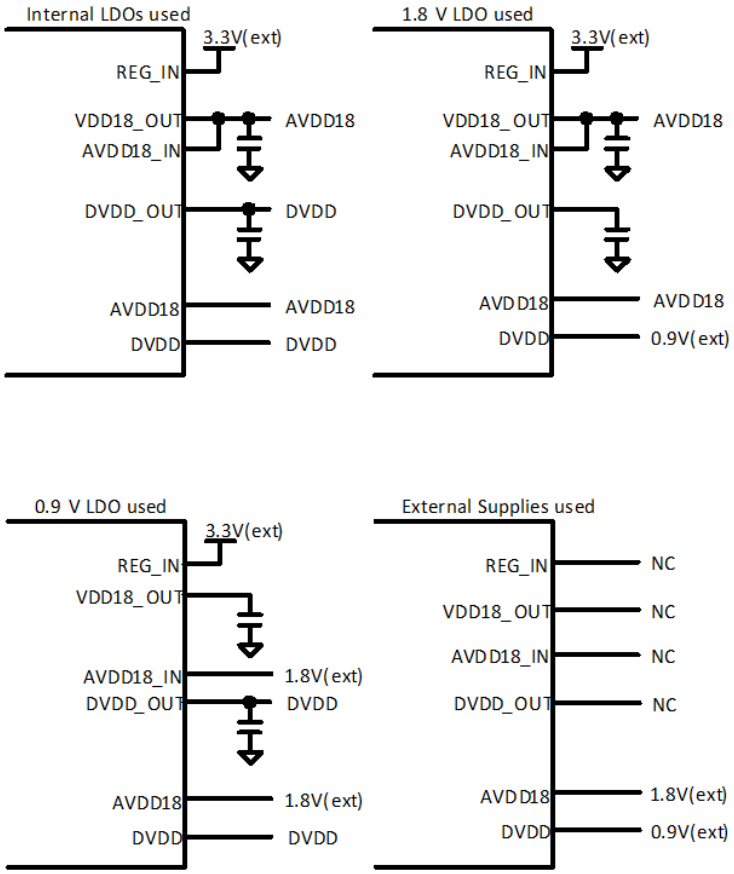
Table 33: Power Supply Options — External 0.9V, Integrated Regulator (REG_IN) Supplies Only 1.8V

Functional Description	AVDD33	AVDDC18/ AVDD18	DVDD	Setup
Supply Source	3.3V	1.8V from Internal Regulator	0.9V from External	Internal regulator enabled but only for 1.8V. 0.9V supplied externally: VDD33 supplied, VDD18_OUT connects to AVDD18_IN and AVDD18. DVDD_OUT is not connected to DVDD and must supply DVDD with bypass capacitors externally.

Table 34: Power Supply Options — External 1.8V to AVDD18 and AVDD18_IN, Integrated Regulator (AVDD18_IN) Supplies DVDD Only

Functional Description	AVDD33	AVDDC18/ AVDD18	DVDD	Setup
Supply Source	3.3V	AVDD18 and AVDD18_IN externally supplied.	DVDD from internal regulator (sourced from AVDD18_IN)	VDD33 supplied externally. Internal regulator enabled but only for DVDD. 1.8V supplied externally to AVDD18 and AVDD18_IN. VDD18_OUT is not connected to AVDD18_IN and AVDD18, but it is still required to have bypass capacitors. DVDD_OUT is connected to DVDD supplies pins. Decoupling capacitors for each DVDD pins and DVDD_OUT are required.

Figure 20: Supply and Regulator Connection Options



Note

- If the dual LDO option is used, then supply ramp requirements must be met. Refer to Figure 27, Dual LDO Startup Timing in the electrical section.
- If the single LDO option is used (DVDD by LDO from AVDD18_IN), then refer to Figure 28, Single LDO Startup Timing (DVDD by LDO from AVDD18_IN).

2.20.1 AVDD18

AVDD18 is used as the 1.8V analog supply.

It is used as a 1.8V analog supply for the XTAL_IN/OUT pins. AVDD18 can be supplied externally with 1.8V or via the 1.8V regulator.

2.20.2 AVDD18_IN

AVDD18_IN is the internal regulator 1.8V input and is a supply for the DVDD regulator. For details, refer to Figure 20, Supply and Regulator Connection Options.

2.20.3 AVDD33

AVDD33 is used as a 3.3V analog supply.

2.20.4 DVDD

DVDD is used as the 0.9V digital supply. DVDD can be supplied externally with 0.9V, or via the internal 0.9V regulator.

2.20.5 REG_IN

REG_IN is used as the 3.3V supply to the internal regulator that generates the 1.8V for AVDD18 and 0.9V for DVDD. If both the 1.8V and 0.9V regulators are not used, then REG_IN must be left floating.

2.20.6 VDD18_OUT

VDD18_OUT is the internal regulator 1.8V output. For details, refer to Figure 20, Supply and Regulator Connection Options. If 1.8V internal regulator is used, then this must be connected to 1.8V power plane that connects to AVDD18.

2.20.7 DVDD_OUT

DVDD_OUT is the internal regulator 0.9V output. When 0.9V internal regulator is used, DVDD_OUT must be connected to the DVDD plane. For details, refer to Figure 20, Supply and Regulator Connection Options.

2.20.8 VDDO

VDDO supplies all digital I/O pins which use LVCMOS I/O standards. The supported voltages are 1.8V, 2.5V, or 3.3V. For VDDO 1.8V operation, the power can be supplied by the internal regulator. For operation in 2.5V mode, the user must set register 4.8214.15 to 1.

Note LEDs cannot be used for VDDO 1.8V operation.

2.20.9 Power Supply Sequencing

On power-up, no special power supply sequencing is required. If the all external supply option is used and internal LDOs are not used, then no special power sequencing is required.

If the dual LDO option is used, then supply ramp requirements must be met. Refer to Figure 27, Dual LDO Startup Timing in the electrical section. If the single LDO option is used (DVDD by LDO from AVDD18_IN), then refer to Figure 28, Single LDO Startup Timing (DVDD by LDO from AVDD18_IN).

2.21 Precision Time Protocol (PTP) Timestamping Support

PTP is used by IEEE specifications to determine the time of day for systems across a network. The IEEE specifications are IEEE 802.1AS, IEEE 1588 version 1[1], and IEEE 1588 version 2. The PTP protocol is typically used in audio video bridging (PTP) applications, or industrial and test automation applications.

The fundamental concept is to be able to timestamp the PTP frames with high precision as close to the physical wires as possible. As such, performing the timestamping in the PHY increases the accuracy compared to performing it in the MAC or higher layers since the MAC interface FIFOs can add up to ±2 bytes of uncertainty.

The PTP core in the device comprises two sub-cores: Packet Timestamping and Time Application Interface (TAI). The timestamping core supports timestamping of frame formats as defined in IEEE 802.1AS, IEEE 1588 version 1[1], and IEEE 1588 version 2 frames.

2.21.1 PTP Control

To support the PTP Timestamping function, the device has three pins that are global to the entire PHY:

- PTP Event Request input pin (the TX_ENABLE/GPIO[2] pin is used for this purpose)
- PTP Trigger Generate output pin (the TX_ENABLE/GPIO pin is used for this purpose)
- Interrupt pin

2.21.1.1 PTP Event Request

The PTP Event Request input pin can be configured to capture an external event (referred to as EventReq) and record the time at which the event occurred using the PTP Global Time Register (PTP Global Time Register – registers 4.8C1E and 4.8C0F). Users must program 4.87F0.7:4 to select whether TX_ENABLE or GPIO are used to enable this function. The definition of an external event is a low-to-high transition or a high-to-low transition on the TX_ENABLE/GPIO pin. Register 4.8C00 bit 13 (Event Phase) selects which transition (rising or falling) is used. The event time is captured in EventCapRegister (Event Capture Register – registers 4.8D01 and 4.8D02). This field is validated by the EventCapValid bit (TAI Global Configuration Register – register 4.8D00).

2.21.1.2 PTP Trigger Generate

The PTP Trigger Generate output pin is used to output an external signal (referred to as TrigGenResp) when the internal Time of Day counter matches a value programmed into a PHY register. When there is a match, this output will go from low to high or from high to low, based on register 4.8C00 bit 12 (TrigPhase). The TX_ENABLE or GPIO pin is used for this function. It is selected by setting register 4.87F0.7:4 selection. The trigger output can also be a pulse or a clock, depending on what is programmed in register 4.8C00, bit 1 (TrigMode).

2.21.1.3 PTP Control Register

The PTP circuit timestamps packets as they pass through the PHY. The register control to this function can be accessed via registers 4.88xx to 4.8Fxx. The PTP circuit can be powered down when it is not used via register 4.87F0.9. When register 4.87F0.9 is set to 1, registers 4.88xx to 4.8Fxx are not accessible since the entire circuit is powered down.

By default, register 4.87F0.9 is set to 1. It must be set to 0 to enable PTP.

1. IEEE 1588 version 1 frames must be converted into IEEE 1588 version 2 format for the PTP to process the frames. Hardware acceleration is not supported for IEEE 1588 version 1 frames.
2. Refer to Section 1.2.4, TX_ENABLE/GPIO/Interrupt Interface, on page 23 for details on TX_ENABLE/GPIO pin.

For the register descriptions, see Table 202, PTP Control Register 1, on page 154 (for 100BASE-T1) and Table 203, PTP Control Register 2, on page 155 (for 1000BASE-T1).

2.21.2 Packet Timestamping

2.21.2.1 Timestamping without Hardware Acceleration

The device supports two sets of hardware arrival timestamp registers to be able to capture two different PTP event messages' timestamp before the CPU reads the timestamp registers out of the device. For every incoming PTP message type, either PTPArr0Time (PTP Arrival 0 Time Registers – registers 4.880A and 4.880B) or PTPArr1Time (PTP Arrival 1 Time Registers – registers 4.881D and 4.881E) can be chosen by configuring TSArrPtr (PTP Global Configuration Register 2 – register 4.8E02). The SequenceID from the PTP Common header is captured as part of Arrival 0, Arrival 1, and/or Departure timestamp register sets, so the software can correlate the collected timestamps with the received or transmitted PTP event message. The hardware can be enabled to generate an interrupt upon capturing the timestamp information by writing a 0x1 to the interrupt enable register bits PTPArrIntEn (PTP Port Configuration Register 2 – register 4.8802) for incoming PTP event messages or PTPDepIntEn (PTP Port Configuration Register 2 – register 4.8802) for outgoing PTP event messages. In addition to generating an interrupt on the interrupt pin, an interrupt status (PTPArr0IntStatus, PTPArr1IntStatus, and PTPDepIntStatus) gets generated, which indicates if there were to be an error related to the timestamp register. The interrupt status gets set to 0x1 when the timestamp counter gets overwritten before the previous timestamp registers have been read out. The interrupt status gets set to a 0x2, when a timestamp could not be captured for a PTP event message because DisTSOverwrite (PTP Port Configuration Register – register 4.8800) is set to 0x1.

Given that the device registers are accessed in units of 16 bits, to retain the entire 32-bit timestamp and the associated error messages and the SequenceID for a given PTP frame, the hardware treats the Arrival 0 block registers (registers 4.8808 to 4.890B), Arrival 1 block registers (registers 4.880C, 4.881D, 4.881E, and 4.880F), and Departure block registers (registers 4.8900 to 4.8903) as a group and atomic operations are supported for these block of registers.

The device does not alter the contents of any PTP packet in either ingress or egress direction. Timestamping at the device level does not involve adding a timestamp to a packet or changing its CRC. It also does not involve the device looking at timestamps that are embedded within a packet. The PHY does not add any additional latency when the PTP function is enabled. The PHY only identifies that a packet is a PTP frame and records the enter and exit time. The PHY does this by parsing the packet for certain fields as described in sections to follow in this document. If the packet is identified as such a PTP packet, then the device loads the value of an internal "time of day counter" to a register showing the time for the first byte or SFD of the packet. The device then can inform the CPU or the PTP higher level firmware/software that such an event occurred by activating an interrupt pin. The CPU can then read the relevant registers to find out if the event was in the Rx or Tx direction and the value of the "time of day counter" when the event happened.

Using the previously described time information and following the PTP protocol, the CPU or higher level entity can then determine the offset in time of day between a Grand Master Clock and the SLAVE node, as well as the frequency difference between the Grand Master Clock and the SLAVE clock in case they are not frequency locked. These calculations are above the PHY level. The PHY provides full flexibility by allowing its time of day counter to be adjusted based on the CPU's calculations, as well as a totally new time of day value to be entered. The CPU can also use the time information provided by the PHY to create PTP packets that inform the link partners or the Grand Master when the packets had arrived or left the port in question.

The maximum jitter associated with capturing the timestamps collected by the logic is one TSClkPer (TAI Global Configuration Register 1 – register 4.8C01). There are inherent delay variations introduced in PHY layer pipelines both in receive and transmit direction, which add to the overall jitter of the timestamps collected by the hardware and frequency/phase computations done in PTP protocol software.

For achieving higher accuracies in terms of PTP, it is recommended that an external clock device is used to adjust the timestamping clock with the frequency/phase offset information computed in PTP protocol software. The frequency and/or phase adjusted clock can in turn be fed back into the device to be used by the timestamping logic.

2.21.2.2 Timestamping with Hardware Acceleration

Hardware acceleration is available and can be turned on to offload the CPU from processing timestamp information.

Without the hardware acceleration, PTP frames are detected and the timestamp information is extracted and placed in registers so there is no alteration of any frames. A CPU or a higher level entity must access the relevant registers to obtain the timestamp information.

With the hardware acceleration, timestamp information is inserted directly into the PTP frame before it is transmitted to the CPU. So the CPU can obtain the timestamp information when the frame is received and is not required to access registers. In this case, PTP frames are being modified and additional latency is introduced due to the frame buffering and timestamp insertion.

Frames Involved

Hardware acceleration is achieved by modifying the seven frames mentioned earlier based on the mode of operation. Table 35 lists the fields of each of these frames.

Table 35: List of Frame's Fields

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion
1	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType
1 2	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS -1588 Rsvd –802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS -1588 Rsvd –802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Data Receive Path

To accelerate the frames in hardware, the egress port requires information from the ingress port. The frame's ingress timestamp value is required at the egress port to calculate the frame's residence time in the switch. When event frames ingress the switch, the hardware must embed the arrival time into the frame (in the 4 bytes RSVD location). In addition to the arrival time, in some cases, the correction field must be updated with the mean path delay and the delay asymmetry values at the ingress port.

Table 36: Receive Path Frame Modifications

Receive path
Fields highlighted in
Gray – Decode these fields in hardware (to determine if it is a supported PTP frame)
Blue – Modify these fields of the frame (as needed) in hardware
Green – Capture these fields of the frame in hardware to use for comparisons of associated frames

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion
1	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType
1	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP
2	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS - 1588 Rsvd – 802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS - 1588 Rsvd – 802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Data Transmit Path

Hardware acceleration involves modifying some of the frame's fields at the egress port. The required information is extracted from the frames and used to update them before transmitting the frames. The ingress time value should be extracted from the reserved location and the field zeroed out. Correction field will be updated on top of any modifications made at the ingress port.

Table 37: Transmit Path Frame Modifications

Transmit path
Fields highlighted in
Gray – Decode these fields in hardware (to determine if it is a supported PTP frame)
Blue – Modify these fields of the frame (as needed) in hardware
Green – Capture these fields of the frame in hardware to use for comparisons of associated frames
Red – Hardware can't modify these fields. The modification has to be done by software (after checking for associated frames)

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
1	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType
1	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP
2	MessageLength	Message Length	MessageLength	Message Length	MessageLength	MessageLength	MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	Flag Field	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS -1588 / Rsvd –802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS -1588 / Rsvd –802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Frame Ingress Path Modification

When a frame ingresses a port, decoding its header determines if it is a PTP frame. If hardware acceleration is enabled (HA bit register 4.8802), then IEEE 1588/802.1AS layer 2 frames of know time domains (PTP Global – register 4.8F02) and version number (PTP Global – register 4.8E07) are accelerated in hardware. The event frame's ingress time (IntPTPTime Register PTP Global – register 4.8E07) is placed in the 4 bytes of reserved space in the frame (bytes 17–20). The correction field of the frames is updated with MeanPathDelay and IngressDelayAsymmetry values whenever applicable, based on the mode of operation as described on "Equations Defining Frame Field Values" on page 73.

When a frame contains unknown domain number, unknown message type, or unsupported version number, it cannot be accelerated by hardware. In such cases, the event frame's arrival time (domain specific time or the hardware timer value) is embedded into the frame itself based on the ArrTSMode register value (PTP Port – register 4.8802) so that the CPU has the ingress time information. If the ArrTSMode value is zero, the frame's arrival time is placed in the status registers (PTP Port – registers 4.8808 to 4.880F, 4.881D, 4.881E, and 4.8900).

An approximate latency of 8-byte times is introduced in the data path to achieve the hardware acceleration. Switching between bypass mode (no acceleration) and hardware acceleration mode should be done only when the port is idle to avoid corrupting the frames.

Frame Transmit Path Modification

When a frame egresses a port, decoding its header determines if it is a PTP frame. If hardware acceleration is enabled (HA bit register 4.8802), then IEEE 1588/802.1AS layer 2 frames of know time domains (register 4.8F02) and version number (register 4.8E07, index 0x0) are accelerated in hardware. These frames could be coming from an ingress port (hardware accelerated at ingress) or from the CPU port (CPU must place the required information into the frames).

The event frame's ingress time (IntPTPTime Register – register 4.8E07) is extracted from the 4 bytes of reserved space in the frame (bytes 17–20) for use in further calculations and the reserved bytes zeroed out (unless KeepRxData bit of action vectors is set). The OriginTS field and the Correction field of the frames are updated whenever applicable, based on the mode of operation as described on "Equations Defining Frame Field Values" on page 73.

An approximate latency of 12-byte times is introduced in the data path to achieve the hardware acceleration. Switching between bypass mode (no hardware acceleration) and hardware acceleration mode should be performed only when the port is idle to avoid corrupting the frames.

Sync and Follow_Up Frames

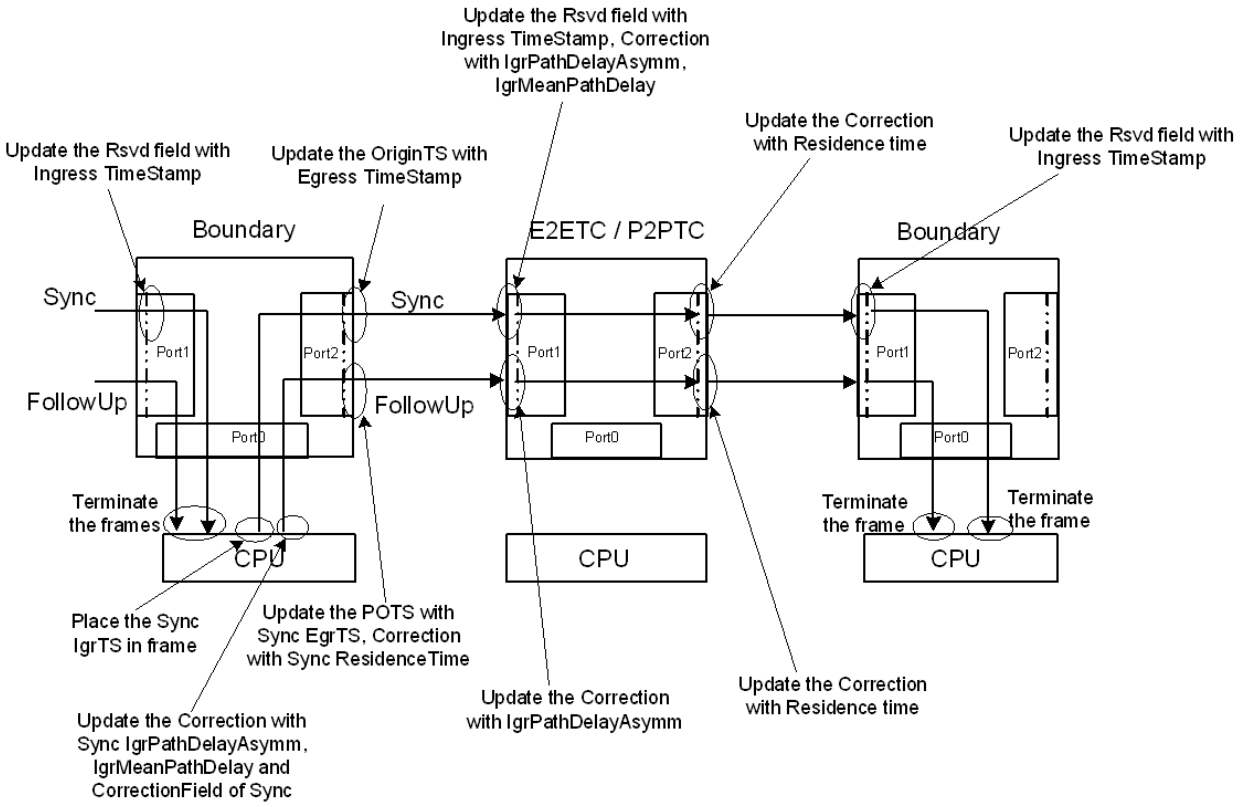
Sync and FollowUp frames travel in the same direction: from the master to the slave. These frames contain master's timing information. A FollowUp frame and Sync frame are said to be associated frames if their SourcePortID and the SeqID match. A FollowUp frame should be modified only after checking its SourcePortID and SeqID against the previously received Sync frame to ensure that the associated frames are modified correctly. The fields to be updated in the FollowUp frame are ahead of the SourcePortID and the SeqID fields. The compare and then modify method results in a long latency, so the modify and then compare method is used to avoid the latency and FollowUp frames are modified on the fly even before checking their SourcePortID and SeqID. After such modifications, when the SourcePortID and SeqID fields are reached in the frame, they are compared with that of the previous Sync frame. If they do not match, then the FCS value of the FollowUp frame is purposefully corrupted before transmitting the frame.

At ingress, the hardware inserts the receive time into the Sync frames. The CorrectionField of the Sync and FollowUp frames is updated with MeanPathDelay and IngressDelayAsymmetry values whenever applicable, based on the mode of operation.

At the egress port, the Sync frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The Sync frame's OriginTS and CorrectionField are modified based on the equations matrix. The residence time of the Sync frame is saved to be used in updating the CorrectionField of the FollowUp frame when applicable. The FollowUp frame's preciseOriginTS and CorrectionField are modified on the egress path based on the equations matrix.

Figure 21 lists all possible modifications required on Sync and FollowUp frames. However, the changes described in the figure do not all occur at the same time. Based on the mode, the device is in for example, one-step, two-step, IEEE 1588, and so on, only some of the changes will be made at a time.

Figure 21: Sync and FollowUp Frame's Hardware Acceleration Path



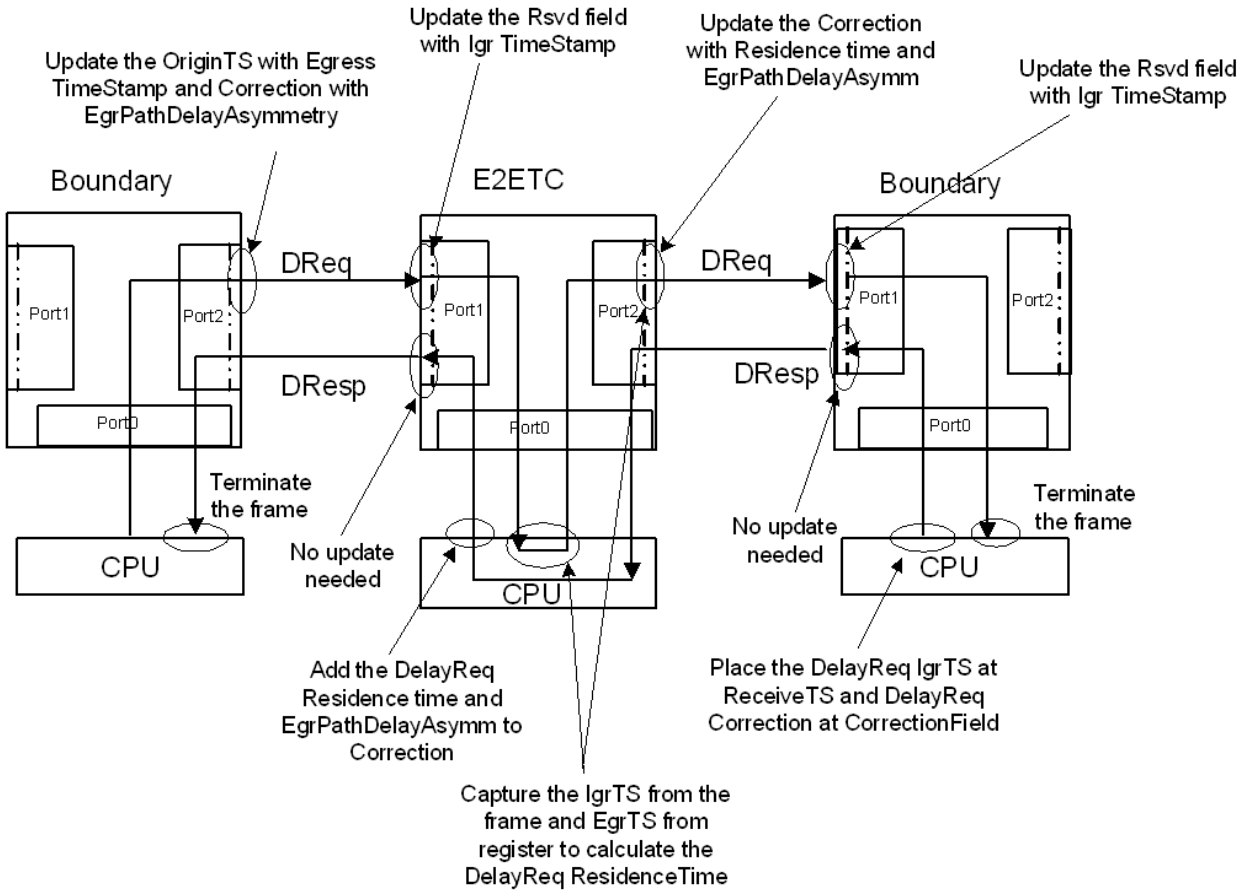
Delay_Request and Delay_Response Frames

DelayReq and DelayResp frames travel in opposite directions. DelayReq frame is sent by the slave and DelayResp frame is sent by the master port. At ingress, the hardware inserts the receive time into the DelayReq frames before sending them to the CPU. At egress port, the DelayReq frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The DelayReq frame's OriginTS and CorrectionField are modified based on the equations matrix. DelayReq frame's egress time is placed into the status registers so that the CPU can extract this information and use it to update the DelayResp frame.

A DelayReq frame and DelayResp frame are said to be associated frames if their SourcePortID and the SeqID match. A DelayResp frame should be modified with information from previously received DelayReq only after matching its SourcePortID and SeqID to ensure that they are associated frames. However, the hardware at egress port of DelayResp frame does not have the SourcePortId or SeqID values of the received DelayReq frame (opposite direction). So the CPU must check SourcePortId and SeqId of the frames and add in the correct DelayReq frame's information (residence time, CorrectionField value and EgrPathDelayAsymm) to the DelayResp frames before transmission. The hardware does not modify/accelerate the DelayResp frames at egress.

Figure 22 lists all possible modifications needed on DelayReq and DelayResp frames. However, the changes described in the figure do not all occur at the same time. Based on the mode, the device is in for example, one-step, two-step, IEEE 1588, and so on, only some of the changes will be made at a time.

Figure 22: DelayReq and DelayResp Frame's Hardware Acceleration Path



PDelayRequest, PDelayResponse, and PDelayResponseFollowUp Frames

PDelayReq frame is sent by the initiator to the responder. At ingress, the hardware inserts the receive time into the PDelayReq frames before sending them to the CPU. At egress port, the PDelayReq frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The PDelayReq frame's OriginTS and CorrectionField are modified based on the equations matrix. PDelayReq frame's egress time is placed into the status registers so that the CPU can extract this information and use it to update the PDelayResp/ PDelayRespFollowUp frame.

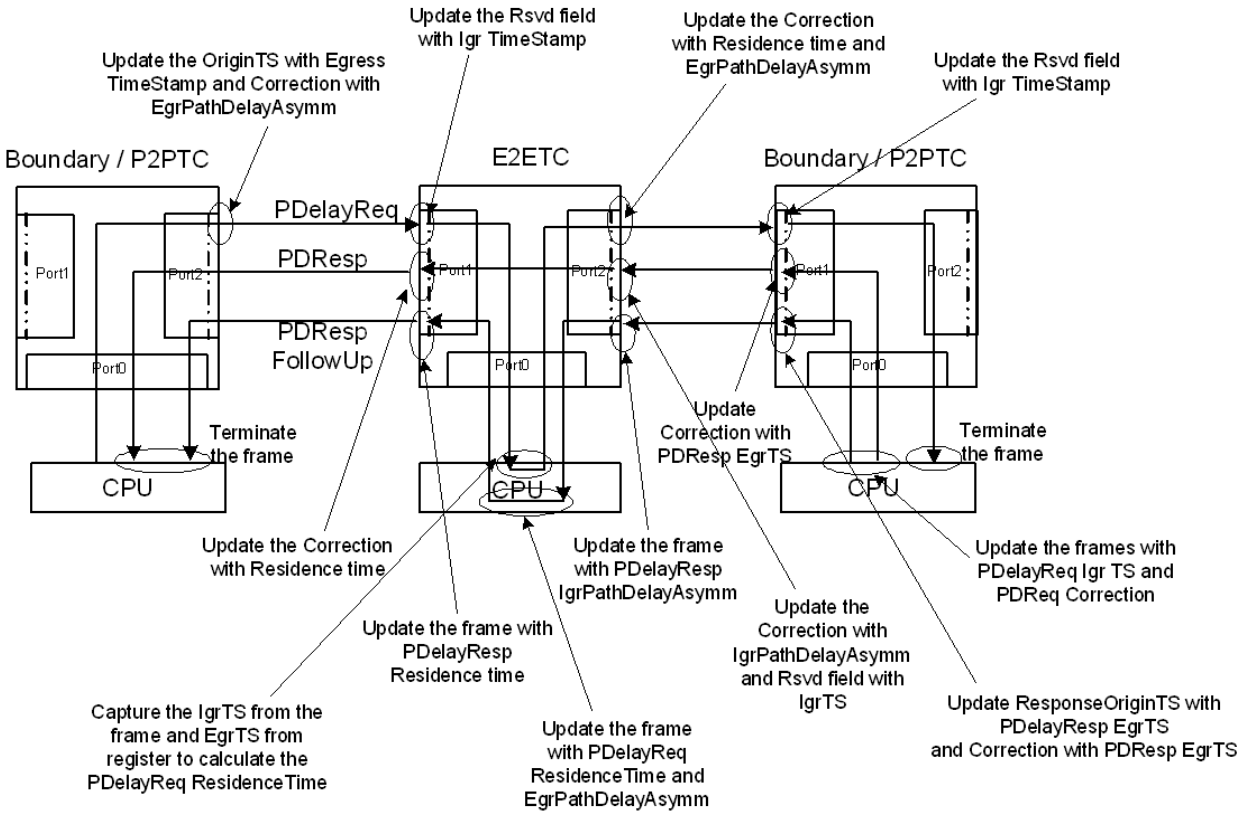
The PDelayResp frame is sent by the responder to the initiator, that is, in opposite direction than the PDelayReq frame. At ingress, the hardware inserts the receive time into the PDelayResp frames. A PDelayReq frame and PDelayResp frame are associated frames if the SourcePortID and SeqID of PDelayReq frame matches with the ReqPortID and the SeqID of PDelayResp frame. A PDelayResp frame should be modified only after checking its ReqPortID and SeqID against the SourcePortId and SeqID of previously received PDelayReq frame to ensure that the associated frames are modified correctly. However, the hardware at egress port of PDelayResp frame does not have the SourcePortId or SeqID values of the received PDelayReq frame (opposite direction). So the CPU must match the frames and add in the correct PDelayReq frame's information to the PDelayResp

frames before transmission. The CorrectionField value of PDelayReq must be added to the CorrectionField of PDelayResp frames when applicable. The CPU should place the PDelayReq frame's IgrTS in the 4 reserved bytes (bytes 17–20 of PTP header) of PDelayResp frames when applicable. At egress, the hardware extracts this information and updates the PDelayResp frame's ReqReceiptTS and CorrectionField based on the equation's matrix.

PDelayResp and PDelayRespFollowUp frames travel in the same direction, from the responder to the initiator. A PDelayRespFollowUp frame and PDelayResp frame are associated with each other if their ReqPortID and the SeqID match. A PDelayRespFollowUp frame should be modified only after checking its ReqPortID and SeqID against the previously received PDelayResp frame to ensure that the associated frames are modified correctly. The fields to be updated in the PDRespFollowUp frame are ahead of the ReqPortID and the SeqID fields. The compare and then modify method results in a long latency, so the modify and then compare method is used to avoid the latency, PDelayRespFollowUp frames are modified on the fly even before checking their ReqPortID and SeqID. After such modifications, when the ReqPortID and SeqID fields are reached in the frame, they are compared with that of the previous PDelayResp frame. If they do not match, then the FCS value of the PDelayRespFollowUp frame is purposefully corrupted before transmitting the frame. Similar to the PDelayResp frame's case, the hardware depends on the CPU to make PDelayReq-related timing information changes to PDelayRespFollowUp whenever applicable.

Figure 23 lists all possible modifications needed on PDelayReq, PDelayResp, and PDelayRespFollowUp frames. However, it should be noted that the changes described in the figure do not all occur at the same time. Based on the mode the device is in for example, one-step, two-step, IEEE 1588, and so on, only some of the changes will be made at a time.

Figure 23: PDelayReq, PDelayResp, and PDelayRespFollowUp Frame's Hardware Acceleration Path



Equations Defining Frame Field Values

The following tables describe the equations that govern the frame field values based on various configurations supported.

Table 38: Sync Frame Equations Implemented

1. The boxes filled in red depict the special cases where the device works differently than described in IEEE spec. The text describes the device's behavior in those cases.
2. The text highlighted in light grey is the ingress path function that is not performed in hardware. The frame is sent to CPU and it should take care of this portion.
3. The text highlighted in green is the information that CPU is required to supply the hardware in the egress path. That portion needs to be placed in the frame by the software.
4. Rest of the portion is done in hardware (combination of the ingress path and egress path)

			Ordinary / Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Sync	**One Step**	**1588**	**OriginTS** = SyncEgrTS **CorrectionField** = Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**OriginTS**=Rx's OriginTS **Correction**= Rx's CorrectionField + IgrMeanPathDelay + ResidenceTime + IgrPathDelayAsym	**OriginTS**=Rx's OriginTS **Correction**= Rx's CorrectionField + ResidenceTime + IgrPathDelayAsym
	Two Step w/ Rx TwoStepFlag = False	**1588**	NA	**OriginTS**=Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*	**OriginTS**=Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag = True	**1588**	**OriginTS**= Rx's OriginTS (0 or estimate SyncEgrTS) OR SyncEgrTS (Program action reg bit) **CorrectionField**= Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**OriginTS**=Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*	**OriginTS**=Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
		802.1 AS	**OriginTS** - NA **CorrectionField**= Rx's CorrectionField (0) *i.e frame not modified*	NA	NA

Table 39: FollowUp Frame Equations Implemented

			Ordinary / Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
FollowUp	One Step	1588	NA	**PreciseOriginTS**=Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*	**PreciseOriginTS**= Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ RxTwoStepFlag = False	1588	NA	**PreciseOriginTS**=Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*	**PreciseOriginTS**= Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ RxTwoStepFlag = True	1588	**PreciseOriginTS**= SyncEgrTS **Correction** = Rx's CorrectionField (0 – CorrectionField Sync)	**PreciseOriginTS**= Rx's PreciseOriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrMeanPathDelay + IgrPathDelayAsym	**PreciseOriginTS**= Rx's PreciseOriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrPathDelayAsym
		802.1AS	**PreciseOriginTS**= (a) If GrandMaster: SyncEgrTS (b) If not the GrandMaster: Rx's PreciseOriginTS **Correction** = (a) If GrandMaster: Rx's CorrectionField (0) (b) If not the GrandMaster: Rx's CorrectionField + ResidenceTime + PropagationDelay (MeanPathDelay) + IgrPathDelayAsym	NA	NA

Table 40: DelayReq-Resp Frame Equations Implemented

			Ordinary / Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Delay Req	One Step	1588	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** =Rx's OriginTS **Correction** = Rx's CorrectionField + ResidenceTime - EgrPathDelayAsym
	Two Step w/ Rx TwoStepFlag = False	1588	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag = True	1588	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
		802.1AS	N/A	N/A	N/A
Delay Resp	One Step	1588	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag =False	1588	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField + ResidenceTime DelayReq – EgrPathDelayAsym of DelayReq *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag = True	1588	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField + ResidenceTime DelayReq – EgrPathDelayAsym of DelayReq *i.e frame not modified*
		802.1AS	N/A	N/A	N/A

Table 41: PDelayReq Frame Equations Implemented

			Ordinary / Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Req	**One Step**	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + Residence Time PdelayReq – EgrPathDelayAsym
	Two Step w/ Rx TwoStepFlag =False	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag = True	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
		802.1AS	**OriginTS** = NA **Correction** = Rx's CorrectionField (0) *i.e frame not modified*	NA	NA

Table 42: PDelayResp Frame Equations Implemented

			Ordinary / Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Resp	**One Step**	**1588**	**ReqReceiptTS** = Rx's ReqReceiptTS (0) **Correction** = CorrectionField of PdelayReq + (PDRespEgrTS – PDReqIgrTS) **Rsvd** = PDReqIgrTS **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS (0) **Correction** = CorrectionField of PdelayReq + (PDRespEgrTS – PDReqIgrTS) **Rsvd** = PDReqIgrTS **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField + ResidenceTime Pdelay_Resp + IgrPathDelayAsym
	Two Step w/ Rx TwoStepFlag = False	**1588**	NA	NA	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag = True	**1588**	**ReqReceiptTS** = (a) Rx's ReqReceiptTS (0) OR (b) ReqReceiptTS (PDelayReqIgrTS) **Correction** = (a) Rx's CorrectionField (0) OR (b) Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = (a) Rx's ReqReceiptTS (0) OR (b) ReqReceiptTS (PDelayReqIgrTS) **Correction** = (a) Rx's CorrectionField (0) OR (b) Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField *i.e frame not modified*
		802.1AS	**ReqReceiptTS** = Rx's ReqReceiptTS (PDelayReqIgrTS) **Correction** = Rx's CorrectionField (0) *i.e frame not modified*	NA	NA

Table 43: PDelayRespFollowUp Frame Equations Implemented

			Ordinary / Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
PdelayRespFollowUp	**One Step**	**1588**	NA	NA	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag = False	**1588**	NA	NA	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's CorrectionField *i.e frame not modified*
	Two Step w/ Rx TwoStepFlag = True	**1588**	**ResponseOriginTS** = (a) Rx's ResponseOriginTS (0) OR (b) PdelayRespEgrTS **Correction** = Correction Field PdelayReq + (a) PdelayRespEgrTS-PdelayReqIgrTS OR (b) 0 **Rsvd** = (a) PdelayReqIgrTS	**ResponseOriginTS** = (a) Rx's ResponseOriginTS (0) OR (b) PdelayRespEgrTS **Correction** = Correction Field PdelayReq + (a) PdelayRespEgrTS-PdelayReqIgrTS OR (b) 0 **Rsvd** = (a) PdelayReqIgrTS	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's Correction field + Residence Time of PdelayReq + Residence Time of PdelayResp + IgrPathDelayAsym of PDelayResp – EgrPathDelayAsym of PDelayReq
		802.1AS	**ResponseOriginTS** = PdelayRespEgrTS **Correction** = Rx's Correction field (0)	NA	NA

The PdelayResp and PdelayRespFollowUp frames follow either scheme (a) or (b) based on the register selection.

2.21.3 Time Application Interface (TAI)

PTP provides both frequency and time of day with respect to the PTP Grand Master for the entire PTP network. In a given endpoint device (media talker or a media listener), when the PTP Grand Master aware clock and time are available, it must be transported over to the rest of the subsystem without loss of accuracy. For example, if a Digital Video Recorder (DVR) is the end device, the network clock and time must be seamlessly transported to the video SoC and/or storage SoC as well as to the host processor. This ensures that when the media is played out of the DVR, the network time aware presentation time of the content is required to be carried through.

The TAI Timing Interface Block supports features required for the previously described purpose. This block utilizes two signals to offer various services. One signal is called EventRequest input signal, and the second is called TriggerGenerate output signal.

Using the previously described signals, there are several functions that this block supports:

- An event pulse capture function
- Multiple event counter function
- A trigger pulse generate function with pulse width control
- A trigger clock generate function with digital clock compensation
- A multi-PTP device time sync function

2.21.3.1 Event Pulse Capture Interface

In many IEEE 1588 applications such as industrial automation, it is important to precisely capture the time at which a particular event has occurred. The event is defined by a low-to-high or high-to-low transition on an external signal called EventRequest. The event time is captured in EventCapRegister (registers 4.8D01 and 4.8D02). This field is validated by EventCapValid bit (TAI Global Configuration – register 4.8D00).

The captured event time register must be read out by the software and the valid bit must be cleared before the hardware captures another event. If there were to be two back-to-back events before the software read the results of the first event, then an error indication is set in EventCapErr (TAI Global Configuration – register 4.8D00). If the user chooses that the hardware overwrites the Event capture register, then it can be configured by setting a 0x1 to EventCapOv (TAI Global Configuration – register 4.8C00).

When an event has been captured, the software can optionally (EventCapIntEn – register 4.8C00) be interrupted and an EventInt (register 4.8C09) bit is also set.

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration – register 4.8C01). The minimum pulse width of the EventRequest signal must be 1.5 times the TSClkPer (TAI Global Configuration – register 4.8C01). For the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events must be 150 ns plus 5 times the TSClkPer amount.

2.21.3.2 Multiple Event Counter Function

Similar to the previously described Event Pulse capture interface, if multiple events must be captured for an application to detect how many times a particular event is happening on the EventRequest input signal, EventCtrStart (TAI Global Configuration Register – register 4.8C00) must be set to 0x1 and EventCapOv (TAI Global Configuration Register – register 4.8C00) must be set to 0x1.

The Multiple Event Counter function is capable of capturing up to 255 events in EventCapCtr (TAI Global Configuration – register 4.8C09).

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration – register 4.8C01). The minimum pulse width of the EventRequest signal must be 1.5 times the TSClkPer (TAI Global Configuration – register 4.8C01). For the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events must be 150 ns plus 5 times the TSClkPer amount.

Note

In the multiple event counter mode, the EventCapRegister (registers 4.8D01 and 4.8D02) indicate the timestamp value for the last captured event register.

2.21.3.3 Trigger Pulse Generate Function

In many PTP applications, the time of day computed in PTP must be distributed in some form to the rest of the node. One commonly used method is to generate a pulse whenever the PTP Global Time matches a certain configured value. The pulse gets output on a TrigGenResp output signal.

The previously described function can be achieved by the following:

a) Configuring the TrigMode (TAI Global Configuration Register 4.8C00) to 0x1 and
b) Configuring the time amount when the pulse must be generated in TrigGenAmt (TAI Global Configuration Registers 4.8C02 and 4.8C03) and
c) Configuring the TrigGenReq (TAI Global Configuration Register 4.8C00) to 0x1

The PTP Global Timer gets compared to the TrigGenAmt, and upon a match a pulse signal gets generated on the TrigGenResp output signal.

Optionally, after generating the TrigGenResp pulse, the CPU can be notified by setting TrigGenIntEn (TAI Global Configuration Register 4.8C00), and along with the pulse output the TrigGenInt bit (TAI Global Configuration Register 4.8C08) gets set. Upon receiving the interrupt, it is the function of the CPU to clear the interrupt bit.

The pulse width of the output signal can be controlled by PulseWidth (TAI Global Configuration Register 4.8C05). Do not set the PulseWidth to a zero value.

2.21.3.4 Trigger Clock Generate Function

Similar to the trigger pulse generation function described above, the same set of registers can be used to generate a periodic clock. The value specified in TrigGenAmt (TAI Global Configuration Register 4.8C02 and 4.8C03) is used to generate the base period of the clock output. For this functional mode, the TrigMode (TAI Global Configuration Register 4.8C00) must be set to 0x0 and TrigGenReq (TAI Global Configuration Register 4.8C00) must be set to 0x1.

The output clock can be compensated by configuring field TrigClkComp (TAI Global Configuration Register 4.8C04) and TrigClkCompSubps (TAI Global Configuration Register 4.8C05). This field specifies the remainder amount for the clock that is being generated with the period specified by TrigGenAmt. The TrigClkComp amount gets constantly accumulated and when this accumulated amount exceeds the value specified in TSClkPer, a TSClkPer gets added to the output clock momentarily to compensate for the remainder accumulated over time.

A start time for the clock may be chosen (TAI Global Registers 4.8C09 and 4.8C0A and Register 4.8C0A). Also, a compensation direction may be chosen by indicating the amount to add or subtract in register 4.8C04, bit 15 (TrigCompDir).

Note

TrigGenAmt should be set to no less than two times the TSCLKPer amount.

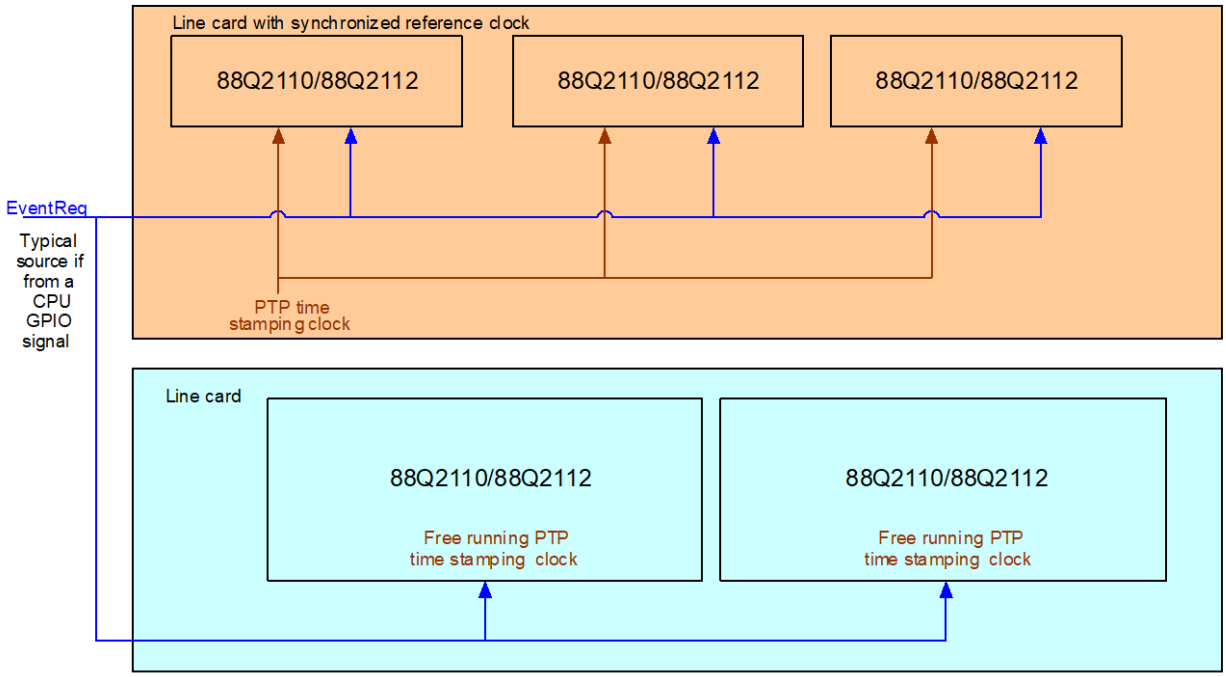
2.21.3.5 Multi-PTP Device Time Sync Function

When PTP is enabled on devices on enterprise, service provider line cards and/or chassis, it is important for various PTP-capable devices on the system to have the common notion of PTP Global Time. Typically, a central processing card is present in these chassis, which runs the PTP software for the entire chassis, and all the data line cards send the PTP frames and the timestamp information to the central PTP software entity. Given that there can be so many ports on each line card and each of the line cards may be plugged into the chassis at different times, the PTP Global

Time counter value in each of the PTP devices on the line cards may not be synchronized. The hardware must provide a sure short way for all the PTP-capable devices across various line cards, regardless of when the line cards were powered on, to be synchronized to the same PTP Global Time so that the PTP protocol software does not have to remember the offsets with respect to the PTP Grand Master and also with respect to each of these devices.

The background for this feature is that the PTP nodes derive the time of day via PTP message exchange. The derived time of day consists of 64 bits of seconds and 32 bits of nanoseconds. The PTP slave nodes are expected to derive the frequency and phase offset information with respect to the PTP Grand Master node. The derived offset information is used to periodically adjust various device PTP global timer values. For multi-PTP (Marvell devices only) capable devices, the goal is to synchronize all the nodes with a common 32-bit nanoseconds field and also adjust the nanoseconds field with the computed PTP Grand Master offset information.

Figure 24: Multiple Devices Across Multiple Line Cards Connected by an EventReq Input Signal



This feature is enabled by setting MultiPTPSyncMode (TAI Global Configuration Register 4.8C00) to 0x1. When this bit is enabled, the functions EventRequest and TriggerGen are disabled.

When MultiPTPSyncMode is 0x1, a low-to-high or high-to-low transition on the EventRequest signal triggers transfer of TrigGenAmt to the PTP Global Timer register. At the timer of the low-to-high or high-to-low transition for further software time correlation, the EventCapTime register is also updated with the value of the PTP Global Time before it gets overwritten.

Though the previously described schema ensures that the PTP Global Time register value is synchronized, the following are possible sources of jitter associated from a system level (which can be avoided):

a) The reference clock sources for various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards may not be synchronized.

b) The added delays in the clock path between various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards.

c) Inherent operating system related jitter from the point a command is issued to when it actually gets executed in hardware. This is applicable for EventReq pulse generation from a GPIO as well. This tends to be more predictable with real-time operating systems.

One guaranteed method to avoid the previously mentioned jitter factors a and b is by using a flip-flop with the EventReq as the data input and PTP timestamping clock as the clock input into the flop and the flop output gets distributed with matched delays across various PTP devices that support the multi-sync EventReq. One method to reduce the operating system associated uncertainties is to choose an operating system in which the scheduler tasks are predictable down to 1s of nanoseconds accuracy.

2.21.4 ReadPlus Command

The PTP Global Time Registers are used as 32-bit global timer value that is running off of the free-running PHY clock. A Read from the PTP Global Time Registers must be done with the ReadPlus command. A Read directly to the PTP Global Time Registers without using the ReadPlus command will return 0. The PTP Global Time Registers value can be loaded directly by writing back-to-back to the PTP Global Time Register Byte 3 & 2 – register 4.8C0F first followed by PTP Global Time Register Byte 1 & 0 – register 4.8C1E.

To read from the PTP Global Time Register:

1. Write to Register 4.8E1E = 0x8E0E (ReadPlus command from PTP Global Time Register).
2. Read from Register 4.8E1F (PTP Global Time Registers bits [15:0]).
3. Read from Register 4.8E1F (PTP Global Time Registers bits [31:16]).

Also, the new TOD-related registers are all only ReadPlus (registers in the 4.8Fxx space).

To read from the PTP TOD-related Register:

1. Write to Register 4.8E1E = 0x8F10 (ReadPlus command from TOD Load Point Register).
2. Read from Register 4.8E1F (PTP TOD Load Point Registers bits [15:0]).
3. Read from Register 4.8E1F (PTP TOD Load Point Registers bits [31:16]).

Note

These registers must use the ReadPlus command; otherwise, the read-back value is incorrect:

- 4.8Fxx
- 4.8C1E and 4.8C0F
- 4.8C02 and 4.8C03
- 4.8C09 and 4.8C0A
- 4.8D01 and 4.8D02

3 General Registers

Table 44 defines the register types used in the register map.

Table 44: Register Types

Type	Description
LH	Register field with latching high function. If the status is high, then the register is set to 1 and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If the status is low, then the register is cleared to 0 and remains 0 until a read operation is performed through the management interface or a reset occurs.
RES	Reserved. All reserved bits are read as 0 unless otherwise noted.
Retain	The register value is retained after a software reset is executed.
RO	Read only.
ROC	Read only clear. After read, the register field is cleared.
R/W	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, the register field is cleared to 0.
SC	Self-Clear. Writing a 1 to this register causes the desired function to be immediately executed, then the register field is automatically cleared to 0 when the function is complete.
Update	This is the value written to the register field does not take effect until a soft reset is executed.
WO	Write only. Reads from this type of register field return undefined data.
NR	Non-Rollover Register

PHY MDIO Register Description

The device supports Clause 45 XMDIO register access protocol. The device also supports Clause 22 MDIO access to registers in Clause 45 XMDIO register space using registers 13 and 14.

The registers in this device are divided into the following sections:

- IEEE PMA/PMD Registers
- Common Control Registers
- IEEE PCS Registers
- IEEE Auto-Negotiation Registers
- 100BASE-T1 Copper Unit Advance PCS Registers
- 1000BASE-T1 Copper Unit Advance PCS Registers
- Copper Unit Advance Auto-Negotiation Registers
- RGMII Registers
- SGMII Registers
- PTP Registers

3.1 IEEE PMA/PMD Registers

Table 45: IEEE PMA/PMD Registers — Register Map

Register Name	Register Address	Table and Page
PMA/PMD Control Register 1	Device 1, Register 0x0000	Table 46, p. 86
PMA/PMD Device Identifier Register 1	Device 1, Register 0x0002	Table 47, p. 86
PMA/PMD Device Identifier Register 2	Device 1, Register 0x0003	Table 48, p. 86
PMA/PMD Speed Ability Register	Device 1, Register 0x0004	Table 49, p. 86
PMA/PMD Devices In Package Register 1	Device 1, Register 0x0005	Table 50, p. 87
PMA/PMD Devices In Package Register 2	Device 1, Register 0x0006	Table 51, p. 87
PMA/PMD Package Identifier Register 1	Device 1, Register 0x000E	Table 52, p. 88
PMA/PMD Package Identifier Register 2	Device 1, Register 0x000F	Table 53, p. 88
BASE-T1 PMA/PMD Extended Ability Register	Device 1, Register 0x0012	Table 54, p. 88
BASE-T1 PMA/PMD Control Register	Device 1, Register 0x0834	Table 55, p. 88
100BASE-T1 PMA/PMD Test Control Register	Device 1, Register 0x0836	Table 56, p. 89
BASE-T1 Control Register	Device 1, Register 0x0900	Table 57, p. 89
1000BASE-T1 PMA Status Register	Device 1, Register 0x0901	Table 58, p. 89
1000BASE-T1 Training Register	Device 1, Register 0x0902	Table 59, p. 90
1000BASE-T1 Link Partner Training Register	Device 1, Register 0x0903	Table 60, p. 90
1000BASE-T1 Test Mode Control Register	Device 1, Register 0x0904	Table 61, p. 90

Table 46: PMA/PMD Control Register 1
Device 1, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x1	SC	1 = PMA/PMD reset 0 = Normal operation
14	Reserved	RO	0x0	0x0	Set to 0.
13	Speed Select	RO	0x0	Retain	Bits [6,13] = 10 – Operation at 1000BASE-T1 Bits [6,13] = 01 – Operation at 100BASE-T1
12	Reserved	RO	0x0	0x0	
11	Low Power	R/W	0x0	0x0	1 = Low Power mode 0 = Normal operation
10:7	Reserved	RO	0x0	0x0	Set to 0.
6	Speed Select	RO	0x1	Retain	Bit 6, bit 13 00 = Reserved 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
5:1	Reserved	RO	0x00	0x00	Set to 0.
0	PMA Loopback	R/W	0x0	Retain	1 = Drop link and loop data back in PMA. 0 = Normal operation

Table 47: PMA/PMD Device Identifier Register 1
Device 1, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bits 3:18	RO	0x002B	0x002B	Bits 3 to 18 of the Marvell OUI

Table 48: PMA/PMD Device Identifier Register 2
Device 1, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bits 19:24	RO	0x02	0x02	Bits 19:24 of the Marvell OUI
9:4	Model Number	RO	0x18	0x18	The model number is 011000.
3:0	Revision Number	RO	See Description.	See Description.	This is the revision number. Refer to the Release Notes for detailed information.

Table 49: PMA/PMD Speed Ability Register (Sheet 1 of 2)
Device 1, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Set to 000000000.

Table 49: PMA/PMD Speed Ability Register (Sheet 2 of 2)
Device 1, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
6	10M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 10 Mbps.
5	100M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 100 Mbps.
4	1000M Capable	RO	0x1	0x1	1 = PMA/PMD is capable of operating at 1000 Mbps.
3:1	Reserved	RO	0x0	0x0	Set to 000.
0	10G Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 10 Gbps.

Table 50: PMA/PMD Devices In Package Register 1
Device 1, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 00000000.
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation is present in the package. 0 = Auto-Negotiation is not present in the package.
6	Reserved	RO	0x0	0x0	Set to 0.
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS is present in the package. 0 = DTE XS is not present in the package.
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS is present in the package. 0 = PHY XS is not present in the package.
3	PCS Present	RO	0x1	0x1	1 = PCS is present in the package. 0 = PCS is not present in the package.
2	WIS Present	RO	0x0	0x0	1 = WIS is present in the package. 0 = WIS is not present in the package.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD is present in the package. 0 = PMA/PMD not present in the package.
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers are present in the package. 0 = Clause 22 registers are not present in the package.

Table 51: PMA/PMD Devices In Package Register 2
Device 1, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor-specific Device 2 Present	RO	0x0	0x0	1 = A vendor-specific device 2 is present. 0 = A vendor-specific device 2 is not present.
14	Vendor-specific Device 1 Present	RO	0x0	0x0	1 = A vendor-specific device 1 is present. 0 = A vendor-specific device 1 is not present.
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000.

Table 52: PMA/PMD Package Identifier Register 1
Device 1, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bits 3:18	RO	0x002B	0x002B	Bits 3:18 of the Marvell OUI

Table 53: PMA/PMD Package Identifier Register 2
Device 1, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bits 19:24	RO	0x02	0x02	Bits 19:24 of the Marvell OUI
9:4	Model Number	RO	0x18	See Description.	This is the same as 1.0003.9:4.
3:0	Revision Number	RO	0x1	See Description.	This is the same as 1.0003.3:0.

Table 54: BASE-T1 PMA/PMD Extended Ability Register
Device 1, Register 0x0012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	0x0000	
1	1000BASE-T1 Ability	RO	0x1	0x1	1 = PMA/PMD is able to perform 1000BASE-T1. 0 = PMA/PMD is not able to perform 1000BASE-T1.
0	100BASE-T1 Ability	RO	0x1	0x1	Invalid

Table 55: BASE-T1 PMA/PMD Control Register
Device 1, Register 0x0834

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x1	0x1	The value is always 1 and writes are ignored.
14	Master/Slave Config Value	R/W	cfg_ master	Retain	1 = Configure the PHY as master. 0 = Configure the PHY as slave.
13:4	Reserved	RO	0x000	0x000	Set to 000000000000.
3:0	Type Selection	R/W	Strap	Retain	0000 = 100BASE-T1 0001 = 1000BASE-T1

Table 56: 100BASE-T1 PMA/PMD Test Control Register
Device 1, Register 0x0836

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	100BASE-T1 Test Mode Control	R/W	0x0	Retain	11x = Reserved 101 = Test mode 5 100 = Test mode 4 011 = Reserved 010 = Test mode 2 001 = Test mode 1 000 = Normal operation
12:0	Reserved	RO	0x0000	0x0000	Set to 000000000000.

Table 57: BASE-T1 Control Register
Device 1, Register 0x0900

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x1	0x0	1 = PMA/PMD reset 0 = Normal operation
14	Global PMA Transmit Disable	R/W	0x0	Retain	0 = Enable transmitters. 1 = Disable transmitters.
13:12	Reserved	RO	0x0	0x0	
11	Low Power	R/W	0x0	0x0	1 = Low Power mode 0 = Normal operation
10:0	Reserved	RO	0x000	Retain	

Table 58: 1000BASE-T1 PMA Status Register
Device 1, Register 0x0901

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x0	Retain	Ignore when read.
9	Receive Fault Ability	RO	0x0	Retain	1 = PMA/PMD has the ability to detect a fault condition on the Rx path. 0 = PMA/PMD does not have the ability to detect a fault condition on the Rx path.
8	Low Power Ability	RO	0x1	Retain	1 = PMA/PMD supports Low Power mode. 0 = PMA/PMD does not support Low Power mode.
7:3	Reserved	RO	0x00	Retain	Ignore when read.
2	Received Polarity	RO	0x0	Retain	1 = Reverse polarity is reversed. 0 = Reverse polarity is not revered.
1	Receive Fault	RO	0x0	Retain	1 = A fault condition is detected. 0 = A fault condition is not detected.
0	Receive Link Status	RO, LL	0x0	Retain	1 = The PMA/PMD receive link is up. 0 = The PMA/PMD receive link is down.

Table 59: 1000BASE-T1 Training Register Device 1, Register 0x0902

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	Retain	Set to 0s.
10:4	User Field	R/W	0x00	Retain	This is the 7-bit user-defined field.
3:2	Reserved	RO	0x0	Retain	Set to 0s.
1	OAM Advertisement	R/W	0x1	Retain	1 = The OAM ability is advertised to the link partner. 0 = The OAM ability is not advertised to the link partner.
0	EEE Advertisement	R/W	0x0	Retain	1 = The EEE ability is advertised to the link partner. 0 = The EEE ability is not advertised to the link partner.

Table 60: 1000BASE-T1 Link Partner Training Register Device 1, Register 0x0903

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	Retain	
10:4	Link Partner User Field	RO	0x00	Retain	This is the 7-bit user-defined field received from the link partner.
3:2	Reserved	RO	0x0	Retain	Set to 0s.
1	OAM Advertisement	RO	0x0	Retain	1 = The link partner OAM ability is advertised 0 = The link partner OAM ability is not advertised
0	EEE Advertisement	R/W	0x0	Retain	1 = The link partner EEE ability is advertised. 0 = The link partner EEE ability is not advertised.

Table 61: 1000BASE-T1 Test Mode Control Register Device 1, Register 0x0904

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode Control	R/W	0x0	Retain	111 = Test mode 7 110 = Test mode 6 101 = Test mode 5 100 = Test mode 4 011 = Reserved 010 = Test mode 2 001 = Test mode 1 000 = Normal operation
12:0	Reserved	RO	0x0000	Retain	

3.2 Common Control Registers

Table 62: Common Control Registers — Register Map

Register Name	Register Address	Table and Page
Reset and Control Register	Device 3, Register 0x8000	Table 63, p. 91
Tx Disable Status Register	Device 3, Register 0x8002	Table 64, p. 92
SyncE Control Register	Device 3, Register 0x8004	Table 65, p. 92
Interrupt Enable Register	Device 3, Register 0x8010	Table 66, p. 92
GPIO Interrupt Status Register	Device 3, Register 0x8011	Table 67, p. 93
Temperature Sensor Register 2	Device 3, Register 0x8041	Table 68, p. 94
Temperature Sensor Register 3	Device 3, Register 0x8042	Table 69, p. 94
Temperature Sensor Register 4	Device 3, Register 0x8043	Table 70, p. 95
Interrupt Enable Register	Device 3, Register 0xFE16	Table 71, p. 95
Interrupt Status Register	Device 3, Register 0xFE17	Table 72, p. 95
TDR Control Register	Device 3, Register 0xFEC3	Table 73, p. 96
TDR Status Register 1	Device 3, Register 0xFEDB	Table 74, p. 96
TDR Status Register 2	Device 3, Register 0xFEDC	Table 75, p. 96
I/O Voltage Control Register	Device 4, Register 0x8214	Table 76, p. 96
LPSD Register 1	Device 3, Register 0x801C	Table 77, p. 97
LPSD Register 2	Device 3, Register 0x801D	Table 78, p. 97
SQI Register	Device 3, Register 0xFC4C	Table 79, p. 98

Table 63: Reset and Control Register
Device 3, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RGMII Software Reset	R/W	0x0	Retain	RGMII Software Reset, not self-clearing 0 = Disable, no reset 1 = Enable, perform a software reset of the T-unit.
14	Reserved	R/W	0x0	Retain	
13	SGMII Software Reset	R/W	0x0	Retain	SGMII Software Reset, not self-clearing 0 = Disable, no reset 1 = Enable, perform a software reset of the T-unit.
12:4	Reserved	R/W	0x000	Retain	
3	TX Disable Feature Enable	R/W	0x1	Retain	1 = Enable TX Disable Feature. Tx packets can be stopped by TX_ENABLE pin. 0 = Disable TX Disable Feature. TX_ENABLE has no effect on Tx packets.
2:0	Reserved	R/W	0x0	Retain	

Table 64: Tx Disable Status Register
Device 3, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	Retain	Read 00000.
2	VDD09 Ready	RO	0x0	Retain	
1	VDD03 Ready	RO	0x0	Retain	
0	Status of Disable	RO	0x0	Retain	0 = Tx packets are not blocked. 1 = Tx packets are blocked.

Table 65: SyncE Control Register
Device 3, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	SyncE Link Down Disable	R/W	0x0	Retain	This selects what the SyncE clock output is during link down. 1 = SyncE clock is low. 0 = SyncE clock is the local 125 MHz clock.
0	SyncE Clock Enable	R/W	0x0	Retain	1 = Enable SyncE clock to go out on the GPIO pin. 0 = Disable SyncE.

Table 66: Interrupt Enable Register (Sheet 1 of 2)
Device 3, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
15	PTP Interrupt (Negative Level)	R/W	0x0	Retain	0 = Disable 1 = Enable
14	PTP Interrupt	R/W	0x0	Retain	0 = Disable 1 = Enable
13	100BT1 Interrupt Neg Edge	R/W	0x0	Retain	0 = Disable 1 = Enable
12	100BT1 Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
11	Includes Interrupt for Temperature Sensor	R/W	0x0	Retain	0 = Disable 1 = Enable
10:8	Reserved	R/W	0x0	Retain	
7	Pmt_link_dwn Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
6	Pmt_link_up Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
5	SGMII Interrupt (Negative Edge) Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
4	NT Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable

Table 66: Interrupt Enable Register (Sheet 2 of 2)
Device 3, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Reserved	R/W	0x0	Retain	
2	LED [1] Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
1	LED [0] Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
0	GPIO [0] Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable

Table 67: GPIO Interrupt Status Register (Sheet 1 of 2)
Device 3, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
15	PTP Interrupt (Negative Level)	RO, LH	0x0	0x0	0 = No Interrupt_Mask has occurred. 1 = An Interrupt_Mask has occurred.
14	PTP Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
13	100BT1 Interrupt (Negative Level) Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
12	100BT1 Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
11	TEMP Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
10:8	Reserved	RO, LH	0x0	0x0	
7	LINKDWN Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
6	LINKUP Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
5	SGMII Interrupt (Negative Edge) Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
3	Reserved	RO, LH	0x0	0x0	
2	LED [1] Interrupt Status	RO, LH	0x0	0x0	This bit is not valid unless register 3.8014.7 = 1 and 3.8013.2 = 0. 0 = No interrupt has occurred. 1 = An interrupt has occurred.
1	LED [0] Interrupt Status	RO, LH	0x0	0x0	This bit is not valid unless register 3.8014.3 = 1 and 3.8013.1 = 0. 0 = No interrupt has occurred. 1 = An interrupt has occurred.

Table 67: GPIO Interrupt Status Register (Sheet 2 of 2)
Device 3, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
0	GPIO [0] Interrupt Status	RO, LH	0x0	0x0	This bit is not valid unless register 3.8013.0 = 0. 0 = No interrupt has occurred. 1 = An interrupt has occurred.

Table 68: Temperature Sensor Register 2
Device 3, Register 0x8041

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Average Test Mode	R/W	0x0	Retain	1 = Average over 16 samples 0 = Normal, the number of samples to average over is determined by 3.8042.12:11.
14:8	Reserved	RO	0x00	Retain	Set to 0s.
7	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
6	Temperature Sensor Interrupt	RO, LH	0x0	Retain	1 = The temperature has reached the threshold. 0 = The temperature is below the threshold.
5	One Shot Temperature Sample	R/W	0x0	Retain	This bit is valid only when 3.8042.15:14 == 2'b10. 1 = Temperature sense 0 = Idle
4:0	Reserved	RO	xx	xx	Set to 0s.

Table 69: Temperature Sensor Register 3 (Sheet 1 of 2)
Device 3, Register 0x8042

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Temperature Sense Enable	R/W	0x3	Retain	11 = Disable 10 = Use 3.8041.5. 00 = Sample every 1 second. 01 = Use sense rate on 3.8041.10:8.
13	Reserved	R/W	0x0	Retain	
12:11	Temperature Sensor Number of Samples to Average	R/W	0x1	Retain	00 = Average over 2^6 samples 01 = Average over 2^8 samples 10 = Average over 2^10 samples 11 = Average over 2^12 samples This register is ignored when 3.8041.15 = 1.
10:8	Temperature Sensor Sampling Rate	R/W	0x5	Retain	Sampling Rate 000 = Reserved 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = 2.36 ms 110 = 6.47 ms 111 = 11.93 ms

Table 69: Temperature Sensor Register 3 (Sheet 2 of 2)
Device 3, Register 0x8042

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Temperature Sensor Average Reading (8-bit)	RO	xx	xx	Temperature in C = 3.8042.7:0 - 75, that is, for 100^{o}C, the value is 10101111.

Table 70: Temperature Sensor Register 4
Device 3, Register 0x8043

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Temperature Interrupt Threshold	R/W	0x96	Retain	Temperature in C = 3.8043.15:8 - 75, that is, for 100^{o}C, the value is 10101111. If the temperature in register 3.8043.7:0 is equal or greater than this field, then the Temperature Sensor Interrupt register (3.FE17.8) will be set when the interrupt is enabled (3.FE16.8 = 1'b1).
7:0	Temperature Sensor Instantaneous Reading	RO	0x00	0x00	Instantaneous temperature reading based on sample rate specified in register 3.8042.10:8. Temperature in C = 3.8043.7:0 - 75, that is, for 100^{o}C, the value is 10101111. If the value in this register is equal or greater than register 3.8043.15:8, then the Temperature Sensor Interrupt register (3.FE17.8) will be set when the interrupt is enabled (3.FE16.8 = 1'b1).

Table 71: Interrupt Enable Register
Device 3, Register 0xFE16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x00	Retain	Reserved
8	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = Enable the interrupt pin to toggle. 0 = The interrupt is disabled.
7:0	Reserved	R/W	0x00	Retain	

Table 72: Interrupt Status Register
Device 3, Register 0xFE17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	RO	0x00	Retain	
8	Temperature Sensor Reached Threshold	RO, LH	0x0	Retain	Write 1 to clear the status, LH. 1 = The temperature has reached the threshold. 0 = The temperature is below the threshold.
7:0	Reserved	RO, LH	0x00	Retain	

Table 73: TDR Control Register
Device 3, Register 0xFEC3

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Enable TDR Function	R/W, SC	0x0	Retain	Enable TDR function, self-clearing.
12	Start TDR Test	R/W	0x0	Retain	1 = Start TDR test.
11:7	Set Amplitude	R/W	0x1F	Retain	This is the amplitude of generated pulse.
1:0	Set Width of Pulse	R/W	0x3	Retain	This is the width of the generated pulse.

Table 74: TDR Status Register 1
Device 3, Register 0xFEDB

Bits	Field	Mode	HW Rst	SW Rst	Description
10	TDR Test Over	RO	0x0	Retain	1 = TDR test over
9:0	TDR Distance	RO	0x000	Retain	TDR Distance

Table 75: TDR Status Register 2
Device 3, Register 0xFEDC

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	TDR Amplitude	RO	0x00	Retain	TDR Amplitude

Table 76: I/O Voltage Control Register
Device 4, Register 0x8214

Bits	Field	Mode	HW Rst	SW Rst	Description
15	VDDO Level	R/W	0x0	Retain	The VDDO supply voltage used when 1.8V is not used. The bit mapping is as follows: 0 = 3.3V 1 = 2.5V This register defaults to 0 (VDDO = 3.3V). If VDDO = 2.5V, then this bit must be programmed to 1.
14:0	Reserved	R/W	0x0000	Retain	

Table 77: LPSD Register 1
Device 3, Register 0x801C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0000	Retain	
2	LPSD Local Wake Status	RO	0x0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because a pulse was received at the WAKE_IN pin. 0 = The device did not power up due to a pulse received at the WAKE_IN pin.
1	LPSD Remote Wake Status	RO	0x0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because of the energy received at the MDIP/N pins. 0 = The device did not power up due to the energy received at the MDIP/N pins.
0	LPSD Power Down Enable	R/W	0x0	Retain	1 = Enable an LPSD power down. 0 = Do not enable an LPSD power down.

Table 78: LPSD Register 2
Device 3, Register 0x801D

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable LPSD Circuit Programming	R/W, SC	0x0	Retain	1 = Write digital register values to the LPSD circuit.
14:13	Set WAKE_IN Pulse Width	R/W	0x0	Retain	Allows for setting the pulse width needed at the WAKE_IN pin to power up the device after an LPSD power down. 00 = 10 µs 01 = 0.5 ms 10 = 4 ms 11 = 16 ms
12	Disable LPSD Local Wake Up	R/W	0x0	Retain	Disable LPSD local wake up after an LPSD power down. 1 = The device will not wake up if a pulse is received at the WAKE_IN pin. 0 = The device will wake up if a pulse is received at the WAKE_IN pin.
11	Disable LPSD Remote Wake Up	R/W	0x0	Retain	Disable LPSD remote wake up after an LPSD power down. 1 = The device will not wake up if energy is received at the MDIP/N pins. 0 = The device will wake up if energy is received at the MDIP/N pins.
10:0	Reserved	R/W	0x000	Retain	

Table 79: SQI Register
Device 3, Register 0xFC4C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x0	0	Reserved
9:0	SQI Measurement	RO	0x0	0	This is the averaged accumulative symbol slicer errors. It provides a quality metric of the received signal in PAM2 or PAM3 modes. It can be used to approximate the SNR observed at the slicer input.

3.3 IEEE PCS Registers

Table 80: IEEE PCS Registers — Register Map

Register Name	Register Address	Table and Page
PCS Control Register 1	Device 3, Register 0x0000	Table 81, p. 99
PCS Status Register 1	Device 3, Register 0x0001	Table 82, p. 100
PCS Device Identifier Register 1	Device 3, Register 0x0002	Table 83, p. 100
PCS Device Identifier Register 2	Device 3, Register 0x0003	Table 84, p. 100
PCS Devices In Package Register 1	Device 3, Register 0x0005	Table 85, p. 101
PCS Devices In Package Register 2	Device 3, Register 0x0006	Table 86, p. 101
PCS Status Register 2	Device 3, Register 0x0008	Table 87, p. 101
PCS Package Identifier Register 1	Device 3, Register 0x000E	Table 88, p. 102
PCS Package Identifier Register 2	Device 3, Register 0x000F	Table 89, p. 102
1000BASE-T1 PCS Status Register 2	Device 3, Register 0x0021	Table 90, p. 102
PCS Control Register	Device 3, Register 0x0900	Table 91, p. 102
PCS 1000BASE-T1 Status Register 1	Device 3, Register 0x0901	Table 92, p. 103
PCS 1000BASE-T1 Status Register 2	Device 3, Register 0x0902	Table 93, p. 103
OAM Register 0	Device 3, Register 0x0904	Table 94, p. 103
OAM Register 1	Device 3, Register 0x0905	Table 95, p. 104
OAM Register 2	Device 3, Register 0x0906	Table 96, p. 104
OAM Register 3	Device 3, Register 0x0907	Table 97, p. 104
OAM Register 4	Device 3, Register 0x0908	Table 98, p. 105
OAM Register 5	Device 3, Register 0x0909	Table 99, p. 105
OAM Register 6	Device 3, Register 0x090A	Table 100, p. 105
OAM Register 7	Device 3, Register 0x090B	Table 101, p. 105
OAM Register 8	Device 3, Register 0x090C	Table 102, p. 106
OAM Register 9	Device 3, Register 0x090D	Table 103, p. 106

Table 81: PCS Control Register 1 (Sheet 1 of 2)
Device 3, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x1	0x1	This bit will perform a software reset of the copper unit. 1 = Reset 0 = Normal
14	Loopback	R/W	0x0	Retain	1 = Loopback 0 = Normal
13	Speed Select	RO	0x0	0x0	BIT [6,13] = 10 - Operation at 1000BASE-T1 BIT [6,13] = 01 - Operation at 100BASE-T1
12	Reserved	RO	0x0	0x0	Set to 0.
11	Low Power	RO	Strap	Retain	This bit will power down the copper unit. 1 = Low Power mode 0 = Normal

Table 81: PCS Control Register 1 (Sheet 2 of 2)
Device 3, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
10:7	Reserved	RO	0x0	0x0	This bit has no effect. Write as 0.
6	Speed Select	RO	0x1	Retain	Set to 0.
5:0	Reserved	RO	0x00	0x00	Set to 0.

Table 82: PCS Status Register 1
Device 3, Register 0x0001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	0x0000	Set to 0000.
1	Low Power Ability	RO	0x1	0x1	1 = PCS supports Low Power mode. 0 = PCS does not support Low Power mode.
0	Reserved	RO	0x0	0x0	Set to 0.

Table 83: PCS Device Identifier Register 1
Device 3, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bits 3:18	RO	0x002B	0x002B	Bits 3:18 of the Marvell OUI

Table 84: PCS Device Identifier Register 2
Device 3, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bits 19:24	RO	0x02	0x02	Bits 19:24 of the Marvell OUI
9:4	Model Number	RO	0x18	0x18	The model number is 011000.
3:0	Revision Number	RO	See Description.	See Description.	This is the revision number. Refer to the Release Notes for more information.

Table 85: PCS Devices In Package Register 1
Device 3, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 00000000.
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation is present in the package. 0 = Auto-Negotiation is not present in the package.
6	Reserved	RO	0x0	0x0	Set to 0.
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS is present in the package. 0 = DTE XS is not present in the package.
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS is present in the package. 0 = PHY XS is not present in the package.
3	PCS Present	RO	0x1	0x1	1 = PCS is present in the package. 0 = PCS is not present in the package.
2	WIS Present	RO	0x0	0x0	1 = WIS is present in the package. 0 = WIS is not present in the package.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD is present in the package. 0 = PMA/PMD is not present in the package.
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers are present in the package. 0 = Clause 22 registers are not present in the package.

Table 86: PCS Devices In Package Register 2
Device 3, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor-specific Device 2 Present	RO	0x0	0x0	1 = A vendor-specific device 2 is present. 0 = A vendor-specific device 2 is not present.
14	Vendor-specific Device 1 Present	RO	0x0	0x0	1 = A vendor-specific device 1 is present. 0 = A vendor-specific device 1 is not present.
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000.

Table 87: PCS Status Register 2
Device 3, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = The device is responding to this address.
13:12	Reserved	RO	0x0	0x0	Set to 00.
11	Transmit Fault	RO, LH	0x0	0x0	1 = There is a fault on the Tx path. 0 = There is no fault on the Tx path.
10	Receive Fault	RO, LH	0x0	0x0	1 = There is a fault on the Rx path. 0 = There is no fault on the Rx path.
9:0	Reserved	RO	0x000	0x000	Set to 0000000.

Table 88: PCS Package Identifier Register 1
Device 3, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	Bits 3:18 of the Marvell OUI

Table 89: PCS Package Identifier Register 2
Device 3, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x02	0x02	Bits 19:24 of the Marvell OUI
9:4	Model Number	RO	0x18	See Description.	This is the same as 3.0003.9:4.
3:0	Revision Number	RO	See Description.	See Description.	This is the same as 3.0003.3:0.

Table 90: 1000BASE-T1 PCS Status Register 2
Device 3, Register 0x0021

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Setting 0.
14	Latched High Bit Error Rate	RO, LH	0x0	0x0	1 = PCS has reported a high BER. 0 = PCS has not reported a high BER.
13:8	Reserved	RO	0x00	0x00	Setting 0.
7:0	Errored Blocks Counter	RO, NR	0x00	0x00	Errored Blocks Counter The counter clears on read. The counter will peg at all 1s.

Table 91: PCS Control Register
Device 3, Register 0x0900

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x1	0x1	This bit will perform a software reset of the copper unit. 1 = Reset 0 = Normal
14	Loopback	R/W	0x0	Retain	1 = Loopback 0 = Normal
13:0	Reserved	RO	0x0000	0x0000	Setting 0.

Table 92: PCS 1000BASE-T1 Status Register 1
Device 3, Register 0x0901

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x0	0x0	Ignore when read.
7	Fault	RO	0x0	0x0	1 = There is a fault condition (pcs_tx_fault or pcs_rx_fault). 0 = There is no fault condition.
6:3	Reserved	RO	0x0	0x0	Ignore when read.
2	Link Status	RO, LL	0x0	0x0	1 = The PCS link is up. 0 = The PCS link is down.
1:0	Reserved	RO	0x0	0x0	Ignore when read.

Table 93: PCS 1000BASE-T1 Status Register 2
Device 3, Register 0x0902

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	0x00	Set to 0000.
10	Receive Link Status	RO	0x0	0x0	1 = The PCS receive link is up. 0 = The PCS receive link is down.
9	PCS High BER	RO	0x0	0x0	1 = The PCS is reporting a high BER. 0 = The PCS is not reporting a high BER.
8	Block Lock	RO	0x0	0x0	1 = The PCS is locked to received blocks. 0 = The PCS is not locked to received blocks.
7	Latched High BER	RO, LH	0x0	0x0	1 = The PCS has reported a high BER. 0 = The PCS has not reported a high BER.
6	Latched Block Lock	RO, LL	0x0	0x0	1 = The PCS has block lock. 0 = The PCS does not have block lock.
5:0	BER Counter	RO, NR	0x00	0x00	This is the BER counter.

Table 94: OAM Register 0 (Sheet 1 of 2)
Device 3, Register 0x0904

Bits	Field	Mode	HW Rst	SW Rst	Description
15	OAM Message Valid	RO	0x0	Retain	This bit is used to indicate message data in registers 3.904.11:8, 3.905, 3.906, 3.907, and 3.908 are valid and ready to be loaded. This bit must self clear when registers are loaded by the state machine. 1 = Message data in registers are valid. 0 = Message data in registers are not valid.
14	Toggle Value	RO	0x0	Retain	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.

Table 94: OAM Register 0 (Sheet 2 of 2)
Device 3, Register 0x0904

Bits	Field	Mode	HW Rst	SW Rst	Description
13	OAM Message Received	RO, LH	0x0	Retain	This bit must self clear on read. 1 = 1000BASE-T1 OAM message received by the link partner. 0 = 1000BASE-T1 OAM message not received the by link partner.
12	Receive Message Toggle Value	RO	0x0	Retain	Toggle value of message that was received by the link partner as indicated in 3.904.13.
11:8	Message Number	R/W	0x0	Retain	This is the user-defined message number to send.
7:4	Reserved	RO	0x0	Retain	
3	Ping Received	RO	0x0	Retain	Received Ping Tx value from latest good 1000BASE-T1 OAM frame received.
2	Ping Transmit	R/W	0x0	Retain	Ping value to send to the link partner.
1:0	Local SNR	RO	0x0	Retain	00 = NA 01 = LPI refresh is insufficient to maintain PHY SNR. Request the link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.

Table 95: OAM Register 1
Device 3, Register 0x0905

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 1	R/W	0x00	Retain	Message octet 1. LSB transmitted first.
7:0	OAM Message 0	R/W	0x00	Retain	Message octet 0. LSB transmitted first.

Table 96: OAM Register 2
Device 3, Register 0x0906

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 3	R/W	0x00	Retain	Message octet 3. LSB transmitted first.
7:0	OAM Message 2	R/W	0x00	Retain	Message octet 2. LSB transmitted first.

Table 97: OAM Register 3
Device 3, Register 0x0907

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 5	R/W	0x00	Retain	Message octet 5. LSB transmitted first.
7:0	OAM Message 4	R/W	0x00	Retain	Message octet 4. LSB transmitted first.

Table 98: OAM Register 4
Device 3, Register 0x0908

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 7	R/W	0x00	Retain	Message octet 7. LSB transmitted first.
7:0	OAM Message 6	R/W	0x00	Retain	Message octet 6. LSB transmitted first.

Table 99: OAM Register 5
Device 3, Register 0x0909

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LP OAM Message Valid	RO, SC	0x0	Retain	This bit is used to indicate message data in registers 3.909.11:8, 3.90A, 3.90B, 3.90C, and 3.90D are stored and ready to be read. This bit must self clear when register 3.2317 is read. 1 = Message data in registers are valid. 0 = Message data in registers are not valid.
14	Toggle Value	RO	0x0	Retain	Toggle value received with message.
13:12	Reserved	RO	0x0	Retain	
11:8	LP Message Number	RO	0x0	Retain	Message number from link partner
7:2	Reserved	RO	0x00	Retain	
1:0	Link Partner SNR	RO	0x0	Retain	00 = NA 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.

Table 100: OAM Register 6
Device 3, Register 0x090A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 1	RO	0x00	0x00	Message octet 1. LSB transmitted first.
7:0	Link OAM Message 0	RO	0x00	0x00	Message octet 0. LSB transmitted first.

Table 101: OAM Register 7
Device 3, Register 0x090B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 3	RO	0x00	0x00	Message octet 3. LSB transmitted first.
7:0	Link OAM Message 2	RO	0x00	0x00	Message octet 2. LSB transmitted first.

Table 102: OAM Register 8
Device 3, Register 0x090C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 5	RO	0x00	0x00	Message octet 5. LSB transmitted first.
7:0	Link OAM Message 4	RO	0x00	0x00	Message octet 4. LSB transmitted first.

Table 103: OAM Register 9
Device 3, Register 0x090D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 7	RO	0x00	0x00	Message octet 7. LSB transmitted first.
7:0	Link OAM Message 6	RO	0x00	0x00	Message octet 6. LSB transmitted first.

3.4 IEEE Auto-Negotiation Registers

Table 104: IEEE Auto-Negotiation Registers — Register Map

Register Name	Register Address	Table and Page
Auto-Negotiation Device Identifier Register 1	Device 7, Register 0x0002	Table 105, p. 107
Auto-Negotiation Device Identifier Register 2	Device 7, Register 0x0003	Table 106, p. 108
Auto-Negotiation Devices In Package Register 1	Device 7, Register 0x0005	Table 107, p. 108
Auto-Negotiation Devices In Package Register 2	Device 7, Register 0x0006	Table 108, p. 108
Auto-Negotiation Package Identifier Register 1	Device 7, Register 0x000E	Table 109, p. 109
Auto-Negotiation Package Identifier Register 2	Device 7, Register 0x000F	Table 110, p. 109
BASE-T1 Auto-Negotiation Control Register	Device 7, Register 0x0200	Table 111, p. 109
BASE-T1 Auto-Negotiation Status Register	Device 7, Register 0x0201	Table 112, p. 110
Auto-Negotiation Advertisement Register 1	Device 7, Register 0x0202	Table 113, p. 110
Auto-Negotiation Advertisement Register 2	Device 7, Register 0x0203	Table 114, p. 111
Auto-Negotiation Advertisement Register 3	Device 7, Register 0x0204	Table 115, p. 111
Link Partner Base Page Ability Register 1	Device 7, Register 0x0205	Table 116, p. 111
Link Partner Base Page Ability Register 2	Device 7, Register 0x0206	Table 117, p. 112
Link Partner Base Page Ability Register 3	Device 7, Register 0x0207	Table 118, p. 112
Next Page Transmit/Extended Next Page Transmit Register	Device 7, Register 0x0208	Table 119, p. 112
Extended Next Page Transmit Unformatted Code Field U0 to U15 Register	Device 7, Register 0x0209	Table 120, p. 113
Extended Next Page Transmit Unformatted Code Field U16 to U31 Register	Device 7, Register 0x020A	Table 121, p. 113
Link Partner Next Page/Link Partner Extended Next Page Ability Register	Device 7, Register 0x020B	Table 122, p. 113
Link Partner Extended Next Page Ability Unformatted Code Field U0 to U15 Register	Device 7, Register 0x020C	Table 123, p. 114
Link Partner Extended Next Page Ability Unformatted Code Field U16 to U31 Register	Device 7, Register 0x020D	Table 124, p. 114

Table 105: Auto-Negotiation Device Identifier Register 1
Device 7, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bits 3:18	RO	0x002B	0x002B	Bits 3:18 of the Marvell OUI

Table 106: Auto-Negotiation Device Identifier Register 2
Device 7, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bits 19:24	RO	0x02	0x02	Bits 19:24 of the Marvell OUI
9:4	Model Number	RO	0x18	0x18	Set to 011000.
3:0	Revision Number	RO	See Description.	See Description.	This is the revision number. Refer to the Release Notes for more information.

Table 107: Auto-Negotiation Devices In Package Register 1
Device 7, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 0000000000.
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation is present in the package. 0 = Auto-Negotiation is not present in the package.
6	Reserved	RO	0x0	0x0	Set to 0.
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS is present in the package. 0 = DTE XS is not present in package.
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS is present in the package. 0 = PHY XS is not present in the package.
3	PCS Present	RO	0x1	0x1	1 = PCS is present in the package. 0 = PCS is not present in the package.
2	WIS Present	RO	0x0	0x0	1 = WIS is present in the package. 0 = WIS is not present in the package.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD is present in the package. 0 = PMA/PMD is not present in the package.
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers are present in the package. 0 = Clause 22 registers are not present in the package.

Table 108: Auto-Negotiation Devices In Package Register 2
Device 7, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor-specific Device 2 Present	RO	cfg_vendor_two_pres_a	cfg_vendor_two_pres_a	1 = A vendor-specific device 2 is present. 0 = A vendor-specific device 2 is not present.
14	Vendor-specific Device 1 Present	RO	cfg_vendor_one_pres_a	cfg_vendor_one_pres_a	1 = A vendor-specific device 1 is present. 0 = A vendor-specific device 1 is not present.
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000.

Table 109: Auto-Negotiation Package Identifier Register 1
Device 7, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bits 3:18	RO	0x002B	0x002B	Bits 3:18 of the Marvell OUI

Table 110: Auto-Negotiation Package Identifier Register 2
Device 7, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bits 19:24	RO	0x02	0x02	Bits 19:24 of the Marvell OUI
9:4	Model Number	RO	0x18	See Description.	This is the same as 7.0003.9:4.
3:0	Revision Number	RO	See Description.	See Description.	This is the same as 7.0003.3:0.

Table 111: BASE-T1 Auto-Negotiation Control Register
Device 7, Register 0x0200

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x1	0x1	This bit will perform a software reset of the T-unit. 1 = Reset 0 = Normal
14:13	Reserved	RO	0x0	Retain	
12	Auto-Negotiation Enable	R/W	0x0	Retain	A change in this bit will cause Auto-Negotiation to restart. 1 = Enable the Auto-Negotiation process. 0 = Disable the Auto-Negotiation process.
11:10	Reserved	RO	0x0	Retain	
9	Restart Auto-Negotiation	R/W, SC	0x0	0x0	Setting this bit will cause Auto-Negotiation to restart. 1 = Restart the Auto-Negotiation process. 0 = Normal operation
8:0	Reserved	RO	0x000	0x000	

Table 112: BASE-T1 Auto-Negotiation Status Register Device 7, Register 0x0201

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	
6	Page Received	RO, LH	0x0	0x0	This bit is set when a new link code word has been received and is stored in registers 7.0019, 7.001A, and 7.001B if extended next pages are used, and in register 7.0019 if regular next pages are used. 1 = A new page has been received. 0 = A new page has not been received.
5	Auto-Negotiation Complete	RO	0x0	0x0	1 = The Auto-Negotiation process is complete. 0 = The Auto-Negotiation process is not complete.
4	Remote Fault	RO, LH	0x0	0x0	1 = A remote fault condition has been detected. 0 = A remote fault condition has not been detected.
3	Auto-Negotiation Ability	RO	0x1	0x1	1 = The PHY is able to perform Auto-Negotiation. 0 = The PHY is not able to perform Auto-Negotiation.
2	Link Status	RO, LL	0x0	0x0	This bit indicates whether link status was down since the last read. For the current link status, read this register back-to-back. 1 = The link is up. 0 = The link is down.
1:0	Reserved	RO	0x0	0x0	

Table 113: Auto-Negotiation Advertisement Register 1 Device 7, Register 0x0202

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	If 1000BASE-T1 is advertised or extended next page is advertised and enabled, then the required next pages are automatically transmitted. Register 7.0010.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
14	Acknowledge	RO	0x0	0x0	The value is always 0, writes are ignored.
13	Remote Fault	R/W	0x0	Retain	1 = Set the remote fault bit. 0 = Do not set the remote fault bit.
12	Enable Device in Force Mode During Auto-Negotiation	R/W	0x0	Retain	1 = Force master. 0 = Slave
11:10	Pause	R/W	0x0	Retain	This is used to advertise Pause capability; capability is not related to the PHY.
9:5	Echoed Nonce Field	R/W	0x00	Retain	
4:0	Selector Field	R/W	0x01	Retain	This is the selector field mode. 00001 = 802.3

Note

A write to register 7.202.15:0 does not take effect until any of the following occurs:

- There is a software reset (register 1.0000.15, 3.0000.15, 7.0200.15, or any other software reset).
- A low power (register 1.0000.11, 3.0000.11, or any other low power) transitions from low power down to normal operation.
- A Restart Auto-Negotiation is asserted (register 7.0200.9).
- Auto-Negotiation Enable toggles (register 7.0200.12).

Table 114: Auto-Negotiation Advertisement Register 2
Device 7, Register 0x0203

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Technology Ability Field	R/W	0x005	Retain	
4	Prefer Master	R/W	Strap	Retain	
3:0	Transmitted Nonce Field	R/W	0x0	Retain	

Note

This register is the same as 7.0202.

Table 115: Auto-Negotiation Advertisement Register 3
Device 7, Register 0x0204

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Technology Ability Field	R/W	0x0000	Retain	

Note

This register is the same as 7.0202.

Table 116: Link Partner Base Page Ability Register 1 (Sheet 1 of 2)
Device 7, Register 0x0205

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word bit 15 1 = The link partner is capable of next page. 0 = The link partner is not capable of next page.
14	Acknowledge	RO	0x0	0x0	Received Code Word bit 14 1 = The link partner received a link code word.

Table 116: Link Partner Base Page Ability Register 1 (Sheet 2 of 2)
Device 7, Register 0x0205

Bits	Field	Mode	HW Rst	SW Rst	Description
13	Remote Fault	RO	0x0	0x0	Received Code Word bit 13 1 = The link partner has detected a remote fault. 0 = The link partner has not detected a remote fault.
12	Force Master/Slave	RO	0x0	0x0	Received Code Word bit 12 1 = The link partner will force the master.
11:10	Pause	RO	0x0	0x0	Received Code Word bit 11 1 = The link partner requests an asymmetric pause. 0 = The link partner does not request an asymmetric pause.
9:5	Echoed Nonce Field	RO	0x00	0x00	This is the link partner Echoed Nonce field.
4:0	Selector Field	RO	0x00	0x00	This is the link partner Selector field.

Table 117: Link Partner Base Page Ability Register 2
Device 7, Register 0x0206

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Technology Ability Field	RO	0x000	Retain	This is the link partner Technology field.
4:0	Transmitted Nonce Field	RO	0x00	Retain	This is the link partner Echoed Nonce field.

Table 118: Link Partner Base Page Ability Register 3
Device 7, Register 0x0207

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Technology Ability Field	RO	0x0000	Retain	This is the link partner Technology Ability field.

Table 119: Next Page Transmit/Extended Next Page Transmit Register
Device 7, Register 0x0208

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	Transmit Code Word bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word bit 13
12	Acknowledge 2	R/W	0x0	0x0	Transmit Code Word bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word bits [10:0]

Note

A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded.
This register is used for regular next page exchange and extended next page exchange.
A link fail will clear register 7.0208.

Table 120: Extended Next Page Transmit Unformatted Code Field U0 to U15 Register Device 7, Register 0x0209

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	R/W	0x0000	0x0000	U15 to U0

Note

A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded, so register 7.0209 should be written before register 7.0208 is written.
This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.0209.

Table 121: Extended Next Page Transmit Unformatted Code Field U16 to U31 Register Device 7, Register 0x020A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	R/W	0x0000	0x0000	U31 to U16

Note

A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded, so register 7.020A should be written before register 7.0208 is written.
This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.020A.

Table 122: Link Partner Next Page/Link Partner Extended Next Page Ability Register Device 7, Register 0x020B

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Receive Code Word bit 15
14	Acknowledge	RO	0x0	0x0	Receive Code Word bit 14
13	Message Page	RO	0x0	0x0	Receive Code Word bit 13
12	Acknowledge 2	RO	0x0	0x0	Receive Code Word bit 12
11	Toggle	RO	0x0	0x0	Receive Code Word bit 11
10:0	Message/Unformatted Field	RO	0x000	0x000	Receive Code Word bits [10:0]

Note

This register is used for regular next page exchange and extended next page exchange.
A link fail will clear register 7.020B.

Table 123: Link Partner Extended Next Page Ability Unformatted Code Field U0 to U15 Register Device 7, Register 0x020C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	RO	0x0000	0x0000	U15 to U0

Note

This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.020C.

Table 124: Link Partner Extended Next Page Ability Unformatted Code Field U16 to U31 Register Device 7, Register 0x020D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	RO	0x0000	0x0000	U31 to U16

Note

This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.020D.

3.5 100BASE-T1 Copper Unit Advance PCS Registers

Table 125: 100BASE-T1 Copper Unit Advance PCS Registers — Register Map

Register Name	Register Address	Table and Page
100BASE-T1 Copper Control Register	Device 3, Register 0x8100	Table 126, p. 116
100BASE-T1 Status Register	Device 3, Register 0x8108	Table 127, p. 116
100BASE-T1 Status Register	Device 3, Register 0x8109	Table 128, p. 117
100BASE-T1 Specific Interrupt Enable Register	Device 3, Register 0x8112	Table 129, p. 117
Copper Interrupt Status Register	Device 3, Register 0x8113	Table 130, p. 118
Interrupt Status Register	Device 3, Register 0x8117	Table 131, p. 118
Link Drop Counter Register	Device 3, Register 0x8120	Table 132, p. 118
MAC Specific Control Register	Device 3, Register 0x8210	Table 133, p. 119
MAC Specific Interrupt Enable Register	Device 3, Register 0x8212	Table 134, p. 119
MAC Specific Status Register	Device 3, Register 0x8213	Table 135, p. 119
Tx FIFO Overflow/Underflow Counter Register	Device 3, Register 0x8214	Table 136, p. 120
Counter Control Register	Device 3, Register 0x8220	Table 137, p. 120
Bad Link Counter Register	Device 3, Register 0x8221	Table 138, p. 120
Bad SSD Counter Register	Device 3, Register 0x8222	Table 139, p. 120
Bad ESD Counter Register	Device 3, Register 0x8223	Table 140, p. 121
Rx Error Counter Register	Device 3, Register 0x8224	Table 141, p. 121
Receiver Status Register	Device 3, Register 0x8230	Table 142, p. 121
Interrupt Enable Register	Device 3, Register 0x8300	Table 143, p. 122
Interrupt Status Register	Device 3, Register 0x8301	Table 144, p. 122
GPIO/TX_ENABLE Control Register	Device 3, Register 0x8302	Table 145, p. 122
GPIO/TX_ENABLE Control Register	Device 3, Register 0x8303	Table 146, p. 123
GPIO/TX_ENABLE Control Register	Device 3, Register 0x8304	Table 147, p. 123
GPIO/LED Control Register	Device 3, Register 0x8305	Table 148, p. 124
LED Function Control Register	Device 3, Register 0x8310	Table 149, p. 124
LED Polarity Control Register	Device 3, Register 0x8311	Table 150, p. 125
LED Timer/INTn Control Register	Device 3, Register 0x8312	Table 151, p. 126
Copper Port Packet Generation Register	Device 3, Register 0x8610	Table 152, p. 126
Copper Port Packet Size Register	Device 3, Register 0x8611	Table 153, p. 127
Checker Control Register	Device 3, Register 0x8612	Table 154, p. 127
Packet Generator Control Register	Device 3, Register 0x8613	Table 155, p. 127
Copper Port Packet Counter Register	Device 3, Register 0x8614	Table 156, p. 128
Copper Port CRC Counter Register	Device 3, Register 0x8615	Table 157, p. 128
BIST Control Register	Device 3, Register 0x8617	Table 158, p. 128
BIST Status Register	Device 3, Register 0x8618	Table 159, p. 128
BIST Counters Register	Device 3, Register 0x8619	Table 160, p. 128

Table 126: 100BASE-T1 Copper Control Register Device 3, Register 0x8100

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14	Copper Line Loopback	R/W	0x0	0x0	1 = Enable the loopback of MDI to MDI. 0 = Normal operation
13:10	Reserved	R/W	0x0	Retain	
9	PCS Automatic Polarity Detection and Correction	R/W	0x0	Retain	When this bit is a 1 and the PCS is slave, the PCS Rx will detect the polarity, and correct the Rx polarity if a polarity swap is observed. In addition, it will also reverse the polarity on the Tx. The detected Rx polarity status is shown in 3.8109.1.
8:2	Reserved	R/W	0x00	Retain	
1	Tx Polarity Reversal Enable	R/W	0x0	Retain	1 = Tx PCS polarity is reversed. 0 = Tx PCS polarity is not reversed.
0	Disable Jabber	R/W	0x0	Retain	1 = Disable the jabber function. 0 = Enable the jabber function.

Table 127: 100BASE-T1 Status Register Device 3, Register 0x8108

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14	Master/Slave Configuration Resolution	RO	0x0	0x0	1 = The local PHY configuration is resolved to the master. 0 = The local PHY configuration is resolved to the slave.
13	Local Receiver Status	RO	0x0	0x0	1 = The local receiver is OK. 0 = The local receiver is not OK.
12	Remote Receiver Status	RO	0x0	0x0	1 = The remote receiver is OK. 0 = The remote receiver is not OK.
11:10	Reserved	RO	Always 0x0	Always 0x0	
9	Copper Link Status	RO, LL	0x0	0x0	This register bit indicates when link was down since the last read. For the current link status, either read this register back-to-back or read register 3.8109.2 (Copper Link Real Time). 1 = The link is up. 0 = The link is down.
8	Jabber Detect	RO, LH	0x0	0x0	1 = A jabber condition is detected. 0 = A jabber condition is not detected.
7:0	Idle Error Count	RO, ROC	0x00	Retain	MSB of Idle Error Counter These bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 128: 100BASE-T1 Status Register
Device 3, Register 0x8109

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	R/W	0x0	Retain	
3	Auto-Negotiation Resolved	RO	0x0	0x0	1 = The Auto-Negotiation is resolved. 0 = The Auto-Negotiation is not resolved.
2	Copper Link (Real Time)	RO	0x0	0x0	1 = The link is up. 0 = The link is down.
1	Polarity (Real Time)	RO	0x0	0x0	1 = Reversed 0 = Normal This bit is only valid when 3.8100.9 is 1.
0	Jabber (Real Time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

Table 129: 100BASE-T1 Specific Interrupt Enable Register
Device 3, Register 0x8112

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
7:2	Reserved	R/W	0x0	Retain	
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.

Table 130: Copper Interrupt Status Register Device 3, Register 0x8113

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	
10	Copper Link Status Changed	RO, LH	0x0	0x0	1 = The link status has changed. 0 = The link status has not changed.
9	Copper Symbol Error	RO, LH	0x0	0x0	1 = There is a symbol error. 0 = There is no symbol error.
8	Copper False Carrier	RO, LH	0x0	0x0	1 = There is a false carrier. 0 = There is no false carrier.
7:2	Reserved	RO	0x0	0x0	
1	Polarity Changed	RO, LH	0x0	0x0	1 = The polarity has changed. 0 = The polarity has not changed.
0	Jabber	RO, LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 131: Interrupt Status Register Device 3, Register 0x8117

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	0x0000	Reserved
0	Port 0 Interrupt	RO	0x0	0x0	If there is at least 1 copper port, then this bit indicates port 0's interrupt status; otherwise, it is invalid. 1 = An interrupt is active on port 0. 0 = No interrupt is active on port 0.

Table 132: Link Drop Counter Register Device 3, Register 0x8120

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x0C	Retain	
7:0	Link Drop Counter	RO, ROC	0x00	Retain	This counter increments every time the link transitions from up to down. The counter saturates at 0xFF (maximum value) and is cleared when read.

Table 133: MAC Specific Control Register
Device 3, Register 0x8210

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Copper Tx FIFO Depth	R/W	0x1	Retain	00 = This supports 10 KB at ±100 ppm. 01 = This supports 15 KB at ±100 ppm. 10 = This supports 20 KB at ±100 ppm. 11 = This supports 25 KB at ±100 ppm.
13:2	Reserved	R/W	0x00	Retain	
1	Phase FIFO Mode Enable	R/W	0x0	Retain	1 = Enable
0	Shallow FIFO Mode Enable	R/W	0x0	Retain	1 = Enable

Table 134: MAC Specific Interrupt Enable Register
Device 3, Register 0x8212

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
6:4	Reserved	R/W	0x0	Retain	
3	FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
2	FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
1:0	Reserved	R/W	0x0	Retain	

Table 135: MAC Specific Status Register
Device 3, Register 0x8213

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 0x00	Always 0x00	
7	FIFO Over/Underflow	RO, LH	0x0	0x0	1 = There is an overflow/underflow error 0 = There is no FIFO error.
6:4	Reserved	RO	Always 0x0	Always 0x0	
3	FIFO Idle Inserted	RO, LH	0x0	0x0	1 = Idle is inserted. 0 = No idle is inserted.
2	FIFO Idle Deleted	RO, LH	0x0	0x0	1 = Idle is deleted. 0 = Idle is not deleted.
1:0	Reserved	RO	Always 0x0	Always 0x0	

Table 136: Tx FIFO Overflow/Underflow Counter Register
Device 3, Register 0x8214

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Tx FIFO Over/Underflow Counter	RO, ROC	0x0000	Retain	This is a 16-bit counter for Tx FIFO overflow/underflow error. The counter saturates at 0xFFFF (maximum value) and will clear on read.

Table 137: Counter Control Register
Device 3, Register 0x8220

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0	Retain	
1	Bad Link/SDD/ESD Counter Control	R/W	0x0	Retain	This controls the counters in registers 3.8221 to 3.8223. 1 = The counters count the number of cycles. 0 = The counters count the number of events.
0	Rx Error Counter Control	R/W	0x0	Retain	This controls the counters in register 3.8224. 1 = The counters count the number of cycles. 0 = The counters count the number of events.

Table 138: Bad Link Counter Register
Device 3, Register 0x8221

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad Link Counter	RO, ROC	0x00	Retain	If register 3.8220.1 = 1, then it counts each cycle of RX_ER assertion in the LINK FAILED state. If register 3.8220.1 = 0, then it counts each event of RX_ER assertion in the LINK FAILED state. The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 139: Bad SSD Counter Register
Device 3, Register 0x8222

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad SSD Counter	RO, ROC	0x00	Retain	If 3.8220.1 = 1, then it counts each cycles of RX_ER assertion in the BAD SSD state. If 3.8220.1 = 0, then it counts each events of RX_ER assertion in the BAD SSD state. The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 140: Bad ESD Counter Register
Device 3, Register 0x8223

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad ESD Counter	RO, ROC	0x00	Retain	If register 3.8220.1 = 1, then it counts each cycle of RX_ER assertion in the BAD ESD2, BAD END, and Rx ERROR states. If register 3.8220.1 = 0, then it counts each event of RX_ER assertion in the BAD ESD2, BAD END, and Rx ERROR states. The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 141: Rx Error Counter Register
Device 3, Register 0x8224

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Rx Error Counter	RO, ROC	0x00	Retain	If register 3.8220.0 = 1, then it counts each cycle of RX_ER assertion in the 25 MHz domain. If register 3.8220.0 = 0, then it counts each event of RX_ER assertion in the 25 MHz domain. The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 142: Receiver Status Register
Device 3, Register 0x8230

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	SQI Level	RO, ROC	0x0	0x0	This is the Signal Quality Index. The SQI level is listed from 0 to 15 in accordance with the ascending signal quality. The SQI level is reported as 0 during the link up process and if there is no link up.
11:6	Reserved	RO, ROC	0x00	0x00	
5	Link Status	RO, ROC	0x0	0x0	1 = The link status is OK.
4	Remote Receiver Status	RO, ROC	0x0	0x0	1 = The remote receiver status is OK.
3	Local Receiver Status	RO, ROC	0x0	0x0	1 = The local receiver status is OK.
2	Polarity Done Status	RO, ROC	0x0	0x0	1 = The polarity is done.
1	Alignment Done Status	RO, ROC	0x0	0x0	1 = The alignment is done.
0	Descrambler Lock Status	RO, ROC	0x0	0x0	1 = The descrambler is locked.

Table 143: Interrupt Enable Register
Device 3, Register 0x8300

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x000	Retain	
1	TX_ENABLE Interrupt Enable	R/W	0x0	Retain	1 = Enable
0	GPIO Interrupt Enable	R/W	0x0	Retain	1 = Enable

Table 144: Interrupt Status Register
Device 3, Register 0x8301

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO, LH	0x000	0x000	
1	TX_ENABLE Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
0	GPIO Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.

Table 145: GPIO/TX_ENABLE Control Register
Device 3, Register 0x8302

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	TX_ENABLE Data	R/W	0x0	Retain	This bit has no effect unless register 3.8304.3 = 1. When 3.8303.1 = 0, a read to this register will reflect the state of the TX_ENABLE pin and a write will write the output register, but have no effect on the TX_ENABLE pin. When 3.8303.1 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the TX_ENABLE pin.
0	GPIO Data	R/W	0x0	Retain	This bit has no effect unless register 3.8304.11 = 1. When 3.8303.0 = 0, a read to this register will reflect the state of the GPIO pin and a write will write the output register, but have no effect on the GPIO pin. When 3.8303.0 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the GPIO pin.

Table 146: GPIO/TX_ENABLE Control Register Device 3, Register 0x8303

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	TX_ENABLE Pin Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8304.3 = 1. 0 = Input 1 = Output
0	GPIO Pin Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8304.11 = 1. 0 = Input 1 = Output

Table 147: GPIO/TX_ENABLE Control Register Device 3, Register 0x8304

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	
11	GPIO Pin Function	R/W	0x0	Retain	GPIO Pin Function 0 = GPIO is used for an LED function. 1 = GPIO is used for a GPIO function.
10:8	GPIO Interrupt Select	R/W	0x0	Retain	The interrupt is effective only when 3.8303.0 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low
7:4	Reserved	R/W	0x0	Retain	
3	TX_ENABLE Pin Function	R/W	0x0	Retain	This is the TX_ENABLE Pin Function. 0 = TX_ENABLE pin is used for LED function. 1 = TX_ENABLE pin is used for GPIO function.
2:0	TX_ENABLE Interrupt Select	R/W	0x0	Retain	The interrupt is effective only when 3.8303.1 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low

Table 148: GPIO/LED Control Register Device 3, Register 0x8305

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0	Retain	
1	TX_ENABLE Open Drain Control	R/W	0x0	Retain	1 = Open drain I/O
0	GPIO Open Drain Control	R/W	0x0	Retain	1 = Open drain I/O

Table 149: LED Function Control Register Device 3, Register 0x8310

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x0	0x0	
7:4	GPIO Pin Control for LED Functionality	R/W	0x1	Retain	The GPIO pin must be configured in LED function mode, otherwise 3.8310.7:4 has no effect. 0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = Reserved 0110 = On - 100 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
3:0	TX_ENABLE Pin Control for LED Functionality	R/W	0x1	Retain	The TX_ENABLE pin must be configured in LED function mode, otherwise register 3.8310.3:0 has no effect. 0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 2 blinks - 100 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = Reserved 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

Table 150: LED Polarity Control Register
Device 3, Register 0x8311

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	GPIO Pin Mix Percentage for LED Functionality	R/W	0x8	Retain	This register is only used when GPIO is configured in LED function mode. When using two-terminal bi-color LEDs, the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
11:8	TX_ENABLE Pin Mix Percentage for LED Functionality	R/W	0x8	Retain	This register is only used when TX_ENABLE is configured in LED function mode. When using two-terminal bi-color LEDs, the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
7:4	Reserved	R/W	0x0	Retain	
3:2	GPIO Pin Polarity for LED Functionality	R/W	0x0	Retain	This register is only used when GPIO is configured in LED function mode. 00 = On - drive GPIO low, Off - drive GPIO High 01 = On - drive GPIO high, Off - drive GPIO Low 10 = On - drive GPIO low, Off - tri-state GPIO 11 = On - drive GPIO high, Off - tri-state GPIO
1:0	TX_ENABLE Pin Polarity For LED Functionality	R/W	0x0	Retain	This register is only used when TX_ENABLE is configured in LED function mode. 00 = On - drive LED low, Off - drive LED High 01 = On - drive LED high, Off - drive LED Low 10 = On - drive LED low, Off - tri-state LED 11 = On - drive LED high, Off - tri-state LED

Table 151: LED Timer/INTn Control Register
Device 3, Register 0x8312

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INTn	R/W	0x0	Retain	1 = The INTn pin was forced to be asserted. 0 = Normal operation
14:12	Pulse Stretch Duration	R/W	0x4	Retain	000 = No pulse stretching 001 = 21 to 42 ms 010 = 42 to 84 ms 011 = 84 to 170 ms 100 = 170 to 340 ms 101 = 340 to 670 ms 110 = 670 ms to 1.3s 111 = 1.3 to 2.7s
11	Interrupt Polarity	R/W	0x1	Retain	0 = Interrupt active high 1 = Interrupt active low
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:4	Reserved	R/W	0x0	Retain	
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

Table 152: Copper Port Packet Generation Register (Sheet 1 of 2)
Device 3, Register 0x8610

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7	Packet Generator Transmit Trigger	R/W	0x0	Retain	This bit is only valid when all of the following are true: • bit 6 =1 • bit 3 =1 • 3.8611.15:0 is not equal to all 0s A read of this bit gives the following: 1 = Packet generator transmit is done. 0 = Packet generator is transmitting data. When this bit is 1, a write of 0 will trigger the packet generator to transmit again. When this bit is 0, a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self Clear Control	R/W	0x0	Retain	0 = Bit 3 will self-clear after all packets are sent. 1 = Bit 3 will stay high after all packets are sent.

Table 152: Copper Port Packet Generation Register (Sheet 2 of 2)
Device 3, Register 0x8610

Bits	Field	Mode	HW Rst	SW Rst	Description
5	Reserved	R/W	0x0	Retain	
4	Enable CRC Checker	R/W	0x0	Retain	1 = Enable 0 = Disable
3	Enable Packet Generator	R/W	0x0	Retain	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = For 10/100/1000 Mbps = A5, 5A, A5, 5A
1	Length of Packet to Transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored Packet	R/W	0x0	Retain	1 = Tx packets with CRC errors and symbol error 0 = No error

Table 153: Copper Port Packet Size Register
Device 3, Register 0x8611

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Burst	R/W	0x0000	Retain	0x0000 = Continuous 0x01 to 0xFFFF = Burst 1 to 65535 packets

Table 154: Checker Control Register
Device 3, Register 0x8612

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	Retain	Reserved
4	CRC Counter Reset	R/W, SC	0x0	0x0	1 = Reset This bit will self-clear after write to 1.
3:0	Reserved	R/W	0x0	Retain	Reserved

Table 155: Packet Generator Control Register
Device 3, Register 0x8613

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Packet Generator Constant Payload Enable	R/W	0x0	Retain	1 = The payload of the packet controlled by 3.8613.14 when packet generator is enabled. 0 = The payload of the packet controlled by 3.8610.2 when packet generator is enabled.
14	Packet Generator Constant Payload Value	R/W	0x0	Retain	1 = All 1s in the payload when 3.8613.15 = 1 0 = All 0s in the payload when 3.8613.15 = 1
13:8	Reserved	R/W	0x00	Retain	
7:0	Packet Generator Inter-Packet Gap	R/W	0x0B	Retain	This value plus 1 is IPG in bytes.

Table 156: Copper Port Packet Counter Register
Device 3, Register 0x8614

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Count	RO	0x0000	Retain	0x0000 = No packets were received. 0xFFFF = 65535 packets were received (maximum count). Bit 3.8610.4 must be set to 1 for this field to be valid.

Table 157: Copper Port CRC Counter Register
Device 3, Register 0x8615

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	CRC Error Count	RO	0x0000	Retain	0x0000 = No CRC errors were detected in the packets received. 0xFFFF = 65535 CRC errors were detected in the packets received (maximum count). Bit 3.8610.4 must be set to 1 for this field to be valid.

Table 158: BIST Control Register
Device 3, Register 0x8617

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W, SC	0x0000	Retain	
0	BIST Enable	R/W, SC	0x0	Retain	1 = BIST enable 0 = BIST disable

Table 159: BIST Status Register
Device 3, Register 0x8618

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0000	Retain	
2:0	BIST Status	RO	0x0	Retain	0x0 = Not started 0x1 = In progress 0x4 = Aborted 0x6 = No error 0x7 = Error

Table 160: BIST Counters Register
Device 3, Register 0x8619

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	BIST Packet Count	RO, ROC	0x00	Retain	0x00 = No packets were received. 0xFF = 256 packets were received (maximum count) Bit 3.8617.0 must be set to 1 for this field to be valid.
7:0	BIST Error Count	RO, ROC	0x00	Retain	0x00 = No CRC errors were detected in the received packets. 0xFF = 256 CRC errors were detected in the received packets (maximum count). Bit 3.8617.0 must be set to 1 for this field to be valid.

3.6 1000BASE-T1 Copper Unit Advance PCS Registers

Table 161: 1000BASE-T1 Copper Unit Advance PCS Registers — Register Map

Register Name	Register Address	Table and Page
GPIO Data Register	Device 3, Register 0x8012	Table 162, p. 129
GPIO Function and Interrupt Tri-state Control Register	Device 3, Register 0x8013	Table 163, p. 130
GPIO Interrupt Register	Device 3, Register 0x8014	Table 164, p. 131
Open Drain Control Register	Device 3, Register 0x8015	Table 165, p. 132
Function Control Register	Device 3, Register 0x8016	Table 166, p. 132
LED [1:0] Polarity Control Register	Device 3, Register 0x8017	Table 167, p. 133
LED Timer Control Register	Device 3, Register 0x8018	Table 168, p. 134
PCS Control Register	Device 3, Register 0xFD00	Table 169, p. 135
Packet Generator Control Register	Device 3, Register 0xFD04	Table 170, p. 135
Packet Generator Parameters Register	Device 3, Register 0xFD05	Table 171, p. 136
Packet Checker Control Register	Device 3, Register 0xFD07	Table 172, p. 136
Packet Checker Count Register	Device 3, Register 0xFD08	Table 173, p. 136
Tx FIFO Control Register	Device 3, Register 0xFD20	Table 174, p. 136

Table 162: GPIO Data Register (Sheet 1 of 2)
Device 3, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	R/W	0x0	Retain	
13:3	Tst_led Lane Select	R/W	0x000	Retain	When 3.8012.11 = 0: 0x - Output 4 LSB of tst_led 1x - Output 4 MSB of tst_led When 3.812.11 = 1: 00 - Output bits [1:0] of tst_led 01 - Output bits [3:2] of tst_led 10 - Output bits [5:4] of tst_led 11 - Output bits [7:6] of tst_led
2	LED [1] Data	R/W	0x0	Retain	This bit has no effect unless register 3.8014.7 = 1. When 3.8013.2 = 0, a read to this register will reflect the state of the LED [1] pin, and a write will write the output register, but have no effect on the LED [1] pin. When 3.8013.2= 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the LED [1] pin.
1	LED [0] Data	R/W	0x0	Retain	This bit has no effect unless register 3.8014.3 = 1. When 3.8013.1 = 0, a read to this register will reflect the state of the LED [0] pin and a write will write the output register, but have no effect on the LED [0] pin. When 3.8013.1 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the LED [0] pin.

Table 162: GPIO Data Register (Sheet 2 of 2)
Device 3, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
0	GPIO Data	R/W	0x0	Retain	When 3.8013.0 = 0, a read to this register will reflect the state of the GPIO pin, and a write will write the output register, but have no effect on the GPIO pin. When 3.8013.0 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the GPIO pin.

Table 163: GPIO Function and Interrupt Tri-state Control Register (Sheet 1 of 2)
Device 3, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x000	Retain	Set to 0s.
11	Tri-state on Interrupt Pin	R/W	0x0	Retain	0 = Tri-state is enabled; the interrupt pin is configured as an input. 1 = Tri-state is disabled.
10	Observe LED on GPIO	R/W	0x1	Retain	1 = The LED pin is driven on GPIO. 0 = The LED is not driven on GPIO.
9	Open Drain Control	R/W	0x0	Retain	INT open drain control 1 = This is an open drain I/O where the output is driven LOW for an active interrupt and tri-stated for an inactive one and there would be an external pull-up to drive the line HIGH.
8	Open Source Control	R/W	0x0	Retain	INT open source control 1 = This is an open source I/O where the output is driven HIGH for an active interrupt and tri-stated for an inactive one and there would be an external pull-down to drive the line LOW.
7	LED/GPIO Data from 1000BASE_T1 Valid	R/W	0x0	Retain	0 = If bit 6 is set, then overwrite mode so that LED/GPIO value should be from 100BASE-T1 LED registers. 1 = If bit 6 is set, then overwrite mode so that LED/GPIO value should be from 1000BASE-T1 LED/GPIO register.
6	LED/GPIO Overwrite Control	R/W	0x0	Retain	This is the LED/GPIO value from 100 or 1000BASE-T1 based on bit 7.
5	LED Drive Ability	R/W	0x0	Retain	Fast LED mode 0 = LED pads drive LEDs. 1 = LED pads can drive fast signals.
4	GPIO [0] Functionality	R/W	0x0	Retain	GPIO [0] functionality GPIO [0] will either take over the final function of LED [1] or remain GPIO as the 1000BASE-T1 had one LED only. 0 = GPIO [0] 1 = LED [1]
3	LED [0] Functionality	R/W	0x0	Retain	LED [0] functionality LED [0] will either take over the final function of LED [1] or remain LED [0] as the 1000BASE-T1 had one LED only. 0 = LED [0] 1 = LED [1]

Table 163: GPIO Function and Interrupt Tri-state Control Register (Sheet 2 of 2)
Device 3, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
2	LED [1] Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8014.7 = 1. 0 = Input 1 = Output
1	LED [0] Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8014.3 = 1. 0 = Input 1 = Output
0	GPIO [0] Output Enable	R/W	0x1	Retain	0 = Input 1 = Output

Table 164: GPIO Interrupt Register
Device 3, Register 0x8014

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	R/W	0x00	Retain	
10:8	GPIO [0] Select	R/W	0x0	Retain	Interrupt is effective only when 3.8013.0 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low
7	LED [1] Function	R/W	0x0	Retain	0 = LED [1] is used for an LED function. 1 = LED [1] is used for a GPIO function.
6:4	LED[1] Select	R/W	0x0	Retain	Interrupt is effective only when 3.8013.5 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low
3	LED [0] Function	R/W	0x0	Retain	0 = LED [0] is used for an LED function. 1 = LED [0] is used for a GPIO function.
2:0	LED [0] Select	R/W	0x0	Retain	Interrupt is effective only when 3.8013.4 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low

Table 165: Open Drain Control Register
Device 3, Register 0x8015

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RW	0x00	Retain	
9:8	Slew Rate Left Side I/O Pads	RW	0x3	Retain	Slew Rate for Left Side I/O Pads - GPIO, TX_ENABLE, and so on Fastest slew rate to slowest: 11, 10, 01, 00
7:4	Reserved	RW	0x3	Retain	
3	Reserved	RW	0x0	Retain	
2	LED [1] Open Drain Control	RW	0x0	Retain	1 = Open drain I/O
1	LED [0] Open Drain Control	RW	0x0	Retain	1 = Open drain I/O
0	GPIO Open Drain Control	RW	0x0	Retain	1 = Open drain I/O

Table 166: Function Control Register (Sheet 1 of 2)
Device 3, Register 0x8016

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7:4	LED [1] Control	R/W	0x7	Retain	If 3.0x8016.3:2 is set to 11, then 3.0x8016.7:4 has no effect. 0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - SGMII Link, Off - Else 0110 = On - 1000 Mbps Link, Off - Else 0111 = Reserved 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved

Table 166: Function Control Register (Sheet 2 of 2)
Device 3, Register 0x8016

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	LED [0] Control	R/W	0x1	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

Table 167: LED [1:0] Polarity Control Register
Device 3, Register 0x8017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LED [1] Mix Percentage	R/W	0x8	Retain	When using two terminal bi-color LEDs, the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
11:8	LED [0] Mix Percentage	R/W	0x8	Retain	When using two-terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
7:4	Reserved	R/W	0x0	Retain	
3:2	LED [1] Polarity	R/W	0x0	Retain	00 = On - Drive LED [1] low, Off - Drive LED [1] high 01 = On - Drive LED [1] high, Off - Drive LED [1] low 10 = On - Drive LED [1] low, Off - Tri-state LED [1] 11 = On - Drive LED [1] high, Off - Tri-state LED [1]
1:0	LED [0] Polarity	R/W	0x0	Retain	00 = On - Drive LED [0] low, Off - Drive LED [0] high 01 = On - Drive LED [0] high, Off - Drive LED [0] low 10 = On - Drive LED [0] low, Off - Tri-state LED [0] 11 = On - Drive LED [0] high, Off - Tri-state LED [0]

Table 168: LED Timer Control Register
Device 3, Register 0x8018

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INT	R/W	0x0	0x0	1 = The int_out_s pin is forced to be asserted. 0 = Normal operation
14:12	Pulse Stretch Duration	R/W	0x4	Retain	000 = No pulse stretching 001 = 21 to 42 ms 010 = 42 to 84 ms 011 = 84 to 170 ms 100 = 170 to 340 ms 101 = 340 to 670 ms 110 = 670 ms to 1.3s 111 = 1.3 to 2.7s
11	Interrupt Polarity	R/W	0x1	Retain	0 = Interrupt active high 1 = Interrupt active low
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:6	Reserved	R/W	0x0	Retain	
5	Timer Speed Up	R/W	0x0	Retain	Internal test mode: Timer Speed Up 1 = Speed up timer. 0 = Normal operation
4	Bypass LED Blinker	R/W	0x0	Retain	Internal test mode: Bypass LED Blinker 1 = Bypass led blinker. 0 = Normal operation
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

Table 169: PCS Control Register
Device 3, Register 0xFD00

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	R/W	0x7	Retain	Reserved
12:7	PCS Host Config	R/W	0x00	0x00	GMII data steering as shown in Figure 13, Data Steering around GMII Interface. Bits 12, 11 (MUX C in Figure 13) 0x = Line Rx to packet checker 10 = Host Tx to packet checker 11 = Packet generator to packet checker Bits 10, 9 (MUX B in Figure 13) 0x = Host Tx to line Tx 10 = Line Rx to line Tx 11 = Packet generator to line Tx Bits 8, 7 (MUX A in Figure 13) 0x = Line Rx to host Rx 10 = Host Tx to host Rx 11 = Packet generator to host Rx
6:0	Reserved	R/W	0x00	0x00	Reserved

Table 170: Packet Generator Control Register
Device 3, Register 0xFD04

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	0x00	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7	Packet Generator Transmit Trigger	R/W, SS	0x0	0x0	This bit is only valid when all of the following are true: • Bit 6 = 1. • Bit 3 = 1. • Bits [15:8] are not equal to all 0s. A read of this bit gives the following: • 1 = Packet generator transmit is done. • 0 = Packet generator is transmitting data. When this bit is 1, a write of 0 will trigger the packet generator to transmit again. When this bit is 0, a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self Clear Control	R/W	0x0	0x0	0 = Bit 3 will self-clear after all packets are sent. 1 = Bit 3 will stay high after all packets are sent.
5:4	Reserved	RO	0x0	0x0	
3	Enable Packet Generator	R/W, SC	0x0	0x0	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	0x0	0 = Pseudo-random 1 = 5A, A5, 5A, A5, and so on
1	Length of Packet to Transmit	R/W	0x0	0x0	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored Packet	R/W	0x0	0x0	1 = Tx packets with CRC errors and symbol error 0 = No error

Table 171: Packet Generator Parameters Register Device 3, Register 0xFD05

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Constant Packet Payload Enable	R/W	0x0	0x0	Enables a constant payload for packets generated by the packet generator. 1 = Enable constant packet payload. 0 = Use other payload options.
14	Constant Packet Payload Type	R/W	0x0	0x0	This bit selects the type of constant payload to use. It is valid only when 3.FD05.15 = 1. 1 = Use all 1s packet payload. 0 = Use all 0s packet payload.
13:8	Reserved	RO	0x00	0x00	
7:0	IPG Length	R/W	12	0x00	The number in bits [7:0] +1 is the number of bytes for IPG.

Table 172: Packet Checker Control Register Device 3, Register 0xFD07

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	
3	CRC Reset	R/W	0x0	0x0	Reset CRC/packet counter.
2	PC Enable	R/W	0x0	0x0	Enable CRC/Packet counter block.
1	Reserved	R/W	0x0	0x0	
0	CRC Sample	R/W	0x0	0x0	Start packet counter and CRC counter sampling.

Table 173: Packet Checker Count Register Device 3, Register 0xFD08

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Error Package Counter Readout	RO	0x00	0x00	Error Package Counter Readout
7:0	Receive Package Counter Readout	RO	0x00	0x00	Receive Package Counter Readout

Table 174: Tx FIFO Control Register Device 3, Register 0xFD20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	0x0000	
1:0	Tx FIFO Depth	R/W	0x1	Retain	00 = This supports 10 KB at ±100 ppm. 01 = This supports 15 KB at ±100 ppm. 10 = This supports 20 KB at ±100 ppm. 11 = This supports 25 KB at ±100 ppm.

3.7 Copper Unit Advance Auto-Negotiation Registers

Table 175: Copper Unit Advance Auto-Negotiation Registers — Register Map

Register Name	Register Address	Table and Page
Auto-Negotiation Status Register	Device 7, Register 0x8001	Table 176, p. 137
Auto-Negotiation Status 2 Register	Device 7, Register 0x8016	Table 177, p. 137
Auto-Negotiation Status Register 2	Device 7, Register 0x801A	Table 178, p. 138

Table 176: Auto-Negotiation Status Register Device 7, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Master/Slave Configuration Fault	RO, LH	0x0	0x0	This register bit will clear on read. 1 = Master/slave configuration fault has been detected. 0 = No master/slave configuration fault has been detected.
14	Master/Slave Configuration Resolution	RO	0x0	0x0	1 = The local PHY configuration is resolved to the master. 0 = The local PHY configuration is resolved to the slave.
13	Remote Receiver Status	RO	0x0	0x0	1 = The remote receiver is OK. 0 = The remote receiver is not OK.
12	Local Receiver Status	RO	0x0	0x0	1 = The local receiver is OK. 0 = The local receiver is not OK.
11:9	Reserved	RO	0x0	0x0	
8	Link Partner Auto-Negotiation Enable	RO	0x0	0x0	This enables the link partner’s Auto-Negotiation.
7:0	Reserved	RO	0x00	0x00	

Table 177: Auto-Negotiation Status 2 Register Device 7, Register 0x8016

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14	Device Link	RO	0x0	0x0	1 = The device link is valid. 0 = The device is not linked.
13:6	Reserved	RO	0x01	0x00	
5	Acknowledge Finished	RO	0x0	0x0	1 = Acknowledge is finished.
4	Page Received	RO	0x0	0x0	1 = The page is received.
3	Clear HCD	RO	0x1	0x1	1 = The HCD is cleared.
2	HCD Resolved	RO	0x0	0x0	1 = Auto-Negotiation HCD has been resolved.
1	Reserved	RO	0x0	0x0	
0	Auto-Negotiation Link	RO	0x0	0x0	1 = FLP exchange is done, wait for link up.

Table 178: Auto-Negotiation Status Register 2
Device 7, Register 0x801A

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14:13	AN Speed Selected	RO	0x2	0x0	01 = 100BT1 Selected 10 = 1000BT1 Selected
12	Auto-Negotiation Page Received	RO	0x0	0x0	1 = The Auto-Negotiation page has been received.
11	Auto-Negotiation HCD Resolved	RO	0x0	0x0	1 = The Speed and Auto-Negotiation settings are resolved.
10	PCS Link	RO	0x0	0x0	1 = The PCS link is done (training finished).
9	Auto-Negotiation Pause Tx	RO	0x0	0x0	1 = Pause Tx.
8	Auto-Negotiation Pause Rx	RO	0x0	0x0	1 = Pause Rx.
7	LP Auto-Negotiation	RO	0x0	0x0	1 = The link partner is able to perform Auto-Negotiation. 0 = The link partner is not able to perform Auto-Negotiation.
6:0	Reserved	RO	0x00	0x00	

3.8 RGMII Registers

Table 179: RGMII Registers — Register Map

Register Name	Register Address	Table and Page
RGMII Output Impedance Control Register	Device 31, Register 0x8000	Table 180, p. 139
Com Port Control Register	Device 31, Register 0x8001	Table 181, p. 140

Table 180: RGMII Output Impedance Control Register
Device 31, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Restart Calibration	R/W, SC	0x0	Retain	Calibration will start when this bit is set to 1. 0 = Normal 1 = Restart
14	Calibration Complete	RO	0x0	Retain	Calibration is done when this bit becomes 1. 0 = The calibration is not done. 1 = The calibration is done.
13	Reserved	R/W	0x0	Retain	
12	Force PMOS/NMOS	R/W	0x0	Retain	1 = Force value from 31.8000.11:8 to PMOS, and 31.8000.7:4 to NMOS (used for manual settings).
11:8	PMOS Value	R/W	See Description.	Retain	0000 = All fingers are off. 1111 = All fingers are on. The automatic calibrated values are stored here after calibration completes. When 31.8000.12 is set to 1, the new calibration value is written into the I/O pad. The automatic calibrated value is lost.
7:4	NMOS Value	R/W	See Description.	Retain	0000 = All fingers are off. 1111 = All fingers are on. The automatic calibrated values are stored here after calibration completes. When 31.8000.12 is set to 1, the new calibration value is written into the I/O pad. The automatic calibrated value is lost.
3	Calibration ODR Enable	R/W	0x1	Retain	1 = Use the on-chip resistor. 0 = Use the off-chip resistor.
2:0	Calibration ODR	R/W	0x3	Retain	000 = 78.8Ω 001 = 64.5Ω 010 = 54.6Ω 011 = 47.3Ω 100 = 41.7Ω 101 = 37.3Ω 110 = 33.8Ω 111 = 30.9Ω

Table 181: Com Port Control Register
Device 31, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RGMII Transmit Timing Control	R/W	0x0**	Update	Changes to this bit are disruptive to the normal operation; any changes to these registers must be followed by software reset (3.8000.15) to take effect. 1 = Transmit clock is internally delayed. 0 = Transmit clock is not internally delayed. **Default value 0x0 if configured to RGMII mode1 TCLK no delay; 0x1 if configured to RGMII mode2 TCLK Delay. Refer to Table 13.
14	RGMII Receive Timing Control	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; so any changes to these registers must be followed by software reset (3.8000.15) to take effect. 1 = Receive clock transition when the data is stable. 0 = Receive clock transition when the data transitions.
13	RXCLK During Power Down	R/W	0x0	0x0	1 = RXCLK toggles during power down. 0 = RXCLK stops during power down.
12	Isolate	R/W	0x0	0x0	1 = Tri-state the output pins of RXC, RXCLK, and RXD. 0 = Normal operation
11:0	Reserved	R/W	0x000	0x000	

3.9 SGMII Registers

Table 182: SGMII Registers — Register Map

Register Name	Register Address	Table and Page
SGMII Control Register	Device 4, Register 0x8000	Table 183, p. 142
SGMII Status Register	Device 4, Register 0x8001	Table 184, p. 143
PHY Identifier Register 1	Device 4, Register 0x8002	Table 185, p. 144
PHY Identifier Register 2	Device 4, Register 0x8003	Table 186, p. 144
SGMII Auto-Negotiation Advertisement	Device 4, Register 0x8004	Table 187, p. 144
SGMII Link Partner Ability/SGMII	Device 4, Register 0x8005	Table 188, p. 145
SGMII Auto-Negotiation Expansion Register	Device 4, Register 0x8006	Table 189, p. 145
SGMII SERDES Specific Control 1 Register	Device 4, Register 0x8010	Table 190, p. 146
SGMII Specific Status Register	Device 4, Register 0x8011	Table 191, p. 146
SGMII Interrupt Enable Register	Device 4, Register 0x8012	Table 192, p. 147
SGMII Interrupt Status Register	Device 4, Register 0x8013	Table 193, p. 148
SGMII Receive Error Counter Register	Device 4, Register 0x8015	Table 194, p. 148
PRBS Control Register	Device 4, Register 0x8017	Table 195, p. 149
PRBS Error Counter LSB Register	Device 4, Register 0x8018	Table 196, p. 149
PRBS Error Counter MSB Register	Device 4, Register 0x8019	Table 197, p. 149
SGMII Specific Control Register 2	Device 4, Register 0x801A	Table 198, p. 150

Table 183: SGMII Control Register (Sheet 1 of 2)
Device 4, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SGMII Reset	R/W	0x0	SC	SGMII Software Reset. Writing 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD of the internal bus is looped back to RXD of the internal bus. Loopback speed is determined by the copper link speed. 1 = Enable loopback. 0 = Disable loopback.
13	Speed Select (LSB)	RO, R/W	0x0	Retain	Bit 6, bit 13. 10 = 1000 Mbps 01 = 100 Mbps 00 = Reserved
12	Auto-Negotiation Enable	R/W	0x1	Retain	If the value of this bit is changed, then the link will be broken and Auto-Negotiation is restarted. When this bit gets set/reset, Auto-Negotiation is restarted (bit 4.0x8000.9 is set to 1). On hardware reset, this bit takes on the value of S_ANEG. 1 = Enable the Auto-Negotiation process. 0 = Disable the Auto-Negotiation process.
11	Power Down	R/W	See Description.	0x0	When the port is switched from power down to normal operation, software reset and Restart Auto-Negotiation are performed even when bits Reset (4.0x8000.15) and Restart Auto-Negotiation (4.0x8000.9) are not set by the user. On hardware reset, this bit assumes the value of ps_mode [1:0]. It will be power down when it is in RGMII mode. 1 = Power down. 0 = Normal operation
10	Isolate	RO	0x0	0x0	This function is not supported.
9	Restart SGMII Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware reset, software reset (4.0x8000.15), or a change in Auto-Negotiation enable (4.0x8000.12), regardless of whether the restart bit (4.0x8000.9) is set. The bit is set when Auto-Negotiation is enabled or disabled in 4.0x8000.12. 1 = Restart the Auto-Negotiation process. 0 = Normal operation

Table 183: SGMII Control Register (Sheet 2 of 2)
Device 4, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Duplex Mode	R/W	0x1	Retain	Writing this bit has no effect unless one of the following events occurs: • A software reset is asserted (register 4.0x8000.15). • A Restart Auto-Negotiation is asserted (register 4.0x8000.9). • An Auto-Negotiation Enable changes (register 4.0x8000.12). • A power down (register 4.0x8000.11) transitions from power down to normal operation. 1 = Full duplex 0 = Half duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	RO, R/W	0x1	Retain	Bit 6, bit 13 10 = 1000 Mbps 01 = 100 Mbps 00 = Reserved
5:0	Reserved	RO	Always 0x00	Always 0x00	

Table 184: SGMII Status Register
Device 4, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO, LH	Always 0x0	Always 0x0	This must be 0.
5	SGMII Auto-Negotiation Complete	RO	0x0	0x0	1 = The Auto-Negotiation process is complete. 0 = The Auto-Negotiation process is not complete. This bit is not set when link is up because of SGMII Auto-Negotiation Bypass or if Auto-Negotiation is disabled.
4	Reserved	RO, LH	Always 0x0	Always 0x0	This must be 0.
3	Auto-Negotiation Ability	RO	0x1	0x1	1 = The PHY is able to perform Auto-Negotiation. 0 = The PHY is not able to perform Auto-Negotiation.
2	SGMII Link Status	RO, LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read register 4.0x8011.10 Link Real Time. 1 = The link is up. 0 = The link is down.
1:0	Reserved	RO, LH	Always 0x0	Always 0x0	This must be 0.

Table 185: PHY Identifier Register 1
Device 4, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bits 3:18	RO	0x0141	0x0141	Marvell OUI is 0x005043: 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 This register represents bits 3 to 18 of the OUI: 0000000101000001 ^ ^ bit 3.....bit18

Table 186: PHY Identifier Register 2
Device 4, Register 0x8003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bits 19:24	RO	Always 0x3	Always 0x3	This register field represents bits 19 to 24 of the OUI: 000011 ^.....^ bit 19...bit 24
9:4	Model Number	RO	0x00	0x00	The model number is 000000.
3:0	Revision Number	RO	0x0	0x0	The revision number is 0000.

Table 187: SGMII Auto-Negotiation Advertisement
Device 4, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link Status	RO	0x0	0x0	0 = The link is not up on the copper interface. 1 = The link is up on the copper interface.
14:13	Reserved	RO	Always 0x0	Always 0x0	This must be 0.
12	Duplex Status	RO	0x0	0x0	0 = The interface is resolved to half duplex. 1 = The interface is resolved to full duplex.
11:10	Speed [1:0]	RO	0x0	0x0	00 = Reserved 01 = The interface speed is 100 Mbps. 10 = The interface speed is 1000 Mbps. 11 = Reserved
9:8	Reserved	RO	0x0	0x0	These bits are always 0. 0 = Disabled 1 = Enabled
7:0	Reserved	RO	Always 0x01	Always 0x01	This must always set to 0x01 per SGMII Specification.

Table 188: SGMII Link Partner Ability/SGMII Device 4, Register 0x8005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	This must be 0.
14	Acknowledge	RO	0x0	0x0	Acknowledge This bit is cleared when the link goes down and loaded when a base page is received. Received Code Word bit 14 1 = The link partner has received a link code word. 0 = The link partner has not received a link code word.
13:0	Reserved	RO	0x0000	0x0000	Received Code Word bits [13:0] This must receive 00_0000_0000_0001 per SGMII Specification.

Table 189: SGMII Auto-Negotiation Expansion Register Device 4, Register 0x8006

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	This must be 00000000000.
3	Link Partner Next Page Able	RO	0x0	0x0	In SGMII mode, this bit is always 0. In 1000BASE-X mode, register 4.8006.3 is set when a base page is received and the received link control word has bit 15 set to 1. This bit is cleared when the link goes down. 1 = The link partner is Next Page able. 0 = The link partner is not Next Page able.
2	Local Next Page Able	RO	Always 0x1	Always 0x1	1 = The local device is Next Page able.
1	Page Received	RO, LH	0x0	0x0	Register 4.8006.1 is set when a valid page is received. 1 = A new page has been received. 0 = A new page has not been received.
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the SERDES receiver has received three non-zero matching valid configuration code groups, and Auto-Negotiation is enabled in register 4.8000.12. 1 = The link partner is Auto-Negotiation able. 0 = The link partner is not Auto-Negotiation able.

Table 190: SGMII SERDES Specific Control 1 Register Device 4, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	SERDES Transmit FIFO Depth	R/W	0x1	Retain	00 = This supports 10 KB at ±100 ppm. 01 = This supports 15 KB at ±100 ppm. 10 = This supports 20 KB at ±100 ppm. 11 = This supports 25 KB at ±100 ppm.
13	Block Carrier Extension Bit	R/W	0x0	Retain	The carrier extension and carrier extension with errors are converted to idle symbols on the RXD only during full-duplex mode. 1 = Enable block carrier extension. 0 = Disable block carrier extension.
12	Reserved	R/W	0x0	Retain	Set to 0.
11	Assert CRS on Transmit	R/W	0x0	Retain	This bit has no effect in full-duplex mode. 1 = Assert on transmit. 0 = Never assert on transmit.
10	Force Link Good	R/W	0x0	Retain	If the link is forced to be good, then the link state machine is bypassed and the link is always up. 1 = The force link is good. 0 = Normal operation
9:8	Reserved	R/W	0x0	Retain	Set to 0.
7:6	Reserved	R/W	0x0	Update	Set to 00.
5:0	Reserved	R/W	0x0	Retain	Set to 0.

Table 191: SGMII Specific Status Register (Sheet 1 of 2) Device 4, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 4.0x8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = Reserved
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 4.0x8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full duplex 0 = Half duplex
12	Reserved	RO	Always 0x0	Always 0x0	
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled, this bit is always 1. 1 = This is resolved. 0 = This is not resolved.

Table 191: SGMII Specific Status Register (Sheet 2 of 2)
Device 4, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Link (real time)	RO	0x0	0x0	1 = The link is up. 0 = The link is down.
9:6	Reserved	RO	Always 0x0	Always 0x0	
5	Sync Status	RO	0x0	0x0	1 = Sync 0 = No sync
4:0	Reserved	RO	Always 0x0	Always 0x0	

Table 192: SGMII Interrupt Enable Register
Device 4, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0x0	Always 0x0	
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
6	Reserved	RO	Always 0x0	Always 0x0	
5	Remote Fault Receive Interrupt Enable	R/W	0x0	0x0	1 = The interrupt is enabled. 0 = The interrupt is disabled.
4	SGMII Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
3:0	Reserved	RO	Always 0x0	Always 0x0	

Table 193: SGMII Interrupt Status Register Device 4, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0x0	Always 0x0	
14	Speed Changed	RO, LH	0x0	0x0	1 = The speed is changed. 0 = The speed is not changed.
13	Duplex Changed	RO, LH	0x0	0x0	1 = The duplex is changed. 0 = The duplex is not changed.
12	Page Received	RO, LH	0x0	0x0	1 = The page is received. 0 = The page is not received.
11	Auto-Negotiation Completed	RO, LH	0x0	0x0	1 = Auto-Negotiation is completed. 0 = Auto-Negotiation is not completed.
10	Link Status Changed	RO, LH	0x0	0x0	1 = Link status has changed. 0 = Link status has not changed.
9	Symbol Error	RO, LH	0x0	0x0	1 = There is a symbol error. 0 = There is no so symbol error.
8	False Carrier	RO, LH	0x0	0x0	1 = There is a false carrier. 0 = There is no false carrier.
7	FIFO Over/Underflow	RO, LH	0x0	0x0	1 = There is an overflow/underflow error. 0 = There is no FIFO error.
6	Reserved	RO	0x0	0x0	
5	Remote Fault Receive Interrupt Enable	RO, LH	0x0	0x0	1 = A remote fault received has changed. 0 = No change on the remote fault has been received.
4	SGMII Energy Detect Changed	RO, LH	0x0	0x0	1 = The Energy Detect state has changed. 0 = No Energy Detect state change has been detected.
3:0	Reserved	RO	Always 0x0	Always 0x0	

Table 194: SGMII Receive Error Counter Register Device 4, Register 0x8015

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	The counter will peg at 0xFFFF and will not roll over. Both false carrier and symbol errors are reported.

Table 195: PRBS Control Register
Device 4, Register 0x8017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Set to 0s.
7	Invert Checker Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
6	Invert Generator Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
5	PRBS Lock	R/W	0x0	Retain	0 = The counter runs freely. 1 = Do not start counting until PRBS locks first.
4	Clear Counter	R/W, SC	0x0	0x0	0 = Normal 1 = Clear counter.
3:2	Pattern Select	R/W	0x0	Retain	00 = PRBS 7 01 = PRBS 23 10 = PRBS 31 11 = Generate 1010101010... pattern.
1	PRBS Checker Enable	R/W	0x0	0x0	0 = Disable 1 = Enable
0	PRBS Generator Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

Table 196: PRBS Error Counter LSB Register
Device 4, Register 0x8018

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count LSB	RO	0x0000	Retain	A read to this register freezes register 4.8019. This is cleared only when register 4.8017.4 is set to 1.

Table 197: PRBS Error Counter MSB Register
Device 4, Register 0x8019

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count MSB	RO	0x0000	Retain	These bits do not update unless register 4.8018 is read first. This is cleared only when register 4.8017.4 is set to 1.

Table 198: SGMII Specific Control Register 2
Device 4, Register 0x801A

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	Set to 0s.
14:7	Reserved	R/W	0x00	0x00	Set to 0s.
6	Serial Interface Auto-Negotiation Bypass Enable	R/W	0x1	Update	Changes to this bit are disruptive to normal operation; so, any changes to these registers must be followed by a software reset to take effect. 1 = Bypass is allowed. 0 = No bypass is allowed.
5	Serial Interface Auto-Negotiation Bypass Status	RO	0x0	0x0	1 = The serial interface link came up because bypass mode timer timed out and SGMII Auto-Negotiation was bypassed. 0 = The serial interface link came up because regular SGMII Auto-Negotiation completed. If this bit is 1, then bit 4.0x8011.11 will be 0.
4	Reserved	R/W	0x0	0x0	Set to 0s.
3	SGMII Transmitter Disable	R/W	0x0	Retain	1 = Transmitter disable 0 = Transmitter enable
2:0	SGMII Output Amplitude	R/W	0x2	Retain	Differential voltage peak measured. See AC/DC section for valid VOD values. 000 = 14 mV 001 = 112 mV 010 = 210 mV 011 = 308 mV 100 = 406 mV 101 = 504 mV 110 = 602 mV 111 = 700 mV

4 PTP Registers

The device's PTP registers are accessible using the MDC and MDIO pins and support the IEEE Serial Management Interface used for PHY devices.

The PTP registers in the device constitute one or more fields. The manner in which each of these fields operate is defined by the field's type. The function of each type is described in Table 199.

Table 199: Register Types

Type	Description
LH	Register field with latching high function. If the status is high, then the register is set to 1 and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If the status is low, then the register is cleared to 0 and remains zero until a read operation is performed through the management interface or a reset occurs.
RES	Reserved. All reserved bits are read as zero unless otherwise noted.
Retain	The register value is retained after a software reset is executed.
RO	Read only.
ROC	Read only clear. After read, the register field is cleared.
RW	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, the register field is cleared to 0.
SC	Self-Clear. Writing a one to this register causes the specified function to be immediately executed, then the register field is automatically cleared to 0 when the function is complete.
Update	The value written to the register field does not take effect until a soft reset is executed.
WO	Write only. Reads from this type of register field return undefined data.
NR	Non-Rollover Register

Table 200: PTP Registers — Register Map (Sheet 1 of 2)

Register Name	Register Address	Table and Page
PTP Reset Control Register	Device 4, Register 0x8600	Table 201, p. 154
PTP Control Register 1	Device 4, Register 0x87F0	Table 202, p. 154
PTP Control Register 2	Device 4, Register 0x87F1	Table 203, p. 155
PTP Port Config Register	Register 4.8800 – PTP Port	Table 204, p. 156
PTP Port Config Register	Register 4.8801 – PTP Port	Table 205, p. 157
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PTP Global Config Register	Register 4.8E01 – PTP Global	Table 224, p. 168
PTP Global Config Register	Register 4.8E02 – PTP Global	Table 225, p. 169
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4.1 PTP Control Registers

Table 201: PTP Reset Control Register
Device 4, Register 0x8600

Bits	Field	Mode	HW Rst	SW Rst	Description
15	PTP Software Reset	R/W, SC	0x0	SC	PTP Software Reset. Writing a 1 to this bit resets the PTP core. When the reset operation is done, this bit is automatically cleared to 0. The reset occurs immediately. 1 = Reset 0 = Normal operation
14:0	Reserved	R/W	0x0000	Retain	

Table 202: PTP Control Register 1
Device 4, Register 0x87F0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Tx-side PTP's SFD Selection	R/W	0x0	Retain	Tx-side PTP's SFD selection. 1 = From tx_en 0 = From SFD
14	Tx-side PTP's Preamble Selection	R/W	0x0	Retain	Tx-side PTP's preamble selection. 1 = Enable the detection of preemptable packets delimiter. 0 = Disable the detection of preemptable packets delimiter.
13	Rx-side PTP's SFD Selection	R/W	0x0	Retain	Rx-side PTP's SFD selection. 1 = From rx_dv 0 = From SFD
12	Rx-side PTP's Preamble Selection	R/W	0x0	Retain	Rx-side PTP's preamble selection 1 = Enable the detection of preemptable packets delimiter. 0 = Disable the detection of preemptable packets delimiter.
11:10	Reserved	R/W	0x0	Retain	
9	PTP Power Down	R/W	0x1	Retain	1 = Power down. 0 = Power up.
8	Reserved	R/W	0x0	Retain	
7:6	PTP Event Request/Trigger Select for TX_ ENABLE Pin	R/W	0x0	Retain	01 = Use the TX_ENABLE pin for PTP output trigger pulse. 10 = Use the TX_ENABLE pin for PTP One Pulse Per Second (1PPS) output. 11 = Use the TX_ENABLE pin for PTP input trigger pulse.
5:4	PTP Event Request/Trigger Select for GPIO Pin	R/W	0x0	Retain	01 = Use the GPIO pin for PTP output trigger pulse. 10 = Use the GPIO pin for PTP for other functions. 11 = Use the GPIO pin for PTP input trigger pulse.
3:1	Reserved	R/W	0x0	Retain	
0	Enable LED/GPIO for PTP Status	R/W	0x0	Retain	This is used to bring PTP ptp_tx_led and ptp_rx_led to the TX_ENABLE pin.

Table 203: PTP Control Register 2
Device 4, Register 0x87F1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Tx-side PTP's SFD Selection for 1G Mode	R/W	0x0	Retain	Tx-side PTP’s SFD selection for 1G mode. 1 = From tx_en 0 = From SFD
14	Tx-side PTP's Preamble Selection for 1G Mode	R/W	0x0	Retain	Tx-side PTP’s preamble selection for 1G mode 1 = Enable the detection of preemptable packets delimiter. 0 = Disable the detection of preemptable packets delimiter.
13	Rx-side PTP's SFD Selection for 1G Mode	R/W	0x0	Retain	Rx-side PTP’s SFD selection for 1G mode. 1 = From rx_dv 0 = From SFD
12	Rx-side PTP's Preamble Selection for 1G Mode	R/W	0x0	Retain	Rx-side PTP’s preamble selection for 1G mode. 1 = Enable the detection of preemptable packets delimiter. 0 = Disable the detection of preemptable packets delimiter.
11:1	Reserved	R/W	0x000	Retain	
0	Enable LED/GPIO for PTP Status for 1G Mode	R/W	0x0	Retain	This is used to bring PTP ptp_tx_led and ptp_rx_led to TX_ENABLE pin for 1G mode.

4.2 PTP Port Registers

Table 204: PTP Port Config Register (Sheet 1 of 2)
Register 4.8800 – PTP Port

Bits	Field	Type	Description
15:12	TransSpec	RWS 0x1	PTP Transport Specific value. The Transport Specific bits present in PTP Common header are used to differentiate between IEEE 1588, IEEE 802.1AS, and so on frames. This is to differentiate between various timing protocols running on either Layer2 or higher protocol layers. In addition to comparing the EtherType to determine that the incoming frame is a PTP frame, the TransSpec bits are compared to the incoming PTP common headers' Transport Specific bits. If there is a match, then hardware logic timestamps the frames indicated by MsgTypeEn and optionally interrupts the CPU. If there is no match and Transport Spec checking is enabled (see the DisTSpecCheck bit below), then the hardware will not perform any operations in the PTP core. For IEEE 1588 networks, this is expected to be configured to a 0x0 and for IEEE 802.1AS networks, this is expected to be configured to 0x1. The only valid TransSpec values for PTP hardware acceleration (PTP Port Register 4.8802) are 0x0 and 0x1.
11	DisTSpec Check	RWR	Disable Transport Specific Check. 0 = Enable checking for Transport Spec. 1 = Disable checking for Transport Spec. When this bit is cleared to 0, the Transport Spec part of the PTP Common header of incoming frames must match the configured TransSpec (above) for timestamping to occur (regardless if the PTP hardware is accelerated). This setting limits PTP timestamping to frames containing a TransSpec value that matches the value in the previously described TransSpec register. This allows timestamping to be limited to only IEEE 1588 or to only IEEE 802.1AS per their frame's Transport Specs (assuming their value is contained in the previously described TransSpec register). When this bit is set to 1, the Transport Spec checking of the PTP frames is not performed before timestamping occurs. This setting allows PTP timestamping for all TransSpec values (although PTP hardware acceleration, PTP Port Register 4.8802, only works on IEEE 1588 and IEEE 802.1AS TransSpec values).
10:2	Reserved	RES	
1	DisTS Overwrite	RWR	Disable Time Stamp Counter Overwriting. 0 = Overwrite unread Time Stamps in the registers with new data. 1 = Keep unread Time Stamps in the registers until read. When this bit is cleared to 0, PTPArr0Time, PTPArr1Time, and PTPDepTime values get overwritten even though their corresponding valid bits (defined in PTP Port Status Data Structure below), are not cleared. When this bit is set to 1, PTPArr0Time, PTPArr1Time and PTPDepTime values do not get overwritten with new timestamps until their corresponding valid bits (defined in PTP Port Status Data Structure below) are cleared.

Table 204: PTP Port Config Register (Sheet 2 of 2)
Register 4.8800 – PTP Port

Bits	Field	Type	Description
0	DisPTP	RWS	Disable Precise Time Stamp logic. 0 = PTP logic on this port is enabled. 1 = PTP logic on this port is disabled. When PTP logic is disabled, the hardware logic does not recognize or timestamp PTP frames, even interrupt generation logic is disabled. This disable disables all modes of PTP on this port (including PTP hardware acceleration if enabled - PTP Port Register 4.8802). **NOTE:** PTP should not be enabled on half-duplex ports when ArrTSMode or HWAccel (PTP Port Register 4.8802) are non zero.

Table 205: PTP Port Config Register
Register 4.8801 – PTP Port

Bits	Field	Type	Description
15:14	Reserved	RES	
13:8	IPJump	RWR	Internet Protocol Jump added to ETJump below. Set this register to point to the start of the frame's IP Version byte (802.1Q tagged frames are automatically compensated by ETJump). This field specifies how many bytes to skip starting at the first byte of the frame's EtherType (that is, where ETJump, below, left off) to jump to the beginning of the IPv4 or IPv6 headers in the frame. If an IPv4 or IPv6 version is found at this location of the frame, then Layer 4 PTP processing occurs from there. This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including MPLS, and so on. For example, if ETJump is programmed to 0xC and IPJump is programmed to 0x16, then this indicates to hardware to skip 0x22 bytes to get to the IP header. It can either be IPv4 or IPv6 header. **NOTE:** A value of 0x0 (default) is a special case that prevents further frame searching if ETJump did not find a match (that is, a zero value in IPJump prevents the IPJump mechanism from searching further).
7:5	Reserved	RES	
4:0	ETJump	RWS 0xC	EtherType Jump points to the start of the frame's EtherType (assuming it is not 802.1Q tagged). This field specifies how many bytes to skip starting from the start of the MAC-DA of the frame to get to the first byte of the EtherType of the frame. Frames found with an 0x8100 EtherType (802.1Q tag) at this location are automatically searched 4 bytes further into the frame for the next EtherType to compare (this extension is done once). If the PTPEType value (PTP Global Register 4.8E00) is found as the Ether Type in the frame, then Layer 2 PTP processing occurs. If 0x0800 or 0x86DD is found, then Layer 4 PTP processing occurs. If none of these values are found, then PTP frame decoding is passed to the IPJump field above. This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including DSA-Tag, IEEE 802.1Q tag, Provider tag, and so on.

Table 206: PTP Port Config Register (Sheet 1 of 2)
Register 4.8802 – PTP Port

Bits	Field	Type	Description
15:8	ArrTSMode	RWR	Arrival Time Stamp Mode. This field is used to configure the Arrival Time Stamp mode as follows: 0x00 = Arrival Time Stamp frame modification is disabled. 0x01 = Add the PTPArr[x]Time associated with enabled PTP Event frames at the end of the frame increasing the frame's size by four bytes. 0x02 to 0x0F = Reserved 0x10 to 0xEF = Overwrite the PTPArr[x]Time associated with enabled PTP. Event frames into the frame without increasing the frame's size. The location in the frame where the PTPArr[x]Time is placed is controlled by this register. It is placed ArrTSMode bytes past the start of the PTP Common Header. **For example, to place the timestamp in the four Reserved bytes in the PTP Common Header, set this register to a value of 0x10.** If the end of the frame is reached prior to the completion of this overwrite, then PTPArr[x]Time is placed at the end of the frame increasing the frame's size by enough bytes for it to fit. 0xF0 to 0xFF = Reserved **NOTE:** All frames will be processed using the above settings unless the frame can be hardware accelerated via setting the HWAccel bit below to 1. **NOTE:** Changing this register's value can only occur when PTP is idle. **NOTE:** Added PTPArr[x]Time bytes that increase the frame's size are included in the MIB counters and policy is performed on the resulting frame (for example, TCAM matching and frame size checking). This register must be 0 if ExtHWAccel (below) is set to 1.
7	FilterAct	RWR	Filter LED Activity. 0 = LED Activity is activated for all frames. 1 = LED Activity is not activated for most IEEE 802.1 frames. This bit can filter all or most of the 802.1 Protocol frames from the Port's Activity LEDs. When this bit is set to 1, all 802.1 protocol frames (those with a DA = 01:C2:80:00:00:0x) will be potentially filtered from the port's Activity LED as determined by the ArrLEDCtrl and DepLEDCtrl registers (PTP Port Register 4.8803). When this bit is cleared to a 0, only the 802.1 gPTP protocol frames will be potentially filtered from the port's Activity LED.

Table 206: PTP Port Config Register (Sheet 2 of 2)
Register 4.8802 – PTP Port

Bits	Field	Type	Description
6	HWAccel	RWR	Port PTP Hardware Acceleration enable. 0 = No acceleration or only Ingress PTP hardware acceleration. 1 = Ingress and Egress PTP hardware acceleration is enabled. Setting this bit to 1 enables PTP hardware acceleration on this port. PTP hardware acceleration will automatically occur in the selected PTPMode (PTP Global Register 4.8E07) for the enabled PTP Domains once a Time Array (PTP Global Registers 4.8F02 to 4.8F0C, and 4.8F1D to 4.8F1E) is configured and enabled. Even then PTP hardware acceleration will only occur for the Transport Specs enabled on this port (PTP Port Register 4.8800). In this mode, any frame that cannot be hardware accelerated will be processed using the settings defined by ArrTSMode above (a type of fallback mode). Clearing this bit to 0 causes all frames to be processed using the settings defined by ArrTSMode above. Do not set this bit to a 1 if ExtHWAccel (below) is set to 1. **NOTE:** PTP Hardware Acceleration requires that the Time Stamping Clock Period (TAI Register 4.8C01) be 8000 picoseconds (8 ns) ±100 ppm. If the PTP_EXTCLK (external clock) is used (TAI Register 4.8C00), then it must also be within this range before enabling PTP Hardware Acceleration. **NOTE:** Changing this register's value can only occur when PTP is idle.
5	KeepSA	RWR	Keep Frame's SA. 0 = Place Port's SA into modified egressing PTP frames. 1 = Keep the frame's SA even for modified egressing PTP frames. Normally when the Data portion of a frame (the part of the frame between the EtherType and the CRC) is modified the address of the modifying entity is placed into the Source Address (SA) field of egressing frames. This is the result for modified PTP frames when this bit is cleared to 0. When this bit is set to 1, the SA portion of PTP frames is not modified.
4:2	Reserved	RES	
1	PTPDepInt En	RWR	PTP Port Departure Interrupt enable. 0 = Disable PTP Departure capture interrupts. 1 = Enable PTP Departure capture interrupts. This field enables the per-port interrupt for outgoing PTP frame from this port. When this bit is set to 1 and this ports' PTPDepTimeValid bit (PTP Port Register 4.8900) is set to 1, a PTP interrupt for this port will be indicted in PTP Global Register (register 4.8E08). **NOTE:** Hardware logic only timestamps the PTP frames when configured to do so by MsgTypeEn field (see PTP Global Register 4.8E00).
0	PTPArrInt En	RWR	PTP Port Arrival Interrupt enable. 0 = Disable PTP Arrival capture interrupts. 1 = Enable PTP Arrival capture interrupts. This field enabled the per-port interrupt for incoming PTP frames from this port. When this bit is set to 1 and this port's PTPArr0TimeValid bit (PTP Port Register 4.8808) or its PTPArr1TimeValid bit (PTP Port Register 4.880C) is set to 1, a PTP interrupt for this port will be indicated in PTP Global Register (register 4.8E08). **NOTE:** Hardware logic only timestamps the PTP frames when configured to do so by MsgTypeEn field (see PTP Global Register 4.8E00).

Table 207: PTP Port Config Register
Register 4.8803 – PTP Port

Bits	Field	Type	Description
15:8	ArrLED Ctrl	RWR	LED control for packets entering the device. When 0x0, if a received frame is classified as a PTP frame or an 802.1 protocol frame, the LED does not blink. But it blinks for every non-PTP or non-802.1 protocol frame. When 0x1, the LED blinks for every received frame classified as a PTP frame or an 802.1 protocol frame. It also blinks for every non-PTP frame or non-802.1 protocol frame. When 0xn, the LED blinks once for every n received frames classified as PTP or 802.1 protocol. It also blinks for every non-PTP frame or non-802.1 protocol frame. **NOTE:** This tracks all received PTP frames (even though the PTP core timestamps only the PTP event messages) and not just PTP frames that require timestamping or it tracks all received 802.1 protocol frames (any frame with a DA = 01:C2:80:00:00:0x). The FilterAct bit in PTP Port (register 4.8802) controls which frames are tracked. This register affect the port's Activity LED only. It does not change how the frames progress through the switch.
7:0	DepLED Ctrl	RWS 0x80	LED control for packets departing the device. When 0x0, if a transmitting frame is classified as a PTP frame or an 802.1 protocol frame, the LED does not blink. But it blinks for every non-PTP frame or non-802.1 protocol. When 0x1, the LED blinks for every transmitting frame classified as a PTP frame or an 802.1 protocol frame. It also blinks for every non-PTP frame or non-802.1 protocol frame. When 0xn, the LED blinks once for every n transmitting frames classified as PTP or 802.1 protocol. It also blinks for every non-PTP frame or non-802.1 protocol frame. **NOTE:** This tracks all transmitting PTP frames (even though the PTP core timestamps only the PTP event messages) and not just PTP frames that require timestamping or it tracks all transmitted 802.1 protocol frames (any frame with a DA = 01:C2:80:00:00:0x). The FilterAct bit in PTP Port (register 4.8802) controls which frames are tracked. This register affect the port's Activity LED only. It does not change how the frames progress through the switch.

Table 208: PTP Port Status Register
Register 4.8808 – PTP Port

Bits	Field	Type	Description
15:3	Reserved	RES	
2:1	PTPArr0IntStatus	RWR	PTP Arrival Time 0 Interrupt Status. The PTP Arrival time 0 Interrupt bit gets set for a given port when an incoming PTP frame is timestamped in PTPArr0Time counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port [register 4.8802]). 0x0 = Normal, that is, none of the error conditions stated below are valid for this packet. 0x1 = This is if the PTPArr0Time counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use arrival0 counters arrived into the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = This is if the incoming frame could not be timestamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr0TimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can occur when there is more than one PTP frame that requires timestamping into arrival 0 counters arrives into the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for policy, CRC, queue congestion, or any other reasons, then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter descriptions (PTP Port Register 4.8905) for further details.
0	PTPArr0 TimeValid	RWR	PTP Arrival 0 Time Valid. When the PTPArr0Time value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port [register 4.8802]), this bit is set to a 0x1 validating the time counter. 0x0 = PTPArr0Time is not valid. 0x1 = PTPArr0Time is valid and PTPArr0IntStatus represents the status information for the PTPArr0Time counter. This is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error, and so on, this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. **NOTE:** This valid bit must be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware is unable to determine if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

**Table 209: PTP Port Status Register
Register 4.8809 – PTP Port**

Bits	Field	Type	Description
15:0	PTPArr0 Time [15:0]	RWR	PTP Arrival 0 Time counter bits [15:0] of a 32-bit register. This indicates the PTP Arrival 0 timestamp value that is captured by the PTP logic for a PTP frame that must be timestamped. The captured timestamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with timestamping within the hardware is one TSClkPer amount. The upper 16 bits of this register are contained in the register below.

**Table 210: PTP Port Status Register
Register 4.880A – PTP Port**

Bits	Field	Type	Description
15:0	PTPArr0 Time [31:16]	RWR	PTP Arrival 0 Time counter bits [31:16] of a 32-bit register. This indicates the PTP Arrival 0 timestamp value that is captured by the PTP logic for a PTP frame that must be timestamped. The captured timestamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with timestamping within the hardware is one TSClkPer amount. The lower 16 bits of this register are contained in the register above.

**Table 211: PTP Port Status Register
Register 4.880B – PTP Port**

Bits	Field	Type	Description
15:0	PTPArr0 SeqId	RWR	PTP Arrival 0 Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose timestamp information has been captured by hardware logic in PTPArr0Time register.

Table 212: PTP Port Status Register
Register 4.880C – PTP Port

Bits	Field	Type	Description
15:3	Reserved	RES	
2:1	PTPArr1IntStatus	RWR	PTP Arrival Time 1 Interrupt Status. The PTP Arrival time 1 Interrupt bit gets set for a given port when an incoming PTP frame is timestamped in PTPArr1Time counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port [register 4.8802]). 0x0 = Normal, that is, none of the error conditions stated below are valid for this packet. 0x1 = This is if the PTPArr1Time counter with its associated valid and SequenceID was overwritten as there were more than one PTP frame that must use arrival1 counters arrived into the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = This is if the incoming frame could n0t be timestamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr1TimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can occur when there is more than one PTP frame that requires timestamping into arrival 1 counters arrives into the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for policy, CRC, the queue congestion or any other reasons then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter description (PTP Port Register 4.8905) for further details.
0	PTPArr1 TimeValid	RWR	PTP Arrival 1 Time Valid. When the PTPArr1Time value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port [register 4.8802]), this bit is set to a 0x1 validating the time counter. 0x0 = PTPArr1Time is not valid. 0x1 = PTPArr1Time is valid and PTPArr1IntStatus represents the status information for the PTPArr1Time counter. This is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error, and so on, this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. **NOTE:** This valid bit must be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware is unable to determine if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 213: PTP Port Status Register Register 4.881D – PTP Port

Bits	Field	Type	Description
15:0	PTPArr1 Time [15:0]	RWR	PTP Arrival 1 Time counter bits [15:0] of a 32-bit register. This indicates the PTP Arrival 1 timestamp value that is captured by the PTP logic for a PTP frame that must be timestamped. The captured timestamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with timestamping within the hardware is one TSClkPer amount. The upper 16 bits of this register are contained in the register below.

Table 214: PTP Port Status Register Register 4.881E – PTP Port

Bits	Field	Type	Description
15:0	PTPArr1 Time [31:16]	RWR	PTP Arrival 1 Time counter bits [31:16] of a 32-bit register. This indicates the PTP Arrival 1 timestamp value that is captured by the PTP logic for a PTP frame that must be timestamped. The captured timestamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as previously described. **NOTE:** Maximum jitter associated with timestamping within the hardware is one TSClkPer amount. The lower 16 bits of this register are contained in the register above.

Table 215: PTP Port Status Register Register 4.880F – PTP Port

Bits	Field	Type	Description
15:0	PTPArr1 SeqId	RWR	PTP Arrival 1 Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose timestamp information has been captured by hardware logic in PTPArr1Time register.

Table 216: PTP Port Status Register
Register 4.8900 – PTP Port

Bits	Field	Type	Description
15:3	Reserved	RES	
2:1	PTPDepIntStatus	RWR	PTP Departure Time Interrupt Status. The PTP Departure time Interrupt bit gets set for a given port when an incoming PTP frame is timestamped in PTPDepTime counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port [register 4.8802]). 0x0 = Normal, that is, none of the error conditions stated below are valid for this packet. 0x1 = This is if the PTPDepTime counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that required to use departure counter departed out of the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = This is if the outgoing frame could not be timestamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPDepTimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can occur when there is more than one PTP frame that requires timestamping into departure counter leaves the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for CRC reasons, then the PTP departure discard counter gets updated (PTPNonTSDepDisCtr or PTPTSDepDisCtr). See the discard counter description (PTP Port Register 4.8905) for further details.
0	PTPDep TimeValid	RWR	PTP Departure Time Valid. When the PTPDepTime value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port [register 4.8802]), this bit is set to a 0x1 validating the time counter. 0x0 = PTPDepTime is not valid. 0x1 = PTPDepTime is valid and PTPDepIntStatus represents the status information for the PTPDepTime counter. This is set by hardware for the frames which are assured to depart the port. For frames with CRC error, and so on, this bit will not be set but either PTPNonTSDepCtr or PTPTSDepCtr is updated. **NOTE:** This valid bit must be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware is unable to determine if software is done reading all the relevant registers for a particular Time counter before clearing the valid bit.

Table 217: PTP Port Status Register
Register 4.8901 – PTP Port

Bits	Field	Type	Description
15:0	PTPDep Time [15:0]	RWR	PTP Departure Time counter bits [15:0] of a 32-bit register. This indicates the PTP Departure timestamp value that is captured by the PTP logic for a PTP frame that must be timestamped. The captured timestamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above. **NOTE:** Maximum jitter associated with timestamping within the hardware is one TSClkPer amount. The upper 16 bits of this register are contained in the register below.

Table 218: PTP Port Status Register
Register 4.8902 – PTP Port

Bits	Field	Type	Description
15:0	PTPDep Time [31:16]	RWR	PTP Departure Time counter bits [31:16] of a 32-bit register. This indicates the PTP Departure timestamp value that is captured by the PTP logic for a PTP frame that must be timestamped. The captured timestamp value is from a Global Timer counter running off of a switch internal clock. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above. **NOTE:** Maximum jitter associated with timestamping within the hardware is one TSClkPer amount. The lower 16 bits of this register are contained in the register above.

Table 219: PTP Port Status Register
Register 4.8903 – PTP Port

Bits	Field	Type	Description
15:0	PTPDep SeqId	RWR	PTP Departure Sequence Identifier. This indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose timestamp information has been captured by hardware logic in PTPDepTime register.

Table 220: Ingress Mean Path Delay Register
Register 4.890C – PTP Port

Bits	Field	Type	Description
15:0	Mean PathDelay	RWR	Ingress Mean Path Delay register. This indicates the cable delay between this port and its link partner in unsigned nanoseconds. This is used in HWAccel PTP mode (PTP Port [register 4.8802]).

Table 221: Ingress Path Delay Asymmetry Register
Register 4.891D – PTP Port

Bits	Field	Type	Description
15	IPDA Sign	RWR	Ingress Path Delay Asymmetry Sign. 0 = The Ingress Path Delay Asymmetry number is added. 1 = The Ingress Path Delay Asymmetry number is subtracted. This indicates the sign of the asymmetry value (below) beyond the Mean Path Delay (PTP Port Register 4.890C) that must be adjusted for more accurate cable measurements.
14:0	Ingress PathDelay Asymmetry	RWR	Ingress Path Delay Asymmetry register. This indicates the asymmetry value beyond the Mean Path Delay (PTP Port Register 4.890C) that must be added for more accurate cable measurements. This register is in unsigned nanoseconds.

Table 222: Egress Path Delay Asymmetry Register
Register 4.891E – PTP Port

Bits	Field	Type	Description
15	EPDA Sign	RWR	Egress Path Delay Asymmetry Sign. 0 = The Egress Path Delay Asymmetry number is added. 1 = The Egress Path Delay Asymmetry number is subtracted. This indicates the sign of the asymmetry value (below) beyond the Mean Path Delay (PTP Port Register 4.890C) that must be adjusted for more accurate cable measurements.
14:0	Egress PathDelay Asymmetry	RWR	Egress Path Delay Asymmetry register. This indicates the asymmetry value beyond the Mean Path Delay (PTP Port Register 4.890C) must be subtracted for more accurate cable measurements. This register is in unsigned nanoseconds.

4.3 PTP Global Registers

Table 223: PTP Global Config Register
Register 4.8E00 – PTP Global

Bits	Field	Type	Description
15:0	PTPEType	RWS to 0x88F7	PTP EtherType. All layer 2 PTP frames are recognized using a combination of a specific EtherType and MessageType values (part of the PTP Common Header). This field is used to identify the EtherType on these frames. The MsgTypeEn (specified below in register 4.8E01) qualifies the types of frames that the hardware must timestamp. For IEEE 802.1AS and IEEE1588 over Layer 2 Ethernet, the EtherType is expected to be programmed to 0x88F7.

Table 224: PTP Global Config Register
Register 4.8E01 – PTP Global

Bits	Field	Type	Description
15:0	MsgType En	RWR	Message Type Time Stamp Enable. MessageType is part of the PTP common header. There are some PTP frames that must be timestamped and some that are not required to be timestamped. This field identifies the PTP frame types that must be timestamped for frames that are not hardware accelerated – see HWAccel in PTP Port Register 4.8802). The MessageType read from PTP frames is vectorized[1] and then used to access the appropriate bit in this register. If the selected bit is set to 1, then that frame type will be timestamped both in ingress and egress: else, that frame type will not be timestamped. For example, if MessageType field (in the PTP common header) with a value of 0x4 must be timestamped in hardware, then MsgTypeEn [4] should be set to 1. Then the incoming PTP frames with a MessageTypefield of 0x4 will get timestamped into one of the Port's two available arrival capture registers (either PTPArr0Time or PTPArr1Time as identified by TSArrPtr [4] bit below). All outgoing PTP frames with the MessageType field of 0x4 will be timestamped into the Port's PTPDepTime capture register.

1. Vectorized refers to converting the hexadecimal MessageType field into a 16-bit binary number.

Table 225: PTP Global Config Register
Register 4.8E02 – PTP Global

Bits	Field	Type	Description
15:0	TSArrPtr	RWR	Time Stamp Arrival Time Capture Pointer. If the incoming PTP frame must be timestamped (based on MsgTypeEn), then this field determines whether the hardware logic should use PTPArr0Time or PTPArr1Time for storing the arriving frames' timestamp information. This field corresponds to the sixteen combinations of the vectorized MessageType. For example, if TSArrPtr [2] is set to a 1, it indicates to the hardware that if MsgTypeEn [2] is set to 1, then PTP frames with MessageType = 0x2 will use PTPArr1Time counter for storing the incoming PTP frames' timestamp. On the contrary: if TSArrPtr [2] is cleared to 0, that indicates to the hardware that if MsgTypeEn [2] is set to 1, then PTP frames with MessageType = 0x2 will use PTPArr0Time counter for storing the incoming PTP frames' timestamp.

Table 226: PTP Global Config Register
Register 4.8E07 – PTP Global

Bits	Field	Type	Description
15	Update	SC	Update Data. When this bit is set to 1, the data written to bits [7:0] will be loaded into the PTP Global Config register referenced by the Pointer bits below. After the write has occurred, this bit self clears to 0.
14:8	Pointer	RWR	Pointer to the desired octet of PTP Global Config. These bits select one of the possible PTP Global Config registers for both read and write operations. A write operation occurs if the Update bit is a one (the registers can be written to by writing this register in a single operation). Otherwise a read of the current Pointer occurs and the data found there is placed in the Data bits below (the desired register can be read by first writing to this register, with Update = 0, and then reading this register). The Pointer bits are used to access the Index registers as follows: 0x00 = PTP Mode Register 0x01 to 0x7F = Reserved
7:0	Data	RWR	Octet Data of the PTP Global Config register referenced by the Pointer bits above.

The index register accessed by the PTP Global Config register is described in the next table.

Table 227: PTP Mode Register, Index: 0x00

Bits	Field	Type	Description
7:5	Reserved	RES	
4	AltScheme	RWR	Alternate Scheme. This bit is used to define the values that are returned in the requestReceiptTimestamp field in IEEE 1588 pDelay Response messages and the correctionField and responseOriginTimestamp in pDelay Response Follow Up messages as follows: 0 = RequestReceiptTimestamp = t2, responseOriginTimestamp = t3 and the correctionField = 0 (fractional ns) 1 = RequestReceiptTimestamp = 0, responseOriginTimestamp = 0 and the correctionField = turnaround time **NOTE:** This bit has no effect if the PTP frame is an IEEE 802.1AS frame (as indicated by the frame's TransSpec field).
3	GrandMstr	RWR	Grand Master Enable. This bit is used to enable hardware support for the ports on this device to act as if they are the PTP Grand Master as follows: 0 = Hardware accelerate with this device is not being the Grand Master. 1 = Hardware accelerate with this device is being the Grand Master.
2	OneStep	RWR	OneStep Enable. This bit is used to enable hardware One Step support for PTP frames in the mode selected by the PTPMode bits below as follows: 0 = Hardware accelerate using AutoFollowUp Two Step frame formats. 1 = Hardware accelerate using One Step frame formats. **NOTE:** This device does not support the receiving of One Step frames and the hardware conversion of these frames into Two Step when the PTPMode is End to End Transparent Clock.
1:0	PTPMode	RWR	PTP Mode. This register selects the PTP Mode of the device (for all ports) as follows: 0x0 = Boundary Clock 0x1 = Peer to Peer Transparent Clock 0x2 = End to End Transparent Clock 0x3 = Reserved For these settings to have an effect, at least one Time Array (PTP Global Registers 4.8F00 to 4.8F0C and 4.8F1D to 4.8F1E) must be configured for the Domain that will be used. This mode will then take effect on the ports whose Hardware Acceleration is enabled (HWAccel is set to 1 in PTP Port Register 4.8802).

Table 228: PTP Status Register
Register 4.8E08 – PTP Global

Bits	Field	Type	Description
15	TrigGen Int	ROC	Trigger Generate mode Interrupt. The TrigGenInt bit gets set by the TAI block when the TrigGenIntEn is set to 1 (TAI Register 4.8C00) and when the one shot pulse is generated (TrigMode is set to 1 in TAI Register 4.8C00). It is cleared by the reading of this register.
14	Event Int	RO	Event Capture Interrupt. This bit gets set by the TAI block when the EventIntEn is set to 1 (TAI Register 4.8C00) and when an EventReq is captured in the EventCap Register. It is cleared by writing a zero to the EventCapValid register (TAI Register 4.8C09). **NOTE:** This interrupt bit will also be set to 1, if enabled, whenever the EventCapValid bit (TAI Register 4.8D00) is set to 1. This allows software to test its interrupt routine.
13:11	Reserved	RES	
10:0	PTPInt [10:0]	RO	These PTP Interrupt bits gets set for a given port when an incoming PTP frame is timestamped and PTPArrIntEn for that port is set to 1. Similarly the PTP Interrupt bits get set for a given port when an outgoing PTP frame is timestamped and PTPDepIntEn for that port is set to 1. The hardware logic sets this per port bit based on the previously described criteria and is cleared upon software reading and clearing the corresponding time counter valid bits that are valid for that port.

Table 229: ReadPlus Command Register
Register 4.8E1E – PTP Global

Bits	Field	Type	Description
15	Read Plus Enable	R/W	Read Plus Enable 1 = Enable 0 = Disable
14:12	Reserved	Res	Reserved
11:8	PTPReg	R/W	PTP Registers 0xE = 4.8Cxx (TAI Registers, Event Capture Registers 0xF = 4.8Fxx (PTP Global Time Array Registers) **NOTE:** These registers must use ReadPlus command otherwise readback value is incorrect. Register 4.8F00 to register 4.8F1F Registers 4.8C1E and 4.8C0F, PTP Global Time [31:0] Registers 4.8C02 and 4.8C03, Trig Generation Amount [31:0] Registers 4.8D01 and 4.8D02, Event Capture Time [31:0] Registers 4.8C09 and 4.8C0A, Trig Generation Time [31:0]
7:5	Reserved	RES	
4:0	PTPAddr	R/W	PTP Address This is the starting address of the PTP registers to be read.

Table 230: ReadPlus Data Register
Register 4.8E1F – PTP Global

Bits	Field	Type	Description
15:0	Read Plus Data	R/W	Read Plus Data This register is used to read out the ReadPlus Data. To read 32-bit wide PTP registers, read from this register back-to-back.

Table 231: PTP Global Time Array Register
Register 4.8F00 – PTP Global

Bits	Field	Type	Description
15:0	ToDLoadPt [15:0]	RWR	Time of Day Load Point Register bits [15:0] of a 32-bit register. The ToDLoadPt register is used in multiple ways, but its contents are always relative to the PTP Global Time (also known as H/W Time) found in TAI Global Registers 4.8C1E and 4.8C0F. This register is used as follows in the various ToD Operations: ToD Store All Registers – it is used to determine the instant in time that the selected Time Array is loaded. The load occurs at the instant the PTP Global Time (TAI Global Registers 4.8C1E and 4.8C0F) matches the contents of this register. ToD Capture – it is used to capture the instant in time that the Capture occurred. On each ToD Capture, the contents of this register will be loaded with the current value contained in the PTP Global Time (TAI Global Registers 4.8C1E and 4.8C0F). The upper 16 bits of this register are contained in the register below.

Table 232: TAI Global Time Array Register
Register 4.8F01 – PTP Global

Bits	Field	Type	Description
15:0	ToDLoadPt [31:16]	RWR	Time of Day Load Point Register bits [31:16] of a 32-bit register. Value to be matched with global timer value – used to either load or capture the TOD. See the description above. The lower 16 bits of this register are contained in the register above.

Table 233: PTP Global Time Array Register
Register 4.8F02 – PTP Global

Bits	Field	Type	Description
15	ToDBusy	SC	Time of Day Busy. This bit must be set to 1 to start a ToD operation (see ToD Op below). Only one ToD operation can be executed at a time, so this bit must be 0 before setting it to 1. When the requested ToD operation completes, this bit will automatically be cleared to 0.
14:12	ToDOp	RWR	Time of Day Opcode. The following ToD Opcodes are supported and are applied to the selected Time Array as indicated below: 0x0, 0x1 = Reserved 0x2 = Store Comp register only to selected TimeArray[1] 0x3 = Store All Registers to selected TimeArray @ ToDLoadPt[2] 0x4 = Capture selected TimeArray, Comp=Comp, and ToDLoadPt=PTPGT[3] 0x5 to 0x7 = Reserved **NOTE:** A Store ToDOp will start the timer if ClkValid below is set to 1.
11	Reserved	RES	
10:9	TimeArray [1:0]	RWR	Time Array. The above ToD operation is performed to/from the physical Time Array specified by this register. The device contains multiple independent Time Arrays where each Time Array comprises: • 10-byte ToD time (PTP Global Registers 4.8F03 to 4.8F07) • 8-byte 1722 time (PTP Global Registers 4.8F08 to 4.8F0B) • 4-byte Compensation (PTP Global Registers 4.8F0C to 4.8F0D) • 1-byte Domain Number (bits [7:0] below) and a 1-bit Clock Valid (bit 8 below)
8	ClkValid	RWR	Clock Valid. When this bit is set to 1 and then stored to a Time Array (by using ToDOp Store All Registers), the selected Time Array will start keeping time using the parameters loaded and that Time Array will be considered active. When this bit is cleared to 0 and then stored to a Time Array, the selected Time Array will stop keeping time and it will be considered inactive.
7:0	Domain Number	RWR	Domain Number. This is the IEEE 1588 or IEEE 802.1ASbt frame Domain Number that is to be associated with the selected Time Array. It is used to select which Time Array is to be used when processing PTP frames in hardware. This Domain number will only be used on active Time Arrays (that is, Time Arrays whose ClkValid bit above is set to 1).

1. Updating only the Comp (Compensation) register is needed when a Time Array is active, but the ppm difference between the local crystal and the associated Time Array's Grand Master clock has changed and must be adjusted
2. Loading all the parameters to a Time Array at a specific ToD Load Pt time is the method used to start a Time Array clock with the predetermined relationship between its associated Grand Master clock and the PTP Global Time (TAI Global Registers 4.8C1E and 4.8C0F).
3. OpCode 0x4 reads the selected Time Array's current clock values. The Tod Load Pt register is set to the current PTP Global Time value so the relationship between the two clock can be compared.

Table 234: PTP Global Time Array Register
Register 4.8F03 – PTP Global

Bits	Field	Type	Description
15:0	ToD Nano [15:0]	RWR	Time Array Time of Day, Nanosecond portion, bits [15:0] of a 32-bit register. The five ToD registers (at PTP Global Registers 4.8F03 to 4.8F07) contain the 10-byte representation of time used in IEEE 1588 and IEEE 802.1AS frames. These registers are used to load this representation of time into the selected Time Array on ToD Store All Registers operations. They contain the selected Time Array's representation of this time after ToD Capture operations complete. The upper 16 bits of this register are contained in the register below.

Table 235: PTP Global Time Array Register
Register 4.8F04 – PTP Global

Bits	Field	Type	Description
15:0	ToD Nano [31:16]	RWR	Time Array Time of Day, Nanosecond portion, bits [31:16] of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 236: PTP Global Time Array Register
Register 4.8F05 – PTP Global

Bits	Field	Type	Description
15:0	ToD Sec [15:0]	RWR	Time Array Time of Day, Seconds portion, bits [15:0] of a 48-bit register. See the description above. The upper 32 bits of this register are contained in the registers below.

Table 237: PTP Global Time Array Register
Register 4.8F06 – PTP Global

Bits	Field	Type	Description
15:0	ToD Sec [31:16]	RWR	Time Array Time of Day, Seconds portion, bits [31:16] of a 48-bit register. See the description above. The lower 16 bits of this register are contained in the register above. The upper 16 bits of this register are contained in the register below.

Table 238: PTP Global Time Array Register
Register 4.8F07 – PTP Global

Bits	Field	Type	Description
15:0	ToD Sec [47:32]	RWR	Time Array Time of Day, Seconds portion, bits [47:32] of a 48-bit register. See the description above. The lower 32 bits of this register are contained in the registers above.

Table 239: PTP Global Time Array Register
Register 4.8F08 – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [15:0]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [15:0] of a 64-bit register. The four 1722 ToD registers (at PTP Global Registers 4.8F08 to 4.8F0B) contain an 8-byte representation of time used in IEEE 1722 frames (IEEE 1722 uses only the lower 32 bits of this time. The 64-bit representation is used in PCI-e and it is a simple extension of the IEEE 1722 representation of time that wraps). These registers are used to load this representation of time into the selected Time Array on ToD Store All Registers operations. They contain the selected Time Array's representation of this time after ToD Capture operations complete. The upper 48 bits of this register are contained in the registers below.

Table 240: PTP Global Time Array Register
Register 4.8F09 – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [31:16]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [31:16] of a 64-bit register. See the description above. The lower 16 bits of this register are contained in the register above. The upper 32 bits of this register are contained in the registers below.

Table 241: PTP Global Time Array Register
Register 4.8F0A – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [47:32]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [47:32] of a 64-bit register. See the description above. The lower 32 bits of this register are contained in the registers above. The upper 16 bits of this register are contained in the register below.

Table 242: PTP Global Time Array Register
Register 4.8F0B – PTP Global

Bits	Field	Type	Description
15:0	1722 Nano [63:48]	RWR	Time Array 1722 Time of Day in Nanoseconds, bits [63:48] of a 64-bit register. See the description above. The lower 48 bits of this register are contained in the registers above.

Table 243: PTP Global Time Array Register
Register 4.8F0C – PTP Global

Bits	Field	Type	Description
15:0	ToD Comp [15:0]	RWR	Time Array Time of Day Compensation bits [15:0] of a 32-bit register. The two Time of Day Compensation registers (at PTP Global Registers 4.8F0C and 4.8F1D) are used to define the ppm difference between the local crystal clocking this PTP block and the PTP Grand Master device that this Time Array is tracking. Bits [30:0] of this register are used to define the difference between these two clocks in increments of 465.661 zeptoseconds (or 4.65661E-19 seconds, which is less than a single attosecond. For reference, picoseconds is 10^{-12}, femptoseconds is 10^{-15}, attoseconds is 10^{-18} and zeptoseconds is 10^{-21}). Set this register to the amount of time required to be added or subtracted to each local 125 MHz PTP clock period to make it match its associated Grand Master's rate (that is, the ppm difference between the two). A difference of 1 ppm for a 125 MHz local PTP clock is 8 femtoseconds (8.0E-15 seconds) or a setting of 17,182 decimal (0x431E) in this register. The full range of this register (0x7FFF FFFF) results in 1.0 ns of compensation per local PTP Clock. Bit 31 of this register is used to indicate the direction of the difference: 0 = The local clock is slow (must add the Comp to each cycle). 1 = The local clock is fast (must subtract the Comp from each cycle). These registers are used to load the required Compensation to the selected Time Array on ToD Store All Registers and on ToD Store only the Comp registers operations. They contain the selected Time Array's Compensation after a ToD Capture operation completes. When a Time Array is set active, use the ToD Store only the Comp register operation to update any detected changes in the ppm difference between the local crystal and its associated Grand Master. The upper 16 bits of this register are contained in the register below.

Table 244: PTP Global Time Array Register
Register 4.8F1D – PTP Global

Bits	Field	Type	Description
15:0	ToD Comp [31:16]	RWR	Time Array Time of Day Compensation bits [31:16] of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 245: PTP Global Time Array Register
Register 4.8F1E – PTP Global

Bits	Field	Type	Description
15:12	1 PPS Width	RWR	Pulse Width for the 1 Pulse Per Second on the Second signal. This register defines the pulse width of the selected 1 PPS signal (see 1 PPS Select bits below) in the units defined by the 1 PPS Width Range bits below. A value of 0x1 in this register selects 1 unit. A value of 0x0 selects 0 units (that is, stops the clock).
11	Reserved	RES	
10:8	1 PPS Width Range	RWR	Pulse Width Range for the 1 Pulse Per Second on the Second signal. This register selects the units of time used to define the 1 PPS Width (above) as follows (each higher numbered selection generates units that are 8x larger than the previous lower numbered selection): 0x0 = 8 ns units for a 125 MHz PTP clock 0x1 = 64 ns units for a 125 MHz PTP clock 0x2 = 512 ns units for a 125 MHz PTP clock 0x3 = 4,096 ns units for a 125 MHz PTP clock 0x4 = 32.768 μs units for a 125 MHz PTP clock 0x5 = 262.144 μs units for a 125 MHz PTP clock 0x6 = 2.097 ms units for a 125 MHz PTP clock 0x7 = 16.777 ms units for a 125 MHz PTP clock The narrowest width is 8 ns (by setting this register to 0x0 and the 1 PPS Width register to 0x1). The widest width is 251 ms or just a bit over ¼ second (by setting this register to 0x7 and the 1 PPS Width register to 0xF).
7:4	Reserved	RES	
3	1 PPS Phase	RWR	Phase of the 1 Pulse Per Second on the Second signal. When this bit is set to 1 the leading edge of the 1 PPS signal (the edge that occurs at the exact start of each second) is the falling edge of the signal. When this bit is cleared to 0, the leading edge of the 1 PPS signal is the rising edge of the signal.
2	Reserved	RES	
1:0	1 PPS Select	RWR	Select for the 1 Pulse Per Second on the Second signal. This register selects the Time Array that is used to generate the 1 PPS signal. Any of the Time Arrays can be selected, but only one at a time can be selected. The selected Time Array will output the leading edge of the 1 PPS signal when its ToD Seconds (PTP Global Registers 4.8F05 to 4.8F07) gets incremented. This increment occurs whenever the Time Array's ToD Nanoseconds (PTP Global Registers 4.8F08 to 4.8F0B) reaches 1,000,000 ns such that this 1 PPS signal occurs at the exact start of each second. The selected 1 PPS signal is available on LED [0] pins.

4.4 PTP TAI Registers

Table 246: TAI Global Config Register (Sheet 1 of 5)
Register 4.8C00 – TAI

Bits	Field	Type	Description
15	Event CapOv	RWR	Event Capture Overwrite. 0 = Capture and Hold first PTP Event. 1 = Capture all PTP Events and Retain the last PTP Event. When this bit is cleared to 0, it configures the hardware to capture a single event, that is, take a snapshot of PTP Global Timer value at the first EventReq (see EventPhase below) and wait for software to read the EventCapRegister before capturing another event. This mode returns the data from the first EventReq. When this bit is set to 1, it enables overwriting the EventCap registers (TAI Registers 4.8C09 to 4.8C0B) whenever an EventReq occurs (see EventPhase below). In this mode, the hardware will overwrite the EventCapRegister even if the previously captured event register data has not been read by the software. This mode returns the data from the last EventReq.
14	EventCtr Start	RWR	Event Counter Start. 0 = Do not increment the Event Capture Counter. 1 = Increment the Event Capture Counter on EventReq's. When this bit is cleared to 0, the EventCapCtr is not modified even when EventReq occurs (see EventPhase below). When this bit is set to 1, it enables incrementing the EventCapCtr register (TAI Register 4.8C09) whenever an EventReq occurs (see EventPhase below).
13	Event Phase	RWR	Event Phase. 0 = Event Requests occur on the rising edge of the PTP_EVREQ LED [1] pin. 1 = Event Requests occur on the falling edge of the PTP_EVREQ LED [1] pin. When this bit is cleared to 0, an EventReq occurs on the rising edge of the PTP_EVREQ input or on the leading edge of PTP_TRIG when internally sampled (see the CaptureTrig bit in TAI Register 4.8C09). When this bit is set to 1, an EventReq occurs on the falling edge of the PTP_EVREQ input or on the trailing edge of PTP_TRIG when internally sampled. When PTP_TRIG is selected to be internally captured (instead of using the PTP_EVREQ LED [1] pin – see Capture Trig in TAI Register 4.8C09) this Event Phase is used to invert the value of the normal internal PTP_TRIG that is captured. When Event Phase = 0, the leading edge (or normal rising edge) of the internal PTP_TRIG is captured. When Event Phase = 1, the trailing edge (or normal falling edge) of the internal PTP_TRIG is captured.

Table 246: TAI Global Config Register (Sheet 2 of 5)
Register 4.8C00 – TAI

Bits	Field	Type	Description
12	TrigPhase	RWR	Trigger Phase. 0 = The PTP Trigger output is active high on the PTP_TRIG LED [1] pin. 1 = The PTP Trigger output is active low on the PTP_TRIG LED [1] pin. When this bit is cleared to 0, the active phase of the PTP_TRIG output to the LED [1] is normal active high. For example, the pulse mode of PTP_TRIG will be normally low with a high pulse and the 50% duty cycle's leading edge is the rising edge. When this bit is set to 1, the active phase of the PTP_TRIG output to the LED [1] is inverted to be active low. For example, the pulse mode of PTP_TRIG will be normally high with a low pulse and the 50% duty cycle's leading edge is the falling edge. **NOTE:** This bit has no effect on the internal phase of PTP_TRIG or any other signal used in the internal blocks of the device.
11	Reserved	RES	
10	IRLClk Gen Req	RWS	Ingress Rate Limiter's Clock Generation Request/Enable. When this bit is set to 1, it enables a 50% duty cycle clock generation for the Ingress Rate Limiter's logic (IRL Clk) as configured by the IRLClkGenAmt, IRLClkComp (both ps and sub-ps) and IRLGenTime fields. On Reset, this IRL Clock defaults to a 3.125 μs rate. This rate can be changed at any time by updating the IRLClkGenAmt and/or IRLClkComp (ps and Sub ps) registers.
9	TrigGen IntEn	RWR	Trigger Generator Interrupt Enable. 0 = Mask interrupts generated by the PTP Trigger logic. 1 = Enable interrupts generated by the PTP Trigger logic. When this bit is cleared to 0, no interrupts are generated by the TrigGen logic. When this bit is set to 1, the TAI block will generate an interrupt whenever a TrigGen pulse event has occurred. This interrupt will appear in the Trigger Mode Interrupt in PTP Global Register 4.8E08.
8	EventCap IntEn	RWR	Event Capture Interrupt Enable. 0 = Mask interrupts generated by the PTP Event Capture logic. 1 = Enable interrupts generated by the PTP Event Capture logic. When this bit is cleared to 0, no interrupts are generated by the EventCap logic. When this bit is set to 1, the TAI block will generate an interrupt whenever an EventReq occurs. This interrupt will appear in the Event Capture Interrupt in PTP Global Register 4.8E08.

Table 246: TAI Global Config Register (Sheet 3 of 5)
Register 4.8C00 – TAI

Bits	Field	Type	Description
7	TrigLock	SC	Trigger Lock. When this bit is set to 1, the leading edge of PTP_TRIG (see TrigPhase above) will be adjusted to the value contained in the TrigGenTime register (TAI Register 4.8D00 and 4.8D01) if and only if the leading edge of PTP_TRIG occurs ± the number of PTP Clocks as defined in the TrigLockRange register below and PTP_TRIG is enabled (TrigGenReq, below, is set to 1) and the TrigGenTime register is non-zero. **NOTE:** The TrigLockRange, the TrigGenTime registers must be configured before this bit is set to 1. Once the TrigGenTime past in time, this bit will self clear (that is, it will be active for only one possible correction per wrap around of the 32-bit Global Timer). This bit will clear if the Global time has passed even if a correction was not required or done. When this bit clears the Lock correction amount, if any, will be registered in the Lock Correction fields for PTP_TRIG (TAI Register 4.8D02).
6:4	TrigLock Range	RWR	Trigger Locking Range. These bits are used along with the TrigLock bit above. They determine the ±error limit to adjust and re-center the leading edge of PTP_TRIG in PTP_CLK increments (8 ns if using the internal clock) or PTP_EXTCLK increments (if using an external PTP clock).
3	Block Update	RWR	Block Update. 0 = Update the 50% duty cycle clock mode registers as written. 1 = Update the 50% duty cycle clock mode registers as a block. When the 50% duty cycle clock mode is enabled (see TrigMode below), the following registers are used to configure that mode: TrigGenAmt (TAI Register 4.8C02 and Register 4.8C03), TrigClkComp (TAI Register 4.8C04) and TrigClkCompSubPs (TAI Register 4.8C05). To compensate for ppm drift between this node's crystal and the Grand Master's crystal, these registers may required periodic updates. The same is true for the IRL clock which is configured using IRLClkGenAmt (TAI Register 4.8C06), IRLClkComp (TAI Register 4.8C07) and IRLClkCompSupPs (TAI Register 4.8C08). Setting this register bit to 1 allows the updated values in these register groups (TAI Registers 4.8C02 to 4.8C05 and TAI Registers 4.8C06 to 4.8C08) to be presented to the hardware together at the same time and at a time when the hardware is not using these register values. This mode ensures smooth, glitch free, updates when the contents of more than one register must change during an update. The contents of the TRIG registers (TAI Registers 4.8C02 to 4.8C05) are presented to the hardware as a block whenever the TrigClkCompSubPs register is written to (at TAI Register 4.8C05). The contents of the IRL_Clk registers (TAI Registers 4.8C06 to 4.8C08) are presented to the hardware as a block whenever the IRLClkCompSubPs register is written to (at TAI Register 4.8C08). This means that it is not required for the software to write all of these registers during an update. Only the registers that are changing must be written to (it is assumed that the sub-picosecond register must be adjusted for each update, so writing to this register triggers the update).

Table 246: TAI Global Config Register (Sheet 4 of 5)
Register 4.8C00 – TAI

Bits	Field	Type	Description
2	MultiPTP Sync	RWR	Multiple PTP device sync mode. This is used in systems where multiple PTP enabled devices' are required to synchronize their PTP Global Time counters (TAI Registers 4.8C1E to 4.8C0F). 0 = Normal Event Request mode 1 = Enable Multiple PTP device sync mode. When this bit is cleared to 0, the EventRequest interface operates normally (that is, an EventReq transfers the value of the PTP Global Time [31:0] register to the EventCapTime [31:0] register based on the setting of the EventCapOv register above). When this bit is set to 1, an EventReq (see EventPhase above) transfers the value in TrigGenAmt [31:0] (TAI Registers 4.8C02 to 4.8C03) into the PTP Global Time [31:0] register (TAI Registers 4.8C1E and 4.8C0F). The EventCapTime [31:0] (TAI Registers 4.8D01 and 4.8D02) is also updated at the same time with the previous value that the PTP Global Time [31:0] register contained prior to be updated.
1	TrigMode	RWR	Trigger Mode. 0 = 50% duty cycle clock mode 1 = Pulse (one-shot) mode When this bit is cleared to 0, the 50% duty cycle clock mode is enabled. In this mode the value specified in the TrigGenAmt is used as the period for generating a 50% duty cycle clock on the PTP_TRIG signal. The minimum clock period that can be generated on the PTP_TRIG signal is 4 times the TSClkPer amount. The frequency of this clock can be adjusted in ps increments (see TrigClkComp, TAI Register 4.8C04) and it can be realigned to a specific time (see TrigLock bit above). The first leading edge of the 50% duty cycle clock will occur the first time the PTP Global Time (PTP TAI Registers 4.8C1E and 4.8C0F) equals the value in the non-zero TrigGenTime register (PTP TAI Registers 4.8D00 and 4.8D01) after TrigGenReq, below, is set to 1. This leading edge control occurs as long as the TrigGenTime register is non-zero. If it is zero, then the leading edge will occur when the TrigGenReq bit below is set to 1 without regard to the PTP Global Time. The phase of the leading edge is controlled by the TrigPhase bit above. When this bit is set to 1, Pulse mode is enabled. This mode matches the PTP Global Timer (TAI Registers 4.8C1E and 4.8C0F) and the TrigGenAmt register (TAI Registers 4.8C02 and 4.8C03) to generate a pulse at that time on the PTP_TRIG signal. The width of the pulse is specified by PulseWidth and PulseWitdhRange (TAI Register 4.8C05). **NOTE:** The minimum pulse width that can be generated is one TSClkPer amount (TAI Register 4.8C01) and the maximum pulse width is more than 30 million times the TSClkPer. The phase of the pulse is controlled by TrigPhase bit above.

Table 246: TAI Global Config Register (Sheet 5 of 5)
Register 4.8C00 – TAI

Bits	Field	Type	Description
0	TrigGen Req	RWR or SC	Trigger Generation Request/Enable. When this bit is set to 1, it enables a one-shot pulse or the 50% duty cycle clock generation on PTP_TRIG as previously configured by the TrigGenAmt, TrigMode, TrigClkComp (ps and Sub ps), PulseWidth, and TrigGenTime fields. If TrigMode (above) is set to 1 (pulse mode), then this bit will self-clear after the pulse occurs (that is, the trailing edge of the pulse as defined by the Pulse Width and Pulse Width Range registers (TAI Register 4.8C05). If TrigMode is cleared to 0, the 50% duty cycle clock will continue running as long as this bit is set to 1.

Table 247: TAI Global Config Register
Register 4.8C01 – TAI

Bits	Field	Type	Description
15:0	TSClkPer	RWS 0x1F40	Time Stamping Clock Period in picoseconds. This field specifies the clock period for the timestamping clock supplied to the PTP hardware. When this device is using the 125 MHz internally generated clock for the PTP hardware, the value of this register must be 0x1F40, or 8000 decimal which indicates a clock period of 8000 ps or 8 ns (or 125 MHz). When this device's PTP hardware is clocked by an external clock (using PTP_EXTCLK – see PtpExtClk in TAI Register 4.8C08) this register must be set to the number of ps in that clock's period.

Table 248: TAI Global Config Register
Register 4.8C02 – TAI

Bits	Field	Type	Description
15:0	TrigGen Amt [15:0]	RWR	Trigger Generation Amount bits [15:0] of a 32-bit register. This field specifies the PTP Time Application Interface trigger generation time amount. When TrigMode is set to 1, the value specified in this field is compared with the PTP Global Timer (TAI Registers 4.8C1E and 4.8C0F) and when it matches the first time, a pulse is generated on PTP_TRIG whose width is controlled by PulseWidth (TAI Register 4.8C05). In this mode there is an internal delay of three TSClkPer before the leading edge of the pulse will be seen on the PTP_TRIG output pin. When TrigMode is cleared to 0, the value in this field is used as a clock period in TSClkPer increments (TAI Register 4.8C01) to generate an output clock on the PTP_TRIG signal (see TrigPhase in TAI Register 4.8C00). In this mode the TrigClkComp amount (TAI Register 4.8C04) and TrigClkCompSubPs (TAI Register 4.8C05) gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer, one TSClkPer amount gets added to or subtracted from the next trailing edge of PTP_TRIG clock output. **NOTE:** In 50% duty cycle clock mode, the contents of this register can be presented to the hardware at the same time all the other 50% duty cycle registers are. See BlockUpdate in TAI Register 4.8C00. The upper 16 bits of this register are contained in the register below.

Table 249: TAI Global Config Register
Register 4.8C03 – TAI

Bits	Field	Type	Description
15:0	TrigGen Amt [31:16]	RWR	Trigger Generation Amount bits [31:16] of a 32-bit register. This field specifies the PTP Time Application Interface trigger generation time amount. See the description above. The lower 16 bits of this register are contained in the register above.

Table 250: TAI Global Config Register
Register 4.8C04 – TAI

Bits	Field	Type	Description
15	TrigComp Dir	RWR	Trig Clock Compensation Direction. When the accumulated TrigClkComp amount (below) exceeds the value in TSClkPer (TAI Register 4.8C01), one TSClkPer amount gets added to or subtracted from the next PTP_TRIG clock output. This bit determines which as follows: 0 = Add one TSClkPer to the next PTP_TRIG cycle. 1 = Subtract one TSClkPer from the next PTP_TRIG cycle.
14:0	TrigClk Comp	RWR	Trigger mode Clock Compensation Amount. This value is in picoseconds as an unsigned number. This field is used in 50% duty cycle clock mode only (when TrigMode is cleared to 0 and TrigGenReq is set to 1). This field specifies the remainder amount in ps for the clock that is being generated with a period specified by the TrigGenAmt (TAI Registers 4.8C02 and 4.8C03). This field must be set as an absolute error number in ps (in other words it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. In the 50% duty cycle clock mode, this register gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer (TAI Register 4.8C01), one TSClkPer amount gets added to or subtracted from the next PTP_TRIG clock output. This requires that the absolute value of TrigClkComp must not exceed the size of the TSClkPer. If it does, then the TSClkPer must be adjusted in size (either up or down) until the remainder that remains is less that the TSClkPer and that value gets put into this register. **NOTE:** In 50% duty cycle clock mode, the contents of this register can be presented to the hardware at the same time all the other 50% duty cycle registers are. See BlockUpdate in TAI Register 4.8C00.

Table 251: TAI Global Config Register
Register 4.8C05 – TAI

Bits	Field	Type	Description
15:12	Pulse Width	RWS 0xF	Pulse width for PTP_TRIG. This pulse width is in units of TSClkPer (TAI Register 4.8C01). This specifies the width of the pulse that gets generated on PTP_TRIG (see TrigPhase in TAI Register 4.8C00) when the one shot pulse mode is selected (TrigMode is set to 1 and TrigGenReq is set to 1). If the PTP_EXTCLK is not used (that is, the internal clock is being used – see PtpExtClk in TAI Register 4.8C08) the TSClkPer, or Pulse Width unit is 8 ns (assuming the Pulse Width Range, below, is 0x0). **NOTE:** Setting this register to 0x0 will cause unpredictable results.
11	Reserved	RES	
10:8	Pulse Width Range	RWR	Pulse Width Range for the PTP_TRIG signal. This register selects the units of time used to define the Pulse Width (above) as follows (each higher numbered selection generates units that are 8x larger than the previous lower numbered selection): 0x0 = 8 ns units for a 125 MHz PTP clock or 1 x TSClkPer 0x1 = 64 ns units for a 125 MHz PTP clock or 8 x TSClkPer 0x2 = 512 ns units for a 125 MHz PTP clock or 64 x TSClkPer 0x3 = 4,096 ns units for a 125 MHz PTP clock or 512 x TSClkPer 0x4 = 32.768 μs units for a 125 MHz PTP clock or 4,096 x TSClkPer 0x5 = 262.144 μs units for a 125 MHz PTP clock or 32,768 x TSClkPer 0x6 = 2.097 ms units for a 125 MHz PTP clock or 262,144 x TSClkPer 0x7 = 16.777 ms units for a 125 MHz PTP clock or 2,097,152 x TSClkPer The narrowest width is 8 ns (assuming a 125 MHz PTP clock) or one TSClkPer (by setting this register to 0x0 and the Pulse Width register, above, to 0x1). The widest width is 251 ms (assuming a 125 MHz PTP clock) or just a bit over ¼ second (by setting this register to 0x7 and the Pulse Width register to 0xF). The maximum number is 31,457,280 TSClkPer.
7:0	TrigClk Comp SubPs	RWR	Trigger mode Clock Compensation Amount. This value is in sub-picoseconds as an unsigned number. This field is used in 50% duty cycle clock mode only (when TrigMode is cleared to 0 and TrigGenReq is set to 1). This field specifies the remainder amount in sub ps increments for the clock that is being generated with a period specified by the TrigGenAmt (TAI Registers 4.8C02 and 4.8C03). This field must be set as an absolute error number in Sub ps (that is, it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. Each unit in this register is $1/256^{th}$ of a ps or approximately 4 femtoseconds (the actual number is 3.90625 femtoseconds per unit). In the 50% duty cycle clock mode, this register gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds on ps, one ps gets added to the accumulated Trig Clock Compensation (TAI Register 4.8C04). **NOTE:** In 50% duty cycle clock mode, the contents of this register can be presented to the hardware at the same time all the other 50% duty cycle registers are presented. The writing to this register is used to transfer this data as a block. See BlockUpdate in TAI Register 4.8C00.

Table 252: TAI Global Status Register
Register 4.8D00 – TAI

Bits	Field	Type	Description
15	Reserved	RES	
14	Capture Trig	RWR	Capture Trig. 0 = Capture PTP_EVREQ pin events. 1 = Capture PTP_TRIG internal events. When this bit is cleared to 0, the Event Capture register looks at events on the PTP_EVREQ pin. When this bit is set to 1, the Event Capture register looks at events from the waveform generated by PTP_TRIG. This allows observing the rising or falling edge of the PTP_TRIG (the EventPhase register is still active, PTP TAI Register 4.8C00) without the requirement of using pins. This is used to ensure the edges have not drifted over time so they can be realigned if required.
13:10	Reserved	RES	
9	EventCap Err	RWR	Event Capture Error. This bit gets set by the hardware logic when an EventReq has occurred (see EventPhase in TAI Register 4.8C00) where the EventCapValid bit, below, is already set to 1 and the EventCapOv bit (TAI Register 4.8C00) is cleared to 0. This condition could occur if the EventReqs are occurring faster than the local CPU can process them (and clear the EventCapValid bit before the next EventReq). Some number of missed EventReq can be seen in the EventCapCtr, below, if it is enabled.
8	EventCap Valid	RWR	Event Capture Valid. This bit is set to 1 whenever the EventCap (Event Capture – TAI Registers 4.8D01 and 4.8D02) register contains the time of a captured event. Software must clear this bit to 0 to enable the EventCap Register to be able to acquire a subsequent event if the EventCapOv (Event Capture Override – TAI Register 4.8C00) is not enabled. Clearing this bit to 0 also clears the EventInt (Event Capture Interrupt – PTP Global Register 4.8E08).
7:0	EventCap Ctr	RWR	Event Capture Counter. This field is incremented once by each EventReq (see EventPhase in PTP TAI Register 4.8C00) as long as EventCtrStart (PTP TAI Register 4.8C00) is set to 1. This counter wraps around and can be cleared by writing 0s to it.

Table 253: TAI Global Status Register Register 4.8D01 – TAI

Bits	Field	Type	Description
15:0	EventCap Register [15:0]	RWR	Event Capture Register bits [15:0] of a 32-bit register. This register captures the value of the PTP Global Timer (TAI Registers 4.8C1E and 4.8C0F) when an EventReq (see EventPhase in TAI Register 4.8C00) has occurred. If the EventCapOv (TAI Register 4.8C00) is set to 1, then this register indicates the time captured for the last event. When EventCapErr is set to 1, the contents in this register no longer represent the time of the first event. **NOTE:** The maximum jitter for the EventCapRegister time amount with respect to the EventReq on the LED/GPIO pin is one TSClkPer amount. **NOTE:** The minimum EventReq input signal high or low width must be equal to or greater than 1.5 times the TSClkPer amount. **NOTE:** For the hardware to capture the EventReq on the LED/GPIO input signal, the minimum gap between two consecutive events must be 150 plus 5 times the TSClkPer amount. The upper 16 bits of this register are contained in the register below.

Table 254: TAI Global Status Register Register 4.8D02 – TAI

Bits	Field	Type	Description
15:0	EventCap Register [31:16]	RWR	Event Capture Register bits [31:16] of a 32-bit register. This register captures the value of the PTP Global Timer (TAI Registers 4.8C1E and 4.8C0F) when an EventReq (see EventPhase in TAI Register 4.8C00) has occurred. See the description above. The lower 16 bits of this register are contained in the register above.

Table 255: TAI Global Status Register Register 4.8C1E – TAI

Bits	Field	Type	Description
15:0	PTPGlobalTime [15:0]	RO	PTP Global Timer bits [15:0] of a 32-bit register. This indicates the global timer value that is running off of the free running switch core clock. This counter wraps around in hardware. To support synchronization of PTP Global Time between multiple devices in a system, this register gets updated with the value specified in TrigGenAmt when MultiPTPSync is set to 1 (TAI Register 4.8C00) and an EventReq occurs (see EventPhase in TAI Register 4.8C00). The upper 16 bits of this register are contained in the register below.

Table 256: TAI Global Status Register
Register 4.8C0F – TAI

Bits	Field	Type	Description
15:0	PTPGlobalTime [31:16]	RO	PTP Global Timer bits [31:16] of a 32-bit register. This indicates the global timer value that is running off of the free running switch core clock. This counter wraps around in hardware. See the description above. The lower 16 bits of this register are contained in the register above.

Table 257: TAI Global Config Register
Register 4.8C09 – TAI

Bits	Field	Type	Description
15:0	TrigGen Time [15:0]	RWR	Trigger Generation Time bits [15:0] of a 32-bit register. This field specifies the PTP Global Time (TAI Registers 4.8C1E and 4.8C0F) where the first leading edge of PTP_TRIG will occur (with a three TSClkPer latency) when PTP Trig is in the continuous square-wave mode (for example, when TrigMode is 0x0, offset 0x00 above) as long as this register's value is not 0. If its value is 0, then the first leading edge of PTP_TRIG will occur when TrigGenReg is set to 1 (TAI Register 4.8C00). This register is also used to for relocking the leading edge of the square wave (see TrigLock in TAI Register 4.8C00). The upper 16 bits of this register are contained in the register below.

Table 258: TAI Global Config Register
Register 4.8C0A – TAI

Bits	Field	Type	Description
15:0	TrigGen Time [31:16]	RWR	Trigger Generation Time bits [31:16] of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 259: TAI Global Config Register (Sheet 1 of 2)
Register 4.8C0B – TAI

Bits	Field	Type	Description
15:5	Reserved	RES	
4	LockCorr Valid	RO	Trig Lock Correction Valid. 0 = Trig Lock Correction is not valid or did not occur. 1 = Trig Lock Correction is valid and did occur. When a Trigger Lock is enabled (TAI Register 4.8C00), this bit is cleared to 0. When the Trigger Lock completes, this bit will be set to 1 only if a Trigger Lock occurred for PTP_TRIG. In this case, the Lock Correction value below will show the amount of adjustment that was made (if any).

Table 259: TAI Global Config Register (Sheet 2 of 2)
Register 4.8C0B – TAI

Bits	Field	Type	Description
3:0	Lock Correction	RO	Trig Lock Correction amount. When the TrigLock bit is set to 1 (TAI Register 4.8C00) enabling a potential clock adjustment, these bits are cleared to 0. When the TrigLock bit is cleared to 0 (indicating that the requested clock adjustment is now past in time), these bits will reflect the magnitude and direction that was applied to the PTP_TRIG leading edge of the generated clock. A value of 0 means no adjustment was necessary. If bit 3 is 1, then the leading edge of the clock was moved *n* number of clocks earlier in time where *n* is shown in bits [2:0]. If bit 3 is 0, then the leading edge of the clock was moved *n* number of clocks later in time where *n* is shown in bits [2:0].

Table 260: TAI Global Config Register
Register 4.8D1E – TAI

Bits	Field	Type	Description
15	Reserved	RES	
14	PtpExtClk	RWR	PTP External Clock select. 0 = Use internal clock for the PTP core. 1 = Use external clock for the PTP core. When this bit is cleared to 0, the PTP core gets its clock from an internal 125 MHz clock based on the device's XTAL_IN input. When this bit is set to 1, the PTP core gets its clock from the device's PTP_EXTCLK pin. **NOTE:** Do not select the PTP_EXTCLK pin unless the pin (CONFIG pin) has a clock and CONFIG pins is configured to be the PTP_EXTCLK.
13:0	Reserved	RES	

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 261: Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA}	Power Supply Voltage on AVDD18 with respect to VSS	–	–	1.98	V
V_{DDAR}	Power Supply Voltage on AVDD33 with respect to VSS	–	–	3.63	V
V_{REG_IN}	Power Supply Voltage on REG_IN (VDD33) with respect to VSS	–	–	3.63	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	–	–	1.0	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS	–	–	3.63	V
V_{PIN}	Voltage Applied to Any Digital Input Pin	–	–	3.63 or VDDO + 0.5 whichever is less	V

5.2 Recommended Operating Conditions

Table 262: Recommended Operating Conditions

Symbol	Parameter	Condition[3]	Min	Typ	Max	Unit
V_{DDA}[1,2]	AVDD18 Supply	For AVDD18	1.71	1.8	1.890	V
V_{DDAR}[1]	AVDD33 Supply	For AVDD33	3.14	3.3	3.46	V
V_{DD}[1,2]	DVDD Supply	For DVDD	0.855	0.9	0.945	V
V_{DDO}[1]	VDDO Supply	For VDDO at 1.8V	1.71	1.8	1.890	V
		For VDDO at 2.5V	2.38	2.5	2.62	V
		For VDDO at 3.3V	3.14	3.3	3.46	V
RSET	Internal Bias Reference	Resistor connected to V_{SS}	–	4990±1% Tolerance	–	Ω
T_A	Ambient Operating Temperature	Automotive Grade 2	-40	–	105	°C
T_J	Maximum Junction Temperature	Automotive Grade 2	–	–	125	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. The recommended operating conditions mentioned here for AVDD18 and DVDD are applicable only when using external supplies. They are not applicable when using internal regulators.
3. The device meets AEC-Q100. ESD HBM: ±2 KV, ±1 KV, ±500V.
   CDM: ±750V corner pins, ±500V all other pins

5.3 Package Thermal Information

Table 263: Thermal Conditions for 88Q2110 40-pin QFN Package

Symbol	Parameter[1]	Condition	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	25.69	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	22.16	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	21.37	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	20.76	–	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	–	10.37	–	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance $\theta_{JC} = (T_J - T_C)/P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	–	10.70	–	°C/W
ψ_{JB}	Junction-to-Board Thermal Characterization Parameter $\psi_{JB} = (T_J - T_{bottom})/P$ P = Total Power Dissipation T_{bottom} = Temperature on the Bottom of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	10.50	–	°C/W
ψ_{JT}	Junction-to-Top-Center Thermal Characterization Parameter $\psi_{JT} = (T_J - T_{top})/P$ P = Total Power Dissipation T_{top} = Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	0.39	–	°C/W

1. Refer to the white paper on T_J Thermal Calculations for detailed information.

Table 264: Thermal Conditions for 88Q2112 48-pin QFN Package

Symbol	Parameter[1]	Condition	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	25.61	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	22.09	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	21.30	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	20.80	–	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	–	10.94	–	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance $\theta_{JC} = (T_J - T_C)/P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	–	10.06	–	°C/W
ψ_{JB}	Junction-to-Board Thermal Characterization Parameter $\psi_{JB} = (T_J - T_{bottom})/P$ P = Total Power Dissipation T_{bottom} = Temperature on the Bottom of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	11.06	–	°C/W
ψ_{JT}	Junction-to-Top-Center Thermal Characterization Parameter $\psi_{JT} = (T_J - T_{top})/P$ P = Total Power Dissipation T_{top} = Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	0.39	–	°C/W

1. Refer to the white paper on T_J Thermal Calculations for detailed information.

5.4 Current Consumption

5.4.1 Current Consumption when Using External Regulators

Note

Table 265, Table 266, Table 267, and Table 268 provide electrical data for the Max setting of fast corner devices at 105°C temperature and supplies running 5% above nominal values. The Typical setting is for typical devices at room temperature of 25°C with external supplies at nominal values. The data was extracted from devices running with an external power supply.

5.4.1.1 Current Consumption AVDD18

Table 265: Current Consumption AVDD18
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{AVDD}	1.8V Power to Analog Core	AVDD18	IEEE Power Down		–	35	36	mA
			RGMII with traffic	1000BASE-T1	–	122	125	mA
				100BASE-T1	–	85	100	mA
			SGMII with traffic	1000BASE-T1	–	137	140	mA
				100BASE-T1	–	100	115	mA

5.4.1.2 Current Consumption AVDD33

Table 266: Current Consumption AVDD33
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{AVDDR}	Analog 3.3V Supply	AVDD33	IEEE Power Down		–	1	1	mA
			RGMII with traffic	1000BASE-T1	–	24	26	mA
				100BASE-T1	–	28	29	mA
			SGMII with traffic	1000BASE-T1	–	24	26	mA
				100BASE-T1	–	28	29	mA

5.4.1.3 Current Consumption DVDD

Table 267: Current Consumption DVDD
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{VDD}	0.9V Power to Digital Core	DVDD	IEEE Power Down		–	9	168	mA
			RGMII with traffic	1000BASE-T1	–	262	427	mA
				100BASE-T1	–	80	218	mA
			SGMII with traffic	1000BASE-T1	–	263	427	mA
				100BASE-T1	–	80	222	mA

5.4.1.4 Current Consumption VDDO

Table 268: Current Consumption VDDO
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition			Min	Typ	Max	Unit
I_{VDDO}	Power to the Digital I/Os	VDDO	IEEE Power Down		VDDO = 3.3V	–	2	6	mA
					VDDO = 2.5V	–	2	5	mA
					VDDO = 1.8V	–	1	4	mA
			RGMII with traffic	1000BASE-T1	VDDO = 3.3V	–	31	34	mA
					VDDO = 2.5V	–	26	29	mA
					VDDO = 1.8V	–	18.6	23	mA
				100BASE-T1	VDDO = 3.3V	–	8	11	mA
					VDDO = 2.5V	–	6	9	mA
					VDDO = 1.8V	–	4	7	mA
			SGMII with traffic	1000BASE-T1	VDDO = 3.3V	–	2	5	mA
					VDDO = 2.5V	–	1.5	4	mA
					VDDO = 1.8V	–	1.1	3	mA
				100BASE-T1	VDDO = 3.3V	–	2	5	mA
					VDDO = 2.5V	–	1.5	4	mA
					VDDO = 1.8V	–	1.1	3	mA

5.4.2 Current Consumption when Using Internal Regulators

5.4.2.1 Current Consumption REG_IN (AVDD18_IN and DVDD by LDO)

Note

In Table 269 and Table 270, the Max setting is for fast corner devices at 85°C temperature using LDO with 3.3V supply at 5% above nominal. The Typical setting is for typical corner device at 25°C temperature using LDO with 3.3V supply at nominal setting.

The 88Q2110/88Q2112 using all direct supplies can meet Grade 2 requirements.

Table 269: Current Consumption Dual LDO REG_IN (AVDD18 and DVDD by LDO)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{REG_IN}	3.3V Internal Regulator Supply	REG_IN	IEEE Power Down		–	47	146	mA
			RGMII with traffic	1000BASE-T1	–	381	533	mA
				100BASE-T1	–	166	280	mA
			SGMII with traffic	1000BASE-T1	–	395	542	mA
				100BASE-T1	–	181	297	mA

Note

When using internal regulators, AVDD18 and DVDD are supplied internally using the 3.3V REG_IN regulator supply. VDDO and AVDD33 must still be supplied externally.

Table 270: Current Consumption Single LDO REG_IN (AVDD18 by LDO)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{REG_IN}	3.3V Internal Regulator Supply	REG_IN	IEEE Power Down		–	35	35	mA
			RGMII with traffic	1000BASE-T1	–	122	125	mA
				100BASE-T1	–	87	101	mA
			SGMII with traffic	1000BASE-T1	–	137	140	mA
				100BASE-T1	–	101	117	mA

Note

When using a single internal regulator, AVDD18 is supplied internally using the 3.3V REG_IN regulator supply. VDDO, DVDD, and AVDD33 must still be supplied externally.

5.4.2.2 Current Consumption AVDD18_IN (DVDD by LDO)

Note

In Table 271, the Max setting is for fast corner devices at 85°C temperature using LDO with 3.3V supply at 5% above nominal. The Typical setting is for typical corner device at 25°C temperature using LDO with 3.3V supply at nominal setting.

The 88Q2110/88Q2112 using all direct supplies can meet Grade 2 requirements.

The 88Q2110/88Q2112 with a single LDO option can meet Grade 3 requirements.

Table 271: Current Consumption Single AVDD18_IN (DVDD by LDO)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{AVDD18_IN}	1.8V Internal Regulator Supply	AVDD18_IN	IEEE Power Down		–	8	139	mA
			RGMII with traffic	1000BASE-T1	–	262	389	mA
				100BASE-T1	–	80	185	mA
			SGMII with traffic	1000BASE-T1	–	263	391	mA
				100BASE-T1	–	81	192	mA

Note

When using a single internal regulator, DVDD is supplied internally using the AVDD18_IN regulator supply. VDDO, AVDD18, and AVDD33 and REG_IN must still be supplied externally.

5.5 DC Operating Conditions

5.5.1 Digital Pins

Table 272: Digital Pins
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins[1]	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage	All digital inputs	VDDO = 3.3V	2.0	–	VDDO + 0.3V	V
			VDDO = 2.5V	1.75	–	VDDO + 0.3V	V
			VDDO = 1.8V	1.26	–	VDDO + 0.3V	V
VIL	Input Low Voltage	All digital inputs	VDDO = 3.3V	–	–	0.8	V
			VDDO = 2.5V	–	–	0.75	V
			VDDO = 1.8V	-0.3	–	0.54	V
VOH	High-level Output Voltage	All digital outputs	–	VDDO - 0.4V	–	–	V
VOL	Low-level Output Voltage	All digital outputs	–	–	–	0.4	V
I_{ILK}	Input Leakage Current	–	–	–	–	10	µA
C_{IN}	Input Capacitance	All pins	–	–	–	5	pF

1. VDDO supplies the TEST, GPIO, TX_ENABLE, MDIO, MDC, INTn, RESETn, TXD [3:0], TXC, TCLK, RCLK, RXC, and RXD [3:0] pins.

5.5.2 TX_ENABLE Pin

Table 273: TX_ENABLE Pin
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
VOH	High-level Output Voltage	TX_ENABLE output	IOH = -8 mA	VDDO - 0.4V	–	–	V
VOL	Low-level Output Voltage	TX_ENABLE output	IOL = 8 mA	–	–	0.4	V
I_{MAX}	Total Maximum Current per Port	TX_ENABLE pin	–	–	–	–	mA
I_{ILK}	Input Leakage Current	TX_ENABLE pin	–	–	–	10	µA
C_{IN}	Input Capacitance	TX_ENABLE pin	–	–	–	5	pF

5.5.3 IEEE Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications:

- 1000BASE-T1

Table 274: PMA Electrical Specifications (IEEE Std 802bp-2016)

Tests	Min	Max	Unit
Maximum Output Droop Negative	–	10	%
Transmitter Distortion	–	15	mV
Transmitter Timing Jitter Master	–	RMS <5, Peak-to-Peak <50	ps
Transmitter Timing Jitter Slave	–	RMS <10, Peak-to-Peak <100	ps
Transmitter Timing Jitter MDI	–	RMS <5, Peak-to-Peak <50	ps
Transmit Power Level	–	5	dBm
Transmitter Power Spectral Density	Fit template		
Transmitter Peak Differential Output	–	1.3	V peak-peak
Transmitter Clock Frequency	–	±100	ppm

5.5.4 SGMII Interface

SGMII specification is a de-facto standard proposed by Cisco. It is available at the Cisco website (ftp://ftp-eng.cisco/smii/sgmii.pdf). It uses a modified LVDS specification based on the IEEE standard 1596.3. Refer to that standard for the exact definition of the terminology used in the following table. The device adds flexibility by allowing programmable output voltage swing and supply voltage option.

5.5.4.1 Transmitter DC Characteristics

Table 275: Transmitter DC Characteristics
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

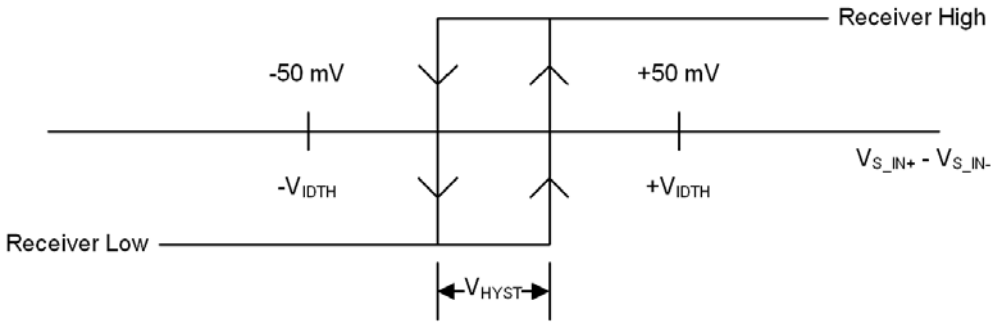
Symbol	Parameter	Min	Typ	Max	Unit
VOH	Output Voltage High	–	–	1600	mV
VOL	Output Voltage Low	700	–	–	mV
VRING	Output Ringing	–	–	10	%
|VOD|	Output Voltage Swing (differential peak)	75	–	–	mV peak
VOS	Output Offset Voltage (also called Common Mode Voltage)	787.5	–	–	mV
RO	Output Impedance (Single-ended) (50Ω Termination)	40	–	60	Ω
Delta R_O	Mismatch in a Pair	–	–	10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1	–	–	25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1	–	–	25	mV
IS+, IS-	Output Current on Short to VSS	–	–	40	mA
IS+-	Output Current when S_OUT+ and S_OUT- are Shorted	–	–	12	mA
IX+, IX-	Power Off Leakage Current	–	–	10	mA

5.5.4.2 Receiver DC Characteristics

Table 276: Receiver DC Characteristics
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_I	Input Voltage Range A or B	675	–	1725	mV
V_{IDTH}	Input Differential Threshold	50	–	50	mV
V_{HYST}	Input Differential Hysteresis	25	–	–	mV
R_{IN}	Receiver 100Ω Differential Input Impedance	80	–	120	Ω

Figure 25: Input Differential Hysteresis



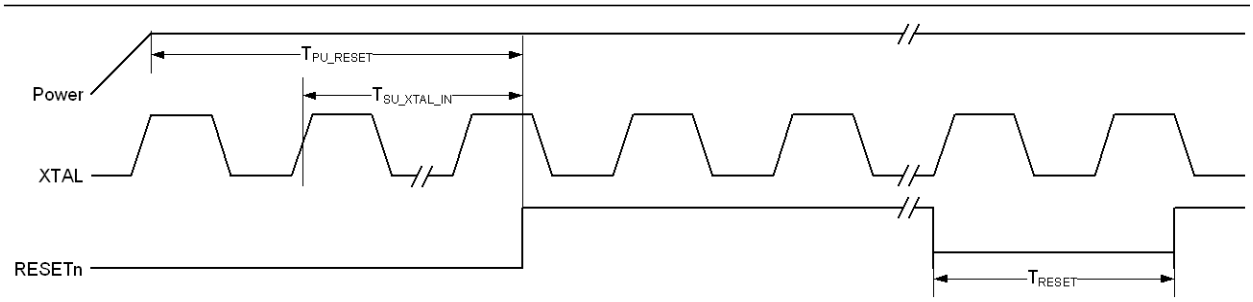
5.6 AC Electrical Specifications

5.6.1 Reset Timing

Table 277: Reset Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
T_{PU_RESET}	Valid Power to RESETn De-asserted	4	–	–	ms
$T_{SU\_XTAL\_IN}$	Number of Valid XTAL_IN Cycles Prior to RESETn De-asserted	10	–	–	clocks
T_{RESET}	Minimum Reset Pulse Width during Normal Operation	4	–	–	ms
T_{RESET_MDIO}	Minimum Wait Time from RESET De-assertion to First MDIO Access	1	–	–	ms

Figure 26: Reset Timing



5.6.2 Power Sequencing for Internal Regulator Options

Table 278: Supply Ramp Sequencing for LDO

Symbol	Parameter	Min	Typ	Max	Unit
$T_{RISE\ (max)}$	The 3.3V supply REG_IN ramp time (T_{RISE}) should be no more than 15 ms.	–	–	15	ms

Figure 27: Dual LDO Startup Timing

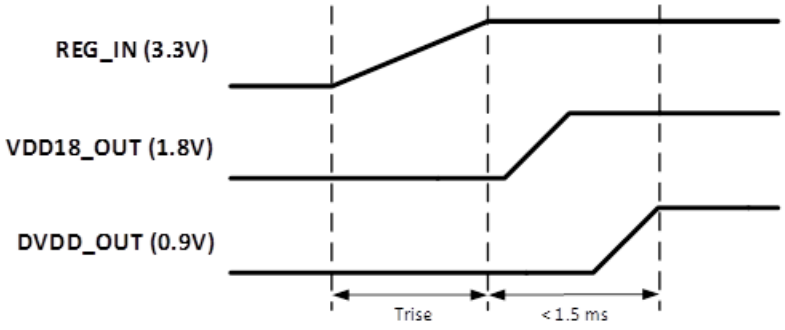
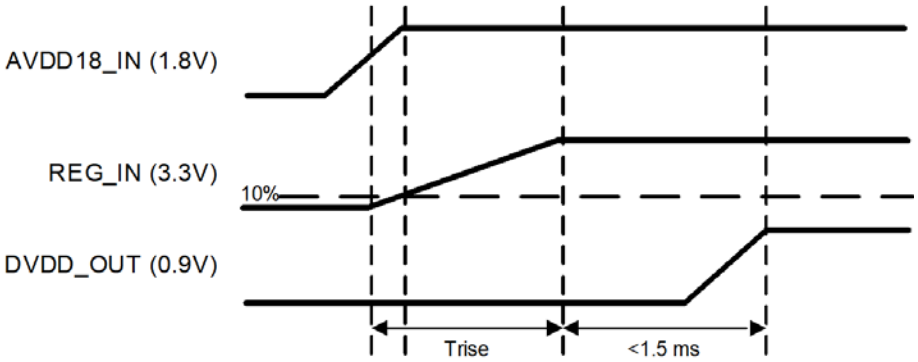


Figure 28: Single LDO Startup Timing (DVDD by LDO from AVDD18_IN)



Note

The 1.8V must ramp up to stable before 3.3V. The 3.3V should ramp no more than 10% until 1.8V is up and stable.

5.6.3 XTAL_IN/XTAL_OUT Timing

Table 279: 25 MHz Oscillator Requirements
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_T	Target Frequency	–	–	25.0	–	MHz
	Frequency Tolerance	–	-100	–	+100	ppm
$T_{P\_XTAL\_IN}$	XTAL_IN Period	–	–	40	–	ns
$V_{SWING\_XTAL\_IN}$	XTAL_IN Swing	See the *Oscillator Shifting Application Note* (MV-S301630-00).	0.8	–	1.8	Vpp
$T_{H\_XTAL\_IN}$	XTAL_IN High Time	–	13	20	27	ns
$T_{L\_XTAL\_IN}$	XTAL_IN Low Time	–	13	20	27	ns
$T_{R\_XTAL\_IN}$	XTAL_IN Rise Time	10 to 90%	–	3.0	–	ns
$T_{F\_XTAL\_IN}$	XTAL_IN Fall Time	10 to 90%	–	3.0	–	ns
$T_{J\_XTAL\_IN}$	XTAL_IN Total Jitter[1]	12 kHz to 20 MHz	–	–	1.0 (SGMII)	ps RMS
					4.0 (RGMII)	
$C_{J\_XTAL\_OUT}$	Capacitor value from XTAL_OUT to ground	Ceramic	–	0.1	–	µF

1. PLL-generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.

Figure 29: XTAL_IN/XTAL_OUT Timing

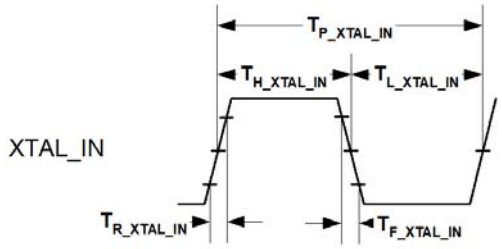


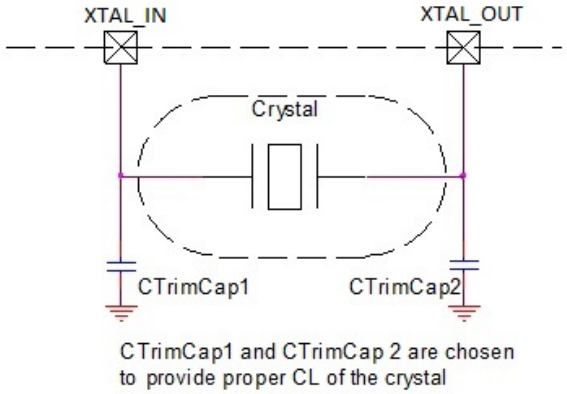
Table 280: 25 MHz Crystal Requirements[1]

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_T	Target Frequency	–	–	25.0	–	MHz
	Frequency Tolerance	–	-100	–	100	ppm
C_L	Load Capacitance	User Specified	–	6	12	pF
C_S	Shunt Capacitance	–	–	–	CL/6	pF
RL or ESR	Equivalent Series Resistance	–	–	100	150	Ω
D_L	Drive Level	–	100	–	–	μW

1. See *How to Use Crystals as Clock Sources Application Note* (MV-S300626-00) for details.

Figure 30: Crystal Reference Schematic

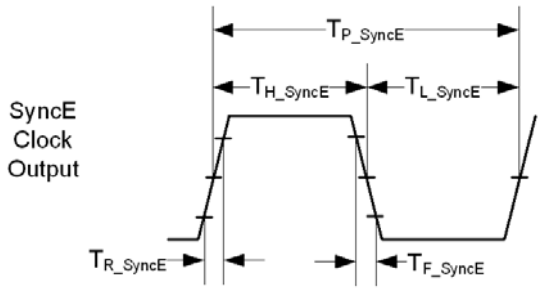


5.6.4 SyncE Recovered Clock Output Timing

Table 281: SyncE Recovered Clock Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_SyncE}	Period	125 MHz	–	8.0002	–	ns
T_{H_SyncE}	High Time	125 MHz	–	3.0833	–	ns
T_{L_SyncE}	Low Time	125 MHz	–	3.6349	–	ns
T_{R_SyncE}	Rise Time	125 MHz	–	0.472	–	ns
T_{F_SyncE}	Fall Time	125 MHz	–	0.445	–	ns
T	Duty Cycle	125 MHz	48.7	49	49.3	%

Figure 31: SyncE Clock Output Timing



5.7 MAC Interface Timing

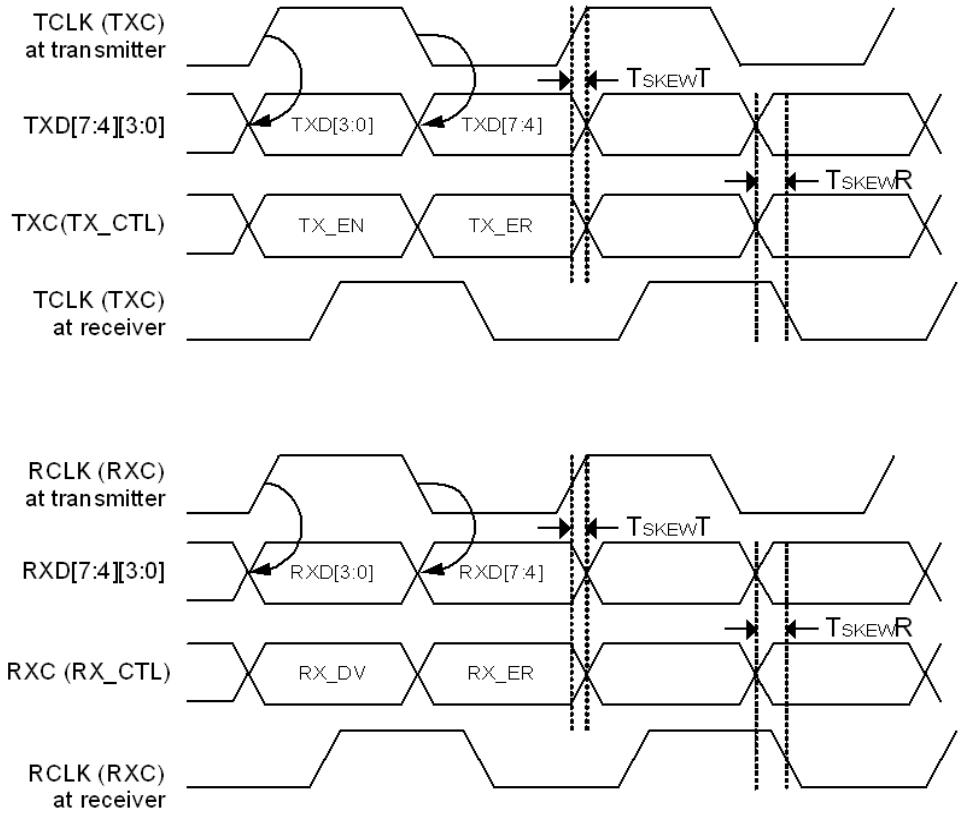
5.7.1 RGMII AC Characteristics

Table 282: RGMII AC Characteristics

(This table is copied from the RGMII Specification. See the four timing modes discussed in Section 5.7.2, RGMII Delay Timing for Different RGMII Modes, on page 207).

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to Clock Output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data to Clock Input Skew (at Receiver)	1.0	–	2.8	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH100}$	High Time for 1000BASE-T	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20 to 80%)	–	–	0.75	ns

Figure 32: RGMII Multiplexing and Timing



This figure is copied from the RGMII Specification. See the four timing modes discussed in Section 5.7.2, RGMII Delay Timing for Different RGMII Modes, on page 207.

5.7.2 RGMII Delay Timing for Different RGMII Modes

5.7.2.1 PHY Input — TCLK Delay

Table 283: PHY Input — TCLK No Delay when Register 31.8001.15 = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{setup}	Setup Time	Register 31.8001.15 = 0	1.0	–	–	ns
T_{hold}	Hold Time		0.8	–	–	ns

Figure 33: TCLK No Delay Timing — Register 31.8001.15 = 0

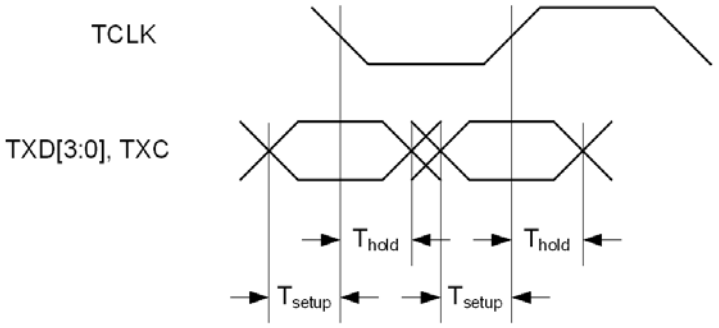
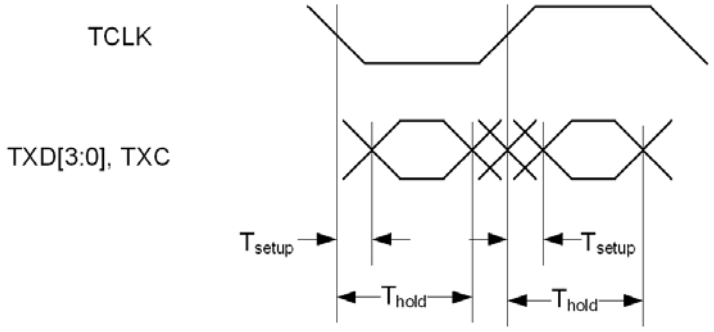


Table 284: PHY Input — TCLK Delay when Register 31.8001.15 = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{setup}	Setup Time	Register 31.8001.15 = 1 (add delay)	-0.9	–	–	ns
T_{hold}	Hold Time		2.7	–	–	ns

Figure 34: TCLK Delay Timing — Register 31.8001.15 = 1



5.7.2.2 PHY Output — RCLK Delay

Table 285: PHY Output — RCLK No Delay when Register 31.8001.14 = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{skew}	Skew Time	Register 31.8001.14 = 0	- 0.5	–	0.5	ns

Figure 35: RGMII RCLK No Delay Timing — Register 31.8001.14 = 0

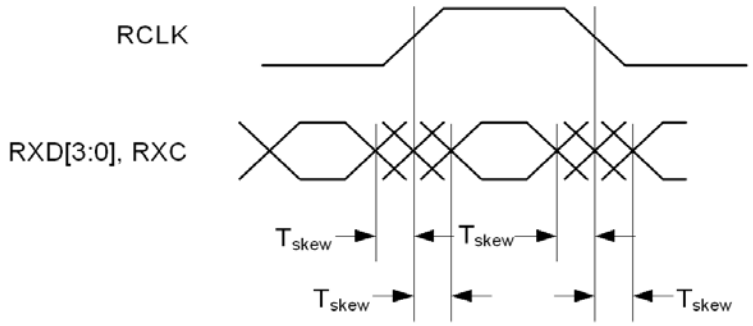
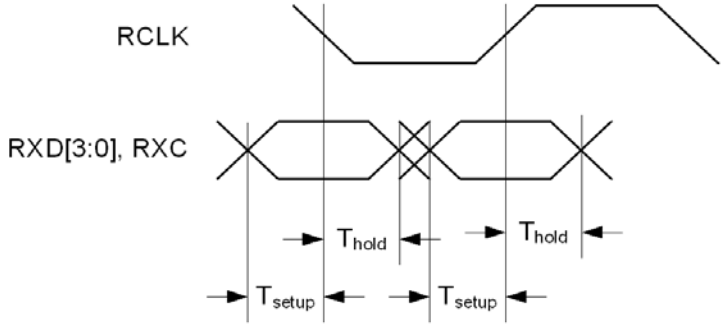


Table 286: PHY Output — RCLK Delay when Register 31.8001.14 = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{setup}	Setup Time	Register 31.8001.14 = 1 (add delay)	1.2	–	–	ns
T_{hold}	Hold Time		1.2	–	–	ns

Figure 36: RGMII RCLK Delay Timing — Register 31.8001.14 = 1



5.7.3 SGMII Interface Timing

Table 287: SGMII Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{FALL}	V_{OD} Fall Time (20 to 80%)	100	–	200	ps
T_{RISE}	V_{OD} Rise Time (20 to 80%)	100	–	200	ps
T_{SKEW1}[1]	Skew between Two Members of a Differential Pair	–	–	20	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14 × rms Random)	–	127	–	ps

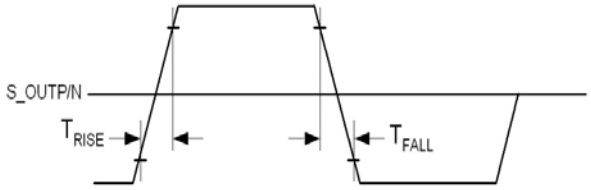
1. Skew measured at 50% of the transition.

5.7.4 SGMII Input AC Characteristics

Table 288: SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14 × rms Random)	–	–	599	ps

Figure 37: Serial Interface Rise and Fall Time



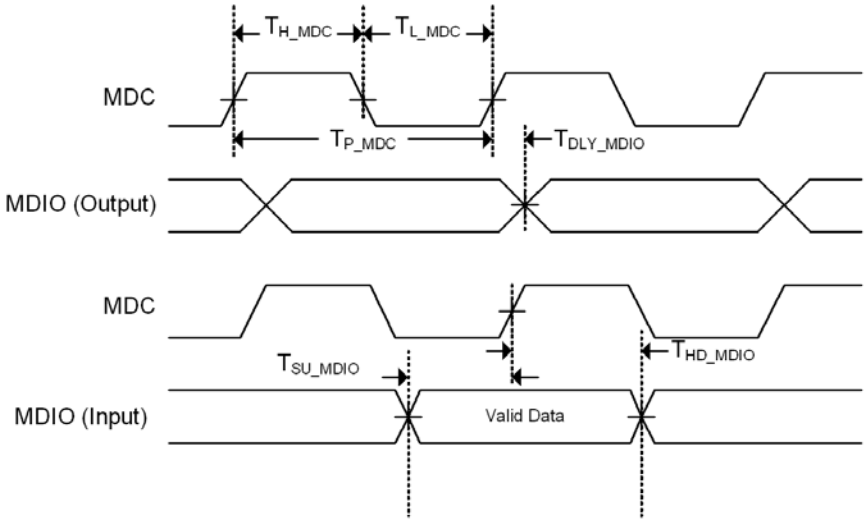
5.8 MDC/MDIO Timing

Table 289: MDC/MDIO Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time	0	–	20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time	10	–	–	ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time	10	–	–	ns
T_{P_MDC}	MDC Period	80	–	–	ns[1]

1. Maximum frequency = 12.5 MHz.

Figure 38: MDC/MDIO Timing



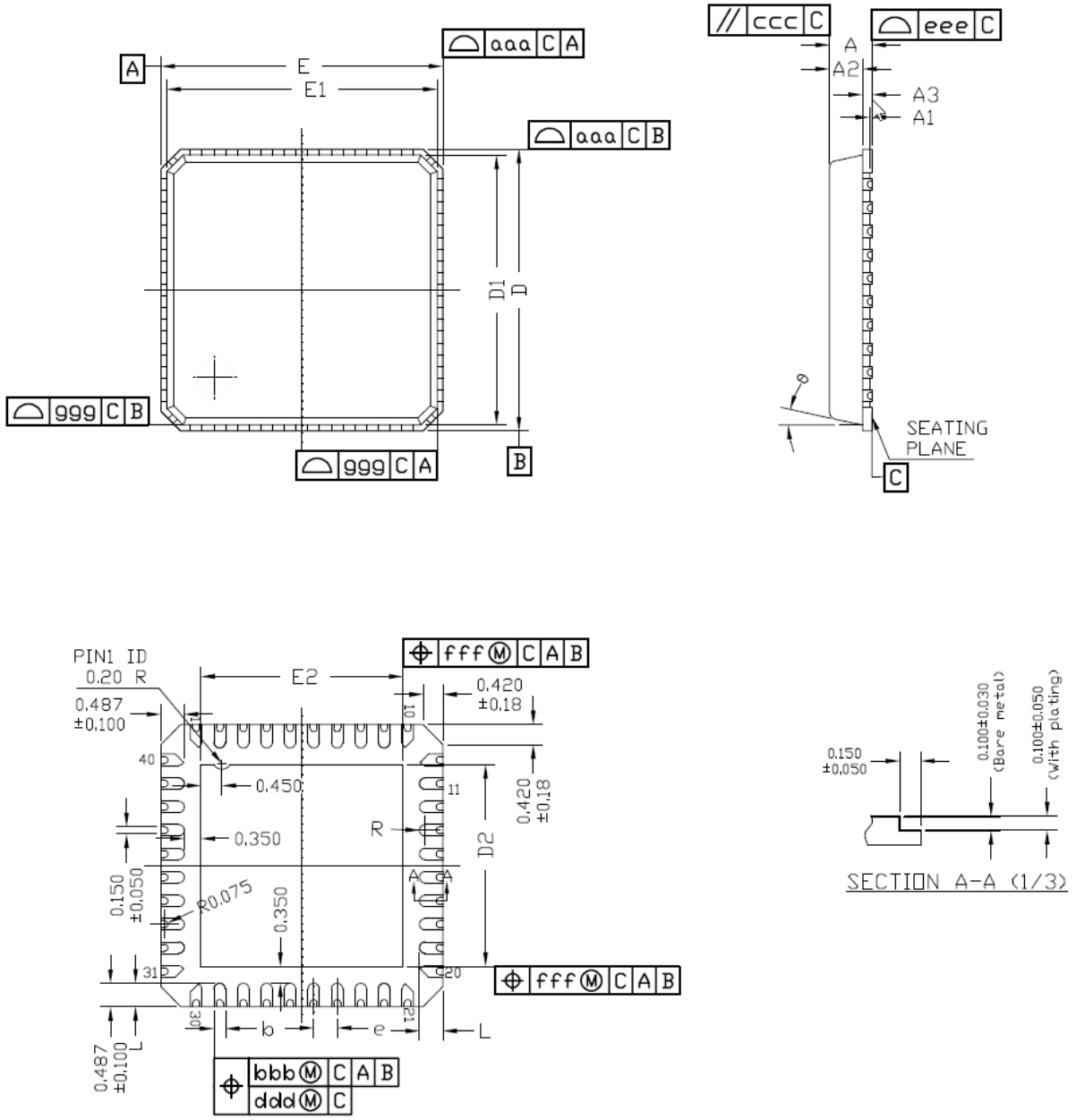
5.9 IEEE Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by a number. For an exact description of the templates and the test conditions, refer to the IEEE specifications.

6 Package Mechanical Dimensions

6.1 40-pin QFN Package

Figure 39: 88Q2110 40-pin QFN Package Mechanical Drawing



6.2 40-pin QFN (6 mm x 6 mm) Package Information

Table 290: 40-pin QFN (6 mm x 6 mm) Package Information

Symbol	Parameter	Min	Typ	Max	Unit
$P_{PRESSURE}$	Maximum pressure on the 40-pin QFN (6 mm x 6 mm) package	–	–	20	N
$T_{STORAGE}$[1]	Storage temperature	-55	–	+125[2]	°C

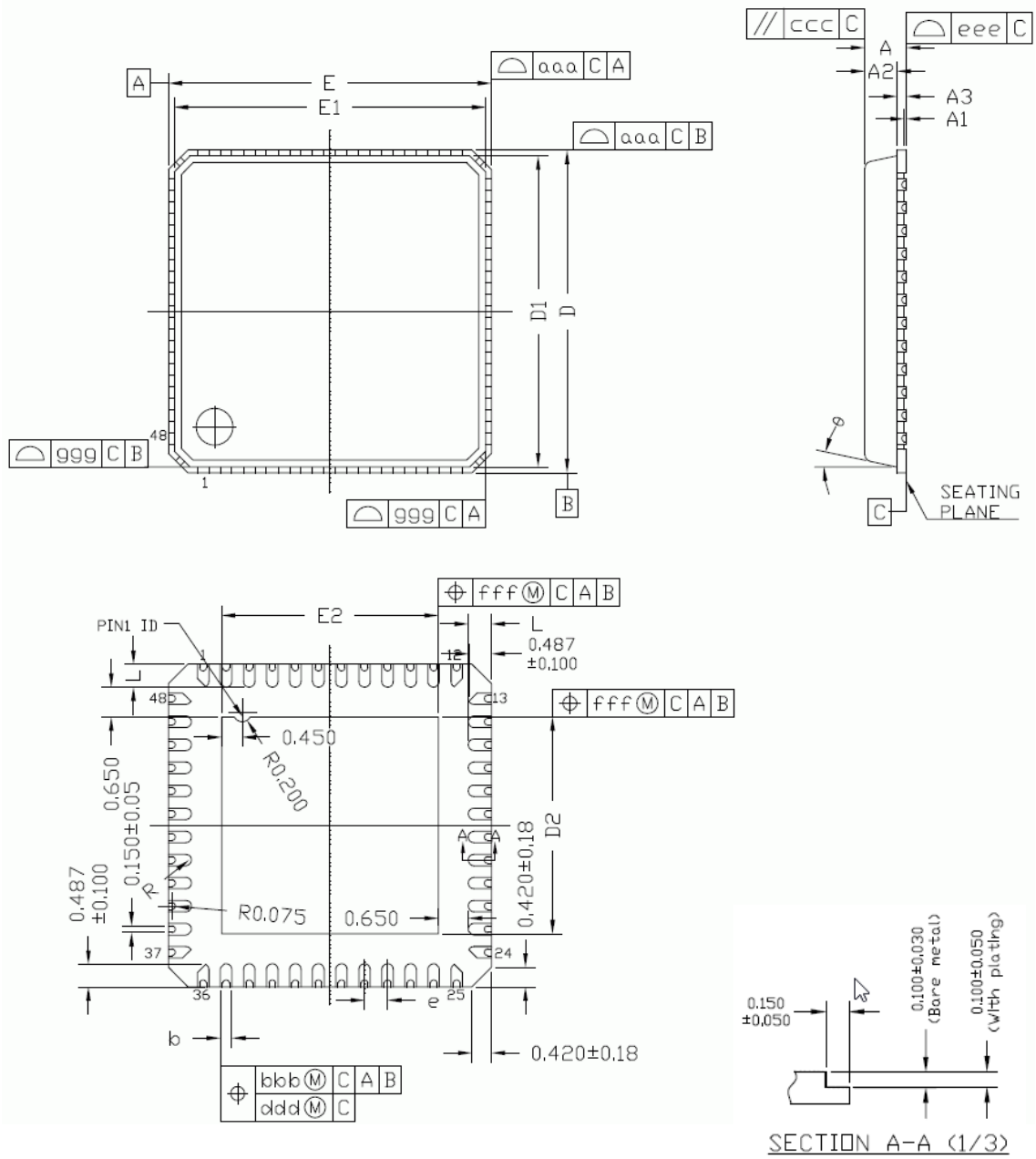
1. The conditions for storing unpowered and unmounted devices are as follows:
   - Packed inside a vacuum-sealed moisture barrier bag with desiccant and humidity indicator card (HIC)
   - Stored at <40°C and <90% relative humidity (RH)
2. 125°C is only used as bake temperature for not more than 24 hours. Long-term storage (for example, weeks or longer) should be kept at 85°C or lower.

Table 291: 88Q2110 40-pin QFN Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.800	0.850	0.900
A1	0.000	0.20	0.050
A2	0.600	0.650	0.700
A3		0.203 REF.	
b	0.180	0.250	0.300
D		6 BSC	
D1		5.750 BSC	
D2	4.200	4.300	4.400
E		6 BSC	
E1		5.750 BSC	
E2	4.200	4.300	4.400
L	0.400	0.500	0.600
e		0.500 BSC	
Θ	0°	--	14°
R	0.090	--	--
Tolerances of Form and Position			
aaa		0.150	
bbb		0.100	
ccc		0.100	
ddd		0.050	
eee		0.080	
fff		0.100	
ggg		0.200	

6.3 48-pin QFN Package

Figure 40: 88Q2112 48-pin QFN Package Mechanical Drawing



6.4 48-pin QFN (7 mm x 7 mm) Package Information

Table 292: 48-pin QFN (7 mm x 7 mm) Package Information

Symbol	Parameter	Min	Typ	Max	Unit
$P_{PRESSURE}$	Maximum pressure on the 48-pin QFN (7 mm x 7 mm) package	–	–	20	N
$T_{STORAGE}$[1]	Storage temperature	-55	–	+125[2]	°C

1. The conditions for storing unpowered and unmounted devices are as follows:
   - Packed inside a vacuum-sealed moisture barrier bag with desiccant and humidity indicator card (HIC)
   - Stored at <40°C and <90% relative humidity (RH)
2. 125°C is only used as bake temperature for not more than 24 hours. Long-term storage (for example, weeks or longer) should be kept at 85°C or lower.

Table 293: 88Q2112 48-Pin QFN Package Dimensions

Symbol	Dimensions in mm		
	Min	Nom	Max
A	0.800	0.850	0.900
A1	0.000	0.20	0.050
A2	0.600	0.650	0.700
A3		0.203 REF.	
b	0.180	0.250	0.300
D		7 BSC	
D1		6.750 BSC	
D2	4.600	4.700	4.800
E		7 BSC	
E1		6.750 BSC	
E2	4.600	4.700	4.800
L	0.400	0.500	0.600
e		0.500 BSC	
Θ	0°	--	14°
R	0.090	--	--
Tolerances of Form and Position			
aaa		0.150	
bbb		0.100	
ccc		0.100	
ddd		0.050	
eee		0.080	
fff		0.100	
ggg		0.200	

7 Part Order Numbering/Package Marking

7.1 Part Order Numbering

Figure 41 shows the ordering part numbering scheme for the device. Refer to the relevant release notes on the Marvell extranet for the latest revision and complete part ordering information.

Figure 41: Sample Part Number

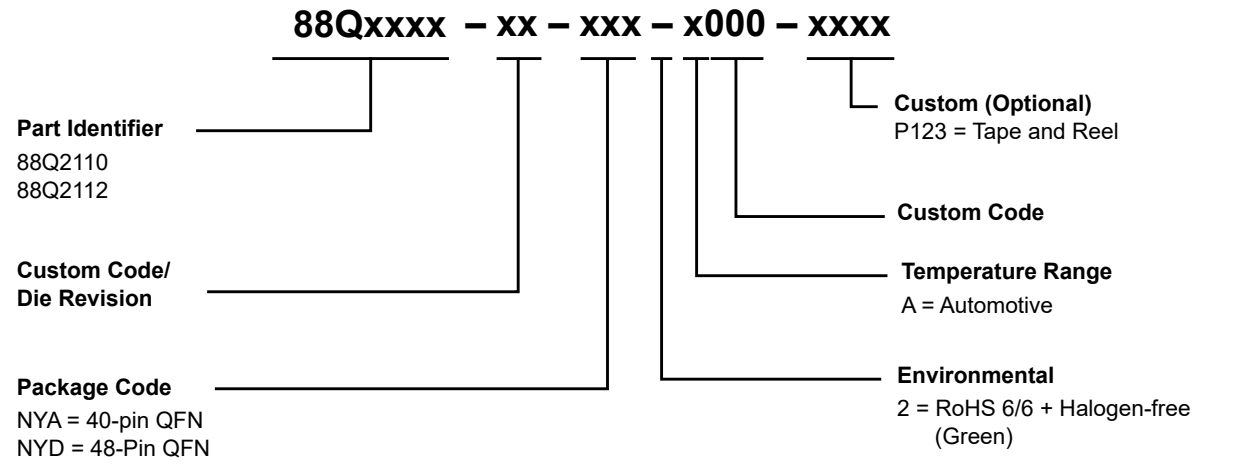


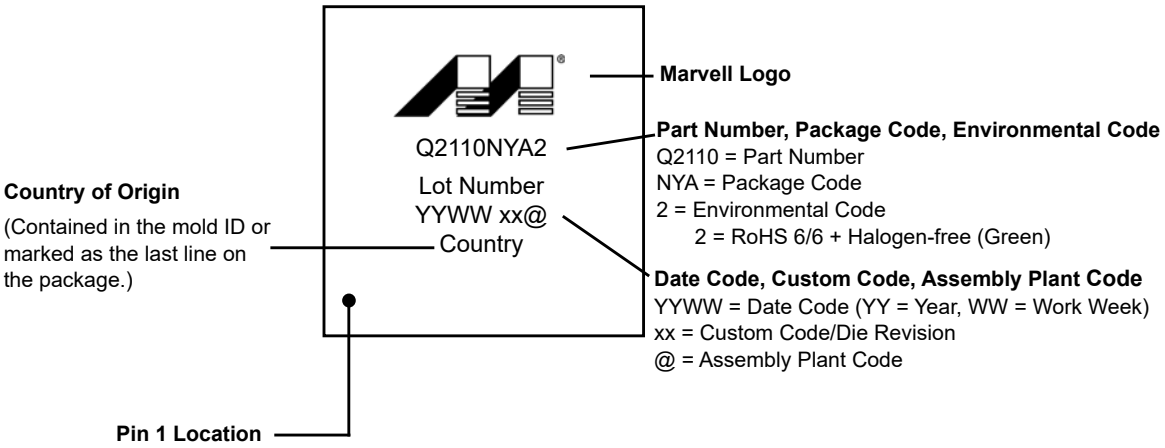
Table 294: 88Q2110/88Q2112 Part Order Options

Package Type	Features	Part Order Number
40-pin QFN	–	88Q2110-XX-NYA2A000 (Automotive, RoHS 6/6 + Halogen-free compliant package) 100/1000BASE-T1 Single Pair Ethernet PHY for Automotive with RGMII
40-pin QFN	–	88Q2110-XX-NYA2A000-P123 (Automotive, RoHS 6/6 + Halogen-free compliant package) 100/1000BASE-T1 Single Pair Ethernet PHY for Automotive with RGMII
48-pin QFN	–	88Q2112-XX-NYD2A000 (Automotive, RoHS 6/6 + Halogen-free compliant package) 100/1000BASE-T1 Single Pair Ethernet PHY for Automotive with RGMII/SGMII
48-pin QFN	–	88Q2112-XX-NYD2A000-P123 (Automotive, RoHS 6/6 + Halogen-free compliant package) 100/1000BASE-T1 Single Pair Ethernet PHY for Automotive with RGMII/SGMII

7.2 Package Marking

Figure 42 shows a sample package marking and pin 1 location for the 88Q2110 40-pin QFN package (Automotive, Green).

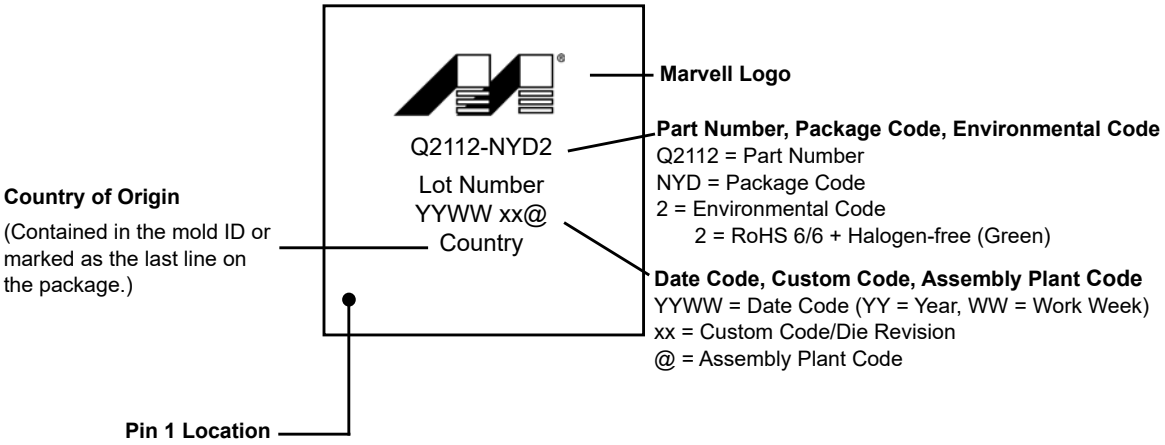
Figure 42: 88Q2110 40-pin QFN Sample Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. The location of the markings is approximate.

Figure 43 shows a sample package marking and pin 1 location for the 88Q2112 48-pin QFN package (Automotive, Green).

Figure 43: 88Q2112 48-pin QFN Sample Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. The location of the markings is approximate.

A Revision History

Table 295: Revision History (Sheet 1 of 15)

Revision	Description	Date
Rev. G	• ***Datasheet release.***	June 19, 2019
Rev. G v7.00	***Section 5, Electrical Specifications*** • Table 268, Current Consumption VDDO updated. ***Section 6, Package Mechanical Dimensions*** • Figure 39, 88Q2110 40-pin QFN Package Mechanical Drawing, on page 212 updated. • Table 291, 88Q2110 40-pin QFN Package Dimensions, on page 213 updated. • Figure 40, 88Q2112 48-pin QFN Package Mechanical Drawing, on page 214 updated. • Table 293, 88Q2112 48-Pin QFN Package Dimensions, on page 215 updated.	June 19, 2019
Rev. F	• ***Datasheet release.***	April 16, 2019
Rev. F v6.05	***Section 5, Electrical Specifications*** • Section 5.7.2.1, PHY Input — TCLK Delay, on page 207 updated. • Table 284, PHY Input — TCLK Delay when Register 31.8001.15 = 1 updated. • Figure 34, TCLK Delay Timing — Register 31.8001.15 = 1, on page 207 updated. • Section 5.7.2.2, PHY Output — RCLK Delay, on page 208 updated. • Table 285, PHY Output — RCLK No Delay when Register 31.8001.14 = 0 updated. • Figure 35, RGMII RCLK No Delay Timing — Register 31.8001.14 = 0, on page 208 updated. • Table 286, PHY Output — RCLK Delay when Register 31.8001.14 = 1 updated. ***Section 7, Part Order Numbering/Package Marking*** • Table 294, 88Q2110/88Q2112 Part Order Options, on page 216 updated.	April 16, 2019

Table 295: Revision History (Sheet 2 of 15)

Revision	Description	Date
Rev. F v6.04	***Product Overview*** • Features updated. ***Section 1, Signal Description*** • Table 6, Clock/Configuration/Reset/I/O updated. ***Section 3, Registers*** • Table 174, Tx FIFO Control Register updated. ***Section 5, Electrical Specifications*** • Table 269, Current Consumption Dual LDO REG_IN (AVDD18 and DVDD by LDO) updated. • Table 270, Current Consumption Single LDO REG_IN (AVDD18 by LDO) updated. • Table 271, Current Consumption Single AVDD18_IN (DVDD by LDO) updated. • Section 5.10 Latency removed. This section will be included in release notes. ***Section 7, Part Order Numbering/Package Marking*** • Figure 41, Sample Part Number, on page 216 updated.	April 15, 2019

Table 295: Revision History (Sheet 3 of 15)

Revision	Description	Date
Rev. F v6.03	***Product Overview*** • Features updated. • Figure 1, MAC Interface to Copper Device Application updated. ***Section 2, PHY Functional Specifications*** • Section 2.2, Copper Media Interface, on page 31 updated. • Section 2.2.4.1, 100/1000BASE-T1, on page 33 updated. • Section 2.3.2.1, 1.25 GHz SERDES Interface, on page 35 updated. • Section 2.9, Advanced Virtual Cable Tester, on page 44 updated. • Section 2.11, Automatic Polarity Detection and Correction, on page 48 updated. • Section 2.12, DME Pages Exchange Complete with No Link, on page 48 updated. • Figure 24, Multiple Devices Across Multiple Line Cards Connected by an EventReq Input Signal, on page 81 updated. ***Section 3, Registers*** • Table 52, PMA/PMD Extended Ability Register removed. • Table 85, PCS Devices In Package Register 1 updated. • Table 86, PCS Devices In Package Register 2 updated. • Table 166, Function Control Register updated. • Table 174, Tx FIFO Control Register updated. • Table 178, Auto-Negotiation Status Register 2 updated. • Table 183, SGMII Control Register updated. • Table 184, SGMII Status Register updated. • Table 187, SGMII Auto-Negotiation Advertisement updated. • Table 188, SGMII Link Partner Ability/SGMII updated. • Table 189, SGMII Auto-Negotiation Expansion Register updated. • Table 190, SGMII SERDES Specific Control 1 Register updated. • Table 191, SGMII Specific Status Register updated. • Table 192, SGMII Interrupt Enable Register updated. • Table 193, SGMII Interrupt Status Register updated. • Table 194, SGMII Receive Error Counter Register updated. • Table 195, PRBS Control Register updated. • Table 196, PRBS Error Counter LSB Register updated. • Table 197, PRBS Error Counter MSB Register updated. • Table 198, SGMII Specific Control Register 2 updated. ***Section 4, PTP Registers*** • Section 4, PTP Registers, on page 151 updated.	April 14, 2019

Table 295: Revision History (Sheet 4 of 15)

Revision	Description	Date
Rev. F v6.02	***Product Overview*** updated. ***Section 1, Signal Description*** • Section 1.2.9, Low Power Signal Detect (LPSD), on page 27 updated. • Table 10, Low Power Signal Detect updated. ***Section 2, PHY Functional Specifications*** • Section 2.1, System Interfaces, on page 31 updated. • Section 2.2.3.1, Analog-to-Digital Converter, on page 32 updated. • Section 2.2.3.2, Analog Active Hybrid, on page 32 updated. • Section 2.2.3.3, Digital Echo Canceller, on page 32 updated. • Section 2.2.3.5, Digital Phase-Locked Loop, on page 33 updated. • Section 2.2.4.1, 100/1000BASE-T1, on page 33 updated. • Section 2.7.1.2, Low Power Signal Detect Mode, on page 41 updated. • Section 2.9.1, VCT Configuration, on page 44 updated. • Table 23, Interrupt Enable Bits updated. • Section 2.20.5, REG_IN, on page 62 updated. ***Section 3, Registers*** • Table 59, 1000BASE-T1 Training Register updated. • Table 60, 1000BASE-T1 Link Partner Training Register updated. • Table 79, SQI Register added. • Table 178: Auto-Negotiation RCV RXCODE Register 1 removed. • Table 179: Auto-Negotiation RCV RXCODE Register 2 removed. • Table 180: Auto-Negotiation RCV RXCODE Register 3 removed. • Table 178, Auto-Negotiation Status Register 2 updated. • Table 180, RGMII Output Impedance Control Register updated. ***Section 5, Electrical Specifications*** • Section 5.10, Latency Timing, on page 214 updated.	April 11, 2019

Table 295: Revision History (Sheet 5 of 15)

Revision	Description	Date
Rev. F v6.01	***Product Overview*** updated. ***Section 2, PHY Functional Specifications*** • Figure 24, Multiple Devices Across Multiple Line Cards Connected by an EventReq Input Signal, on page 81 updated. ***Section 3, Registers*** • Table 46, PMA/PMD Control Register 1 updated. • Table 59, 1000BASE-T1 Training Register updated. • Table 77, LPSD Register 1 updated. • Table 78, LPSD Register 2 updated. • Table 94, OAM Register 0 updated. • Table 95, OAM Register 1 updated. • Table 96, OAM Register 2 updated. • Table 97, OAM Register 3 updated. • Table 98, OAM Register 4 updated. • Table 99, OAM Register 5 updated. • Table 100, OAM Register 6 updated. • Table 101, OAM Register 7 updated. • Table 102, OAM Register 8 updated. • Table 103, OAM Register 9 updated. ***Section 5, Electrical Specifications*** • Table 262, Recommended Operating Conditions updated. • Table 272, Digital Pins updated. • Section 5.7.2.1, PHY Input — TCLK Delay, on page 207 updated. • Table 283, PHY Input — TCLK No Delay when Register 31.8001.15 = 0 updated. • Table 284, PHY Input — TCLK Delay when Register 31.8001.15 = 1 updated. • Figure 33, TCLK No Delay Timing — Register 31.8001.15 = 0, on page 207 updated. • Figure 34, TCLK Delay Timing — Register 31.8001.15 = 1, on page 207 updated. • Section 5.7.2.2, PHY Output — RCLK Delay, on page 208 updated. • Table 285, PHY Output — RCLK No Delay when Register 31.8001.14 = 0 updated. • Table 286, PHY Output — RCLK Delay when Register 31.8001.14 = 1 updated. • Figure 35, RGMII RCLK No Delay Timing — Register 31.8001.14 = 0, on page 208 updated. • Figure 36, RGMII RCLK Delay Timing — Register 31.8001.14 = 1, on page 208 updated.	April 10, 2019

Table 295: Revision History (Sheet 6 of 15)

Revision	Description	Date
Rev. F v6.00	***Section 3, Registers*** • Table 58, 1000BASE-T1 PMA Status Register updated. • Table 59, 1000BASE-T1 Training Register updated. • Table 60, 1000BASE-T1 Link Partner Training Register updated. • Table 90, EEE Capability Register, page 102 removed. • Table 92, PCS 1000BASE-T1 Status Register 1 updated. • Table 112, Auto-Negotiation Resolved EEE Status Register removed. • Table 176, Auto-Negotiation Status Register updated. • Table 187, SGMII Auto-Negotiation Advertisement updated. • Table 190, SGMII SERDES Specific Control 1 Register updated. ***Section 7, Part Order Numbering/Package Marking*** • Figure 43, 88Q2112 48-pin QFN Sample Package Marking and Pin 1 Location updated.	March 15, 2019
Rev. E	• ***Datasheet release.***	September 25, 2018
Rev. E v5.12	***Section 7, Part Order Numbering/Package Marking*** • Table 290, 40-pin QFN (6 mm x 6 mm) Package Information updated. • Table 292, 48-pin QFN (7 mm x 7 mm) Package Information updated.	September 25, 2018
Rev. E v5.11	***Section 3, Registers*** • Table 163, GPIO Function and Interrupt Tri-state Control Register updated. • Table 166, Function Control Register updated • Table 167, LED [1:0] Polarity Control Register updated. • Table 187, SGMII Auto-Negotiation Advertisement updated. • Table 189, SGMII Auto-Negotiation Expansion Register updated. • Table 190, SGMII SERDES Specific Control 1 Register updated. • Table 193, SGMII Interrupt Status Register updated. • Table 196, PRBS Error Counter LSB Register updated. • Table 197, PRBS Error Counter MSB Register updated. ***Section 5, Electrical Specifications*** • Table 270, Current Consumption Single LDO REG_IN (AVDD18 by LDO) updated. • Table 271, Current Consumption Single AVDD18_IN (DVDD by LDO) updated.	September 18, 2018
Rev. E v5.10	**Section 5, Electrical Specifications** • Table 279, 25 MHz Oscillator Requirements updated.	September 12, 2018
Rev. E v5.09	***Section 2, PHY Functional Specifications*** • Section 2.3.2.4, False SERDES Link Up Prevention removed.	September 10, 2018

Table 295: Revision History (Sheet 7 of 15)

Revision	Description	Date
Rev. E v5.08	***Section 3, Registers*** • Table 163, GPIO Function and Interrupt Tri-state Control Register and Table 166, Function Control Register updated. • Section 3.9, SGMII Registers, on page 141 updated. • Table 183, SGMII Control Register and Table 184, SGMII Status Register updated. • Table 187, SGMII Auto-Negotiation Advertisement updated. • Table 194, “Fiber Auto-Negotiation Advertisement/SGMII (Media Mode) Register (Register 16_1.1:0 = 11)” and Table 195, “Fiber Link Partner Ability/1000BASE-X Mode Register (Register 16_1.1:0 = 01)” removed. • Table 188, SGMII Link Partner Ability/SGMII updated. • Table 197, “Fiber Link Partner Ability/SGMII (Media Mode) Register (Register 16_1.1:0 = 11)” removed. • Table 199, “Fiber Next Page Transmit Register”, Table 200, “Fiber Next Page Transmit Register”, and Table 201, “Extended Status Register” removed. • Table 190, SGMII SERDES Specific Control 1 Register and Table 191, SGMII Specific Status Register updated. • Table 198, SGMII Specific Control Register 2 updated. • Table 211, “Packet Generation Register 1”, Table 212, “CRC Counters Register”, Table 213, “Checker Control Register”, and Table 214, “Packet Generation Register 2” removed. ***Section 5, Electrical Specifications*** • Table 261, Absolute Maximum Ratings updated. ***Section 6, Package Mechanical Dimensions*** • Section 6.2, 40-pin QFN (6 mm x 6 mm) Package Information, on page 213 and Section 6.4, 48-pin QFN (7 mm x 7 mm) Package Information, on page 215 added.	September 6, 2018
Rev. E v5.07	***Section 1, Signal Description*** • Table 9, Power, Ground, and Internal Regulators, on page 25 updated the Note following the table. ***Section 2, PHY Functional Specifications*** • Figure 10, LPSD Block Diagram updated. • Section 2.14, LED updated. • Section 2.18.1, Hardware Configuration updated. • Section 2.20.9, Power Supply Sequencing updated. • Table 33, Power Supply Options — External 0.9V, Integrated Regulator (REG_IN) Supplies Only 1.8V updated. • Table 34, Power Supply Options — External 1.8V to AVDD18 and AVDD18_IN, Integrated Regulator (AVDD18_IN) Supplies DVDD Only updated. ***Section 5, Electrical Specifications*** • Table 279, 25 MHz Oscillator Requirements updated. • Table 280, 25 MHz Crystal Requirements updated. • Section 5.6.2, Power Sequencing for Internal Regulator Options added.	August 31, 2018

Table 295: Revision History (Sheet 8 of 15)

Revision	Description	Date
Rev. E v5.06	***Section 2, PHY Functional Specifications*** • Section 2.20.9, Power Supply Sequencing updated. ***Section 5, Electrical Specifications*** • Table 277, Reset Timing updated. • Table 278, Supply Ramp Sequencing for LDO updated.	August 31, 2018
Rev. E v5.05	***Section 5, Electrical Specifications*** • Table 278, Supply Ramp Sequencing for LDO updated. • Table 289, MDC/MDIO Timing updated.	August 29, 2018
Rev. E v5.04	***Section 2, PHY Functional Specifications*** • Figure 20, Supply and Regulator Connection Options updated. ***Section 5, Electrical Specifications*** • Figure 28, Single LDO Startup Timing (DVDD by LDO from AVDD18_IN) updated. • Table 290: IEEE Transceiver Parameters removed.	August 27, 2018
Rev. E v5.03	***Section 5, Electrical Specifications*** • Table 271, Current Consumption Single AVDD18_IN (DVDD by LDO) updated. • Table 277, Reset Timing updated. • Table 278, Supply Ramp Sequencing for LDO added. • Figure 28, Single LDO Startup Timing (DVDD by LDO from AVDD18_IN) updated.	August 10, 2018
Rev. E v5.02	***Section 2, PHY Functional Specifications*** • Table 24, Control Bit Interrupts updated. • Table 33, Power Supply Options — External 0.9V, Integrated Regulator (REG_IN) Supplies Only 1.8V updated. • Table 34, Power Supply Options — External 1.8V to AVDD18 and AVDD18_IN, Integrated Regulator (AVDD18_IN) Supplies DVDD Only updated. • Figure 20, Supply and Regulator Connection Options added. ***Section 5, Electrical Specifications*** • Section 5.4.2.1, Current Consumption REG_IN (AVDD18_IN and DVDD by LDO) updated. • Section 5.4.2.2, Current Consumption AVDD18_IN (DVDD by LDO) added. • Figure 27, Dual LDO Startup Timing added. • Figure 28, Single LDO Startup Timing (DVDD by LDO from AVDD18_IN) added.	August 3, 2018

Table 295: Revision History (Sheet 9 of 15)

Revision	Description	Date
Rev. E v5.01	***Section 5, Electrical Specifications*** • Table 285, Current Consumption Single LDO REG_IN (AVDD18 by LDO), Table 286 Current Consumption AVDD18_IN (DVDD by LDO), Section 5.4.2.2, Current Consumption AVDD18_IN (DVDD by LDO), Table 289 IEEE Transceiver Parameters, and Table 304, IEEE Transceiver Parameters removed. • Table 274, PMA Electrical Specifications (IEEE Std 802bp-2016) added.	July 31, 2018
Rev. E v5.00	***Section 3, Registers*** • Table 32, Power Supply Options — External 0.9V, Integrated Regulator (REG_IN) Supplies Only 1.8V and Table 34, AVDD18_IN, Integrated Regulator (AVDD18_IN) Supplies DVDD Only removed.	June 29, 2018
Rev. D	• ***Datasheet release.***	June 15, 2018
Rev. D v4.02	***Product Overview*** • UTP support added. ***Section 3, Registers*** • Table 111, BASE-T1 Auto-Negotiation Control Register updated.	June 15, 2018
Rev. D v4.01	***Section 3, Registers*** • Table 33, Power Supply Options — External 1.8V to AVDD18 and Table 34, AVDD18_IN, Integrated Regulator (AVDD18_IN) Supplies DVDD Only added. • Table 46, PMA/PMD Control Register 1, Table 47, PMA/PMD Device Identifier Register 1, Table 48, PMA/PMD Device Identifier Register 2, Table 53, PMA/PMD Package Identifier Register 2, Table 57, BASE-T1 Control Register, Table 59, 1000BASE-T1 Training Register, and Table 60, 1000BASE-T1 Link Partner Training Register updated. • Table 51, 10G PMA/PMD Status Register 2, Table 52, 10G PMA Transmit Disable Register, and Table 53, 10G PMA/PMD Signal Detect Register removed. • Table 69, Temperature Sensor Register 3 updated. ***Section 5, Electrical Specifications*** • Section 5.4.1.1, Current Consumption AVDD18 updated. • Section 5.4.1.2, Current Consumption AVDD33 updated. • Section 5.4.1.3, Current Consumption DVDD updated. • Section 5.4.1.4, Current Consumption VDDO updated. • Section 5.4.2.1, Current Consumption REG_IN (AVDD18_IN and DVDD by LDO) updated. • Section 5.4.2.2, Current Consumption AVDD18_IN (DVDD by LDO) added.	May 17, 2018
Rev. D v4.00	***Section 3, Registers*** • Table 69, Temperature Sensor Register 3 updated.	April 11, 2018

Table 295: Revision History (Sheet 10 of 15)

Revision	Description	Date
Rev. C v3.00	***Datasheet release.***	March 19, 2018
Rev. C v3.00	***Section 3, Registers*** • Table 166, Function Control Register updated. ***Section 7, Part Order Numbering/Package Marking*** • Figure 42, 88Q2110 40-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated.	March 19, 2018
Rev. B v2.04	***Product Overview*** updated ***Section 2, PHY Functional Specifications*** • Table 18, Typical MDC/MDIO Read Operation updated. ***Section 3, General Registers*** • Table 69, Temperature Sensor Register 3 updated.	January 5, 2018
Rev. B v2.03	***Section 3, Registers*** • Table 11, 88Q2110 40-pin QFN Pin Assignment List — Alphabetical by Signal Name, Table 12, 88Q2112 48-pin QFN pin Assignment List — Alphabetical by Signal Name, Table 129, 100BASE-T1 Specific Interrupt Enable Register, Table 130, Copper Interrupt Status Register, Table 133, MAC Specific Control Register, and Table 147, GPIO/TX_ENABLE Control Register updated. • Table 148, GPIO/LED Control Register added.	December 20, 2017
Rev. B v2.02	***Section 2, PHY Functional Specifications*** • Table 10, LPSD Block Diagram updated. ***Section 3, General Registers*** • Table 126, 100BASE-T1 Copper Control Register, Table 129, 100BASE-T1 Specific Interrupt Enable Register, Table 130, Copper Interrupt Status Register, Table 133, MAC Specific Control Register, Table 134, MAC Specific Interrupt Enable Register, Table 137, Counter Control Register, Table 138, Bad Link Counter Register, Table 139, Bad SSD Counter Register, Table 141, Rx Error Counter Register, Table 142, Receiver Status Register, Table 147, GPIO/TX_ENABLE Control Register, Table 150, LED Polarity Control Register, Table 152, Copper Port Packet Generation Register, Table 160, BIST Counters Register, Table 183, SGMII Control Register, Table 190, SGMII SERDES Specific Control 1 Register, Table 202, PTP Control Register 1, and Table 203, PTP Control Register 2 updated.	December 7, 2017

Table 295: Revision History (Sheet 11 of 15)

Revision	Description	Date
Rev. B v2.01	***Section 1, Signal Description*** • Figure 2, 88Q2110 Device 40-pin RGMII Package (Top View), on page 19, Figure 3, 88Q2112 Device 48-pin RGMII/SGMII Package (Top View), on page 20 • Section 1.2.4, TX_ENABLE/GPIO/Interrupt Interface, Table 5, TX_ENABLE/GPIO/Interrupt Interface, on page 23, Table 6, Clock/Configuration/Reset/I/O, on page 23, Table 9, Power, Ground, and Internal Regulators, on page 25, Table 11, 88Q2110 40-pin QFN Pin Assignment List — Alphabetical by Signal Name, on page 28, Table 12, 88Q2112 48-pin QFN pin Assignment List — Alphabetical by Signal Name, on page 29, and Figure 4, Device Functional Block Diagram, on page 30 updated LED reference to TX-ENABLE. • Section 2.3.3, Tx Disable Feature added. • Section 2.11, Automatic Polarity Detection and Correction, Section 2.13, GPIO, Section 2.14, LED, Section 2.14.3, Bi-Color LED Mixing, Section 2.14.4, Modes of Operation, and Section 2.14.4.2, Speed Blink updated LED reference to TX-ENABLE. • Table 21, MODE 3 Behavior and Table 22, MODE 4 Behavior updated. • Section 2.16, Interrupt, Section 2.17, Automatic and Manual Impedance Calibration, Section 2.18, Configuring the 88Q2110/88Q2112, Table 25, Sampled Values, and Section 2.19, Temperature Sensor Section 2.21.1, PTP Control, Section 2.21.1.1, PTP Event Request, and Section 2.21.1.2, PTP Trigger Generate updated LED reference to TX-ENABLE. ***Section 3, Registers*** • Table 63, Reset and Control Register, Table 64, Tx Disable Status Register, Table 66, Interrupt Enable Register, Table 67, GPIO Interrupt Status Register, Table 68, Temperature Sensor Register 2, Table 69, Temperature Sensor Register 3, Table 70, Temperature Sensor Register 4, Table 76, I/O Voltage Control Register, Table 77, LPSD Register 1, Table 78, LPSD Register 2, Table 126, 100BASE-T1 Copper Control Register, Table 127, 100BASE-T1 Status Register, Table 128, 100BASE-T1 Status Register, Table 142, Receiver Status Register, Table 143, Interrupt Enable Register, Table 144, Interrupt Status Register, Table 145, GPIO/TX_ENABLE Control Register, Table 146, GPIO/TX_ENABLE Control Register, Table 147, GPIO/TX_ENABLE Control Register, Table 149, LED Function Control Register, Table 150, LED Polarity Control Register, Table 151, LED Timer/INTn Control Register, Table 152, Copper Port Packet Generation Register, Table 162, GPIO Data Register, Table 165, Open Drain Control Register, Table 202, PTP Control Register 1, and Table 203, PTP Control Register 2 updated. • Table 153, GPIO/TX_ENABLE Control Register removed.	November 28, 2017

Table 295: Revision History (Sheet 12 of 15)

Revision	Description	Date
Rev. B v2.01 (continued)	***Section 5, Electrical Specifications*** • Table 272, Digital Pins added LED reference to TX-ENABLE. • Section 5.5.2, TX_ENABLE Pin updated.	November 28, 2017
Rev. A v2.00	***Datasheet release.***	October 20, 2017
Rev. A v1.24	***Section 1, Signal Description*** • Table 9, Power, Ground, and Internal Regulators, on page 25 - updated Note following the table. ***Section 2, PHY Functional Specifications*** • Section 2.5, Synchronizing FIFO jumbo frame size updated. ***Section 3, Registers*** • Table 133, MAC Specific Control Register updated. • Table 173, Packet Checker Count Register updated. • Table 191, SGMII Specific Status Register updated. ***Section 5, Electrical Specifications*** • Section 5.1, Absolute Maximum Ratings updated V_{DD} from 1.1V to 1.0V. • Section 5.2, Recommended Operating Conditions TA added Grade “2”. • Section 5.3, Internal Regulator Specifications removed. • Section 5.8, MDC/MDIO Timing added MDC Period Min value. • Section 5.10.1, Transmit Latency Timing - Figure 37, Transmit Latency Timing updated. • Section 5.10.2, Receive Latency Timing - Figure 38, Receive Latency Timing updated.	October 20, 2017
Rev. A v1.23	***Section 1, Signal Description*** • Table 6, Clock/Configuration/Reset/I/O, on page 23 updated. • Section 1.3, Pin Assignment List — Alphabetical by Signal Name corrected order. ***Section 2, PHY Functional Specifications*** • Figure 4, Device Functional Block Diagram updated. • Section 2.1, System Interfaces updated. • Section 2.3, MAC Interfaces updated. • Section 2.4, Loopback updated. • Section 2.5, Synchronizing FIFO updated. • Section 2.9, Advanced Virtual Cable Tester updated. • Section 2.16, Interrupt updated. • Section 2.17, Automatic and Manual Impedance Calibration updated. • Section 2.18, Configuring the 88Q2110/88Q2112 updated. • Section 2.18.2, Software Configuration — Management Interface updated. • Section 2.19, Temperature Sensor updated. ***Section 5, Electrical Specifications*** • Section 5.6.4, SyncE Recovered Clock Output Timing updated.	October 17, 2017

Table 295: Revision History (Sheet 13 of 15)

Revision	Description	Date
Rev. A v1.22	***Product Overview*** updated. ***Section 1, Signal Description*** • Table 3, Host Interfaces, on page 22 updated. • Table 10, Low Power Signal Detect, on page 27 updated. ***Section 2, PHY Functional Specifications*** • Section 2.2.3.2, Analog Active Hybrid updated. • Table 17, LPSD Electrical Characteristics updated.	October 9, 2017
Rev. A v1.21	***Product Overview*** • Changed integrated switching voltage regulator to linear regulator. ***Section 2, PHY Functional Specifications*** • Section 2.5, Synchronizing FIFO updated. • Section 2.6, Resets updated. • Section 2.8, Auto-Negotiation updated. • Section 2.9, Advanced Virtual Cable Tester updated. • Section 2.10.1, CRC Error Counter and Frame Counter updated. • Section 2.11, Automatic Polarity Detection and Correction updated. • Section 2.16, Interrupt updated. • Section 2.18.2.1, Clause 45 Register Access heading added. • Section 2.18.2.2, Clause 22 MDIO Register Access Method added. • Section 2.19, Temperature Sensor updated. • Table 32, Power Supply Options — External 0.9V, Integrated Regulator (REG_IN) Supplies Only 1.8V 1.0V to 0.9V. ***Section 5, Electrical Specifications*** • Section 5.4.1, Current Consumption when Using External Regulators updated NOTE. • Section 5.4.2.1, Current Consumption REG_IN (AVDD18_IN and DVDD by LDO) added text. • Section 5.6.4, SyncE Recovered Clock Output Timing added section. ***Section 7, Part Order Numbering/Package Marking*** • Figure 42, 88Q2110 40-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated. • Figure 43, 88Q2112 48-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated.	August 30, 2017
Rev. A v1.20	***Section 2, PHY Functional Specifications*** • Section 2.9, Advanced Virtual Cable Tester, on page 44 updated.	August 11, 2017

Table 295: Revision History (Sheet 14 of 15)

Revision	Description	Date
Rev. A v1.19	***Section 2, PHY Functional Specifications*** • Section 2.7.1.2, Low Power Signal Detect Mode, on page 41 updated. • Section 2.11, Automatic Polarity Detection and Correction, on page 48 updated. • Section 2.13, GPIO, on page 48 updated. • Section 2.14, LED, on page 49 updated. • Section 2.16, Interrupt, on page 53 updated. • Section 2.20.5, REG_IN, on page 62 updated 1.0V to 0.9V. • Section 2.20.7, DVDD_OUT, on page 62 updated 1.0V to 0.9V. • Section 2.20.8, VDDO, on page 62 Register identified for 2.5V operation. ***Section 5, Electrical Specifications*** • Table 263, Thermal Conditions for 88Q2110 40-pin QFN Package, on page 191 updated. • Table 264, Thermal Conditions for 88Q2112 48-pin QFN Package, on page 192 updated. • Section 5.4.1.1, Current Consumption AVDD18, on page 193 updated. • Section 5.4.1.2, Current Consumption AVDD33, on page 193 updated. • Section 5.4.1.4, Current Consumption VDDO, on page 194 updated. • Section 5.4.2.1, Current Consumption REG_IN (AVDD18_IN and DVDD by LDO), on page 195 updated.	July 14, 2017
Rev. A v1.18	Pre-release draft version. ***Product Overview*** • LPSD added. ***Section 1, Signal Description*** • Table 10, Low Power Signal Detect, on page 27 updated. ***Section 2, PHY Functional Specifications*** • Table 4, Device Functional Block Diagram, on page 30 updated. • Section 2.7.1.2, Low Power Signal Detect Mode, on page 41 updated. • Table 32, Power Supply Options — External Supplies, on page 59 updated. ***Section 3, Registers*** • Editorial changes ***Section 5, Electrical Specifications*** • Table 279, 25 MHz Oscillator Requirements, on page 203 updated.	March 23, 2017

Table 295: Revision History (Sheet 15 of 15)

Revision	Description	Date
Rev. A v1.17	Pre-release draft version. ***Product Overview*** updated. ***Section 1, Signal Description*** • Table 3, Host Interfaces, on page 22 updated. • Table 4, Management Interface, on page 23 updated. ***Section 2, PHY Functional Specifications*** • Table 13, Modes, on page 31 updated. • Section 2.2, Copper Media Interface: 1000BASE-T1 replaced by 100/1000BASE-T1. • Table 14, RGMII Signal Mapping, on page 34 updated. • Section 2.4.2, Line Loopback updated. • Section 2.5, Synchronizing FIFO updated. • Section 2.15, Synchronous Ethernet (SyncE) Clock added. • Section 2.21, Precision Time Protocol (PTP) Timestamping Support added. ***Section 3, Registers*** • All register subsections updated. • Section 3.2, Common Control Registers, on page 91 added. • Section 3.5, 100BASE-T1 Copper Unit Advance PCS Registers, on page 115 added. ***Section 4, PTP Registers*** added. ***Section 5, Electrical Specifications*** • Section 5.3, Package Thermal Information, on page 191 updated. ***Section 7, Part Order Numbering/Package Marking*** • Table 42, 88Q2110 40-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated. • Table 43, 88Q2112 48-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated. ***Appendix A, Revision History*** added.	February 8, 2017

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