Miniature Bias-Tee Networks Integrated in Micro-coaxial Lines

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***Abstract*— This paper presents miniature broadband bias tee networks designed in a micro-coaxial environment. The process for fabricating the air-filled coaxial lines by wafer-scale sequential metal deposition, referred to as PolyStrata^{TM}, enables hybrid assembly of surface-mount components such as inductors and capacitors, enabling DC blocks and RF chokes. The microcoaxial lines can be designed with a wide variety of characteristic impedances fabricated in the same process, allowing for easier matching to active devices such as power amplifiers, which typically have low input and output impedances. In this paper, bias tee networks in both 12 Ω and 50 Ω environments are demonstrated with 0402 capacitors and 0402 inductors, as well as with monolithically integrated coil inductors. The measured performance shows 14 dB insertion loss from 4 to 16 GHz with a better than 0.75 dB return loss and up to 5 A power handling in a circuit with a 8.3 mm^2 footprint.**

I. Introduction

Bias networks are a necessary part of every active microwave circuit. These three port devices are generally characterized in terms of input and output RF match, isolation between RF and DC ports, insertion loss, bandwidth, DC current handling, RF power handling, and size. For example, commercially available connectorized bias tees cover the range from a few hundred MHz to 50 GHz [1]. Broadband bias tees typically are limited to 500 mA current handling and 2 W RF power, while narrowband (e.g. .8-1 GHz) components handle up to 5 A of DC current [2]. Surface mount bias tees, which have a footprint of about 32 by 28 mm^2, are also available [3] and handle about 0.5 A and operate up to 4.2 GHz.

The goal of this work is to demonstrate miniature bias tees with high DC current and RF power handling capabilities, which are compatible with a micro-coaxial, wafer-scale environment fabricated in a process referred to as PolyStrata^{TM}.

Micro-fabricated air-filled rectangular coaxial lines have been demonstrated over the past few years at microwave and millimeter-wave frequencies in several technologies [4] [5] [6] [7] [8]. The lines implemented in the PolyStrata^{TM} copper process exhibit a very low loss of < 0.1 dB/wavelength at Ka-band [9] and high isolation of 55 dB between two lines that share a common ground wall [10]. A variety of passive components also have been demonstrated in this technology, e.g.: resonators at 44 and 60 GHz [7], 26 GHz [11], V-band filters (f=57.5 GHz) [6], Ka-band filters (f = 9.1 and 29.75 GHz) [12], Ka-band and V-band couplers, e.g. [9] and [13].

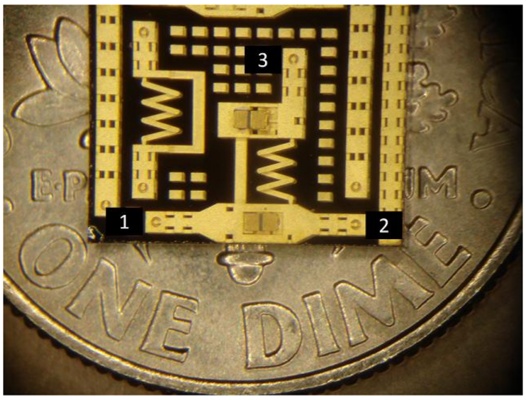

Fig. 1. A gold-plated bias tee fabricated in the PolyStrata^{TM} copper process on an optically flat substrate. The RF ports are labeled 1 and 2, while 3 is the DC port. All ports are compatible with standard 150um and 250um pitch CPW probes for testing. This bias tee includes two 0402 capacitors which are hybridly assembled into the microcoaxial environment while the inductor is fabricated monolithically in the PolyStrata^{TM} process. The size of the bias tee is around 8 mm^2.

More recently, distributed micro-coaxial components covering the range from 2-20 GHz have been demonstrated [14]. This paper presents broadband microcoaxial bias tees with a footprint around 8mm^2 as shown in Figure 1 where surface mount capacitors are assembled into the micro-coaxial environment. One of the advantages of wafer-scale fabricated coaxial lines is the availability of a wide range of characteristic impedances (140 Ω to 6 Ω, a factor of 23 [15]), which give the possibility of better matching to active devices with typically low impedances. Although small, these 3D components can handle tens of watts of microwave power up to 18 GHz [16] making them a good environment for active integration. In this paper, various components required for the bias tee are described, followed by results of several bias tee designs for 4-16 GHz operation.

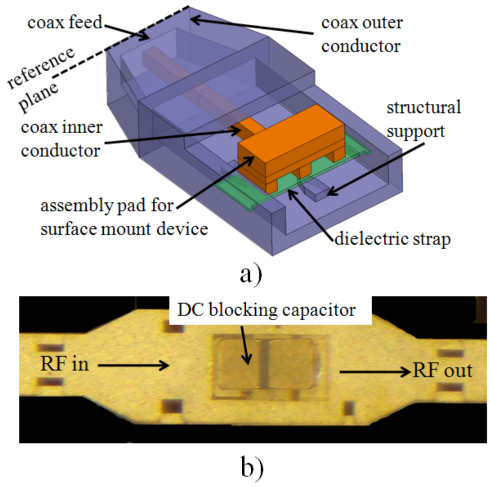

Fig. 2. (a) 3-D geometry of one-half of a surface mount component assembly structure (socket) in the copper-based microcoaxial environment referred to as Polystrata^{TM}. (b) Photograph of a 0402 packaged blocking capacitor mounted in a series socket between two microcoaxial lines.

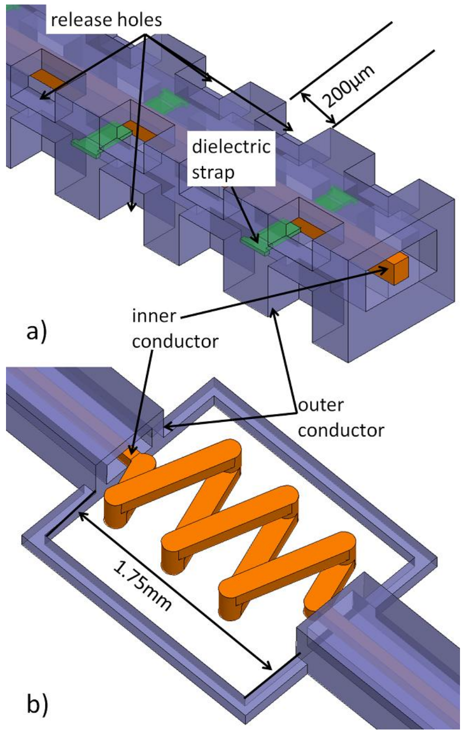

Fig. 3. (a) Sketch of a 50-Ω microcoaxial line with all relevant dimensions. The holes in the outer conductor are used to release the photoresist needed during fabrication. (b) A 3-turn solenoid inductor in the Polystrata^{TM} process, connected in series with the coaxial line. The inner conductor which the inductor is made of is 100 μm by 100 μm in cross-section.

II. Process and Components

The PolyStrata^{TM} process consists of at least five sequentially deposited horizontal copper layers (for a single rectacoax line) on an optically substrate. One of the limitations of the low-temperature PolyStrata^{TM} process thus far has been the inability to monolithically integrate resistors and capacitors. However, the microcoaxial line environment lends itself naturally to hybrid integration, since both center and outer conductors can be designed to accommodate series and/or shunt surface mount devices (SMDs) as shown in Figure 2(a). These assembly structures, referred to as "sockets" are a result of careful electromagnetic design under fabrication constraints. The sockets can be designed to accommodate most standard surface mount packaged devices in series or in shunt, and the following specific components have been assembled and tested as a part of the design procedure:

- series 50 Ω 0303 resistor (US Microwaves thin film);
- shunt 50 Ω 0402 resistor (Yageo thick film);
- series and shunt 0402 package 3 pF and 82 pF capacitor (Dielectric Labs);
- shunt 75 Ω 0402 resistor(Yageo thick film); and
- series 2.2 nH inductor (Coilcraft).

The components are mounted using silver epoxy (Epoxy Technology H20E). The inductors can also be implemented monolithically as copper coils in the PolyStrata^{TM} process. A 50-Ω coaxial line geometry and a series-connected monolithic inductor are shown in Figure 3. Inductors with 1 to 7 turns have been implemented, with high resonant frequencies, relatively high quality factors (Q$\sim$20) and very high current handling capability ($>$ 5 A). In comparison, the highest current handling of the Coilcraft inductors is 2.3 A (a 1.0 nH, 0402 inductor). For bias-tee applications, high resonant frequency, high inductance value and high current handling capability are desirable, while the Q factor is not critical. Thus either monolithic or surface mount inductors can be integrated into the microcoaxial bias tee.

III. Bias Tee Design and Characterization

Bias tees are commonly designed for 50-Ω input and output impedances at the RF ports, which is convenient for all active devices pre-matched to 50-Ω. MMICs usually have integrated biasing networks which take up a significant portion of the expensive real-estate [17], and in addition require off-chip capacitors for stability. The bias tees presented in this work are designed for MMICs which do not use valuable semiconductor area on passive bias elements, and which can also be designed with lower impedance input and output ports. Thus, it would be useful to have bias tee circuit designs for various characteristic impedances. For example, a 12-Ω bias tee is designed on both sides of a socket which houses a low impedance 4-16 GHz power amplifier MMIC with no on-chip bias networks. The 12-Ω ports are then matched to 50 Ω RF input/output through a ultra-broadband microcoaxial impedance matching network. This 4:1 impedance transformer has a 11:1 bandwidth (2-22 GHz) with a small and flat group delay, and is described in [16].

This paper discusses both 12 and 50 Ω bias tee networks. To characterize the assembled surface mount devices in the sockets, as well as the bias tees, PolyStrata^{TM}-based TRL calibrations standards were designed to cover 2-7 GHz and 7-

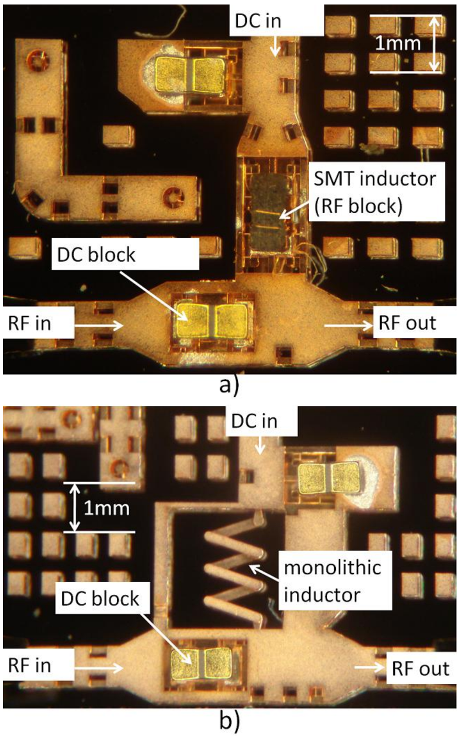

Fig. 4. (a) Photograph of a bias tee implemented in microcoaxial 12-Ω impedance lines with a surface-mount blocking capacitor and RF shorting capacitor, and surface-mount Coilcraft choke. (b) Photograph of bias tee with monolithically integrated PolyStrata 3-turn solenoid choke.

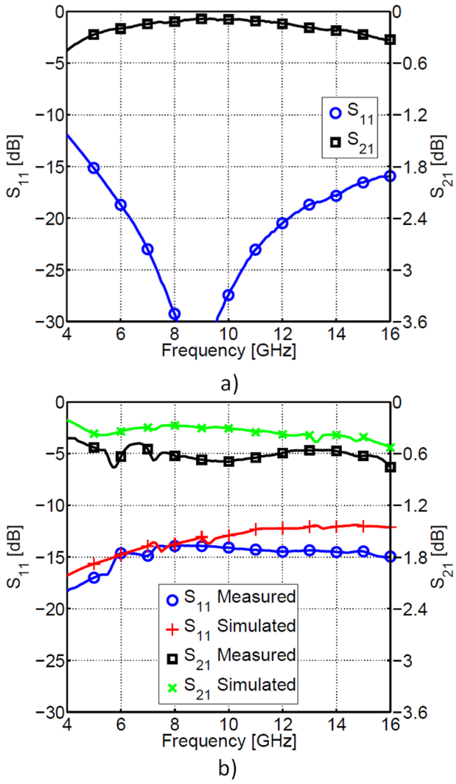

Fig. 5. Measured insertion loss and match for (a) the bias tee from Figure 4 (a) which uses a surface-mount choke and (b) measured and simulated loss and match for the bias tee with a monolithically integrated inductor from Fig. 4 (b).

22 GHz. The calibration standards included transitions from CPW probes to the microcoax, referred to as launches, described in detail in [18]. The reference plane was defined at the edge of the socket in Figure 2(a). Measurements of non-50-Ω impedance devices are de-embedded from 50-Ω calibrated measurements.

A. Bias Tees in a 12 Ω Environment

Photographs of two 12-Ω bias tees are shown in Figure 4: one with a surface mount commercially-available 2.2 nH inductor with a resonant frequency of 15 GHz, and the other with a monolithically integrated 3-turn inductor with simulated inductance of 3.1 nH and a resonant frequency around 12 GHz. Each bias Tee has 0402 3-pF series blocking capacitors and 3-pF shunt capacitors at the DC ports.

The bias tee circuits can also be tuned for specific parameters, such as offsetting parasitic inductance that occurs when wire bonding to a chip. Such tuning can be done with the addition of a shorted stub (Fig. 4(b)) or introducing other parasitics by altering the geometry of the transmission line. Figure 5 shows measured and simulated performance for the two bias tees. The simulations were performed with Ansoft's HFSS finite element code and include all details of the geometry. The surface mount components are modeled as impedance sheets with appropriate value of surface reactance, and with dimensions given by the package. The insertion loss and match for a bias tee with a surface mount inductor are shown in Figure 5(a), and the performance for a bias tee with a PolyStrata^{TM} monolithic 3-turn solenoid choke is shown in Figure 5(b). Both designs show a better than 0.7 dB insertion loss from 4 to 16 GHz with a better than 12 dB match. The bias tees were used with no degradation in a 20-W power amplifier with over 2 A of DC current. All the 12 Ω measurements were de-embeded to 50 Ω to allow use of a 50 Ω, 2-port TRL calibration. As a 3-port TRL was not available, isolation measurements were not taken, though simulation shows that the DC line is isolated 20 dB or better for all impedances presented.

B. Bias Tees in a 50 Ω Environment

The 50 Ω bias-tees designs differ from the 12 Ω bias tees not only in the impedance of the RF transmission line geometry, but also the inductor. Since the DC line is now of the same impedance as the signal line, there is more loading of the RF path by the DC line, leading to reduced isolation. In order to attempt to increase the isolation, the monolithic inductor was made a larger value. When measured on a 2-port network analyzer with the isolated port open, a reflection now occurs around 7 GHz, as seen in Figure 6. In order to understand this resonance, measurements were performed with a power meter and source to monitor the reflection, isolation and transmission, and the results are shown in Figure 7. These

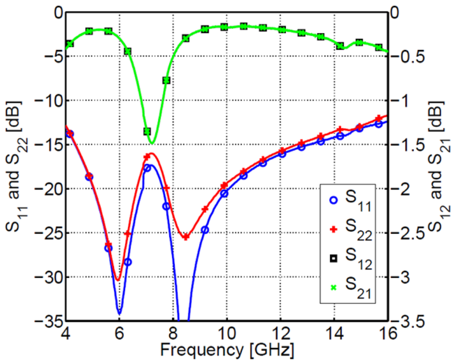

Fig. 6. Measured insertion loss and match for a 50 Ω bias tee.

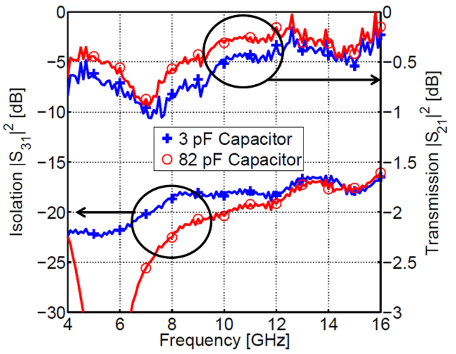

Fig. 7. Measured isolation and transmission for the same 50-Ω bias tee as Fig. 6. The top two curves correspond to the measured transmitted power, and the bottom two to the power measured in the isolated port, normalized to the incident power. Measurements are performed for two values of SMD capacitors.

measurements show that when the isolated port is terminated, the resonance does not exist.

IV. Conclusions

In conclusion, this paper demonstrates miniature high-current high-power bias-tee networks in both 12 and 50 Ω microcoaxial impedance environments. The component can be released from the native substrate and mounted on any hybrid circuit, as has been demonstrated with other components. In addition, the connections to CPW probes (launches) used in this work for measurements can be replaced by suitable transitions to a variety of media. Finally, a comparison with a commercial bias tee and a very compact bias tee using a micromachined inductor is shown in Table 1, indicating that the PolyStrata bias network is a good compromise between size, bandwidth, loss and power/current handling.

Acknowledgment

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TABLE I

Comparison of three bias tees in different technologies.

	Bias Tee Type		
	MEMS [19]	**Picosecond 5545 [1]**	**PolyStrata**
DC Current	50 mA	500 mA	> 5 A
RF Power	Not Available	2 W avg. max	20 W
Area	4 mm^2	645 mm^2	8.3 mm^2
BW (-3 dB)	20 GHz	20 GHz	18 GHz
Capacitance	8.2 pF	30 nF	3 pF
Inductance	18 nH	340 μH	1.2 nH
Insertion Loss	< 1.5 dB f < 24 GHz	< 1.5 dB f < 12 GHz	< 1.5 dB f < 18 GHz
Return Loss	> 10 dB f < 24 GHz	> 12 dB f < 14 GHz	> 10 dB f < 18 GHz

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