

Rtype

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```
addi St0, St0, 1
```

[illegible]

addi St1, St1, 7

operation: addi

PC: 00000000000000000000000000001000

Register File:

St0: 00000000000000000000000000000001

St1: 00000000000000000000000000000111

Ss0: 00000000000000000000000000000000

Ss1: 00000000000000000000000000000000

Instruction Memory:

Mem[0000000000000000000000000000100] = 00100001

Mem[0000000000000000000000000000101] = 00101001

Mem[0000000000000000000000000000110] = 00000000

Mem[0000000000000000000000000000111] = 00000111

Data Memory:

```
operation: add  
PC: 000000000000000000000000000000001100  
Register File:  
    St0: 000000000000000000000000000000000001  
    St1: 000000000000000000000000000000000111  
    Ss0: 0000000000000000000000000000000001000  
    Ss1: 0000000000000000000000000000000000000  
Instruction Memory:  
    Mem[000000000000000000000000000000001000] = 00000001  
    Mem[000000000000000000000000000000001001] = 00001001  
    Mem[000000000000000000000000000000001010] = 10000000  
    Mem[000000000000000000000000000000001011] = 00100000  
Data Memory:
```

[illegible]

[illegible]

Itype

addi St0, St0, 4

operation: addi

PC: 0000000000000000000000000000100

Register File:

St0: 0000000000000000000000000000100

St1: 0000000000000000000000000000000

Ss0: 0000000000000000000000000000000

Ss1: 0000000000000000000000000000000

Instruction Memory:

Mem[0000000000000000000000000000000] = 00100001

Mem[0000000000000000000000000000001] = 00001000

Mem[0000000000000000000000000000010] = 00000000

Mem[0000000000000000000000000000011] = 00000100

Data Memory:

addi St1, St1, 3

operation: addi

PC: 00000000000000000000000000001000

Register File:

St0: 0000000000000000000000000000100

St1: 000000000000000000000000000011

Ss0: 00000000000000000000000000000000

Ss1: 00000000000000000000000000000000

Instruction Memory:

Mem[0000000000000000000000000000100] = 00100001

Mem[0000000000000000000000000000101] = 00101001

Mem[0000000000000000000000000000110] = 00000000

Mem[0000000000000000000000000000111] = 00000011

Data Memory:

```
slti St1, St1, 5
```

operation: slti

PC: 00000000000000000000000000000000**1100**

Register File:

[illegible]

St1: 0000000000000000000000000000000001

[illegible]

Ss1: 0000000000000000000000000000000000

Instruction Memory:

Mem[000000000000000000000000000000001000] = 00101001

Mem[000000000000000000000000000000001001] = 00101001

```
Mem[000000000000000000000000000000001010] = 00000000
```

Mem[000000000000000000000000000000001011] = 00000101

Data Memory:


```
sw $t1, 4($t0)
```

operation: sw

PC: 0000000000000000000000000000000010000

Register File:

St0: 00000000000000000000000000000000**100**

[illegible]

Ss0: 00000000000000000000000000000000

Ss1: 000000000000000000000000000000000000

Instruction Memory:

[illegible]

Mem[000000000000000000000000000000001101] = 00001001

$$\text{Mem}[000000000000000000000000000000001110] = 00000000$$
[illegible]**Data Memory:**

Mem[00000000000000000000000000000000100] = 00000000

Mem[00000000000000000000000000000000101] = 00000000

Mem[00000000000000000000000000000000110] = 00000000

Mem[00000000000000000000000000000000111] = 00000001

```
operation: lw  
PC: 0000000000000000000000000000010100  
Register File:  
    St0: 000000000000000000000000000000000100  
    St1: 000000000000000000000000000000000001  
    Ss0: 000000000000000000000000000000000000  
    Ss1: 000000000000000000000000000000000001  
Instruction Memory:  
    Mem[0000000000000000000000000000010000] = 10001101  
    Mem[0000000000000000000000000000010001] = 00010001  
    Mem[0000000000000000000000000000010010] = 00000000  
    Mem[0000000000000000000000000000010011] = 00000100  
Data Memory:  
    Mem[00000000000000000000000000000100] = 00000000  
    Mem[00000000000000000000000000000101] = 00000000  
    Mem[00000000000000000000000000000110] = 00000000  
    Mem[00000000000000000000000000000111] = 00000001
```

Jtype

ient: beq St1, St0, Initiali

operation: beq

PC: 00000000000000000000000000000000**100**

Register File:

St0: 00000000000000000000000000000000

St1: 000000000000000000000000000000000000

Ss0: 00000000000000000000000000000000

\$s1: 00000000000000000000000000000000

Instruction Memory:

Mem[000000000000000000000000000000000000] = 00010001

[illegible]

```
Mem[0000000000000000000000000000000010] = 00000000
```

```
Mem[000000000000000000000000000000000011] = 00000001
```

Data Memory:

[illegible]

```
addi St1, St1, 3
```

operation: addi

PC: 0000000000000000000000000000**1100**

Register File:

St0: 00000000000000000000000000000000**100**

St1: 00000000000000000000000000000000**11**

```
Ss0: 00000000000000000000000000000000
```

Ss1: 000000000000000000000000000000000000

Instruction Memory:

[illegible]

Mem[000000000000000000000000000000001001] = 00101001

```
Mem[000000000000000000000000000000001010] = 00000000
```

```
Mem[000000000000000000000000000000001011] = 00000011
```

Data Memory:

```
bne St1, St0, Judg
```

operation: bne

PC: 0000000000000000000000000000000010000

Register File:

St0: 00000000000000000000000000000000**100**

St1: 00000000000000000000000000000000**11**

Ss0: 00000000000000000000000000000000

Ss1: 000000000000000000000000000000000000

Instruction Memory:

[illegible]

Mem[000000000000000000000000000000001101] = 00101000

Mem[000000000000000000000000000000001110] = 11111111

[illegible]

Data Memory:

ient: beq St1, St0, Initiali

operation: beq

PC: 000000000000000000000000000010100

Register File:

St0: 00000000000000000000000000000100

St1: 00000000000000000000000000000011

Ss0: 00000000000000000000000000000000

Ss1: 00000000000000000000000000000000

Instruction Memory:

Mem[000000000000000000000000000010000] = 00010001

Mem[000000000000000000000000000010001] = 00101000

Mem[000000000000000000000000000010010] = 11111111

Mem[000000000000000000000000000010011] = 11111111

Data Memory:

j Exit

operation: j

opcode: 000010

address: 00000000000000000000000010101

PC: 00000000000000000000000000000000**1**1000

Register File:

St0: 00000000000000000000000000000000**100**

St1: 00000000000000000000000000000000**11**

Ss0: 000000000000000000000000000000000000

Ss1: 00000000000000000000000000000000

Instruction Memory:

Mem[000000000000000000000000000010000] = 00010001

Mem[000000000000000000000000000010001] = 00101000

Mem[0000000000000000000000000000000010010] = 11111111

Mem[0000000000000000000000000000000010011] = 11111111

Data Memory:


```
Exit:      addi $s0, $s0, 5
```

operation: addi

[illegible]

Register File:

St0: 0000000000000000000000000000000000**100**

St1: 00000000000000000000000000000000**11**

Ss0: 00000000000000000000000000000000101

Ss1: 0000000000000000000000000000000000

Instruction Memory:

Mem[0000000000000000000000000000010100] = 00100010

Mem[0000000000000000000000000000010101] = 00010000

```
Mem[0000000000000000000000000000000010110] = 00000000
```

```
Mem[0000000000000000000000000000000010111] = 00000101
```

Data Memory: