Project	▶
Add Sources...	Alt+A
Close Project	
Save Block Design	Ctrl+S
Save Block Design As...	
Close Block Design	
Constraints	▶
Simulation Waveform	▶
Checkpoint	▶
IP	▶
Text Editor	▶
Import	▶
Export	▶
Print...	Ctrl+P
Exit	

BLOCK DESIGN - design_1

Sources ✕ Design

Q ᚎ ⬦ ➕ ⏱

∨ 🗁 Design Sources (1)
  ∨ ● ⁝ design_1_wrap
    ∨ ⯂ ▣ design_1_i
      ⟩ ● design_1
∨ 🗁 Constraints (1)
  ∨ 🗁 constrs_1 (1)
    📄 design.xdc
∨ 🗁 Simulation Sources (1
  ⟩ 🗁 sim_1 (1)

Hierarchy IP Sources

Export Hardware...
Export Block Design...
Export Bitstream File...
Export Simulation...

Export Hardware

Export hardware platform for software development tools.

☑ Include bitstream

XSA file name: design_1_wrapper

Export to: D:/viva/project_2

OK   Cancel

| Tools | Reports | Window | Layout | View | Hel|

| ☑ | Validate Design | F6 |

Create and Package New IP...

Create Interface Definition...

Enable Partial Reconfiguration...

Run Tcl Script...

Property Editor | Ctrl+J

Associate ELF Files...

Generate Memory Configuration File...

Compile Simulation Libraries...

Download Latest Boards...

Download Latest Example Projects...

Xilinx Tcl Store...

Custom Commands ▶

Launch Vitis

| ♀ | Language Templates |
| ⚙ | Settings... |

Eclipse Launcher

Select a directory as workspace

Vitis IDE uses the workspace directory to store its preferences and development artifacts.

Workspace: D:\viva\project_2\vitis2   Browse...

☐ Use this as the default and do not ask again

▸ **Restore other Workspace**

▸ **Recent Workspaces**

Launch   Cancel

File   Edit   Xilinx   Project   Window   Help

Welcome

XILINX
VITIS

VITIS
IDE

PROJECT

Create Application Project

Create Platform Project

Create Library Project

Import Project

PLATFORM

Add Custom Platform

RESOURCES

Vitis Documentation

Xilinx Developer

File Edit Xilinx Project Window Help

Quick Access

Design Debug

Explorer

Assistant

Console Problems Vitis Log Guidance

Build Console

0 items selected

New Platform Project

Create new platform project

Enter a name for your platform project

Project name: uart

☑ Use default location

Location: D:\viva\project_2\vitis2\uart   Browse...

Choose file system: default ▾

• A system project is a container for multiple applications that would run on different domains of a platform at the same time.

• A domain is the BSP/OS that controls one or more isomorphic processors.

• A platform contains one or more domains.

• A workspace can contain unlimited platforms and unlimited system projects

? | < Back | Next > | Finish | Cancel

Platform Project

Create new platform project

Create a platform project from the output of Vivado [Xilinx Shell Archive (XSA)] or from an existing platform. A platform will enable you to specify options for the kernels, BSPs, as well as settings required for creating new applications. Platforms are currently supported for embedded software developers.

◉ **Create from hardware specification (XSA)**

Create a new platform project from a hardware specification file. You can specify the OS and processor to start with. The platform can be customized later from the platform project editor.

○ **Create from existing platform**

Load the platform definition from an existing platform. You can choose any platform from the platform repository as a base for your platform project.

[?]   [< Back]   [Next >]   [Finish]   [Cancel]

New Platform Project

Platform Project Specification

Provide the hardware and software specification for the new platform project

Hardware Specification

XSA file: D:\viva\project_2\vitis\design_1_wrapper.xsa   Browse...

Software Specification

Operating system: standalone

Processor: microblaze_0

ℹ️ Note: A domain with selected operating system and processor will be added to the platform. The platform project can be modified later to add new domains or change settings.

❓   < Back   Next >   Finish   Cancel

File   Edit   Xilinx   Project   Window   Help

Explorer ⌘

- uart (Out-of-date)
  - bitstream
  - export
  - hw
  - logs
  - microblaze_0
  - resources
  - platform.spr

uart ⌘

type filter text

- uart (Out-o
  - microbl
    - stand
      - Bo

vitis2 - uart/platform.spr - Vitis IDE

File Edit Xilinx Project Window Help

Explorer ⌗

uart (Out of date)
> bitstre
> expor
> hw
> logs
> micro
> resou
> platfo

uart ⌗

New   >

Paste   Ctrl+V
Delete
Refresh

Import Sources...
Export as Archive

Build Project
Clean Project

Copy referenced files into project
Update Hardware Specification

Team   >

Run As   >
Debug As   >

Properties

Assistant ⌗

uart [Plat

vitis2 - uart/platform.spr - Vitis IDE

File   Edit   Xilinx   Project   Window   Help

Explorer ⊠

- ⌄ uart
  - bitstream
  - export
  - hw
  - logs
  - microblaze_0
  - resources
  - platform.spr

uart ⊠

type filter text

- ⌄ uart
  - ⌄ microblaze_0
    - ⌄ standalone on
      - Board Supp

New Application Project

Create a New Application Project

Enter a name for your Application project.

Project name: `uart_test`

☑ Use default location

Location: `D:\viva\project_2\vitis2\uart_test`   Browse...

Choose file system: `default`

System project: `Create New...`   `uart_test_system`

System Project 1	System Project 2		
Baremetal App	Linux App 1	Linux App 2	AI Engine App

A72_0 Baremetal Domain	A72 Linux Domain	AI Engine Domain

Platform

• A system project is a container for multiple applications that would run on different domains of a platform at the same time.

• A domain is the BSP/OS that controls one or more isomorphic processors.

• A platform contains one or more domains.

• A workspace can contain unlimited platforms and unlimited system projects

? | < Back | Next > | Finish | Cancel

New Application Project

Platform

Choose a platform for your project. You can also create an application from XSA through the 'Create a new platform from hardware (XSA)' tab.

Select a platform from repository | **Create a new platform from hardware (XSA)**

Name	Board	Flow	Vendor	Path
uart [custom]		Embedded	xilinx	D:\viva\project_2\vitis2\uart\export\uart\u...
xcvc1902_fixed		Embedded	xilinx	$XILINX_VITIS\platforms\xcvc1902_fixed\...

< Back   Next >   Finish   Cancel

File   Edit   Xilinx   Project   Window   Help

Explorer ⊠

∨ ⤴ uart
  › 📂 bitstream
  › 📂 export
  › 📂 hw
  › 📂 logs
  › 📂 microblaze_0
    📂 resources
  ⤴ platform.spr

Assistant ⊠

⤴ uart [Platform]

New Application Project

Domain

Provide the domain and other software details for your project

Domain: standalone on microblaze_0 ⌄

Language: C ⌄

CPU: microblaze_0

OS: standalone

< Back   Next >   Finish   Cancel

New Application Project

Templates

Select a template to create your project.

Available Templates:

Find: [   ]

- Dhrystone
- Empty Application
- Hello World
- lwIP Echo Server
- lwIP TCP Perf Client
- lwIP TCP Perf Server
- lwIP UDP Perf Client
- lwIP UDP Perf Server
- Memory Tests
- Peripheral Tests
- SREC Bootloader
- SREC SPI Bootloader

Empty Application

A blank C project.

< Back | Next > | Finish | Cancel

File   Edit   Xilinx   Project   Window   Help

- uart
  - bitstream
  - export
  - hw
  - logs
  - microblaze_0
  - resources
  - platform.spr
- uart_test_system [uart]
  - uart_test [standalone on microblaze_0]
    - Includes
    - _ide
    - src
      - lscript.ld
      - README.txt
    - uart_test.prj
  - uart_test_system.sprj

New File

File

Create a new file resource.

Enter or select the parent folder:

uart_test/src

- RemoteSystemsTempFiles
- uart
- uart_test [standalone on microblaze_0]
  - _ide
  - src
- uart_test_system [uart]

File name: uart_echo.c

Advanced >>

Finish   Cancel

```
11  #define UART_TX_EMPTY_MASK    0x00000004
12  #define UART_TX_EMPTY_MASK    0x00000004
13  #define UART_RX_FULL_MASK     0x00000002
14  #define UART_RX_VALID_MASK    0x00000001
15  #define UART_RX_CLEAR_MASK    0x00000002
16  #define UART_TX_CLEAR_MASK    0x00000001
17
18  void uart_puts(char * ch)
19  {
20      int index = 0;
21      while (index<128)
22      {
23          if ((((*(u32 *)(UART_STAT))&UART_TX_FULL_MASK)==0)
24          {
25              if(ch[index]=='\0')
26              {
27                  break;
28              }
29              *(u32 *)(UART_TX_FIFO) = ch[index];
30              index++;
31          }
32          else
33          {
34              //等待发送
35          }
36      }
```

uart_test_system [uart]
- uart_test [s...
  - Binaries
  - Includes
  - _ide
  - Debug
  - src
    - uart_...
    - lscrip...
    - READ...
  - uart_test...
- uart_test_sy...

Assistant
- uart [Platform...
- uart_test_system
  - uart_test [A...
    - **Debug**
    - Release

Context menu:
- New >
- Move To System Project...
- Paste   Ctrl+V
- Delete
- Refresh
- Import Sources...
- Export as Archive
- Build Project
- Clean Project
- Generate Linker Script
- Program FPGA
- Program Flash
- C/C++ Build Settings
- Team >
- Run As >
- Debug As >
- Properties

Run As submenu:
- 1 Launch on Hardware (Single Application Debug)
- 2 Launch on Emulator (Single Application Debug)
- 3 Launch on Hardware (Single Application Debug (GDB))
- Run Configurations...

File Edit Xilinx Project **Window** Help

Explorer

- uart
  - bitstream
  - export
  - hw
  - logs
  - microblaze_0
  - resources
  - platform.spr
- uart_test_system [ua
  - uart_test [standal
    - Binaries

Window menu:

- Explorer
- Assistant
- Vitis Log
- Console
- Guidance
- Show view...
- Design Perspective
- Debug Perspective
- Performance Analysis Perspective
- Open perspective...
- Reset Perspective...
- Preferences

Show View

Java

Java Browsing

Make

Plug-in Development

Profiling

Remote Systems

Tcl

Team

Terminal

Terminal

Tracing

Xilinx

XML

Open   Cancel

Build Console [uart_test, Debug]

```
' '
'Invoking: MicroBlaze Print Size'
mb-size uart_test.elf  |tee "uart_test.elf.size"
   text    data     bss     dec      hex filename
   3032     268    3108    6408     1908 uart_test.elf
'Finished building: uart_test.elf.size'
' '


16:46:20 Build Finished (took 692ms)
```

Terminal ✕

Launch Terminal

Choose terminal: Serial Terminal

Settings

Port: COM4

Baud Rate: 9600

Data Bits: 8

Parity: None

Stop Bits: 1

Flow Control: None

Timeout (sec): 5

Encoding: Default (ISO-8859-1)

OK   Cancel

Serial COM4 (2023/3/16 上午9:38) ⊠

```
Out:hello world

        In:




hello world
```