AOI 312

Group Number: 34

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Group Members :

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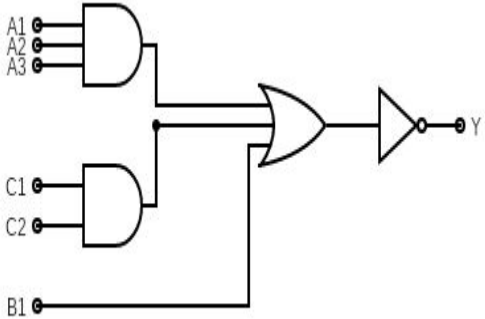
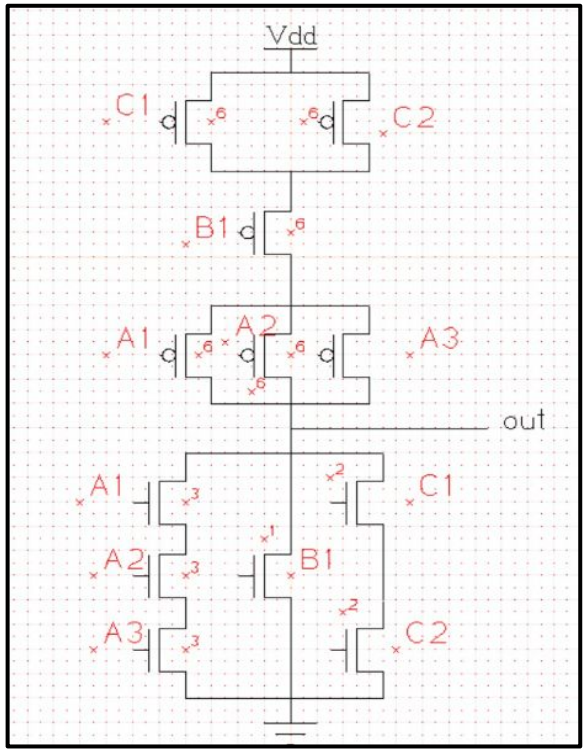
Schematic + Sizing



COMPLEX Sizing-	NON COMPLEX Sizing-
ALL PMOS: 0.81u A1,A2,A3 NMOS: 0.405u B1 NMOS: 0.135u C1,C2 NMOS: 0.270u	A1,A2,A3,C1,C2 PMOS: 0.27u B1 PMOS:0.81 A1,A2,A3 NMOS: 0.405u B1 NMOS: 0.135u C1,C2 NMOS: 0.270u

$$Y = \overline{A1*A2*A3+C1*C2+B1}$$



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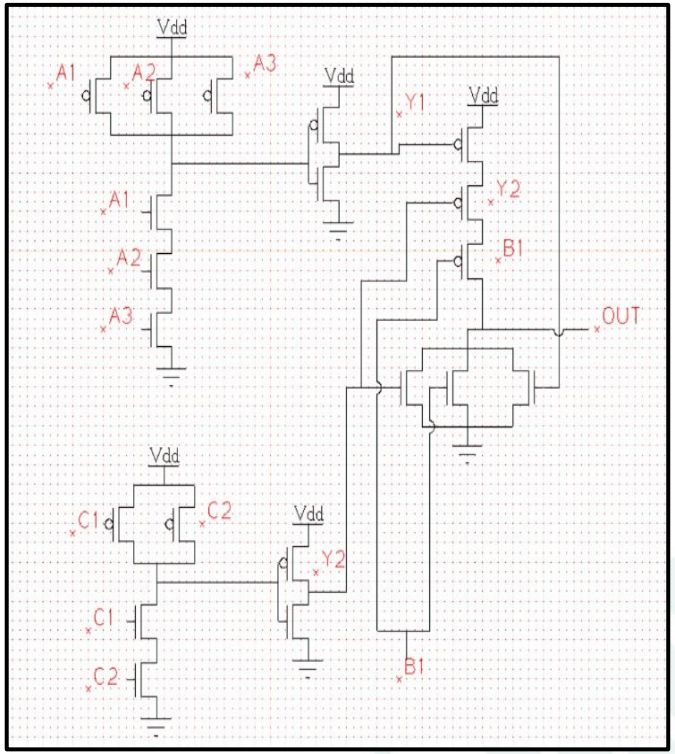
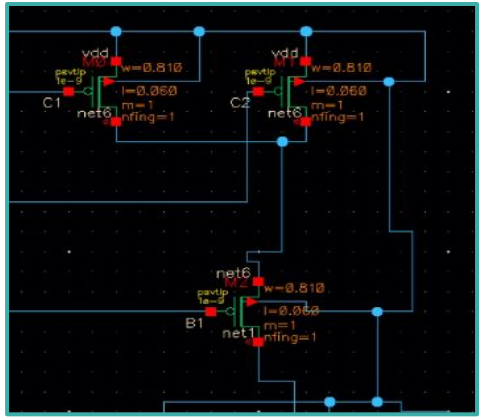
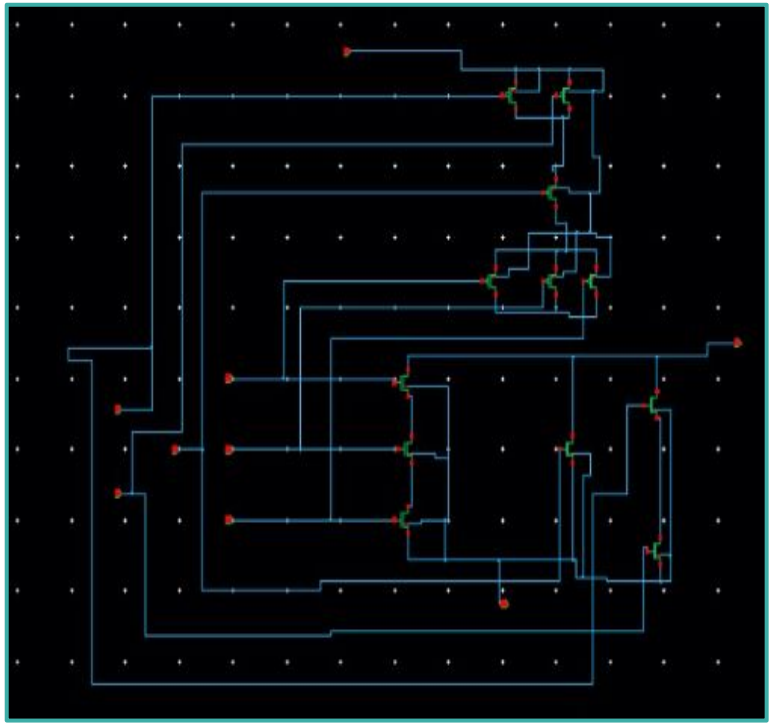
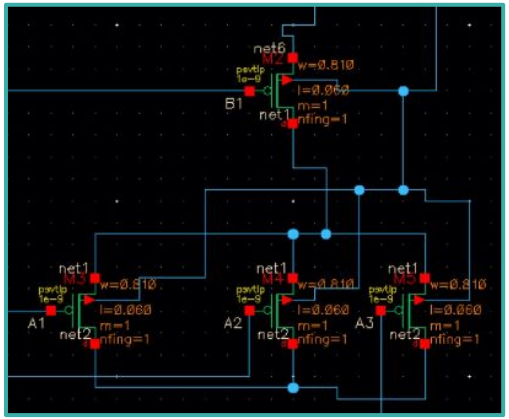


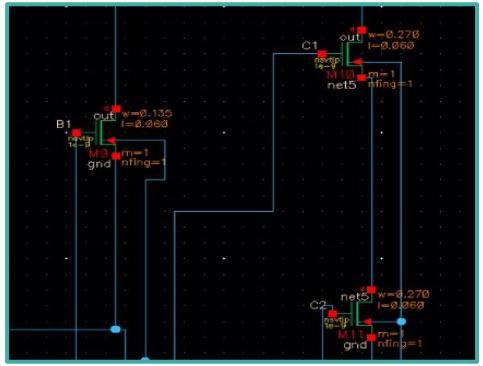
NON COMPLEX

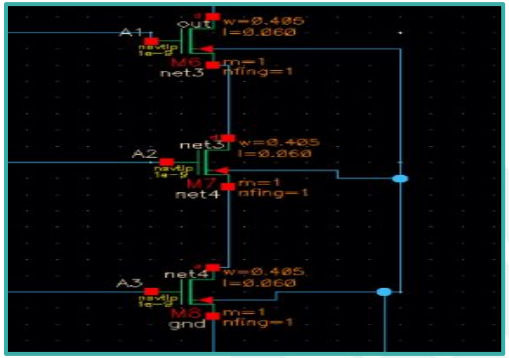
Schematic + Sizing





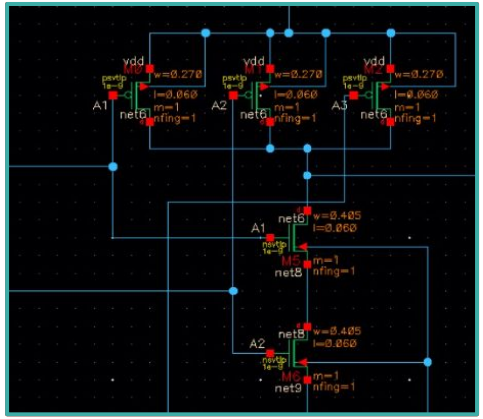


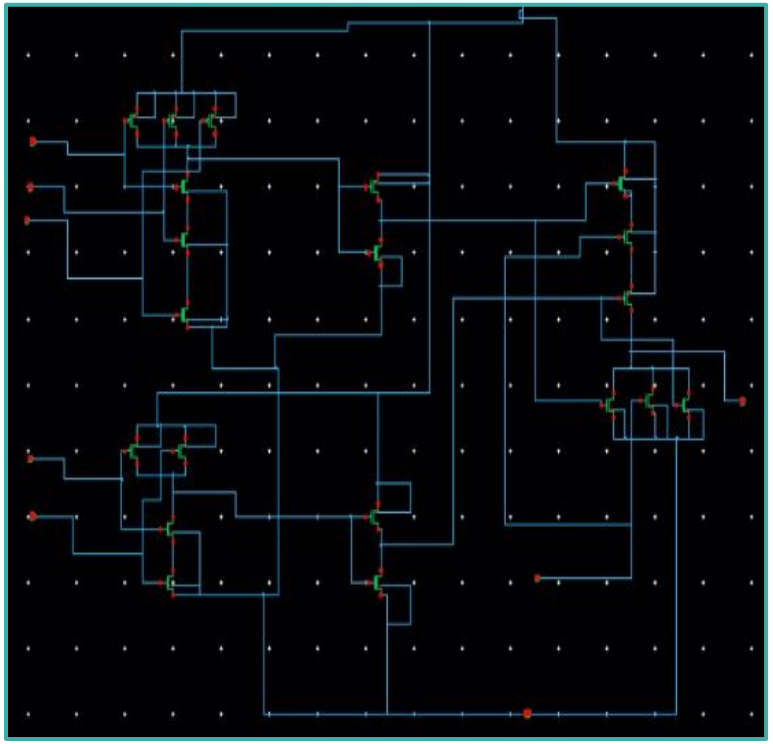


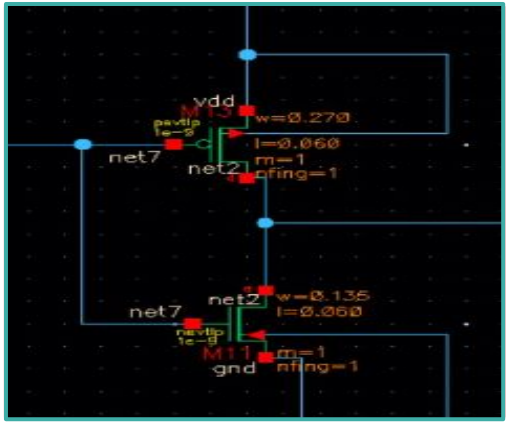


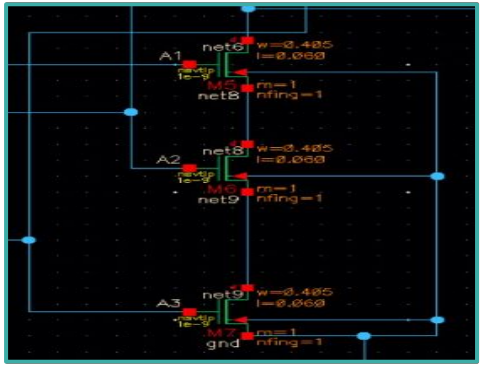
COMPLEX

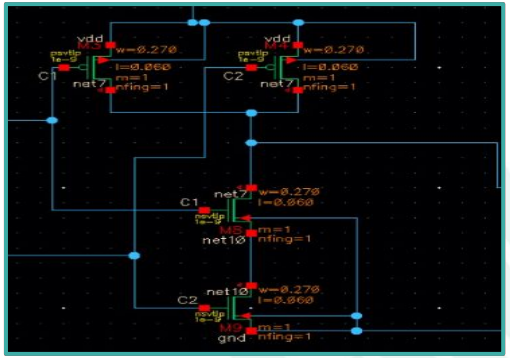
Schematic + Sizing





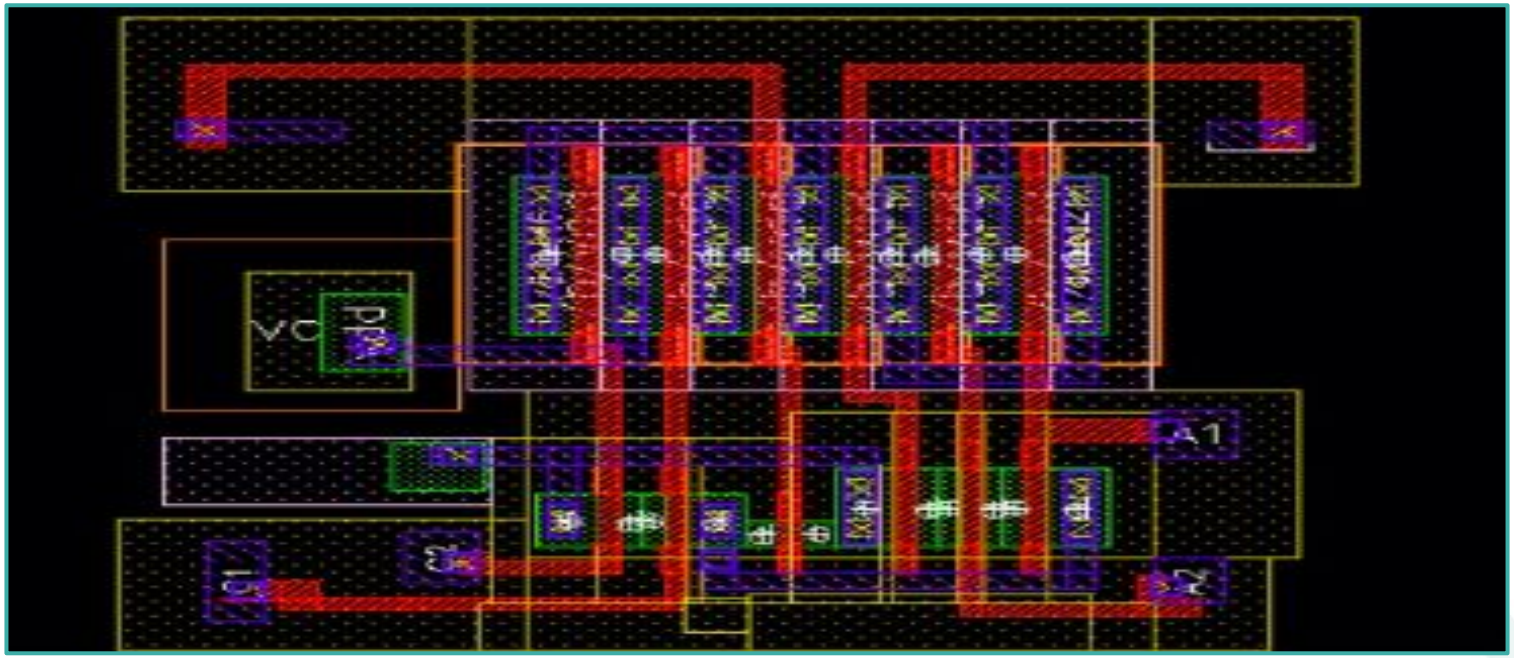






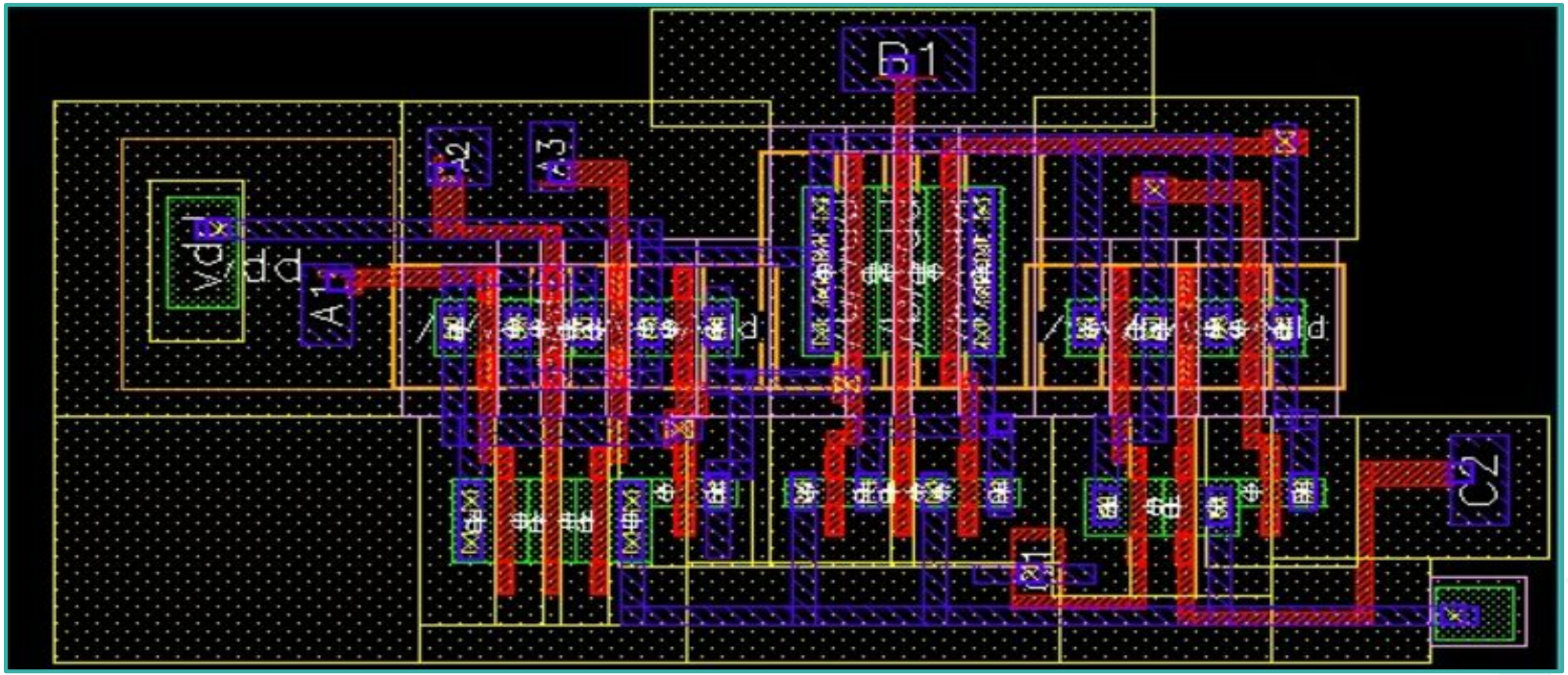
NON COMPLEX

LAYOUT FOR COMPLEX



Area = 2.6*3.7 = 9.62 um2

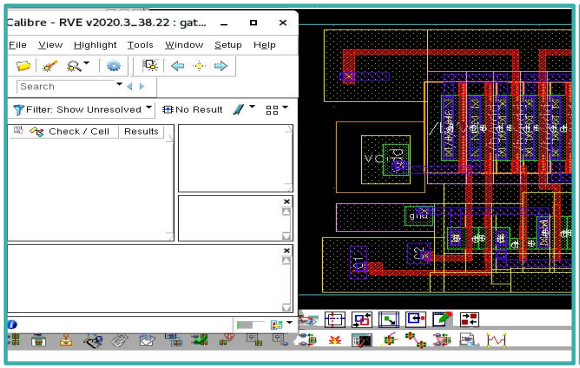
LAYOUT FOR NON COMPLEX

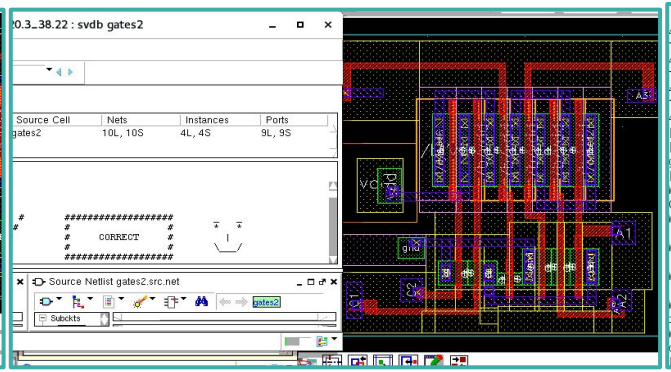


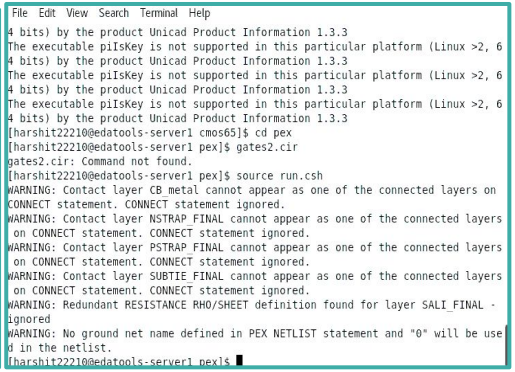
Area = 2.6*6 = 15.6 um2

DRC, LVS, PEX Results

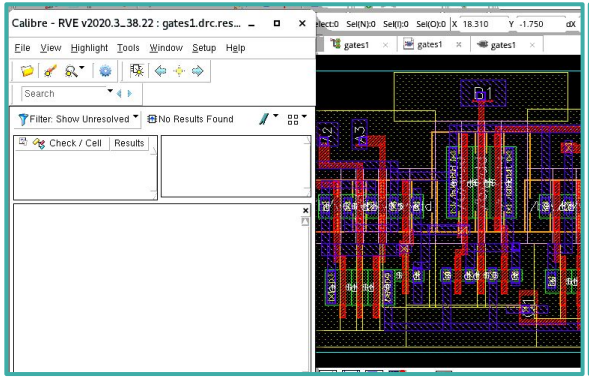
Complex

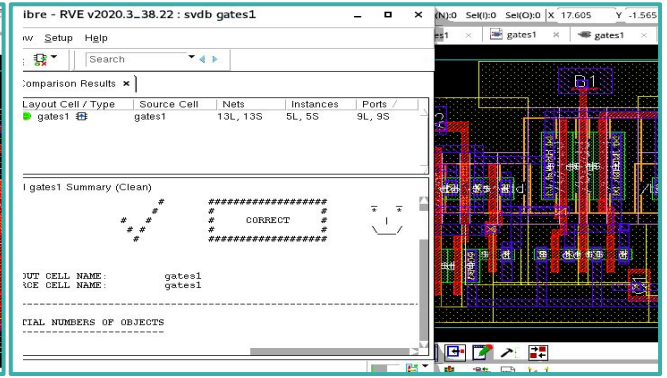


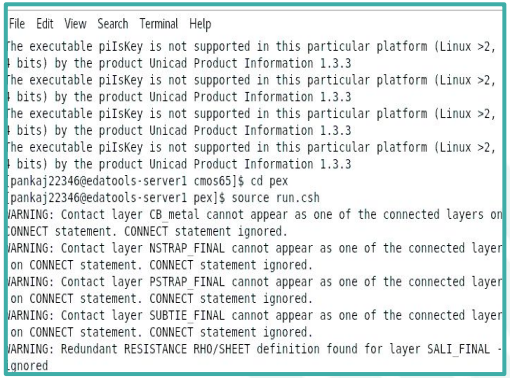




Non Complex



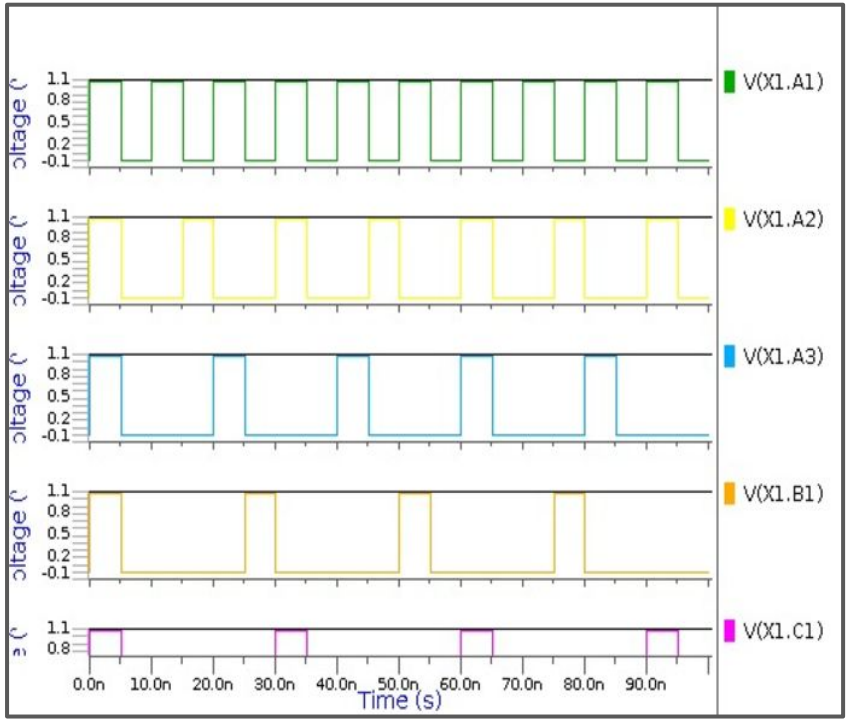


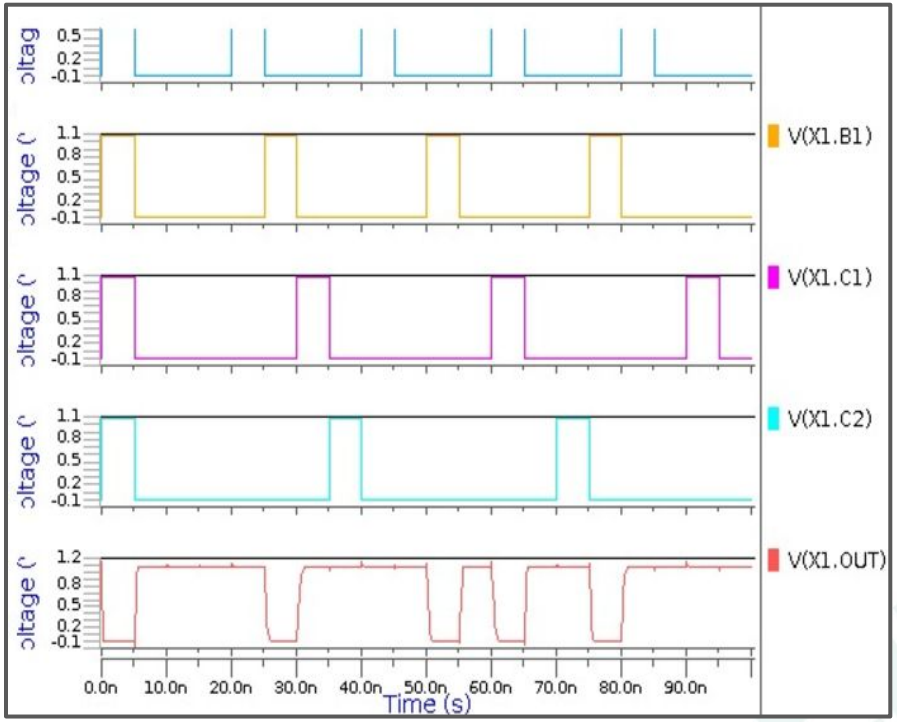


Stimuli For Verification & Verification Plan

A1	A2	A3	C1	C2	B1	AND1	AND2	OR	Y
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	0	0	1
0	0	0	0	1	1	0	0	1	0
0	0	0	1	0	0	0	0	0	1
0	0	0	1	0	1	0	0	1	0
0	0	0	1	1	0	0	1	1	0
0	0	0	1	1	1	0	1	1	0

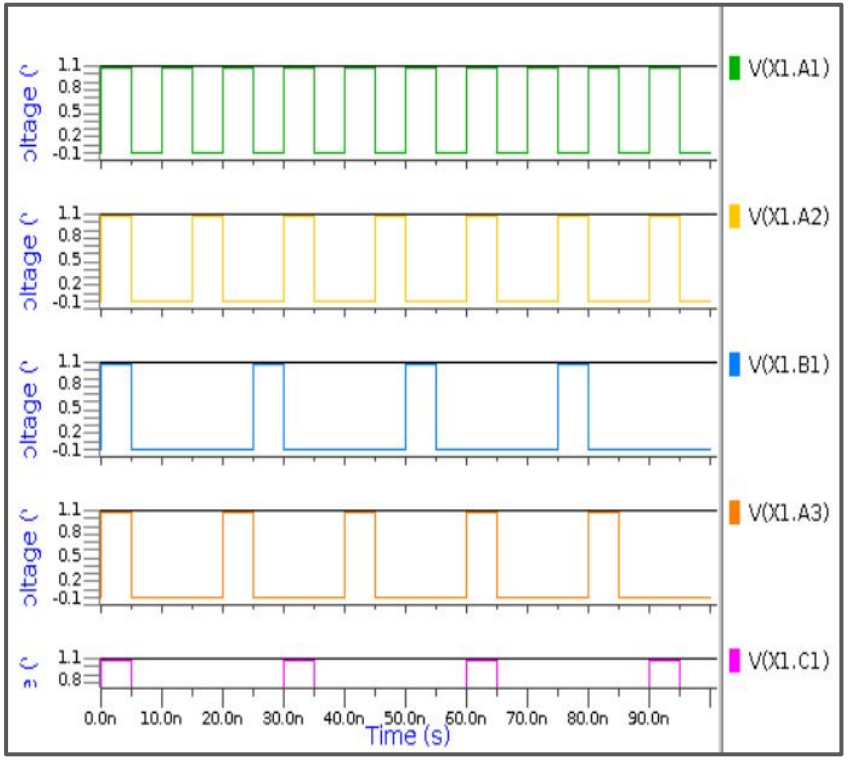
Simulation Waveforms

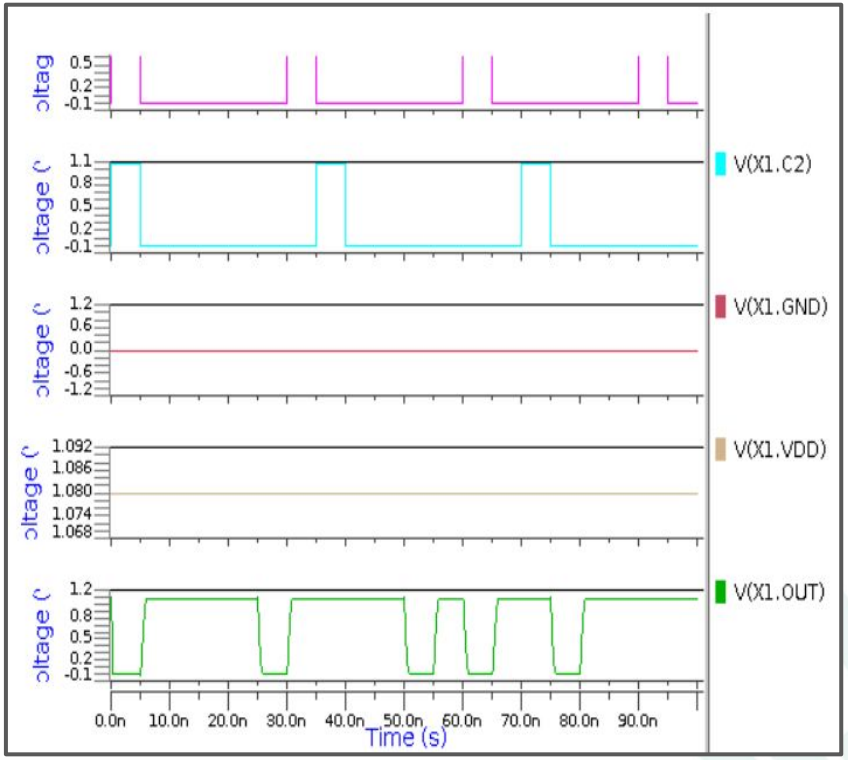




WAVEFORM FOR COMPLEX CIRCUIT

Simulation Waveforms





WAVEFORM FOR NON COMPLEX CIRCUIT

Complex pre and post layout

PVT CORNER	T-FALL (pre layout)	T-RISE (pre layout)	T-CD (pre layout)	T-PD (pre layout)	T-FALL (post layout)	T-RISE (post layout)	T-CD (post layout)	T-PD (post layout)
SS 1.08 125	11.0470	5.4219	0.12131	0.17112	10.4823	5.4281	0.12539	0.17526
SS 1.08 25	10.4261	5.3935	0.10134	0.15486	10.4301	5.3999	0.10635	0.15879
SS 1.08 -40	10.3831	5.3608	0.09725	0.13912	10.3870	5.3678	0.09928	0.14253
TT 1.32 125	10.3230	5.2619	0.07321	0.10455	10.3270	5.2676	0.07436	0.10710
FF 1.32 125	10.2580	5.2160	0.06479	0.08606	10.2640	5.2188	0.06796	0.08866
FF 1.32 -40	10.2040	5.1783	0.04351	0.06898	10.2060	5.1810	0.04813	0.06940

Scale : Nano Seconds

Non Complex pre and post layout

PVT CORNER	T-FALL (pre layout)	T-RISE (pre layout)	T-CD (pre layout)	T-PD (pre layout)	T-FALL (post layout)	T-RISE (post layout)	T-CD (post layout)	T-PD (post layout)
SS 1.08 125	10.4460	5.6358	0.21621	0.24802	10.4491	5.6401	0.21653	0.24835
SS 1.08 25	10.4120	5.5817	0.20326	0.22771	10.4168	5.5887	0.20257	0.23197
SS 1.08 -40	10.3680	5.5371	0.18244	0.20830	10.3702	5.5411	0.18279	0.21223
TT 1.32 125	10.3040	5.3878	0.12780	0.14841	10.3075	5.3899	0.12819	0.15313
FF 1.32 125	10.2440	5.3314	0.10329	0.12396	10.2461	5.3378	0.10364	0.12630
FF 1.32 -40	10.1990	5.2601	0.06988	0.09900	10.2011	5.2641	0.07125	0.10031

Scale : Nano Seconds

Complex v/s Non Complex Design

	COMPLEX	NON-COMPLEX	REMARK
Area	9.62um2	15.6um2	1.62 times area increase for non complex
Fall and Rise Delay	SS 1.08 125	SS 1.08 125	Not much change in T_rise and T_fall from complex to non complex
Contamination Delay	FF 1.32 -40	FF 1.32 -40	Contamination delay increased in Non Complex by 14%
Propagation Delay	SS 1.08 125	SS 1.08 125	Propagation delay increased in Non Complex by 15%

Leakage and power analysis

FF 1.32 125	COMPLEX		NON-COMPLEX	
	Pre layout	Post layout	Pre layout	Post layout
LEAKAGE CURRENT	106.70nA	111.85nA	151.02nA	155.02nA
STATIC POWER	20.695nW	24.93nW	46.47nW	51.23nW
DYNAMIC POWER	2.2798uW	2.3153uW	2.36uW	2.42uW

- Pre Layout vs Post Layout
  - Not much change in Leakage and Power between pre and post layout simulations.
  - Compared to complex designs, non-complex designs exhibit static and leakage power that is nearly 1.5 to 2 times higher, with a slight increase in dynamic power as well.

Conclusion

- The design area has been minimized through a compact layout.
- Minimum design rule checks (DRCs) have been prioritized to lower the overall horizontal width of the layout, contributing to area reduction.
- Non-complex logic requires a greater number of transistors, resulting in increased delays when transitioning from complex to non-complex designs.
- The Contamination And propagation delays are increased for Non-Complex Design
- Complex designs demonstrate greater power efficiency compared to non-complex designs.

Work Distribution

1. **Pankaj Kumar**:
   - Design and development of **non-complex schematic and layout**.
   - Completion of **DRC** and **LVS** checks for non-complex design.
2. **Harshit Sagar**:
   - Analysis and generation of **output waveforms** ,**pre- and post-layout simulations** of **complex design** ,X-circuit design and presentation.
3. **Md Sarfaraz Anwar**:
   - Analysis and generation of **output waveforms** and **pre- and post-layout simulations** of **non-complex design**.
4. **Aditya Kamble**:
   - Design and development of **complex schematic and layout**.
   - Completion of **DRC** and **LVS** checks for complex design.

Thank you