Boolean Operation implementation in 8T SRAM

ECE-611 (Memory Design and Test)

Group Number-18

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Problem Statement

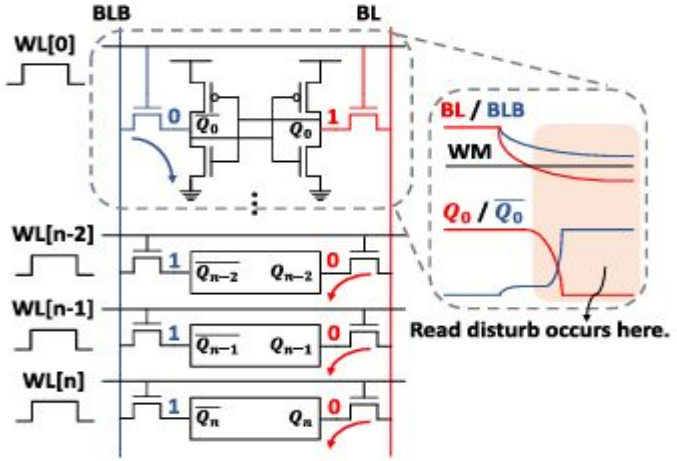
Design an 8T-SRAM in-memory computing circuit that seamlessly integrates NAND and NOR logic functions to overcome data transfer bottlenecks while maintaining stability and energy efficiency.

★ **IMC (In-Memory Computing):**
IMC performs calculations directly within the memory unit, so data doesn't have to move back and forth to the processor. This reduces delays and saves energy.

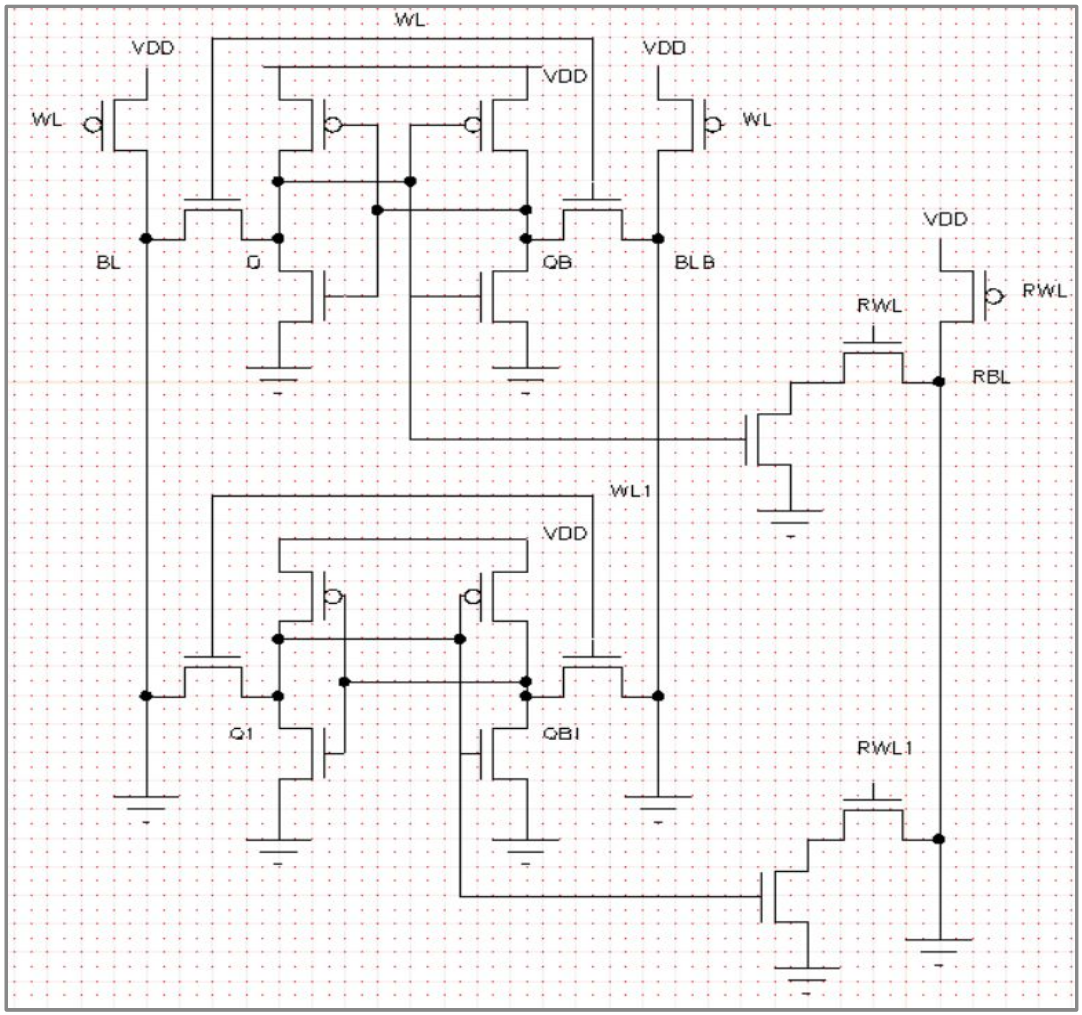
★ **8T SRAM:**
8T SRAM uses extra transistors to allow separate paths for reading and writing. This design improves performance and stability by avoiding interference during these operations.

Challenges

- ★ In SRAM-based In-Memory Computing(IMC) systems, many memory rows are often activated at the same time to improve energy efficiency and processing speed. However, turning on too many rows together can cause the voltage on the bitline (BL) to drop too much. If this voltage drops below a certain limit (called the write trigger voltage), it can accidentally flip some memory bits from 1 to 0, this is called a read disturb.
- ★ We initially implemented the standard 6T SRAM cell for our design. However, due to the issue of read disturb where excessive bitline voltage swing could lead to unintended data flips .We transitioned to an 8T SRAM cell. The 8T design provides better read stability by isolating the read path from the storage nodes, effectively eliminating the read disturb problem and improving overall reliability.



Schematic and Sizing



Basic Sizing (W/L in μm):

- ★ Pull-Up (PU): 0.135
- ★ Pass Gate (PG): 0.205
- ★ Pull-Down (PD): 0.270

A	B	NAND	NOR
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

8T SRAM BITCELLs

Nand and Nor operation

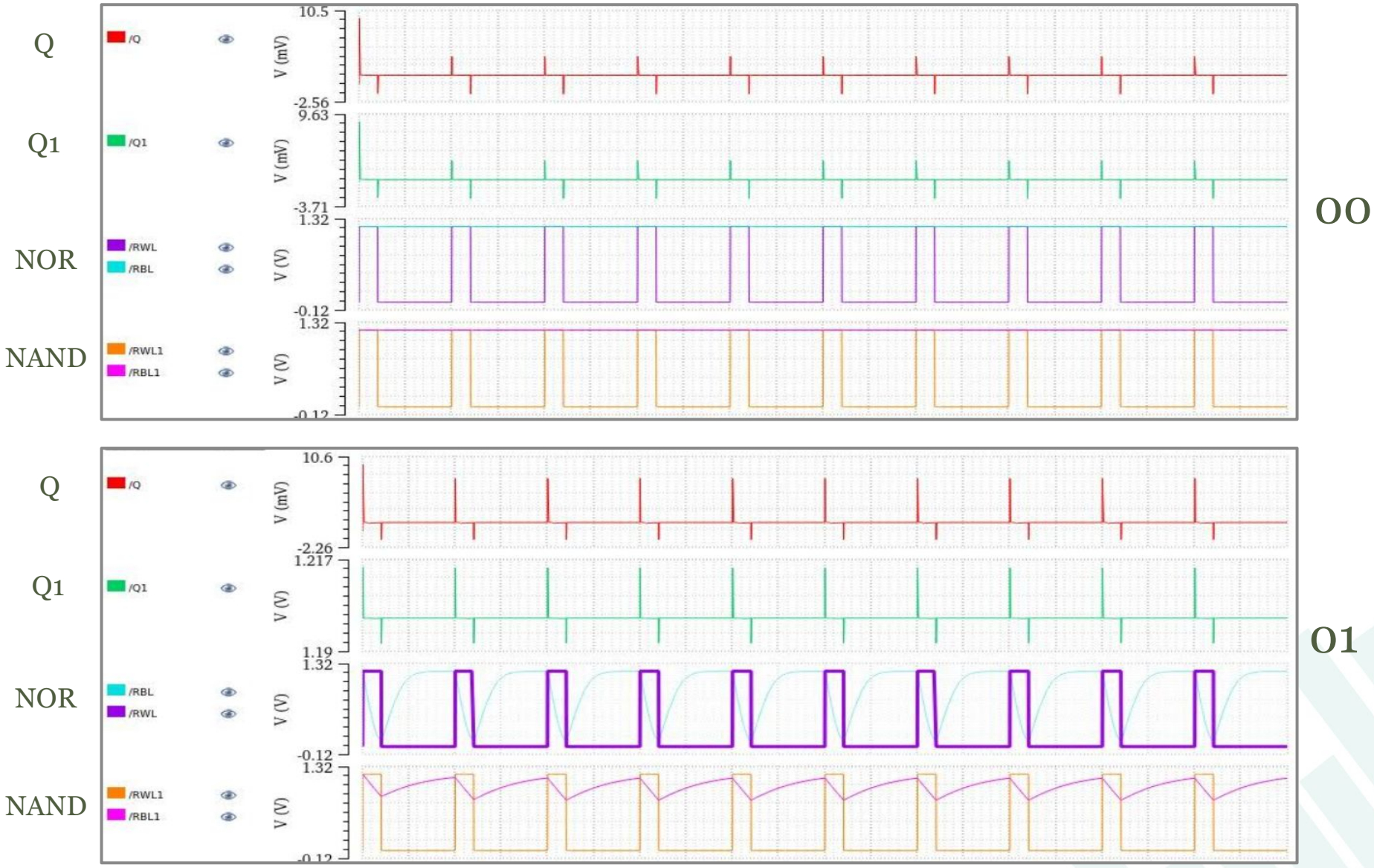
★ **NOR** **Operation:**

In the NOR configuration, the bitline is first precharged to VDD. When the wordline is activated, the NMOS transistors in the bitcells respond based on the input values. If both inputs are 0, the NMOS transistors remain off, and the bitline stays high. However, if either input is 1 (01, 10, or 11), at least one NMOS turns on, allowing the bitline to discharge. This behavior realizes NOR functionality, where the output is high only when all inputs are low.

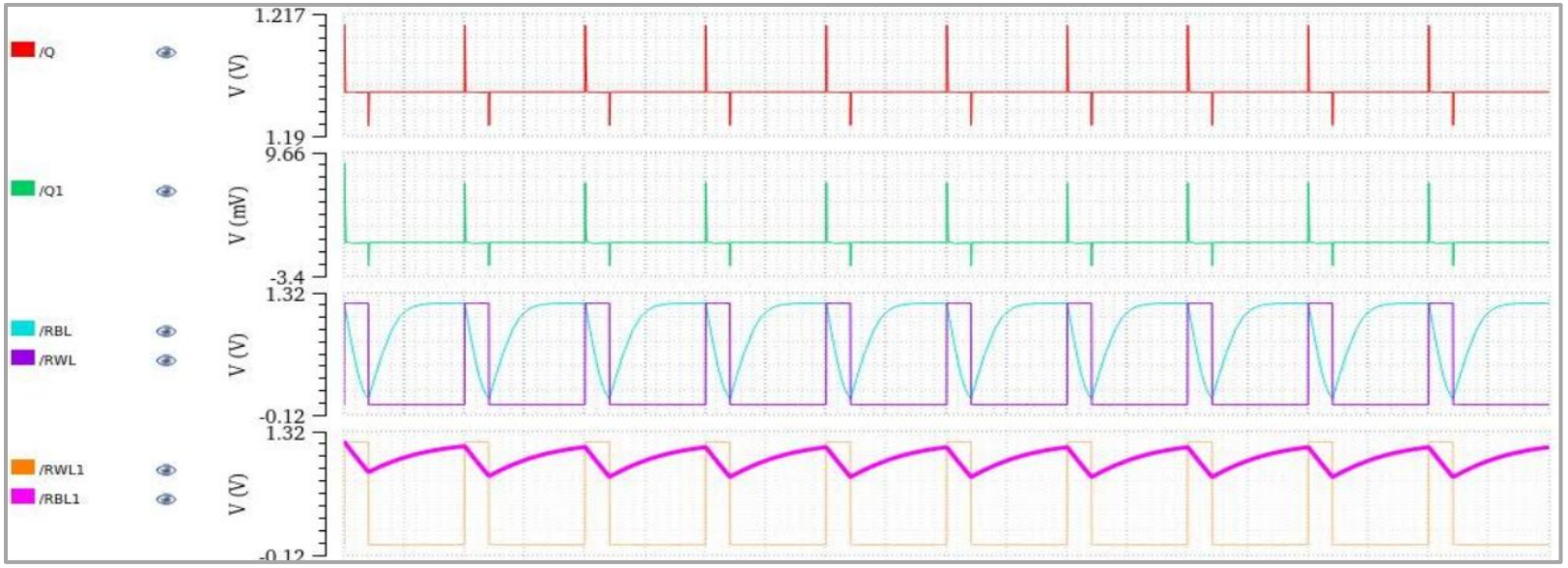
★ **NAND** **Operation:**

To achieve NAND operation, the bitline capacitance is increased and the wordline pulse width is shortened. This setup slows down the discharge rate of the bitline. For inputs 01 or 10, only one NMOS conducts, and the discharge is too slow within the short pulse duration, so the bitline remains high. When both inputs are 1 (11), both NMOS transistors conduct, enabling a faster discharge that pulls the bitline low. This ensures the bitline only discharges for input 11, implementing NAND logic.

Waveforms


Q
Q1
NOR
NAND
/Q
/Q1
/RWL
/RBL
/RWL1
/RBL1
10.5
-2.56
9.63
-3.71
1.32
-0.12
V (mV)
V (V)
OO
Q
Q1
NOR
NAND
/Q
/Q1
/RBL
/RWL
/RWL1
/RBL1
10.6
-2.26
1.217
1.19
1.32
-0.12
V (mV)
V (V)
O1

Waveforms



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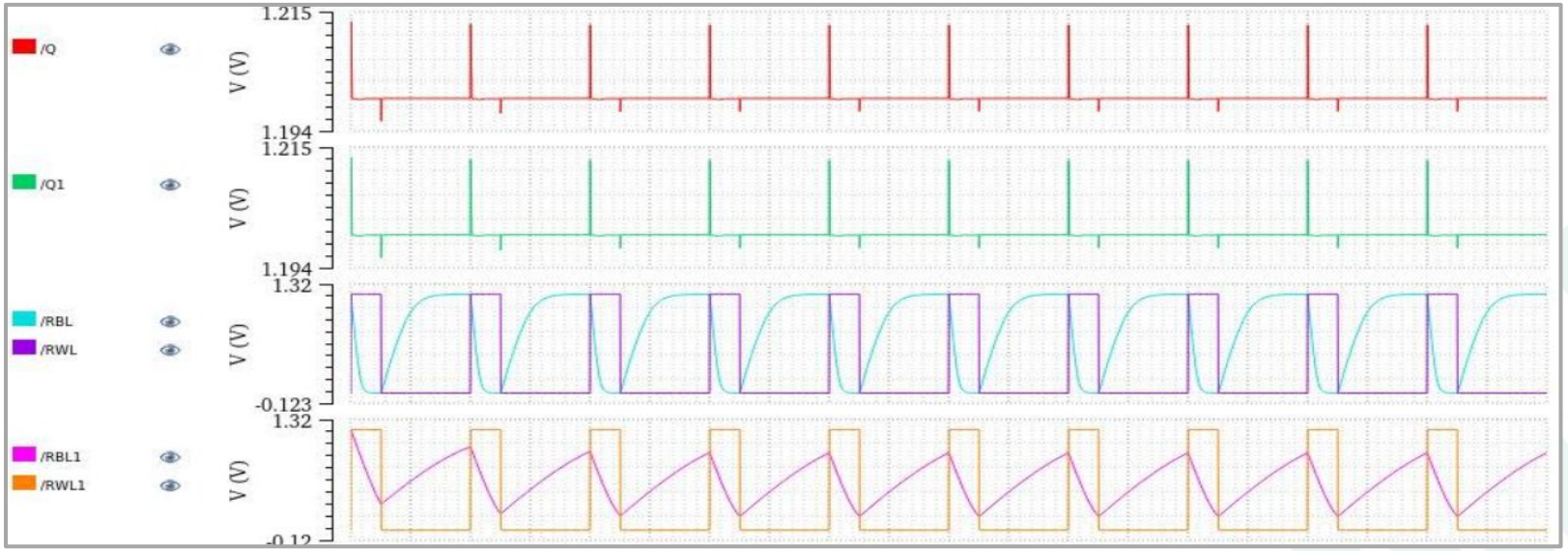

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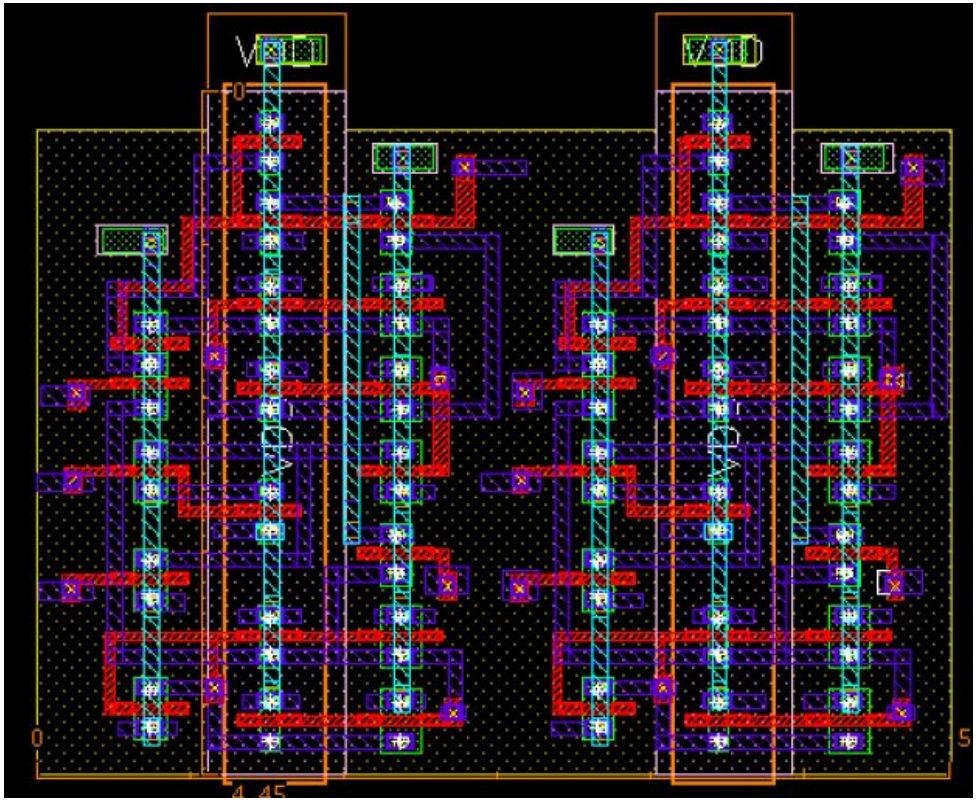
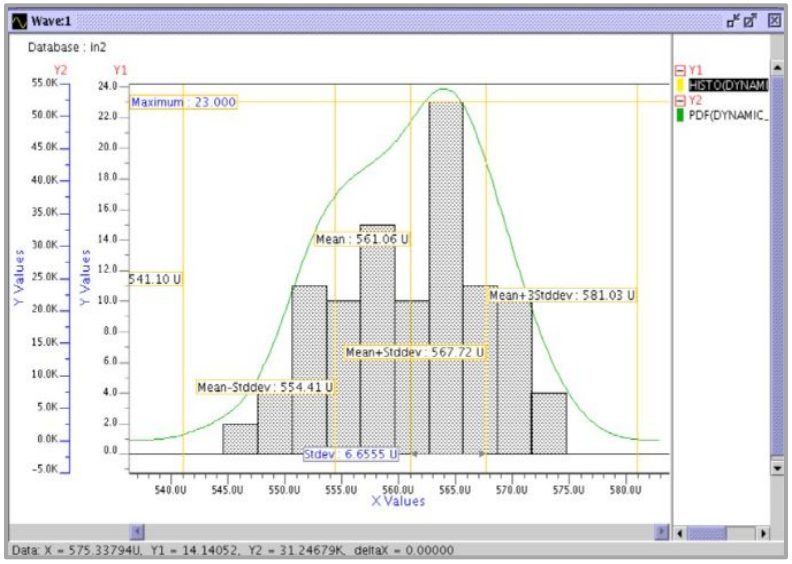
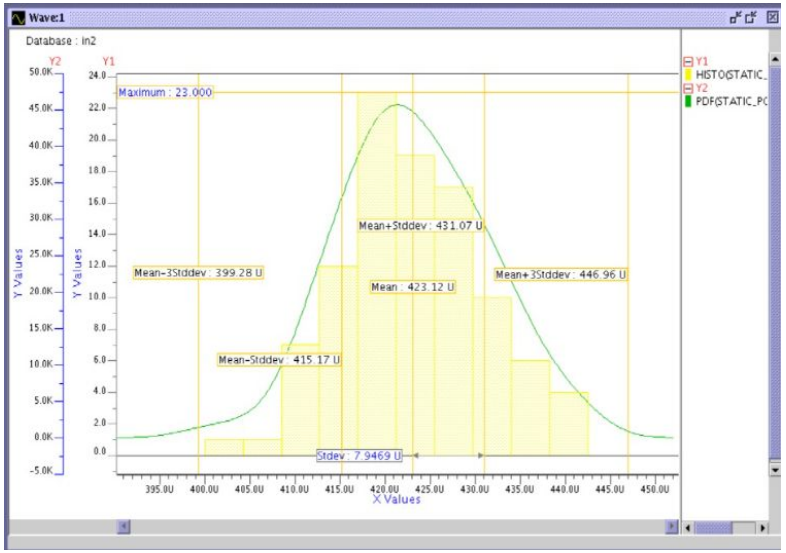
Layout

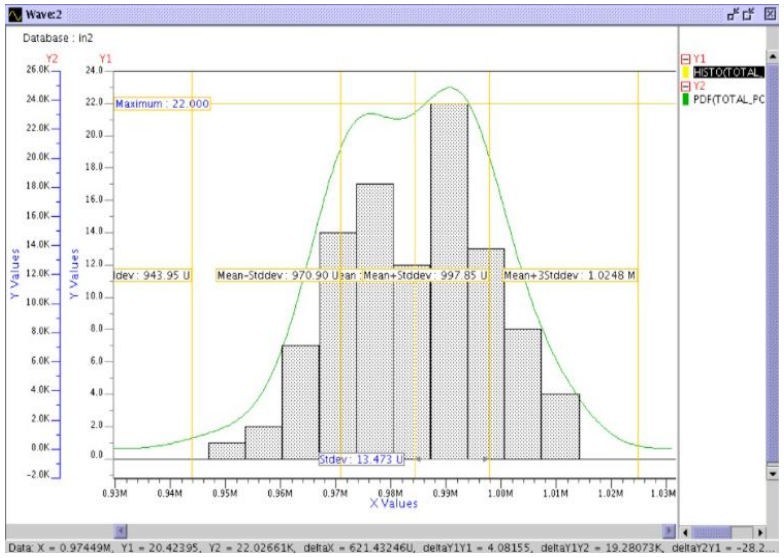


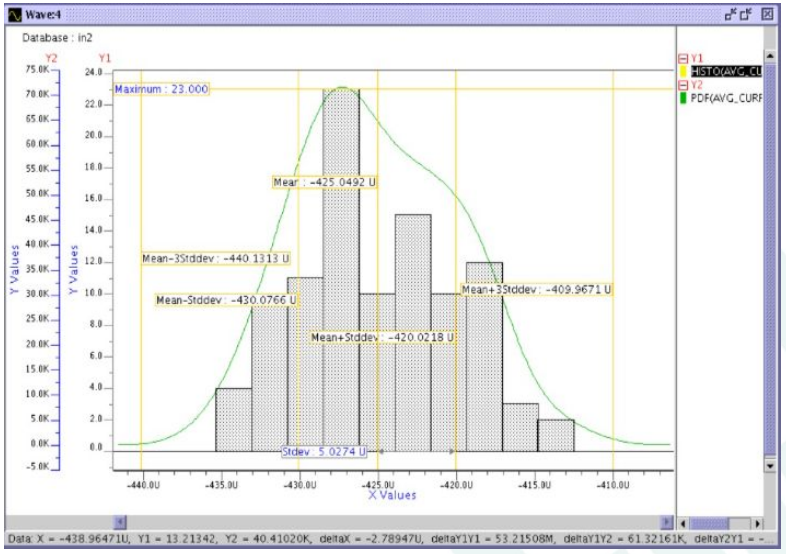
Area:26.25μm²

Graphs


Wave:1
Database : in2
Maximum : 23.000
Mean : 561.06 U
541.10 U
Mean+3Stddev : 581.03 U
Mean+Stddev : 567.72 U
Mean-Stddev : 554.41 U
Stdev : 6.6555 U
X Values
Y Values
HISTO(DYNAMI
PDF(DYNAMIC_
Data: X = 575.33794U, Y1 = 14.14052, Y2 = 31.24679K, deltaX = 0.00000


Wave:1
Database : in2
Maximum : 23.000
Mean+Stddev : 431.07 U
Mean-3Stddev : 399.28 U
Mean : 423.12 U
Mean+3Stddev : 446.96 U
Mean-Stddev : 415.17 U
Stdev : 7.9469 U
X Values
Y Values
HISTO(STATIC_
PDF(STATIC_PC


Wave:2
Database : in2
Maximum : 22.000
Mean-Stddev : 970.90 U
Mean+Stddev : 997.85 U
Mean+3Stddev : 1.0248 M
Stdev : 13.473 U
X Values
Y Values
HISTO(TOTAL_
PDF(TOTAL_PC


Wave:4
Database : in2
Maximum : 23.000
Mean : -425.0492 U
Mean-3Stddev : -440.1313 U
Mean-Stddev : -430.0766 U
Mean+3Stddev : -409.9671 U
Mean+Stddev : -420.0218 U
Stdev : 5.0274 U
X Values
Y Values
HISTO(AVG_CU
PDF(AVG_CURF
Data: X = -438.96471U, Y1 = 13.21342, Y2 = 40.41020K, deltaX = -2.78947U, deltaY1Y1 = 53.21508M, deltaY1Y2 = 61.32161K, deltaY2Y1 = -

Pre & Post Layout Simulations

	LEAKAGE CURRENT (PRE-LAYOUT)	DYNAMIC POWER (PRE-LAYOUT)	STATIC POWER (PRE-LAYOUT)	TOTAL POWER (PRE-LAYOUT)
SS,1.08V,25	-0.178 m	0.192 m	0.146 m	0.338 m
SS,1.08V,125	-0.170 m	0.183 m	0.140 m	0.324 m
SS,1.08V,-40	-0.187 m	0.203 m	0.153 m	0.356 m
TT,1.32V,125	-0.321 m	0.424 m	0.323 m	0.748 m
FF,1.32V,125	-0.379 m	0.501 m	0.382 m	0.883 m
FF,1.32V,-40	-0.428 m	0.565 m	0.424 m	0.990 m

Conclusions and Future Plans

- **Challenges faced:**
  - Read disturb issues,in conventional 6T sram cells, simultaneous activation of multiple worldlines can lead to bit flips.
  - Analysis for different FOM(figures of merit) was challenging to get right.

- **Future Plans:**
  - Expand Logic Capabilities like XOR.
  - Optimize the layout which has some issues .

References

- A. Agrawal, A. Jaiswal, C. Lee, and K. Roy, "X-SRAM: Enabling In-Memory Boolean Computations in CMOS Static Random Access Memories," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4219–4232, Dec. 2018, doi: 10.1109/TCSI.2018.2848999.

- C.-J. Jhang, C.-X. Xue, J.-M. Hung, F.-C. Chang, and M.-F. Chang, "Challenges and Trends of SRAM-Based Computing-In-Memory for AI Edge Devices," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 5, pp. 1773–1786, May 2021, doi: 10.1109/TCSI.2021.3064189.

Contribution:-

All the work has been done mutually by team members.

Thank You