## Floorplanning using Simulated Annealing

#### Manuel Haag

Universitat Politècnica de Catalunya Department of Computer Science

Project for the Course Algorithms for VLSI January 7, 2024



## Floorplanning

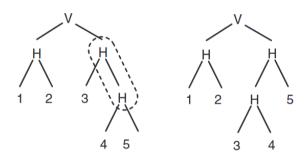
#### Modules

- hard
- rotatable

### Costfunction

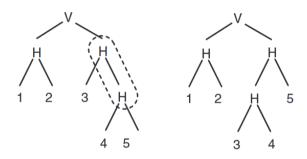
$$\alpha \frac{A}{A_{avg}} + (1 - \alpha) \frac{W}{W_{avg}}$$

## Normalized Polish Expression [1]



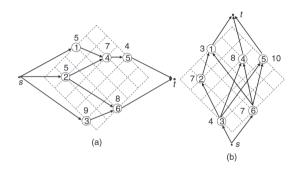
- like Polish Expression, but no VV or HH allowed  $\rightarrow$  no redundant solutions
- only 1 or 2 paths have to be updated ( $> 2 \times$  faster)

## Normalized Polish Expression [1]



- like Polish Expression, but no VV or HH allowed  $\rightarrow$  no redundant solutions
- only 1 or 2 paths have to be updated (>  $2\times$  faster)

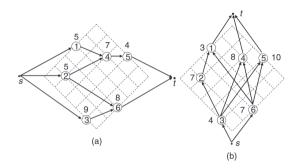
# Sequence Pair [2]



### Computing LCS efficiently

- $O(n \log n)$  algorithm requires balanced tree
- same paper also presents simple  $O(n^2)$  algorithm (>  $6\times$  faster than standard DP)

# Sequence Pair [2]



### Computing LCS efficiently

- $O(n \log n)$  algorithm requires balanced tree
- same paper also presents simple  $O(n^2)$  algorithm (>  $6\times$  faster than standard DP)

## Simulated Annealing

#### Estimate inital temperature

Let p be the initial probability of accepting a move.

$$p < \exp\left(\frac{-\Delta_{avg}}{T_{start}}\right) \Rightarrow T_{start} = \frac{-\Delta_{avg}}{\log p}$$

#### Set cool-rate for n iterations

$$\beta^n T_{start} = T_{end} \Rightarrow \beta = \left(\frac{T_{end}}{T_{start}}\right)^{1/n}$$

## Simulated Annealing

#### Estimate inital temperature

Let p be the initial probability of accepting a move.

$$p < \exp\left(\frac{-\Delta_{avg}}{T_{start}}\right) \Rightarrow T_{start} = \frac{-\Delta_{avg}}{\log p}$$

#### Set cool-rate for n iterations

$$\beta^n T_{start} = T_{end} \Rightarrow \beta = \left(\frac{T_{end}}{T_{start}}\right)^{1/n}$$

### Experiments

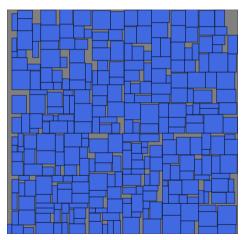
### Setup

- rustc 1.73.0
- 300 modules, 1632 nets instance from GSRC-benchmark
- 5 repetitions
- $10^7$  SA iterations, p = 0.95

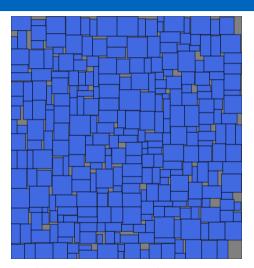
#### Runtime

- Normalized Polish Expression: 253.4s
- Sequence Pair 170.3s

### Results



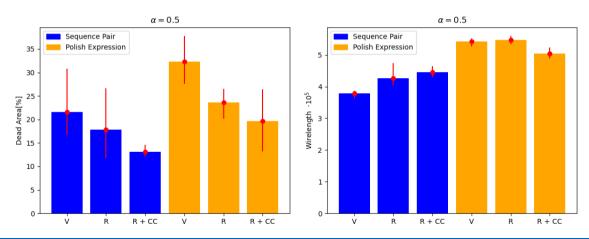
(a) Polish Expression, 7.94% dead area



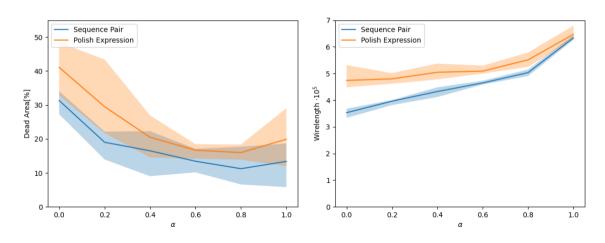
(b) Sequence Pair, 6.44% dead area

### **Experiments - Initial Solution**

• V – vertical, R – recursive bisection, CC – cluster growing order



## Experiments - Different $\alpha$



### References

- [1] D.F. Wong and C.L. Liu. "A New Algorithm for Floorplan Design". In: 23rd ACM/IEEE Design Automation Conference. 1986, pp. 101–107. DOI: 10.1109/DAC.1986.1586075.
- [2] H. Murata et al. "Rectangle-packing-based module placement". In: Proceedings of IEEE International Conference on Computer Aided Design (ICCAD). 1995, pp. 472–479. DOI: 10.1109/ICCAD.1995.480159.