

Lab 4 Answer Sheet

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Date: 22, av 2016

PRELAB:

- ~~X~~ Q1. Consider the Verilog code in section 3.0. Briefly explain how the **always @** structure works.

it is an infinite loop which goes until you tell it to stop.

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- Q2. Write the Verilog code for **lab4step1**. Use the example code given in Section 3.0 and make the necessary changes.

```

Module Farmer(A, F, C, G1, w);
    input F, C, G1, w;
    output A;
    reg A;
    always @(F or C or G1 or w) begin
        case ({F, C, G1, w})
            4'b0000 : A = 'b0;
            4'b0001 : A = 'b0;
            4'b0010 : A = 'b0;
            4'b0011 : A = 'b1;
            4'b0100 : A = 'b0;
            4'b0101 : A = 'b0;
            4'b0110 : A = 'b1;
            4'b0111 : A = 'b1;
            4'b1000 : A = 'b1;
            4'b1001 : A = 'b1;
            4'b1010 : A = 'b0;
            4'b1011 : A = 'b0;
            4'b1100 : A = 'b0;
            4'b1101 : A = 'b0;
            4'b1110 : A = 'b0;
            4'b1111 : A = 'b0;
        endcase
    end
endmodule

```

- Q3. Read Section 4.0 and fill in the Truth Table for *lab4step2*.

Inputs				Outputs		
T	H	P	M	E	F	AC
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	1
1	0	1	1	1	0	0
1	1	0	0	1	0	1
1	1	0	1	1	0	0
1	1	1	0	1	1	1
1	1	1	1	1	1	1

$$E = P(T \cdot H) + \bar{P}(T \cdot \bar{H})$$

$$F = P \cdot T \cdot \bar{H}$$

$$\begin{aligned} AC &= E, \text{ if } M = 0 \\ &= F \text{ if } M = 1 \end{aligned}$$

TA Initials: MS

LAB:

3.0 Use the hardware results to fill in the truth table for *lab4step1*.

Farmer	Cabbage	Goat	Wolf	Alarm
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Hardware results demonstrate correct code. TA Initials: MCB

4.0 Demonstrate hardware results for correct code. TA Initials: CD

temperature and the humidity are high.

Multiplexer:

inputs = {M, E, F}, outputs = {AC}

$$M=0, M=F$$

You have to enter this block in Verilog. When M = 0, we will choose Normal Mode (E), when M = 1, we will choose Power-Saving Mode (F).

$$\begin{cases} M=E \\ M=F \end{cases}$$

- Start a new project and name it lab4step2. Ensure that you start the new project in a new folder (by the same name). Open a new Block Diagram file. This is the Graphic Editor file where all the components of the A/C system will be instantiated.
- Next, create the blocks that would represent the A/C components. Click on the block tool from the upper toolbar (see Figure 2). Left click anywhere on the blank block diagram file and drag your mouse. Repeat this process 2 more times. The three blocks would represent the components of your A/C system. Right click on the 1st block and click **Properties**, rename the block normal, click on I/O tab and enter P,T,H as inputs and E as the output. Repeat the same step for the other blocks. Make sure that the naming convention is same as mentioned in the problem statement above.
- Enter 4 inputs pins (P, H, T, M) and one output pin (AC) in the design file.
- Click on the **Orthogonal Conduit Tool** from the upper toolbar and connect the input pins, output pin and the blocks using the Conduit. This would automatically map the output of one block onto the input of the other block, assuming the names are the same. Refer to the figure below to make sure your design is right.

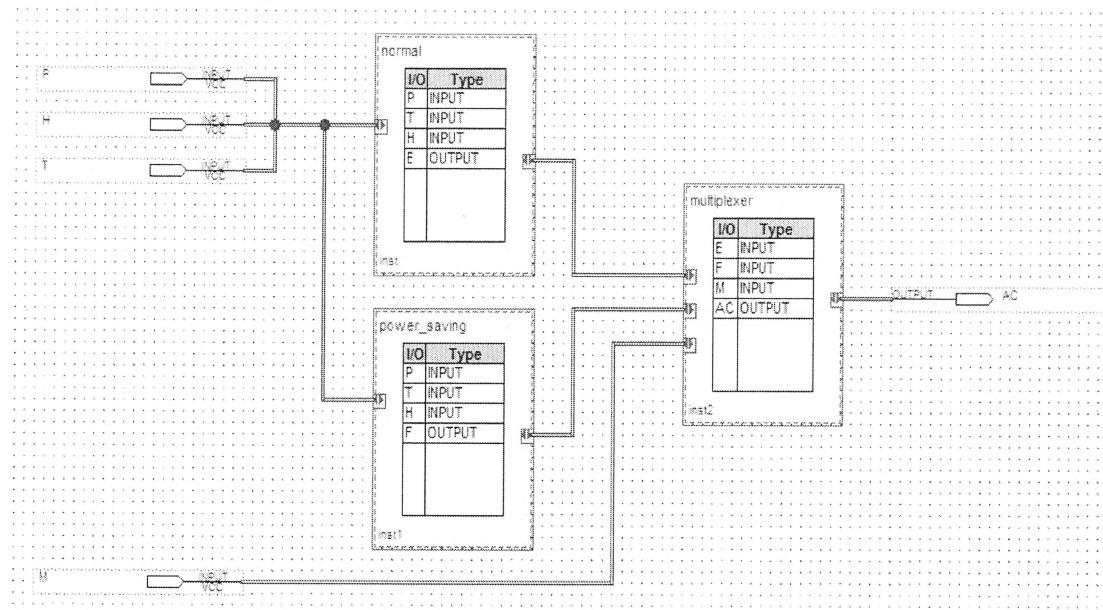


Figure 2: Final Layout of Lab4step2.

- Now that the design is done, write the back-end code for the components. Right click on the normal block and click on **Create Design File from selected Block**. Choose Verilog and click OK. This will open a Verilog file. Write the code for the block before the endmodule statement. Be aware that the inputs and outputs have already been declared. Repeat this step for the rest of the blocks.
- Compile the project and fix any errors. Use the DE2-115 board to verify your circuit works correctly. Get it signed off by the TA.

5.0 Complete

You are done with this lab. Ensure that all lab files are closed, exit Quartus Prime, log off the computer, power down the DE2-115 board, and hand in your answer sheet. **Don't forget to write down your name, student ID, and your lab section number.**