

Lab 5 Answer Sheet

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PRELAB:

- Q1. Use Figure 1 and the table below to fill in the truth table on the next page.

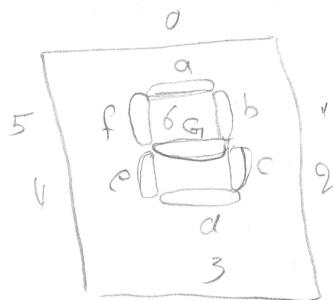
Z	Y	X	W	Display
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

Z	Y	X	W	Display
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

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Z	Y	X	W	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	P
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0
1	0	1	0	0	0	1	0	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	1	0	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

HE



Q2. Write the verilog code for the 7-Segment Display Decoder based on the truth table from Q1. You only need to write the skeleton code (i.e., a code which shows only a rough outline and no unnecessary or repetitive details) below.

```
module Segment (A,B,C,D,E,F,G,z,y,x,w);  
    input z,y,x,w;  
    output A,B,C,D,E,F,G;  
    reg A,B,C,D,E,F,G;  
    always @ (z or y or x or w)  
        begin  
            case ({w,x,y,z})  
                4'b0000 : {A,B,C,D,E,F,G} = 7'b0000001;  
            endcase  
        end  
    endmodule
```

-1

TA Initials: MS

LAB:

3.0 Lab5step0

Hardware demonstrates a good circuit. TA Initials: AW

4.0 Lab5step1

Hardware demonstrates a good circuit. TA Initials: CD

