

Cpr E 281 MINI  
PROJECT  
ELECTRICAL AND COMPUTER  
ENGINEERING  
IOWA STATE UNIVERSITY

(97)

Mini Project Answer Sheet

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Lab Section: K

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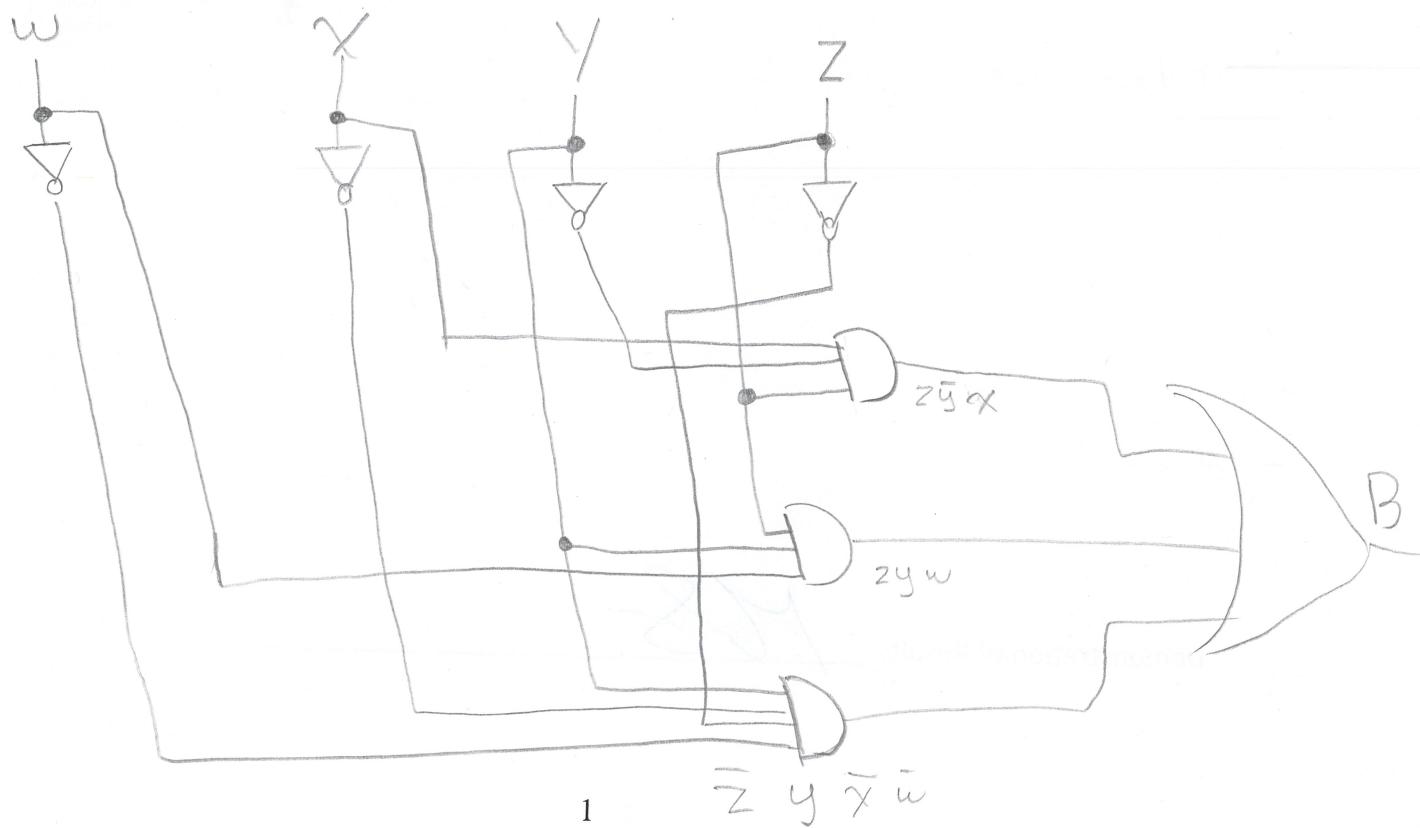
**PRELAB:**

Read the Mini-Project lab document and complete as much of this answer sheet as you can before lab.

TA Initials: M.S.

**LAB:**

- 4.0 Draw Uncle Bob's circuit below, using only AND, OR, and NOT gates.



5.0 Give the shorthand canonical SOP expression for Uncle Bob's circuit and then the Verilog code which implements this behavior:

$$B(W, X, Y, Z) = \frac{\sum_m (2, 5, 11, 13, 15)}{(Z\bar{Y}X) + (ZY\bar{W}) + (\bar{Z}\bar{X}Y\bar{W})}$$

**Verilog:**

module example (B, w, x, y, z);

input w, x, y, z;

output B;

assign B = ( $\bar{z} \& \bar{y} \& x$ ) | ( $z \& y \& w$ ) | ( $\bar{z} \& \bar{x} \& y \& \bar{w}$ );

end module

Demonstration of Results: M8

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6.0 Truth table for Uncle Bob's function B and the 4-bit prime detector function P.

W	X	Y	Z	B	P
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	\	1
0	0	1	1	@	1
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	\	1
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	1	1	0

P

	wx	00	01	11	10
yz		00	01	11	10
00	0	0	0	0	0
01	0	(1)	(1)	0	0
11	(1)	(1)	0	(1)	
10	(1)	0	0	0	0

Simplified SOP Expression:

$$P(W, X, Y, Z) = \underline{X\bar{Y}Z + \bar{W}YZ + \bar{X}YZ + \bar{W}\bar{X}Y}$$

- 7.0 Give your implementation of the correct 4-bit prime detector circuit (**P**) below as either Verilog or a schematic (your choice). Then demonstrate the results:

module example (P, w, x, y, z);

input w, x, y, z;

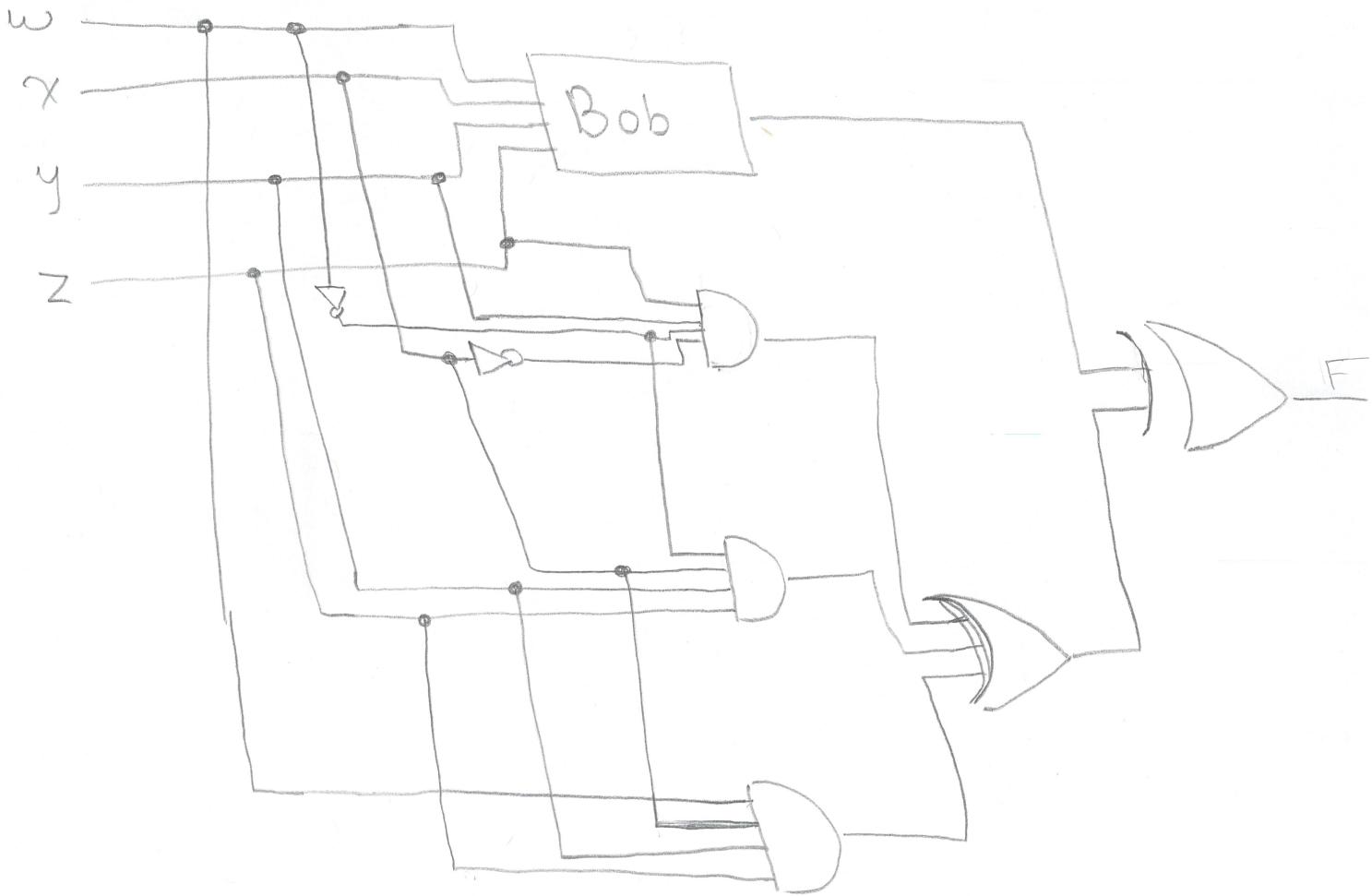
output P;

assign P = (x & ~y & z) | (~w & y & z) | (~x & y & z) |  
(~w & ~x & y);

endmodule

- Demonstration of Results: JGS

8.0 Design and implement a circuit that uses Uncle Bob's circuit but fixes his mistakes.  
Draw it below and demonstrate the results:



-3 extra gates

Demonstration of Results:

Alv

