

## Lab 6 Answer Sheet

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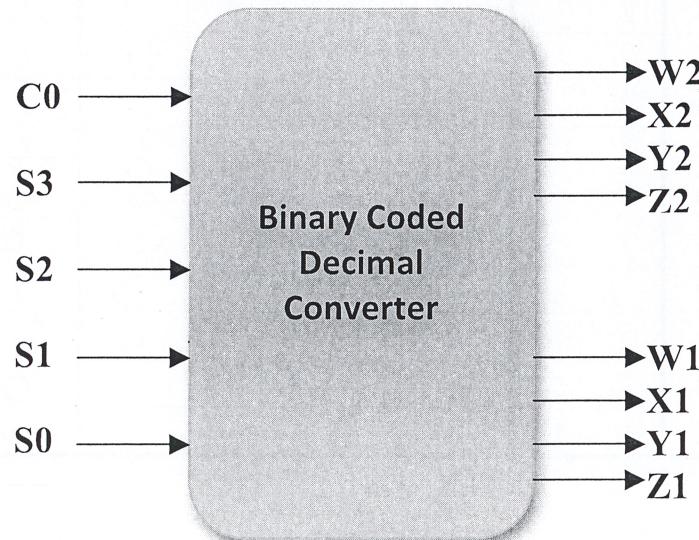
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### PRELAB:

- Q1. Add the following numbers then write them in decimal:

Binary numbers to add a3 a2 a1 a0 + b3 b2 b1 b0	Binary result C0 S3 S2 S1 S0	Decimal conversion D2 D1 (Z2 Y2 X2 W2) (Z1 Y1 X1 W1)
1001 + 0111	10000	16
1011 + 1001	10100	20
1110 + 0101	10011	19
0010 + 1110	10000	16
1101 + 1011	11000	24

- Q2. Consider the five-bit binary result (Co, S3, S2, S1, S0) representation in the table above. We would like to represent each combination as its equivalent in two decimal digits, each of which can be represented in binary as shown in the following table. Finish filling the following truth table.



Lab 6 Answer Sheet

	C0	S3	S2	S1	S0	Decimal	Z2	Y2	X2	W2	Z1	Y1	X1	W1
0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0 1	0	0	0	0	0	0	0	1
2	0	0	0	1	0	0 2	0	0	0	0	0	0	1	0
3	0	0	0	1	1	0 3	0	0	0	0	0	0	1	1
4	0	0	1	0	0	0 4	0	0	0	0	0	1	0	0
5	0	0	1	0	1	0 5	0	0	0	0	0	1	0	1
6	0	0	1	1	0	0 6	0	0	0	0	0	1	1	0
7	0	0	1	1	1	0 7	0	0	0	0	0	1	1	1
8	0	1	0	0	0	0 8	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0 9	0	0	0	0	1	0	0	1
10	0	1	0	1	0	1 0	0	0	0	1	0	0	0	0
11	0	1	0	1	1	1 1	0	0	0	1	0	0	0	1
12	0	1	1	0	0	1 2	0	0	0	1	0	0	1	0
13	0	1	1	0	1	1 3	0	0	0	1	0	0	1	1
14	0	1	1	1	0	1 4	0	0	0	1	0	1	0	0
15	0	1	1	1	1	1 5	0	0	0	1	0	1	0	1
16	1	0	0	0	0	1 6	0	0	0	1	0	1	1	0
17	1	0	0	0	1	1 7	0	0	0	1	0	1	1	1
18	1	0	0	1	0	1 8	0	0	0	1	1	0	0	0
19	1	0	0	1	1	1 9	0	0	0	1	1	0	0	1
20	1	0	1	0	0	2 0	0	0	1	0	0	0	0	0
21	1	0	1	0	1	2 1	0	0	1	0	0	0	0	1
22	1	0	1	1	0	2 2	0	0	1	0	0	0	1	0
23	1	0	1	1	1	2 3	0	0	1	0	0	0	1	1
24	1	1	0	0	0	2 4	0	0	1	0	0	1	0	0
25	1	1	0	0	1	2 5	0	0	1	0	0	1	0	1
26	1	1	0	1	0	2 6	0	0	1	0	0	1	1	0
27	1	1	0	1	1	2 7	0	0	1	0	0	1	1	1
28	1	1	1	0	0	2 8	0	0	1	0	1	0	0	0
29	1	1	1	0	1	2 9	0	0	1	0	1	0	0	1
30	1	1	1	1	0	3 0	0	0	1	1	0	0	0	0
31	1	1	1	1	1	3 1	0	0	1	1	0	0	0	1

**Q3.** Find the logic expressions for Z2, Y2, X2, W2, Z1, Y1, X1, W1 as function of C0, S3, S2, S1 and S0:

$$Z2 = \textcircled{0}$$

$$Y2 = \textcircled{0}$$

$$X2 = C_0(S_2 + S_3)$$

$$W2 = \overline{C_0} \overline{S_3} \overline{S_1} + \overline{C_0} \overline{S_3} \overline{S_2} + S_3 S_2 \overline{S_1} + C_0 \overline{S_3} \overline{S_2}$$

$$Z1 = \overline{C_0} S_3 \overline{S_2} \overline{S_1} + C_0 \overline{S_3} \overline{S_2} S_1 + C_0 S_3 S_2 \overline{S_1}$$

$$Y1 = \overline{C_0} \overline{S_3} S_2 + \overline{C_0} S_2 S_1 + C_0 \overline{S_2} \overline{S_1} + C_0 S_3 \overline{S_2}$$

$$X1 = \overline{C_0} \overline{S_3} S_1 + \overline{S_3} S_2 S_1 + \overline{C_0} S_3 S_2 \overline{S_1} + C_0 \overline{S_2} \overline{S_3} \overline{S_1} + C_0 S_3 \overline{S_2} S_1$$

$$W1 = S_0$$

- Q4. Write the verilog code for the Binary Coded Decimal Converter from Section 3.3 using the assign statement.

*Example:*

**module**

**input** ...

**output** ...

**assign** ...

**endmodule**

```
module bcd(C0, S3, S2, S1, S0, Z2, Y2, X2, W2, Z1, Y1, X1, W1);
    input C0, S3, S2, S1, S0;
    output Z2, Y2, X2, W2, Z1, Y1, X1, W1;
    assign Z2 = 0;
    assign Y2 = 0;
    assign X2 = (C0 & (S2 | S3));
    assign W2 = (~C0 & S3 & S1) | (~C0 & S3 & S2) | (S3 & S2 & S1) | (C0 & ~S3 & ~S1);
    assign Z1 = (~C0 & S3 & ~S2 & ~S1) | (C0 & ~S3 & ~S2 & S1) | (C0 & S3 & S2 & ~S1);
    assign Y1 = (~C0 & ~S3 & S2) | (~C0 & S2 & S1) | (C0 & ~S2 & ~S1) | (C0 & S3 & ~S2);
    assign X1 = (~C0 & ~S3 & S1) | (~S3 & S2 & S1) | (~C0 & S3 & S2 & ~S1) | (C0 & ~S2 & ~S3 & ~S1) |
        (C0 & S3 & ~S2 & S1);
    assign W1 = S0;
endmodule
```

TA Initials: AW

**LAB:**

Hardware demonstrates a good design. TA Initials: MS