CprE 281: Digital Logic
Midterm 2: Friday Oct 28, 2016

Student Name: **Student ID Number:**

Lab Section:	**Mon 9-12(N)**	**Mon 12-3(P)**	**Mon 5-8(R)**	**Tue 11-2(U)**
(circle one)	**Tue 2-5(M)**	**Wed 8-11(J)**	**Wed 6-9(T)**	**Thur 11-2(Q)**
	Thur 11-2(V)	**Thur 2-5(L)**	**Thur 5-8(K)**	**Fri 11-2(G)**

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name and student ID number. TRUE / (FALSE)

(b) When T=1 the output of a T flip-flop divides the frequency of the clock by 2. (TRUE) / FALSE

(c) Any Boolean function can be implemented using only 2-to-4 decoders. (TRUE) / FALSE

(d) The outputs of a code converter are one-hot encoded. TRUE / (FALSE)

(e) The select lines of an 8-to-1 multiplexer are one-hot encoded. TRUE / (FALSE)

(f) A D flip-flop can be implemented with only 6 NOR gates. (TRUE) / FALSE

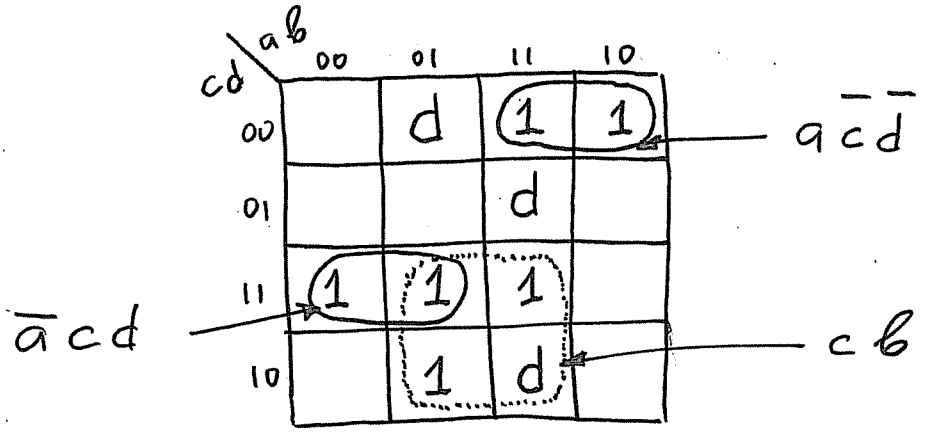
(g) In 2's complement notation: 0101 + 1101 = 0010. (TRUE) / FALSE

(h) In sign and magnitude notation: 0000 < 1000. TRUE / (FALSE)

(i) The total delay through a half-adder is 2 gate delays. TRUE / (FALSE)

(j) A D flip-flop can be implemented with a T flip-flop and one XOR gate. (TRUE) / FALSE

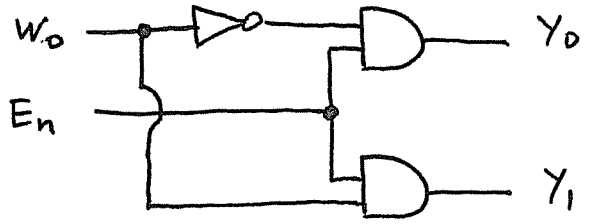
2. Minimization using a K-map (5p)
Draw the K-map for the function f(a,b,c,d) = Σ m(3,6,7,8,12,15) + D(4,13,14).
Then use the K-map to derive the minimized SOP expression for the function f.



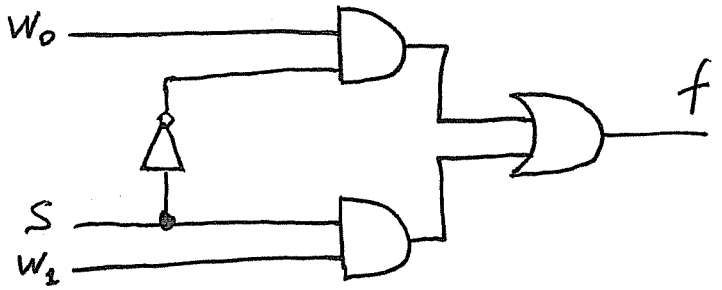
$$f = \bar{a}cd + a\bar{c}\bar{d} + cb$$

3. Basic Circuits (3p + 4p + 4p + 4p = 15p).
In all sub-problems, draw the complete wiring diagram using logic gates (no high-level graphical symbols allowed in this problem). Clearly label all inputs and outputs.

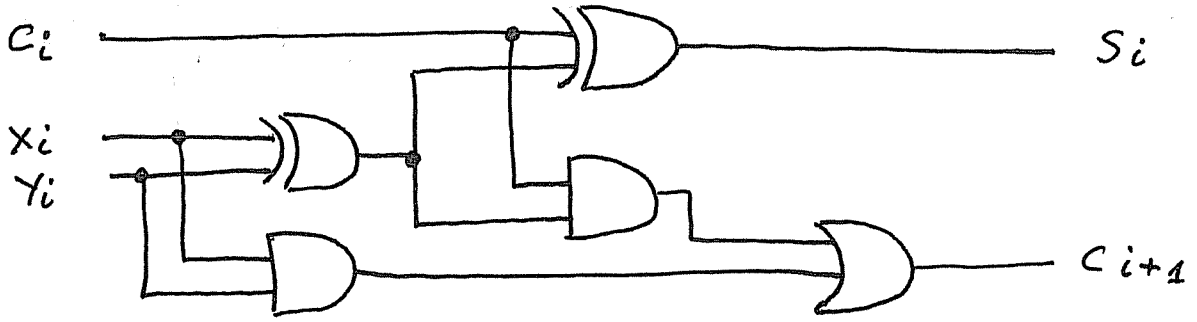
(a) 1-to-2 decoder with enable.



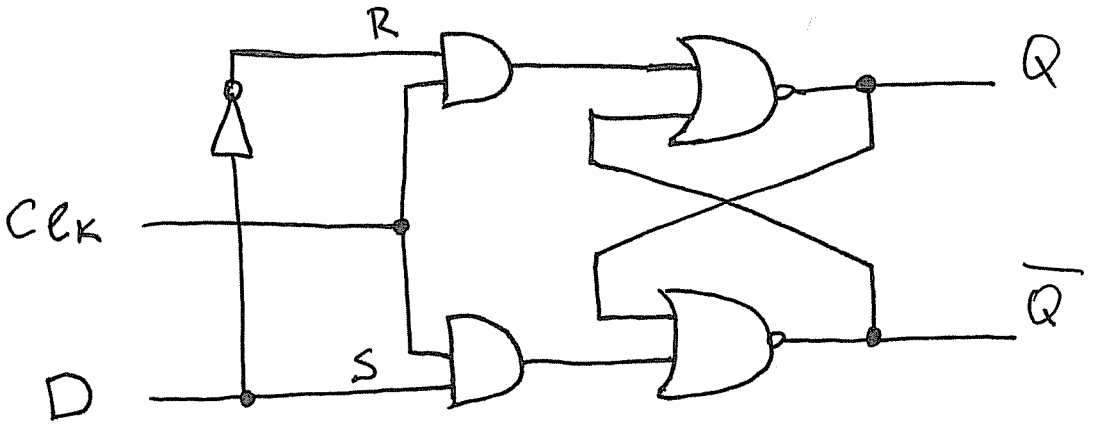
(b) 2-to-1 multiplexer.



(c) Full-adder



(d) Gated D Latch (with NOR gates for the latch).



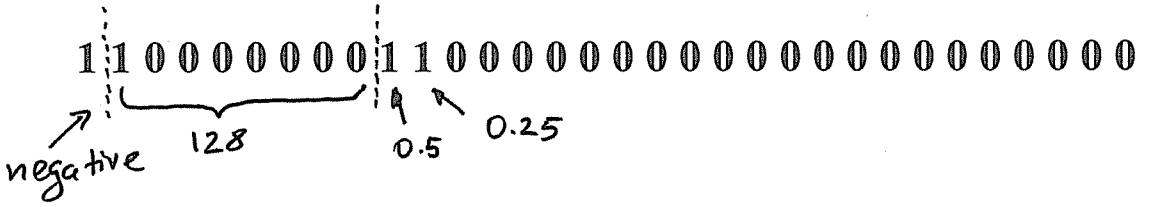
4. Number Conversions (3p + 4p + 4p + 4p = 15p)

(a) Convert 175_{10} to binary:

$$10101111_2 = 175_{10}$$

$175/2 = 87$ 1
$87/2 = 43$ 1
$43/2 = 21$ 1
$21/2 = 10$ 1
$10/2 = 5$ 0
$5/2 = 2$ 1
$2/2 = 1$ 0
$1/2 = 0$ 1

(b) Convert the following 32-bit float number (in IEEE 754 format) to decimal



$$(-1)^1 \times 2^{128-127} \times (1 + 0.5 + 0.25) = (-1) \times 2^1 \times 1.75 = -3.5$$

(c) Write down the 32-bit floating point representation (in IEEE 754 format) for 14.0

$14/8 = 1.75$

-8
60
-56
40
-40
0

$$(-1)^0 \times 2^3 \times 1.75 = (-1)^0 \times 2^{130-127} \times (1 + 0.5 + 0.25)$$

0 10000010 1100.....0

21 zeros

(d) Write down the 32-bit floating point representation (in IEEE 754 format) for -0.75

$$-1.5 \times \frac{1}{2} = -0.75 \Rightarrow (-1)^1 \times 2^{-1} \times (1 + 0.5)$$

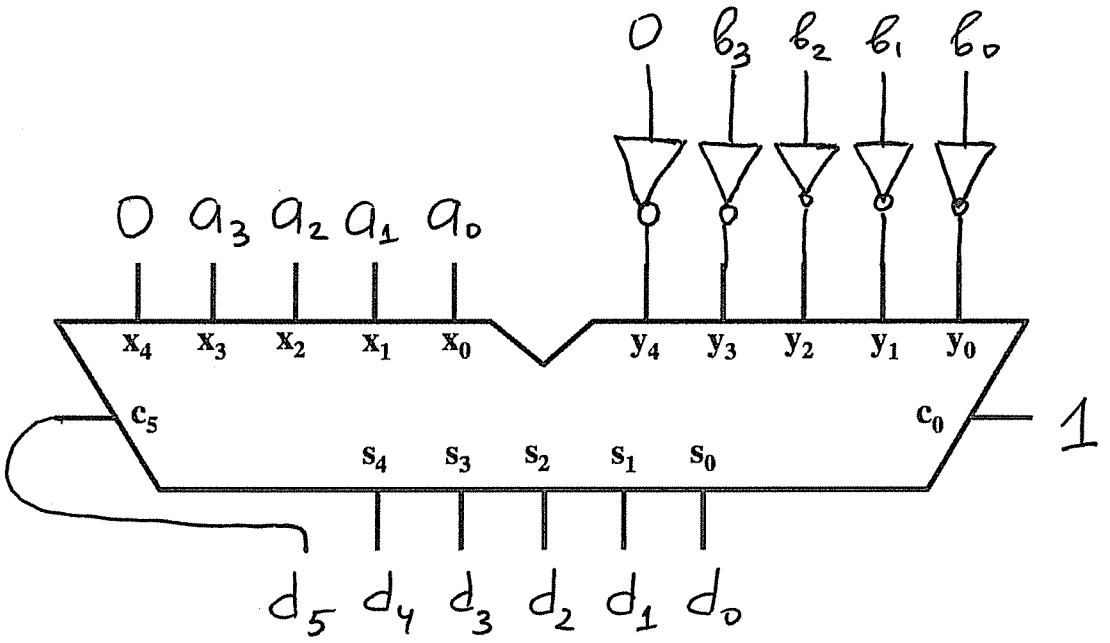
1 01111110 100.....0

22 zeros

5. Implementation Using an Adder (5p + 5p = 10p)

a) Let A=(a3, a2, a1, a0) and B=(b3, b2, b1, b0) be two 4-bit numbers. Draw a circuit that uses the 5-bit adder shown below and any other basic logic gates (ANDs, ORs, or NOTs) to compute the value of D, where D = A - B. Clearly label all inputs and outputs.

(5p)



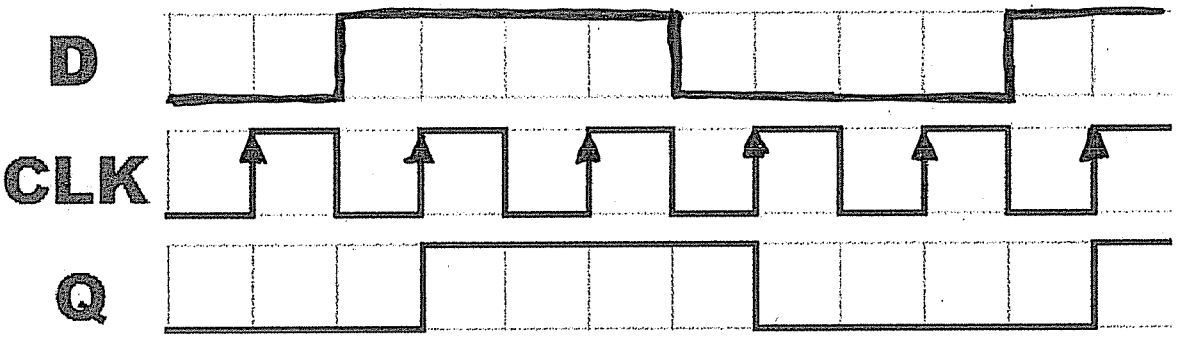
b) Explain your solution. **(5p)**

The subtraction is implemented as addition in 2's complement. Thus, we need to compute the 2's complement of B. This can be done by computing its 1's complement by inverting all bits and then adding 1. The inversion is performed by the NOT gates. The 1 is added as the C_0 carry bit of the adder. Because this is a 5-bit adder both A and B are padded with one zero on the left (most significant bit)

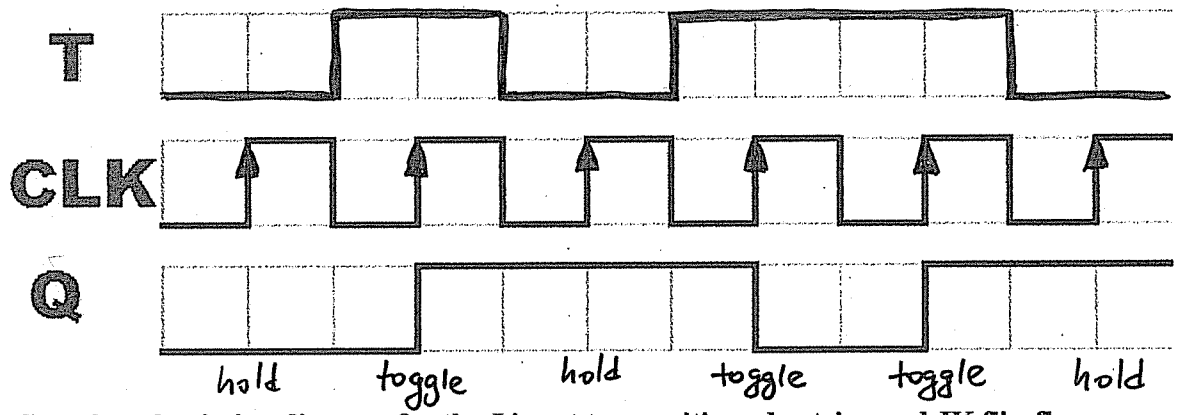
6. Flip-Flops and Timing Diagrams (3 x 5p = 15p)

Complete the timing diagram for the specified flip-flop such that the output Q will be as indicated. Assume that the input signal can change only on the vertical lines. Also, assume that the setup time t_{su} and the hold time t_h are each equal to the width of one square.

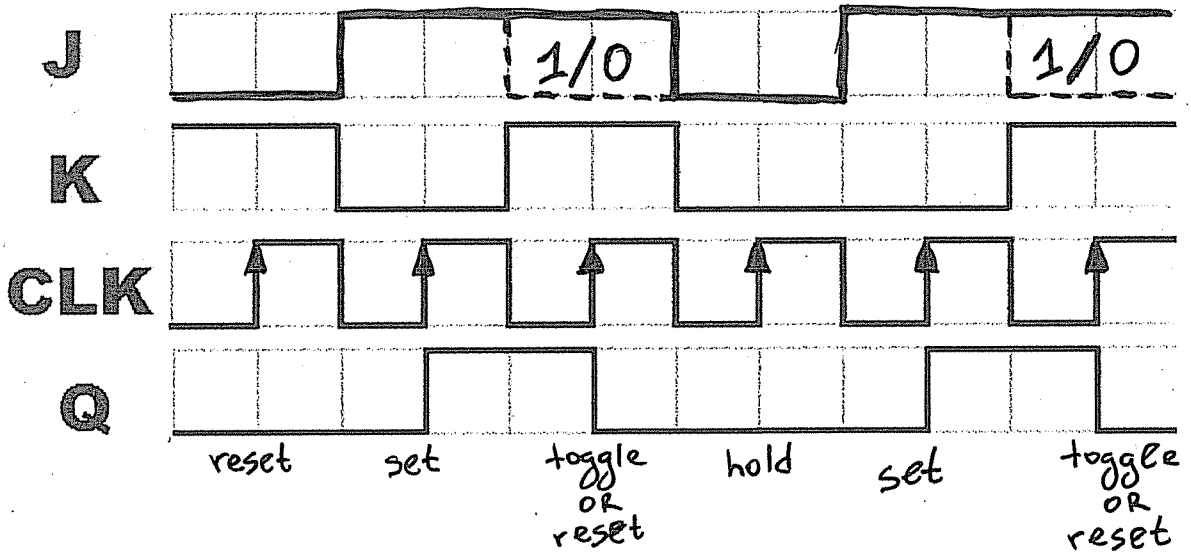
a) **Complete the timing diagram for the D input to a positive-edge triggered D flip-flop.**



b) **Complete the timing diagram for the T input to a positive-edge triggered T flip-flop.**



c) **Complete the timing diagram for the J input to a positive-edge triggered JK flip-flop.**

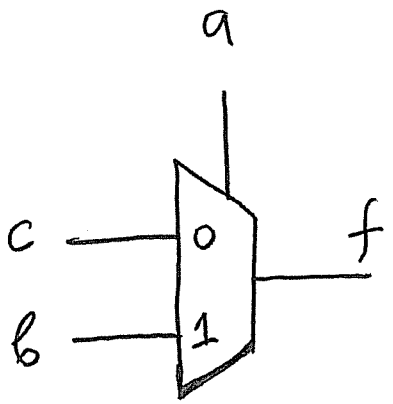


7. Multiplexers (2p + 8p = 10p)

a) Draw the truth table for the function $f = \bar{a}\,c + b\,c + a\,b$ **(2p)**

a	b	c	$\bar{a}c + bc + ab$	f	
0	0	0	0	0	c
0	0	1	1	1	
0	1	0	0	0	
0	1	1	1	1	
1	0	0	0	0	b
1	0	1	0	0	
1	1	0	0	1	
1	1	1	0	1	

b) Implement this function using <u>only</u> 2-to-1 multiplexers and <u>no other logic gates</u>. Assume that the signals a, b, and c are available <u>only</u> in their non-inverted form. (8p)

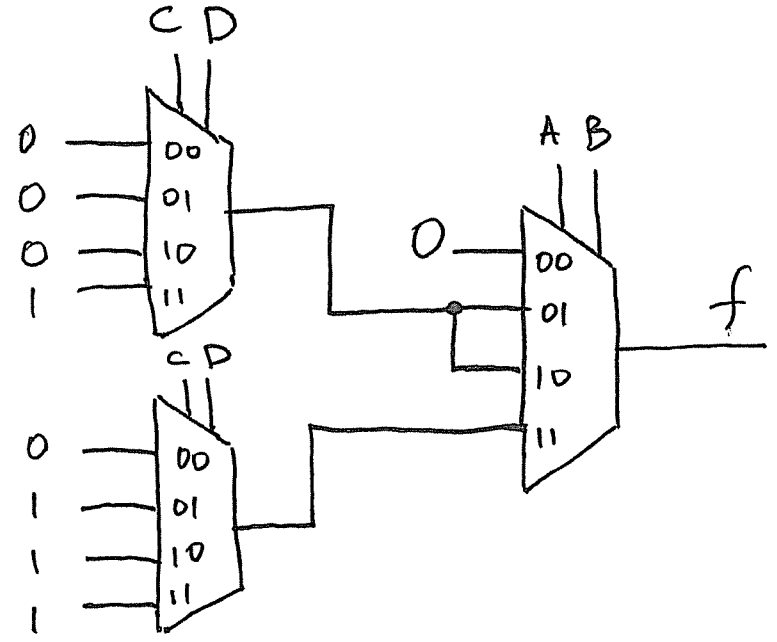


8. More Multiplexers (2p + 8p = 10p)

a) Draw the truth table for the function f = ABC + ABD + ACD + BCD. (2p)

b) Implement the function f using <u>only</u> 4-to-1 multiplexers and <u>no other logic gates</u>. You can assume that the variables are available in both inverted and non-inverted form. Clearly label all inputs, pins, and outputs of your circuit. (8p)

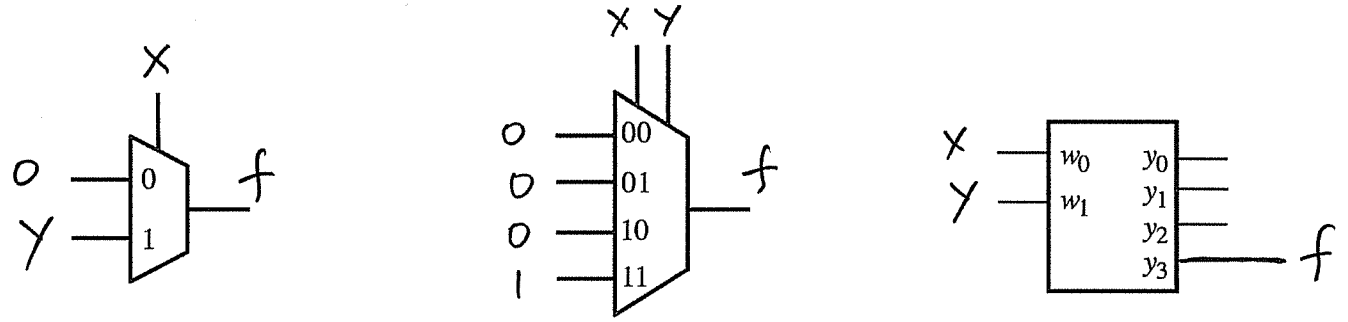
A	B	C	D	ABC	ABD	ACD	BCD	f	
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	
0	0	1	0	0	0	0	0	0	
0	0	1	1	0	0	0	0	0	
0	1	0	0	0	0	0	0	0	AND(C,D)
0	1	0	1	0	0	0	0	0	
0	1	1	0	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	
1	0	0	0	0	0	0	0	0	AND(C,D)
1	0	0	1	0	0	0	0	0	
1	0	1	0	0	0	0	0	0	
1	0	1	1	0	0	1	0	1	
1	1	0	0	0	0	0	0	0	OR(C,D)
1	1	0	1	0	1	0	0	1	
1	1	1	0	1	0	0	0	1	
1	1	1	1	1	1	1	1	1	



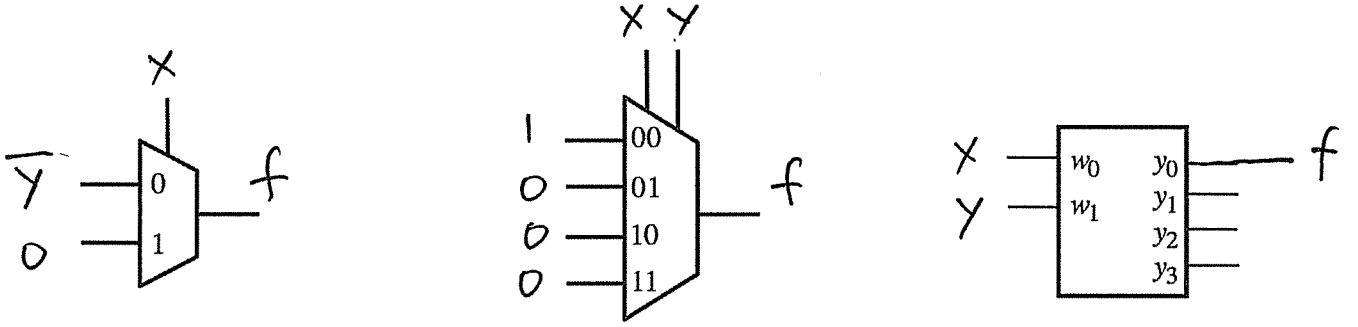
9. Alternative Implementation (10p)

Implement the logic gates AND, NOR, and NOT in three different ways: 1) using a 2-to-1 multiplexer; 2) using a 4-to-1 multiplexer; and 3) using a 2-to-4 decoder. In this problem you are <u>not allowed</u> to use any other logic gates. You can assume that both x and y available in their inverted and non-inverted form, along with the constants 0 and 1. If some implementation is not possible, then indicate that with words. <u>Label all inputs and outputs.</u>

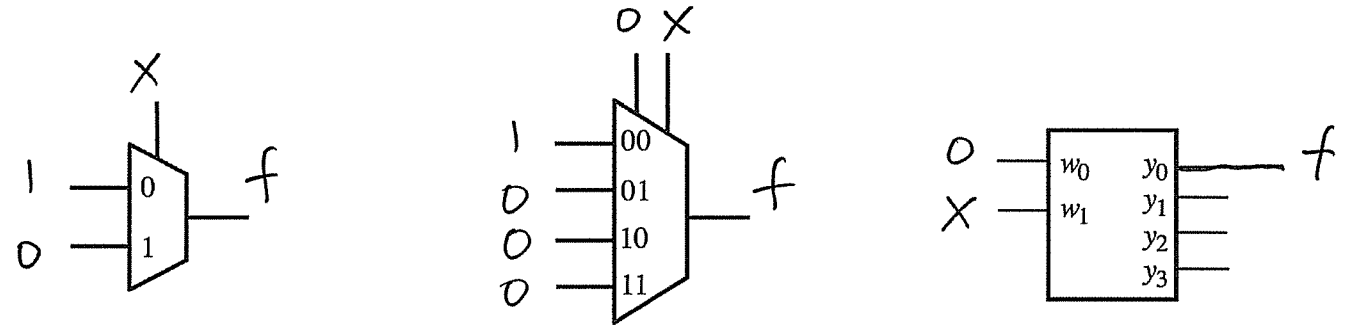
a) Implement in three different ways: f = AND(x, y).



b) Implement in three different ways: f = NOR(x, y).



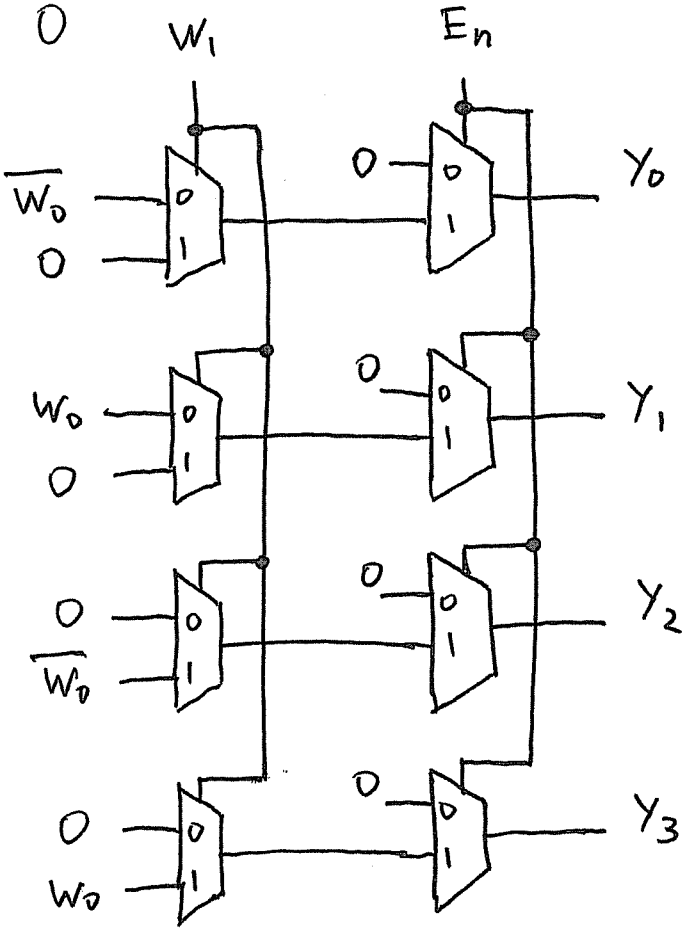
c) Implement in three different ways: f = NOT(x).



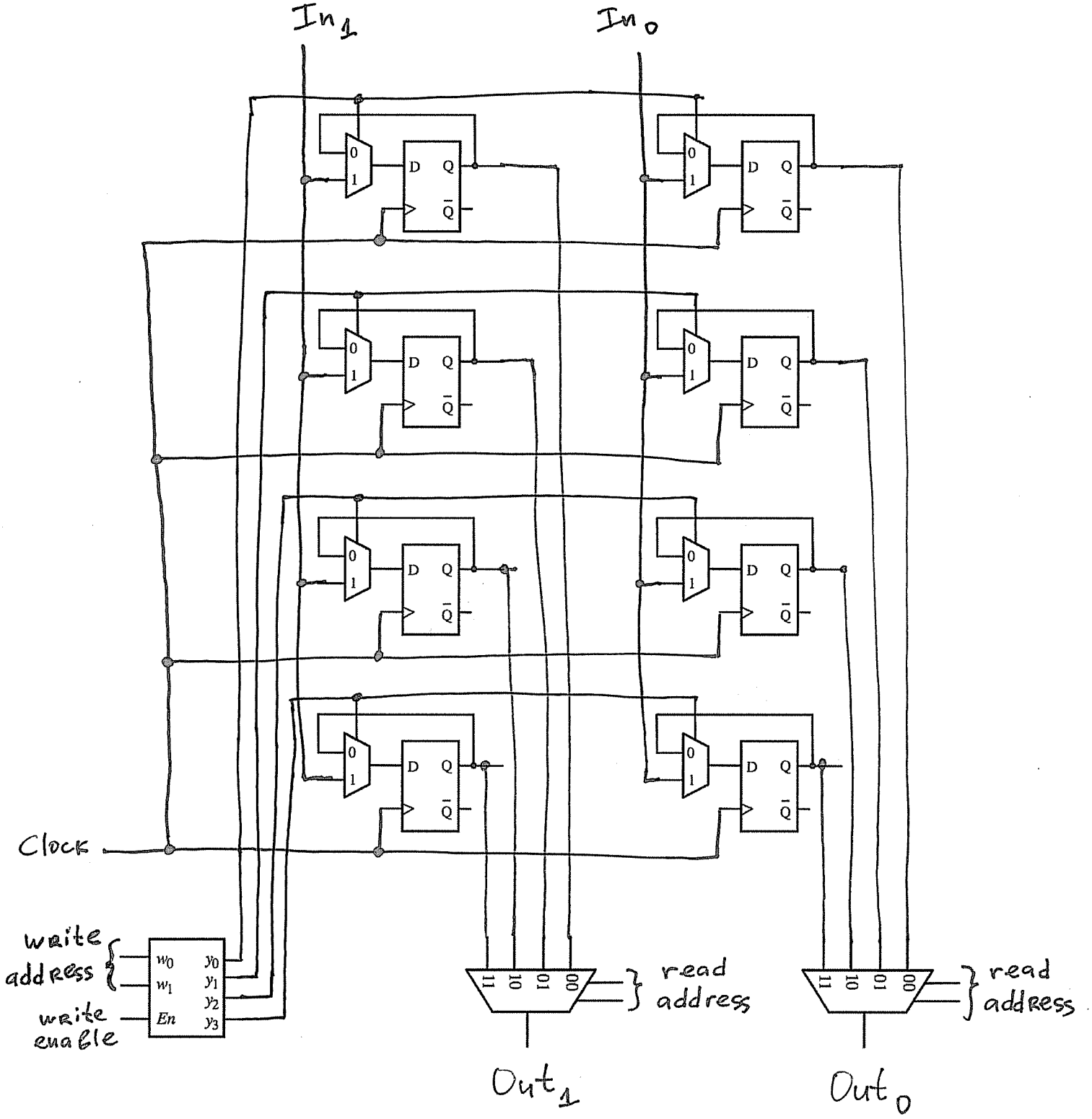
10. Decoder with Multiplexers (5p + 10p = 15p)

(a) Draw the full (i.e., non-abbreviated) truth table for a 2-to-4 decoder with enable.
(b) Implement a 2-to-4 decoder with enable <u>using only</u> 2-to-1 multiplexers and <u>no other</u> logic gates. You can assume that the input variables are available in their regular and inverted form, as well as the constants 0 and 1. Label all inputs, output, and pins of your circuit.

E_n	W_1	W_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0



11. Register File (15p)
Complete the following circuit diagram to implement a register file with four 2-bit registers, one write port, one read port, and one write enable line. Label all inputs and outputs.



Question	Max	Score
1. True/False	10	
2. K-Map Minimization	5	
3. Basic Circuits	15	
4. Number Conversions	15	
5. Adder Implementation	10	
6. Flip-Flops	15	
7. Multiplexers	10	
8. More Multiplexers	10	
9. Alternative Implementation	10	
10. Decoder with Multiplexers	15	
11. Register File	15	
TOTAL:	130	