Sample Solutions

CprE 281: Digital Logic
Midterm 1: Friday Sep 23, 2016

Student Name: **Student ID Number:**

Lab Section:	**Mon 9-12(N)**	**Mon 12-3(P)**	**Mon 5-8(R)**	**Tue 11-2(U)**
(circle one)	**Tue 2-5(M)**	**Wed 8-11(J)**	**Wed 6-9(T)**	**Thur 11-2(Q)**
	Thur 11-2(V)	**Thur 2-5(L)**	**Thur 5-8(K)**	**Fri 11-2(G)**

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name, student ID number, and lab section. TRUE / FALSE

(b) A 4-input AND gate can be implemented with two 2-input AND gates. TRUE / FALSE

(c) In Verilog, ~ has higher precedence than ^. TRUE / FALSE

(d) A 4-to-1 multiplexer has four select input lines and one output. TRUE / FALSE

(e) NOT followed by OR is equivalent to NOR. TRUE / FALSE

(f) Any Boolean function can be implemented using only NAND gates. TRUE / FALSE

(g) An XOR can be constructed with a 2-to-1 multiplexer and a NOT gate. TRUE / FALSE

(h) It is possible to build an OR gate with a 2-to-1 multiplexer. TRUE / FALSE

(i) $(a+b)\cdot(b+c)\cdot(\overline{a}+c) = (a+b)\cdot(\overline{a}+c)$ TRUE / FALSE

(j) In binary, Tatooine has 10 suns. TRUE / FALSE

2. Boolean Expressions (5 x 1p each = 5p)

Write the value (0 or 1) for each Boolean expression, given the initial conditions.

A = 0, B = 1, C = 0, D = 1

(a) $(AD + \overline{BC} + BD)$ 1

(b) $(AC + BC)(BD + CD + 1)$ 0

(c) $(A + B)D$ 1

(d) $(A + B + C + 1)(\overline{A}CD)$ 0

(e) $(AA + BC + D)\overline{C}$ 1

3.Truth Tables (5p + 5p = 10p)

(a) Draw the truth table for the following Boolean function:

$$f(a,b,c) = \underbrace{(a + bc + \bar{b}\,\bar{c})}_{\text{Term 1}}\ \underbrace{(\overline{a\,b\,\bar{c}})}_{\text{Term 2}}$$

a	b	c	a	+ bc	+ $\bar{b} \cdot \bar{c}$	Term 1	ab	$\cdot\ \bar{c}$	Term 2	f
0	0	0	0	0	1	1	0	1	1	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	1	0
0	1	1	0	1	0	1	0	0	1	1
1	0	0	1	0	1	1	0	1	1	1
1	0	1	1	0	0	1	0	0	1	1
1	1	0	1	0	0	1	1	1	0	0
1	1	1	1	1	0	1	1	0	1	1

(b) Draw the truth table for the function f that has the following K-map:

z \ xy	00	01	11	10
0	0	1	0	1
1	0	1	1	1

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

4. Number Conversions (5 x 4p each = 20p)

(a) Convert 42_{10} to binary

$42/2 = 21 \quad 0$
$21/2 = 10 \quad 1$
$10/2 = 5 \quad 0$
$5/2 = 2 \quad 1$
$2/2 = 1 \quad 0$
$1/2 = 0 \quad 1$

$101010_2 = 42_{10}$

(b) Convert 214_5 to binary

$2 \times 5^2 + 1 \times 5^1 + 4 \times 5^0 = 2 \times 25 + 1 \times 5 + 4 \times 1 = 50 + 5 + 4 = 59_{10}$

$59/2 = 29 \quad 1$
$29/2 = 14 \quad 1$
$14/2 = 7 \quad 0$
$7/2 = 3 \quad 1$
$3/2 = 1 \quad 1$
$1/2 = 0 \quad 1$

$111011_2 = 214_5$

(c) Convert 213_4 to hexadecimal:

10 01 11 => $\overbrace{00}^{\text{padding}}$10 0111 => $213_4 = 27_{16}$

$\underbrace{0010}_{2}\ \underbrace{0111}_{7}$

Convert to binary and then group by 4's. Also, pad the two most significant bits with zeros.

(d) Convert $BB8_{16}$ to octal

1011 1011 1000 => $\underbrace{101}_{5}\ \underbrace{110}_{6}\ \underbrace{111}_{7}\ \underbrace{000}_{0}$

$BB8_{16} = 5670_8$

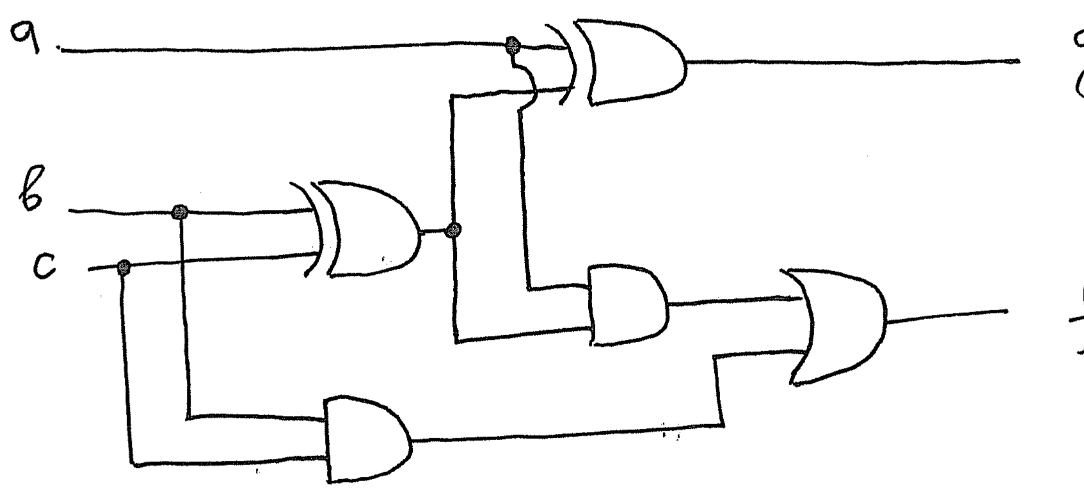
(e) Convert 10010110_2 to decimal

$1 \times 2^7 + 1 \times 2^4 + 1 \times 2^2 + 1 \times 2^1 = 128 + 16 + 4 + 2 = 150_{10}$

5. From Verilog Code to Logic Circuit (10p)

Draw the logic circuit that is described by the following Verilog module:

```
module FG (a, b, c, f, g);
    input a, b, c;
    output f, g;
                                         &
    assign f = ((b ^ c) & a) | (b c);
    assign g = a ^ (b ^ c);
endmodule
```



6. Minimization (3 x 5p = 15p)

(a) Draw the K-map that corresponds to the following Boolean function:

$$f = a\,b\,\bar{c} + b\,\bar{c}\,\bar{d} + c\,d + \bar{a}\,b$$

$a b \bar{c}$

$b\bar{c}\bar{d}$

cd \ ab	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	1	1	1
10	0	1	0	0

cd

$\bar{a}b$

(b) Redraw the K-map from (a) and derive the minimum-cost Sum-of-Products (<u>SOP</u>) expression for f.

$$f = \bar{a}b + cd + \bar{c}b$$

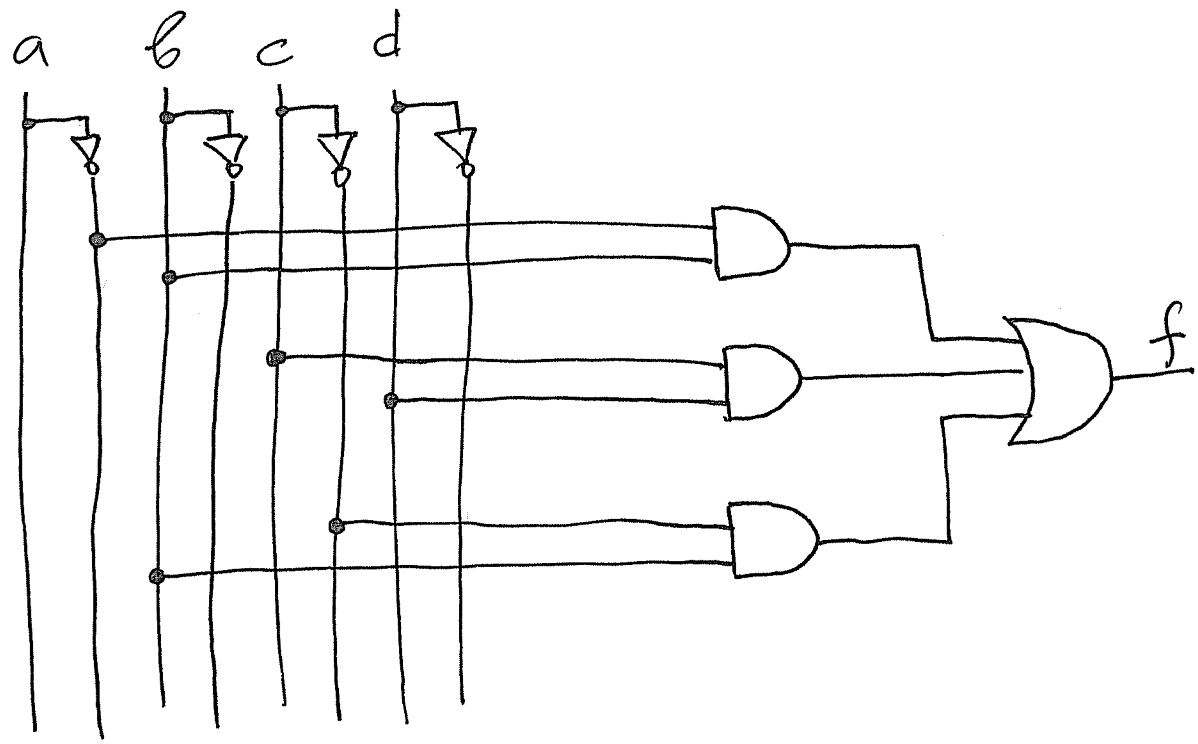
$\bar{c}b$

cd \ ab	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	1	1	1
10	0	1	0	0

cd

$\bar{a}b$

(c) Draw the circuit for the minimum <u>SOP</u> expression. Label all inputs and outputs.



7. Derive the minimum POS expression using a K-map (10p + 5p = 15p)

(a) Use a K-map to derive the minimum-cost POS expression for the following function

$$f(a,b,c,d)=\Sigma m(1, 5, 7, 8, 10, 11, 14) + D(2, 3, 12, 13)$$

cd \ ab	00	01	11	10
00	0	0	d	1
01	1	1	d	0
11	d	1	0	1
10	d	0	1	1

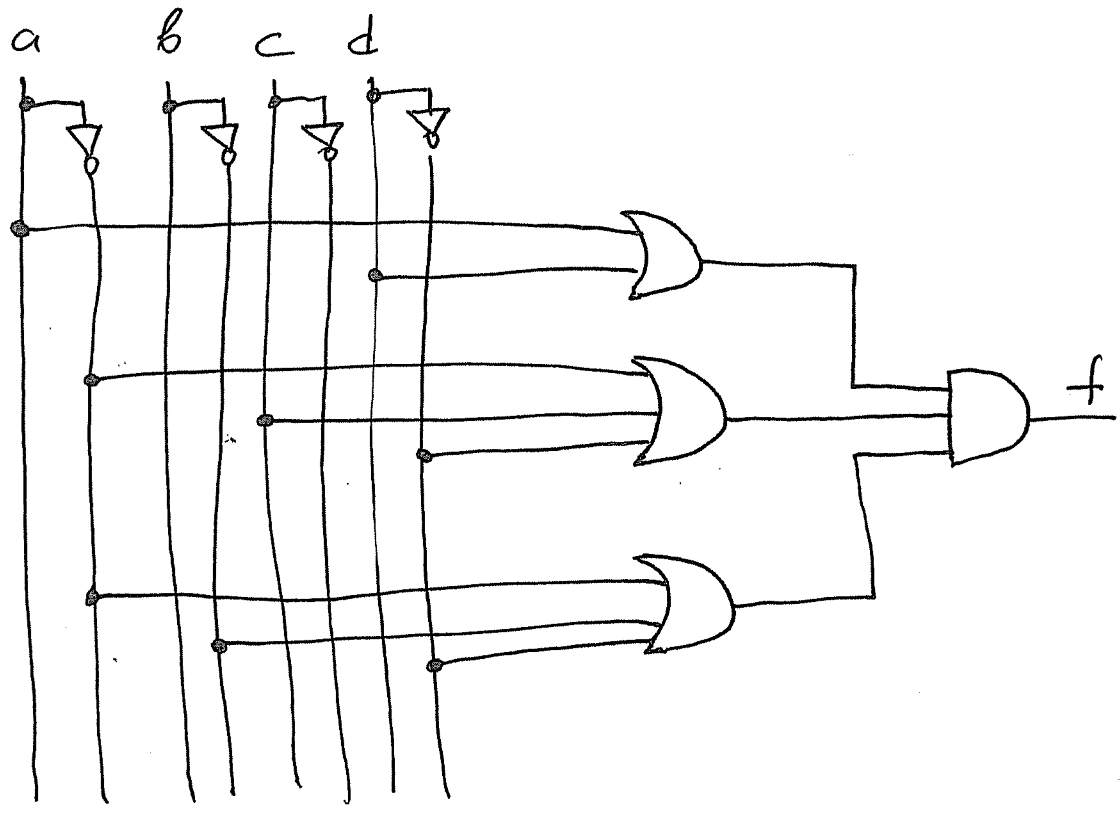
$(a + d)$

$(\bar{a} + c + \bar{d})$

$(\bar{a} + \bar{b} + \bar{d})$

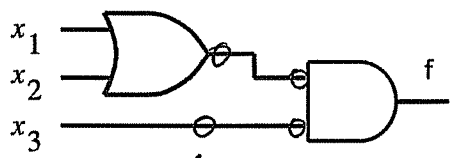
$$f = (a+d)(\bar{a}+c+\bar{d})(\bar{a}+\bar{b}+\bar{d})$$

(b) Draw the circuit diagram for the minimum-cost Product-Of-Sums (POS) expression

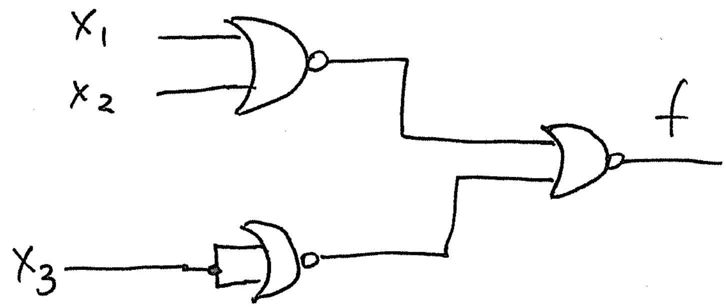


8. NAND/NOR Logic (3 x 5p = 15p)

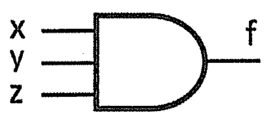
(a) Redraw the following logic circuit using only NOR gates.



need to add a NOT gate here

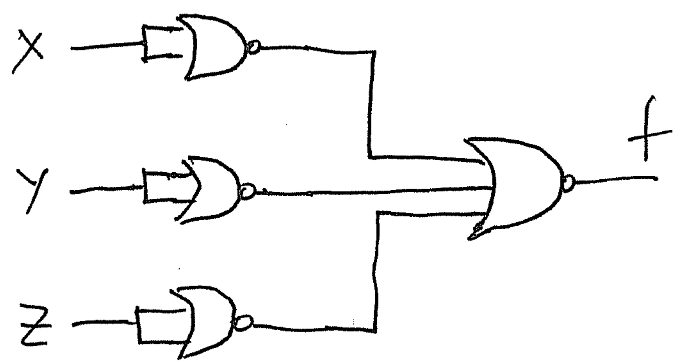


(b) Redraw the following logic circuit using only NOR gates.

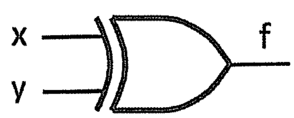


$$f = XYZ = \overline{\overline{XYZ}}$$

$$= \overline{\overline{X} + \overline{Y} + \overline{Z}}$$

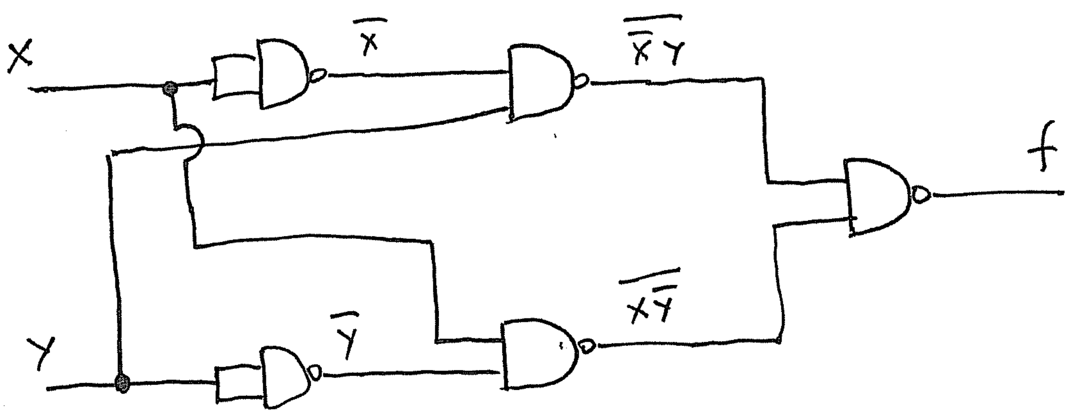


(c) Redraw the following logic circuit using only NAND gates.



$$f = \overline{X}Y + X\overline{Y} = \overline{\overline{\overline{X}Y + X\overline{Y}}}$$

$$= \overline{\overline{\overline{X}Y} \cdot \overline{X\overline{Y}}}$$



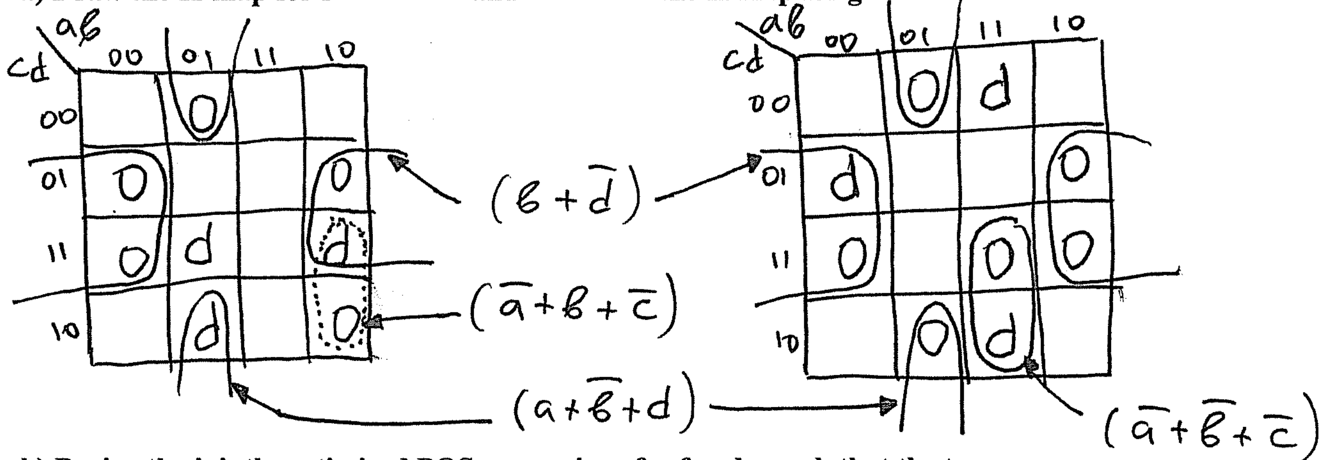
$$f = \overline{\overline{\overline{X}Y} \cdot \overline{X\overline{Y}}}$$

9. Joint Optimization (3 x 5p = 15p)
The outputs f and g of a two-output circuit are specified with the following expressions:

$f(a, b, c, d) = \prod M(1, 3, 4, 9, 10) + D(6, 7, 11)$

$g(a, b, c, d) = \prod M(3, 4, 6, 9, 11, 15) + D(1, 12, 14)$

a) Draw the K-map for f and the K-map for g

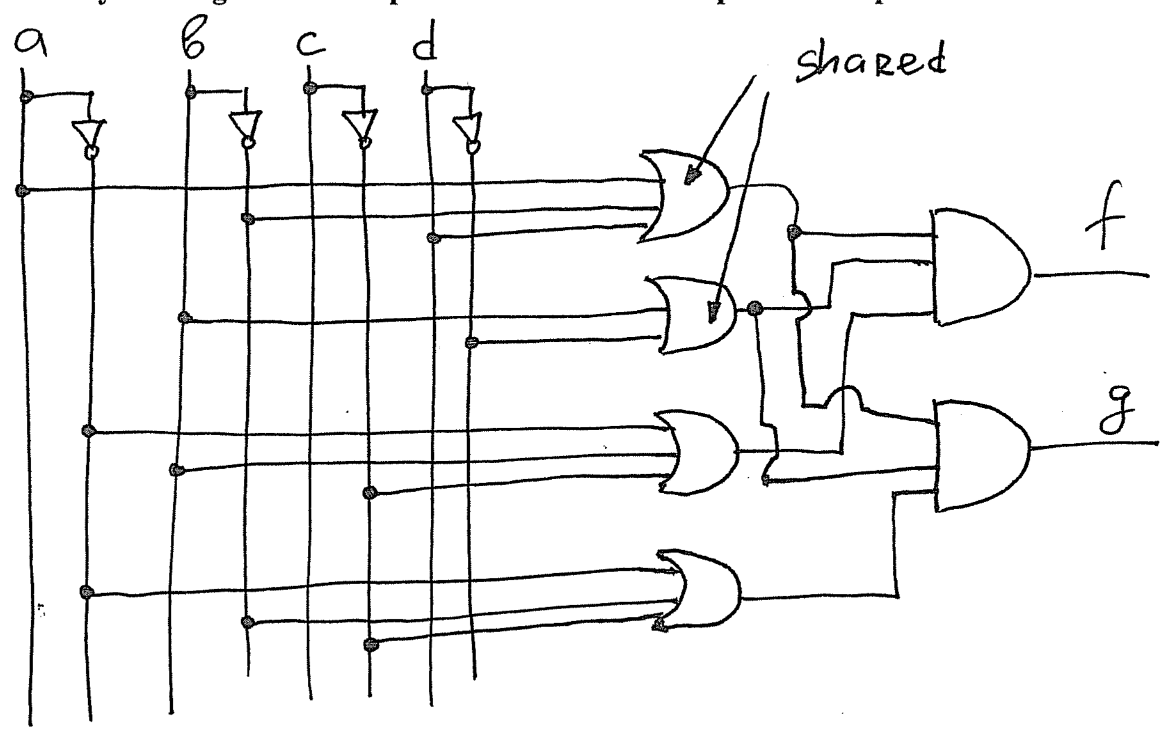


b) Derive the jointly optimized POS expressions for f and g such that the two expressions share two implicants. Note that these are not necessarily prime implicants.

$$f = (a+\bar{b}+d)(b+\bar{d})(\bar{a}+b+\bar{c})$$

$$g = (a+\bar{b}+d)(b+\bar{d})(\bar{a}+\bar{b}+\bar{c})$$

c) Draw the diagram for the jointly optimized circuit. Indicate which logic gates are shared by drawing arrows that point to them. Label all inputs and outputs.



10. DeMorgan's Theorem (15p)

Use the theorems of Boolean algebra to prove DeMorgan's theorem for four variables. In other words, prove that

$$\overline{\underbrace{a+b}_{x}+\underbrace{c+d}_{y}} = \overline{a}\cdot\overline{b}\cdot\overline{c}\cdot\overline{d}$$

Let x and y be two Boolean variables such that $x = a+b$ and $y = c+d$. Then, the left-hand side can be expressed as follows:

$$\overline{x+y} = \overline{x}\cdot\overline{y}$$

This derivation uses De Morgan's theorem for two variables, which is one of the fundamental theorems. Now, expand x and y and apply De Morgan's theorem for two variables twice, i.e.,

$$\overline{x+y} = \overline{x}\cdot\overline{y} = \overline{a+b}\cdot\overline{c+d} = \overline{a}\cdot\overline{b}\cdot\overline{c}\cdot\overline{d}.$$

Therefore,

$$\overline{a+b+c+d} = \overline{a}\cdot\overline{b}\cdot\overline{c}\cdot\overline{d}.$$

Question	Max	Score
1. True/False	10	
2. Boolean Expressions	5	
3. Truth Tables	10	
4. Number Conversions	20	
5. Verilog Module	10	
6. Minimization	15	
7. POS with K-Map	15	
8. NAND/NOR Logic	15	
9. Joint Optimization	15	
10. DeMorgan's	15	
TOTAL:	130	