Cpr E 281 HW09 SOLUTION

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Eleventh Week
Due Date: Monday, Nov. 7, 2016

P1. (15 points)

To construct a register file containing *eight* 16-bit registers, two input ports and three output ports, we use ***w*** number of 16-bit registers with parallel load input, ***x*** number of ***y***-to-1 ***z***-bit multiplexers, and ***p*** number of ***q***-to-***r*** decoders with enable. Specify the values of ***w***, ***x***, ***y***, ***z***, ***p***, ***q***, and ***r***. (2 points for each variable)

Solution:

$w = 8$ (8 registers)

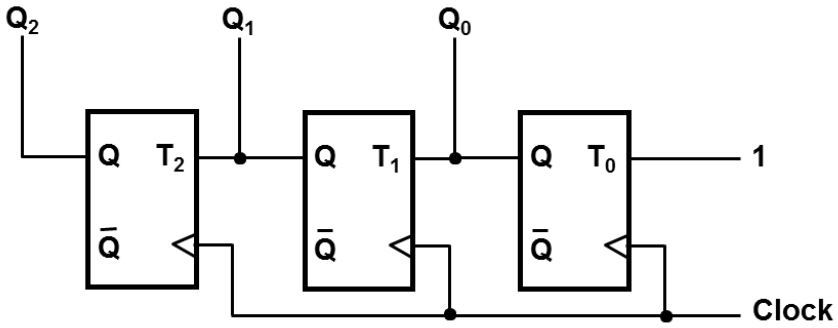
$x = 3$, $y = 8$, $z = 16$ (three output ports for read: 3 8-to-1 16-bit multiplexers)

$p = 2$, $q = 3$, $r = 8$ (two input ports for write: 2 3-to-8 decoders)

P2. (10 points)

What is the counting sequence of the following counter?

Assume the counter starts from $Q_2Q_1Q_0 = 000$.



Solution:

$T_2T_1T_0$:	xxx	→	001	→	011	→	101	→	111	→	001
$Q_2Q_1Q_0$:	000	→	001	→	010	→	111	→	000	→	001

The counting sequence for $Q_2Q_1Q_0$ is: 000→001→010→111 (→000 and repeat).

P3. (20 points)

Answer the following questions for the counters.

a) (5 points) Draw a circuit for a 4-bit asynchronous up-counter using T flip-flops.

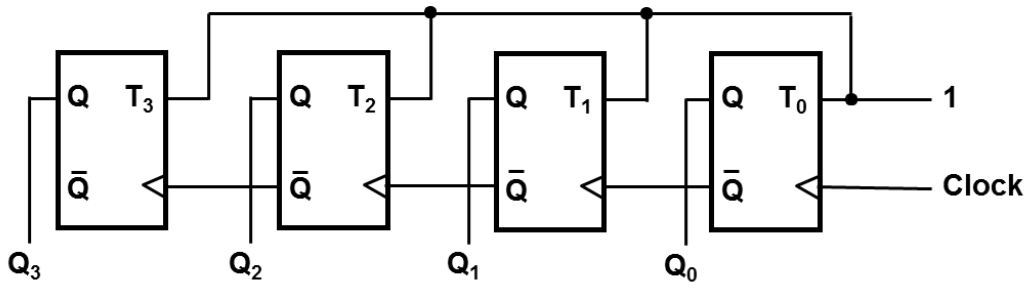
b) (5 points) Draw a circuit for a 4-bit synchronous up-counter using T flip-flops.

c) (5 points) Let $Q_n \ldots Q_2 Q_1 Q_0$ be the bits that represent the count value of an asynchronous counter. What could happen if n is increased?

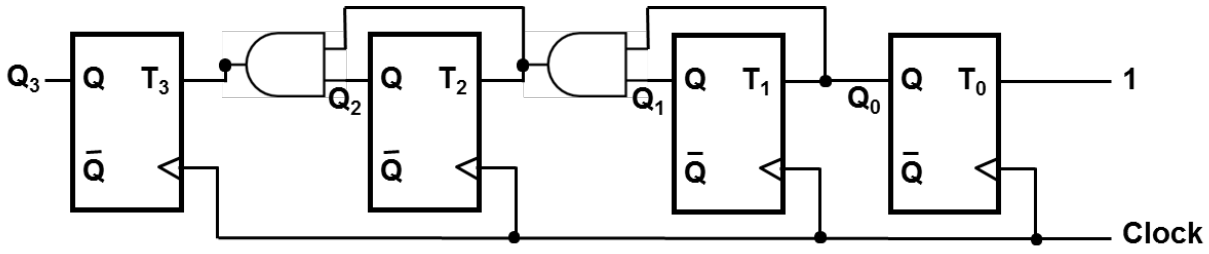
d) (5 points) Could you think of one possible reason that a designer may choose to implement an asynchronous counter over a synchronous counter?

Solution:

a) Asynchronous counter:



b) Synchronous counter:



c) The propagation delays get larger due to cascaded clocking.

d) 1. When only a small amount of bits was constructed (smaller propagation delays).
2. When area is more critical than circuit delays (synchronous counter needs more gates).

P4. (10 points)

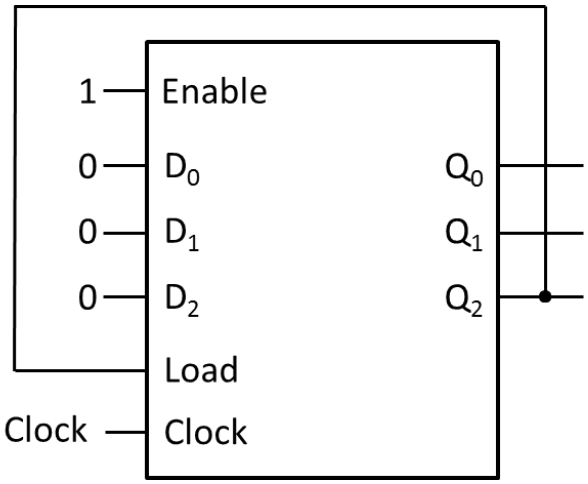
Figure 5.25 in textbook shows the design of a modulo-6 counter with reset synchronization. Could you modify the circuit and make it a modulo-5 counter instead?

Solution:

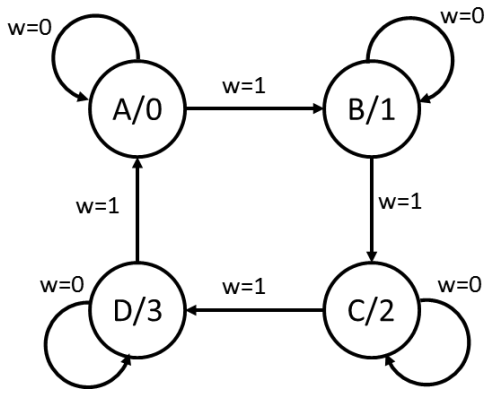
The counting sequence of a modulo-5 counter should be:

000→001→010→011→100→000

Therefore, the counter resets to 000 whenever $Q_2 = 1$.



P5. (25 points) Consider a FSM with the following state diagram:



a) (5 points) Complete the following state table based on the state diagram.
b) (5 points) Encode each state and outputs in (a) with binary numbers to build the following state-assigned table.
c) (5 points) Derive the minimal logic expressions for Y_1, Y_0, z_1, and z_0.
d) (5 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates that are required.
e) (5 points) What does this FSM do? What happens when w=0 and w=1?

Solution:

a)

Present State	Next State		Output
	w=0	w=1	
A	A	B	0
B	**B**	**C**	**1**
C	**C**	**D**	**2**
D	**D**	**A**	**3**

b)

Present State y_1y_0	Next State w=0 Y_1Y_0	Next State w=1 Y_1Y_0	Output z_1z_0
00	**00**	**01**	**00**
01	**01**	**10**	**01**
10	**10**	**11**	**10**
11	**11**	**00**	**11**

c)

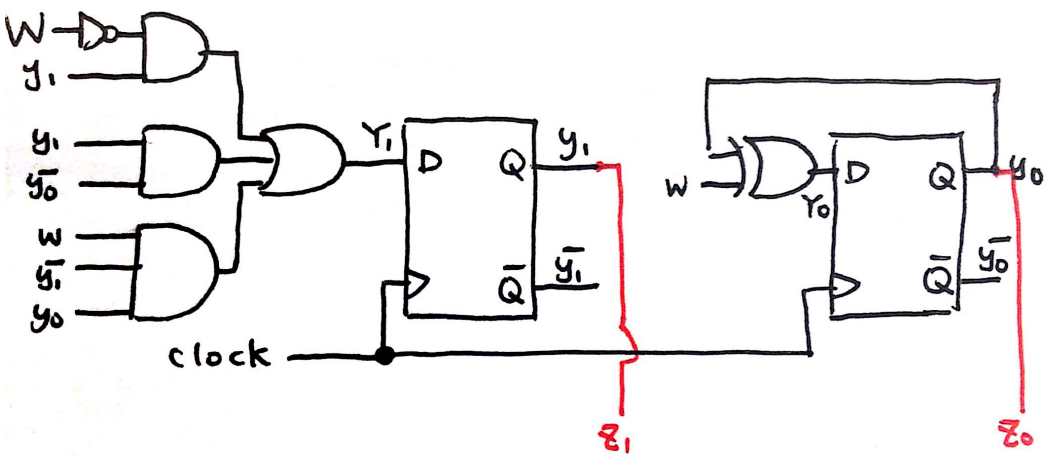
$$Y_1 = \overline{w}y_1 + y_1\overline{y_0} + w\overline{y_1}y_0$$

$$Y_0 = \overline{w}y_0 + w\overline{y_0}$$

$$z_1 = y_1$$

$$z_0 = y_0$$

d)



e) It's a 2-bit up-counter. When w=1, it starts counting. When w=0, it stops counting.

P6. (20 points)

Design a 2-bit counter controlled by an input w. When w=0, it acts as a down-counter. When w=1, it acts as an up-counter. The output shows the current value of counter.

a) (5 points) Draw the state diagram for this counter.

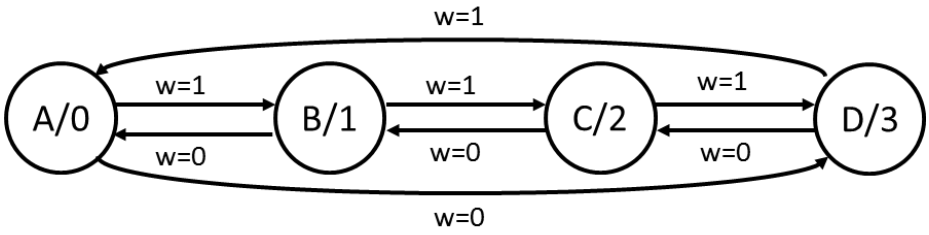
b) (5 points) Derive the state-assigned table for this counter. Each state and output should be encoded with binary numbers.

c) (5 points) Derive the minimal logic expressions for Y_1, Y_0, z_1, and z_0.

d) (5 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates that are required.

Solution:

a)



b)

Present State y_1y_0	Next State w=0 Y_1Y_0	Next State w=1 Y_1Y_0	Output z_1z_0
(A) 00	**11**	**01**	**00**
(B) 01	**00**	**10**	**01**
(C) 10	**01**	**11**	**10**
(D) 11	**10**	**00**	**11**

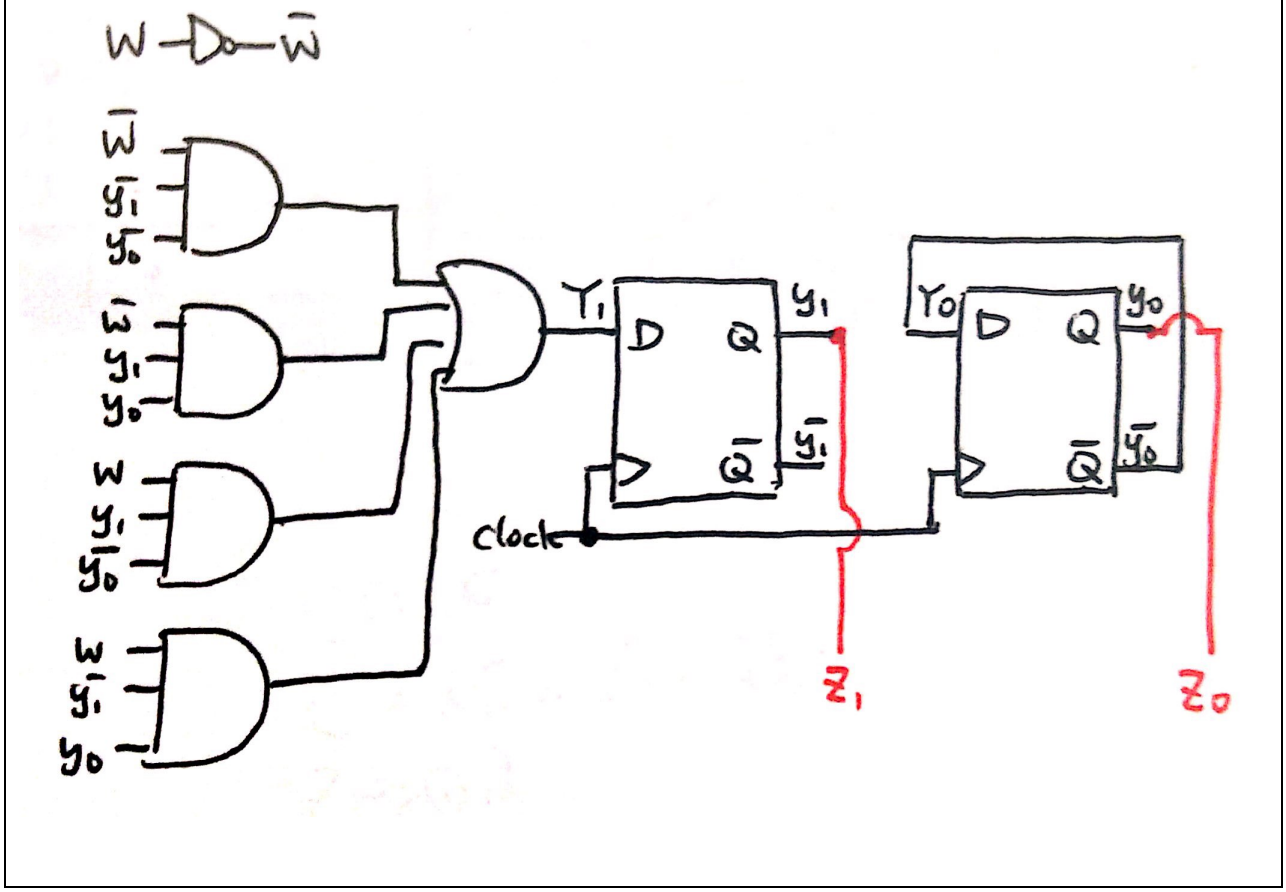
c) $Y_1 = \overline{w}\overline{y_1}\overline{y_0} + \overline{w}y_1y_0 + w\overline{y_1}\overline{y_0} + wy_1\overline{y_0}$

$Y_0 = \overline{y_0}$

$z_1 = y_1$

$z_0 = y_0$

d)


W
D
$\bar{W}$
$\bar{W}$
y_1
y_0
$\bar{W}$
y_1
y_0
W
y_1
$\bar{y}_0$
W
$\bar{y}_1$
y_0
Y_1
D
Q
$\bar{Q}$
y_1
$\bar{y}_1$
Y_0
D
Q
$\bar{Q}$
y_0
$\bar{y}_0$
clock
Z_1
Z_0