Cpr E 281 HW08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Flip-Flops, Registers, and Counters
Assigned Date: Ninth Week
Due Date: Wednesday, Oct. 24, 2016

P1. (10 points)

Consider a basic SR latch with inputs S, R, and outputs Q_a, Q_b. (Figure 5.4 in textbook)

a) (5 points) What would happen to Q_a and Q_b if S=R=1?

b) (5 points) What would happen to Q_a and Q_b if we transit from S=R=1 to S=R=0?

Solution:

a)

S=R=1 will cause $Q_a = Q_b = 0$.

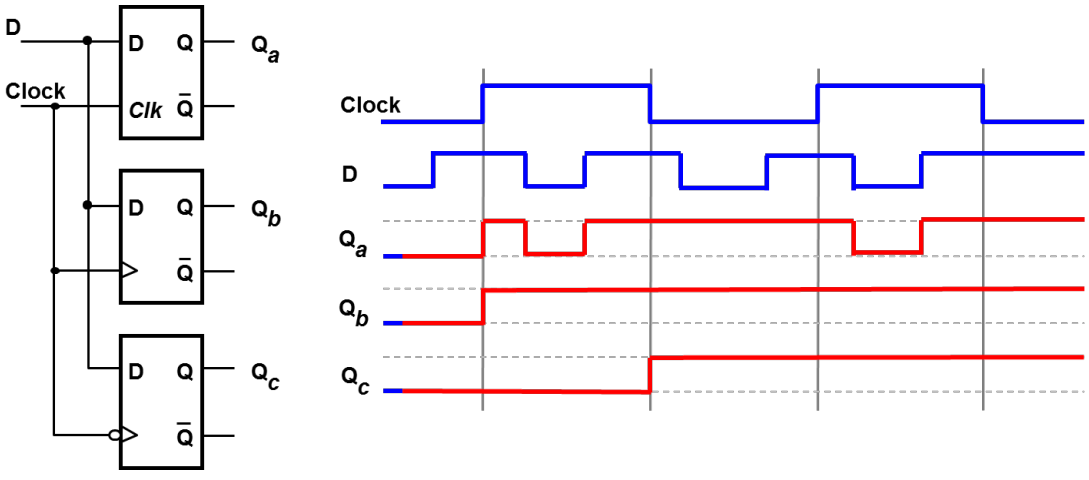
b)

Oscillation will occur. When S=R=1, we have $Q_a = Q_b = 0$. If the next transition is S=R=0, we have $Q_a = Q_b = 1$, which immediately sets $Q_a = Q_b = 0$, and so on.

P2. (15 points)

Complete the following timing diagram for Q_a, Q_b, and Q_c, which are the outputs of a gated D latch, a positive edge-triggered D flip-flop, and a negative edge-triggered D flip-flop. Assume $Q = 0$ initially and no gate delays. (5 points each)

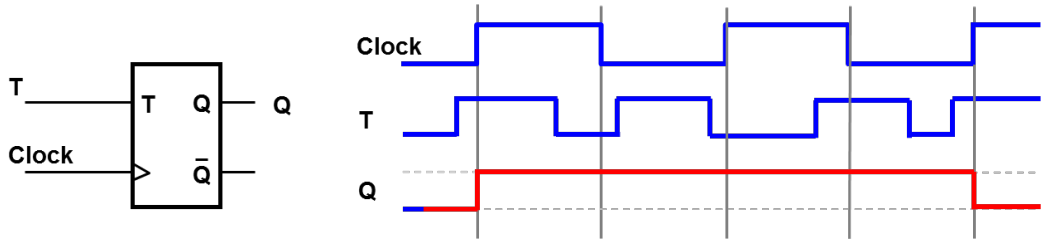
Solution:



P3. (10 points)

Complete the following timing diagram for a T flip-flop. Assume no gate delays.

Solution:



P4. (10 points)

The following truth table can be used to construct a T flip-flop using a D flip-flop.

T	Output		D
	Q(t)	Q(t+1)	
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

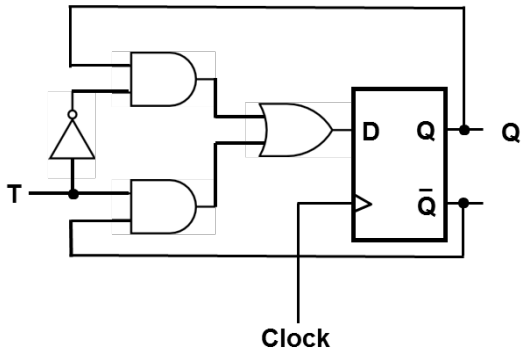
a) (5 points) Write down the simplified SOP expression of D using T and Q(t) for inputs.

b) (5 points) Draw the circuit for a T flip-flop using a D flip-flop and other necessary gates. Make sure you connect the flip-flop to a clock signal.

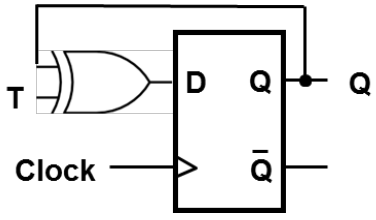
Solution:

a) $D = T'Q(t) + TQ'(t)$

b)



OR



P5. (20 points)

Construct a JK flip-flop using a T flip-flop.

a) (10 points) Complete the following truth table.

b) (5 points) Write down the simplified SOP expression of T using J, K, and Q(t) for inputs.

c) (5 points) Draw the circuit for a JK flip-flop using a T flip-flop and other necessary gates. Make sure you connect the flip-flop to a clock signal.

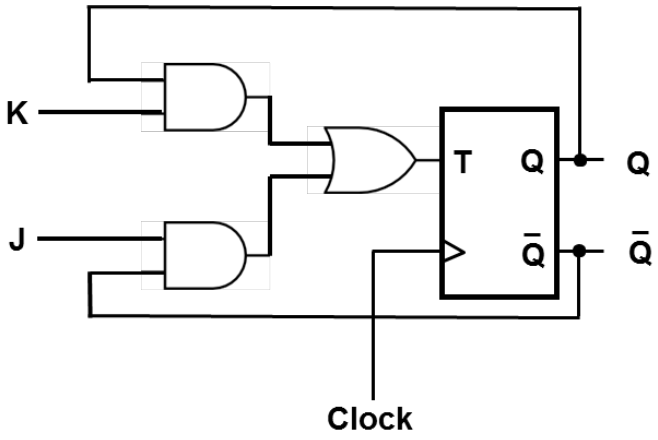
Solution:

a)

J	K	Output		T
		Q(t)	Q(t+1)	
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

b) $T = JQ'(t) + KQ(t)$

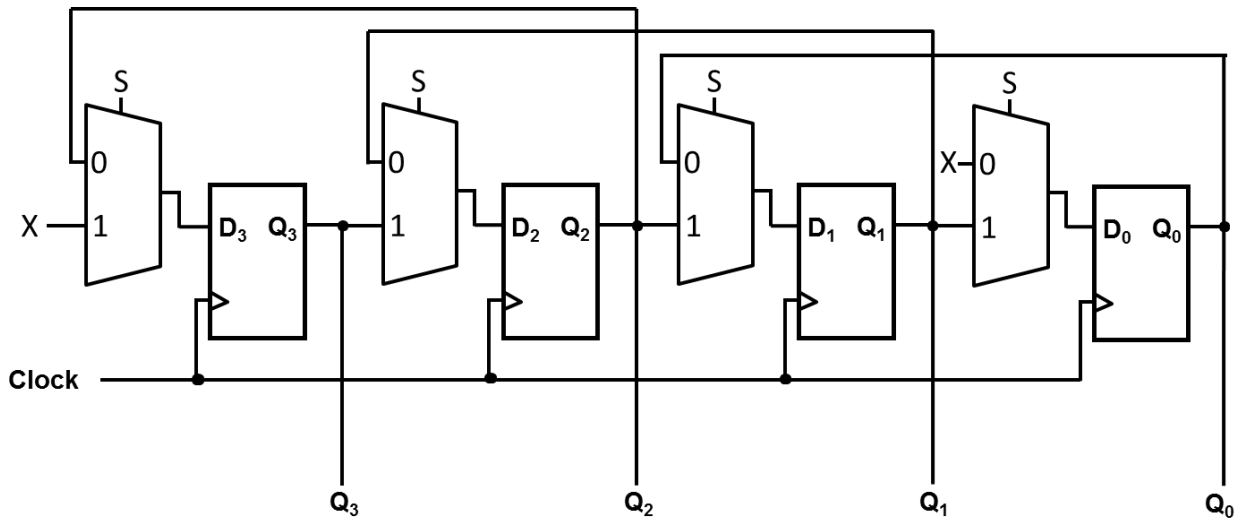
c)



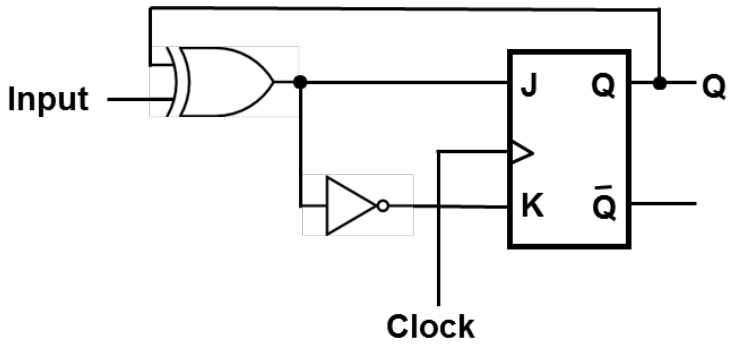
P6. (20 points)

Design a 4-bit shift register that has a control input S, a data input X, and output $Q_3Q_2Q_1Q_0$. When S=0, the register will shift left, i.e., the output becomes $Q_2Q_1Q_0X$. When S=1, the register will shift right and the output becomes $XQ_3Q_2Q_1$. Draw a circuit for such a shift register using 4 D flip-flops and 4 2-to-1 multiplexers.

Solution:



P7. (15points)



a) (10 points) Complete the truth table for the circuit above.

b) (5 points) Based on the truth table, could you identify which flip-flop it is?

Solution:

a)

Input	Q(t)	J	K	Q(t+1)
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	0

b) T flip-flop.