Cpr E 281 HW07 SOLUTION

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Combinational-Circuit Building Blocks
Assigned Date: Eighth Week
Due Date: Monday, Oct. 17, 2016

P1. (10 points)

Consider the following logic function:

$$f(A,B,C) = A'BC' + A'BC + AB'C + ABC$$

a) (5 points) Show the Shannon's expansion of function F using variable A.

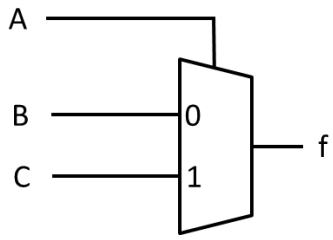
b) (5 points) Implement the circuit for function F using one 2-to-1 multiplexer and a minimal number of other logic gates.

Solution:

a)

$$f(A,B,C) = A' \cdot f(0,B,C) + A \cdot f(1,B,C) \qquad \text{Shannon's expansion using } A$$
$$= A'(BC' + BC) + A(B'C + BC)$$
$$= A'B + AC$$

b)



P2. (20 points)

Consider the following truth table for the function $f(a,b,c,d)$.

a	b	c	d	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1

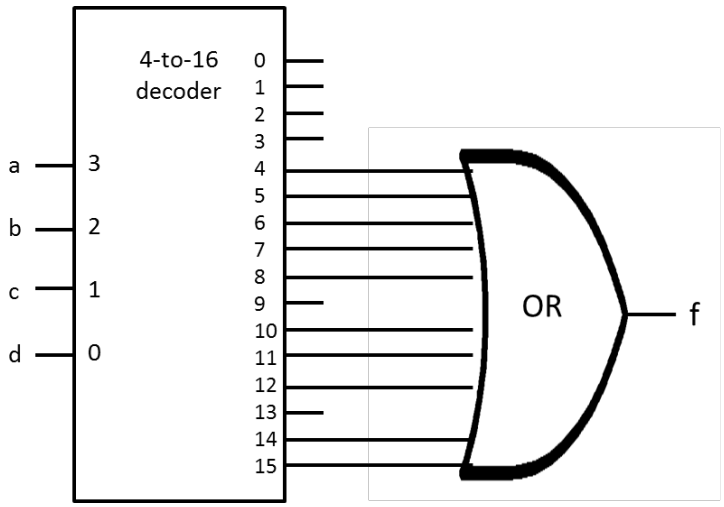
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

a) (10 points) Implement *f* using one 4-to-16 decoder and a minimal number of gates.

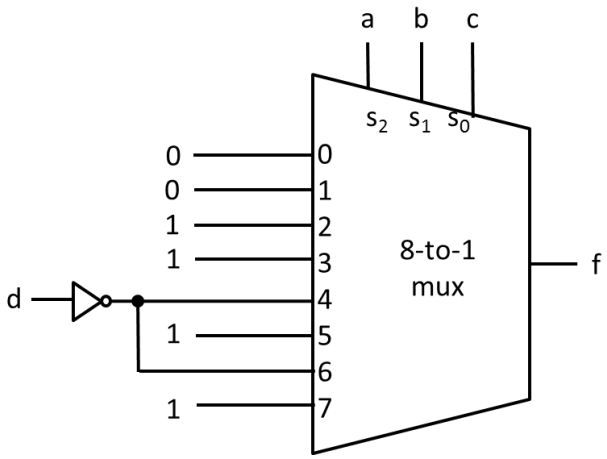
b) (10 points) Implement *f* using one 8-to-1 multiplexer and a minimal number of gates.

Solution:

a)



b)



P3. (10 points)

Show how to construct a 4-to-16 decoder using five 2-to-4 decoders. Assume each 2-to-4 decoder has an ENABLE input (which enables each decoder).

Solution:

The answer is the same as Figure 4.16 in textbook.

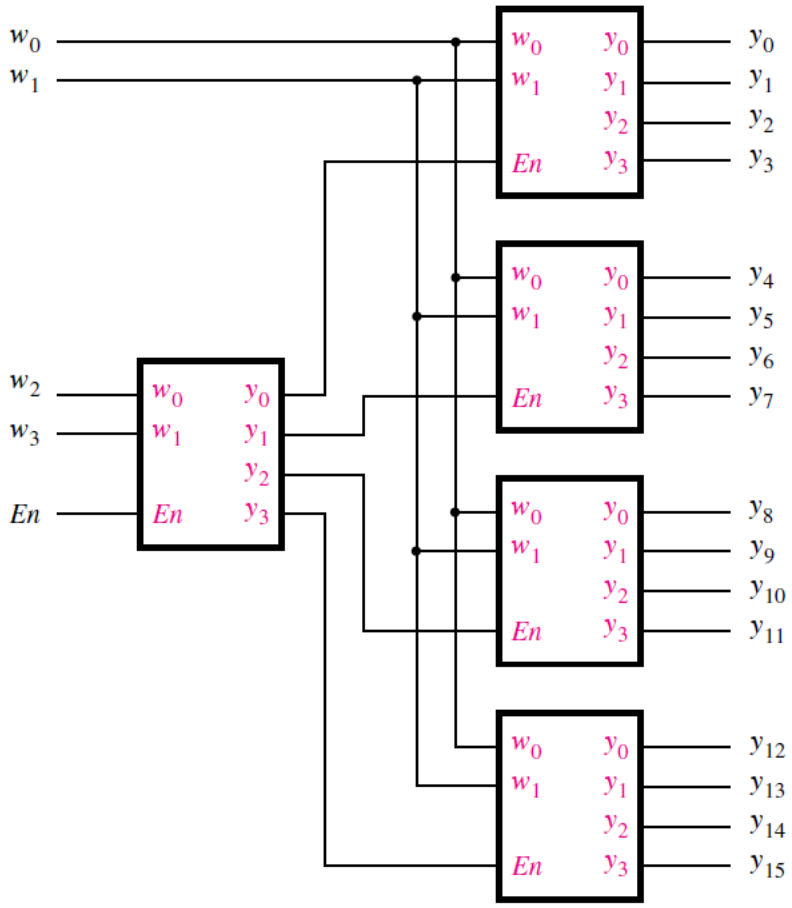
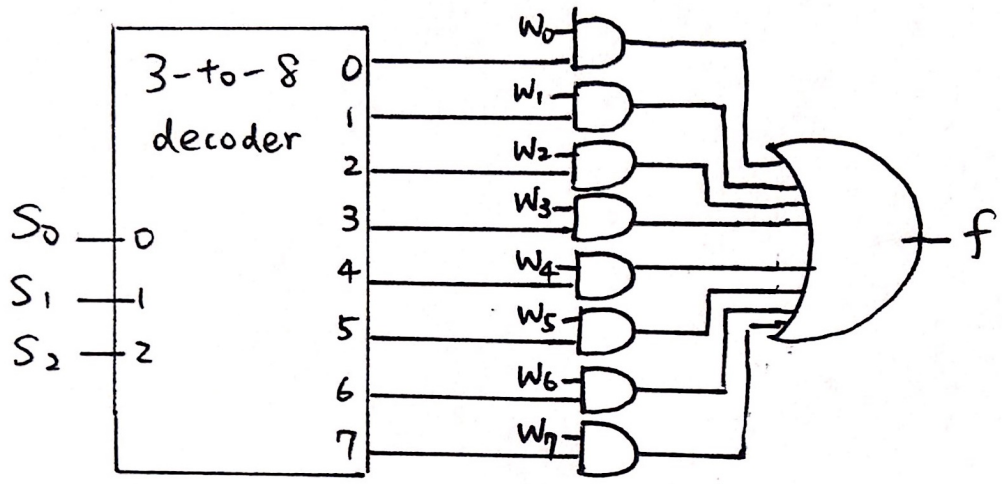


Figure 4.16 A 4-to-16 decoder built using a decoder tree.

P4. (10 points)

Implement the circuit for an 8-to-1 multiplexer using a 3-to-8 decoder and other necessary gates. The circuit should have control inputs $s_2 s_1 s_0$, data inputs $w_7 w_6 w_5 w_4 w_3 w_2 w_1 w_0$, and an output f.

Solution:



P5. (20 points)

Design a 4-to-2 priority encoder with the same inputs and outputs as in Figure 4.20 in the textbook, but with the following priority order: $w_3 < w_2 < w_1 < w_0$

a) (10 points) Show the truth table of this encoder.

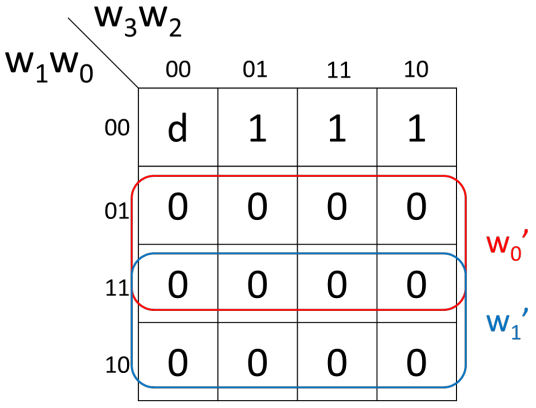
b) (10 points) Derive the minimal POS expression for y_1, y_0, and z, respectively.

Solution:

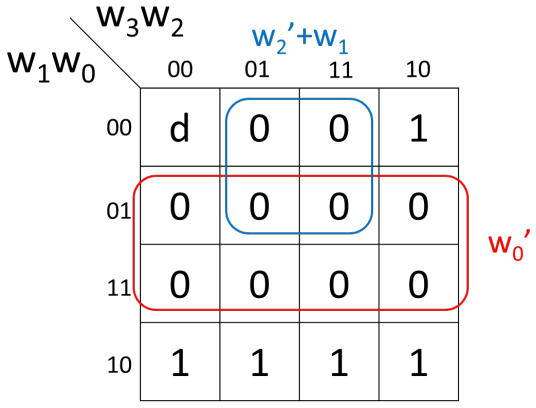
a)

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
x	x	x	1	0	0	1
x	x	1	0	0	1	1
x	1	0	0	1	0	1
1	0	0	0	1	1	1

b)



$$y_1 = w_1' w_0'$$



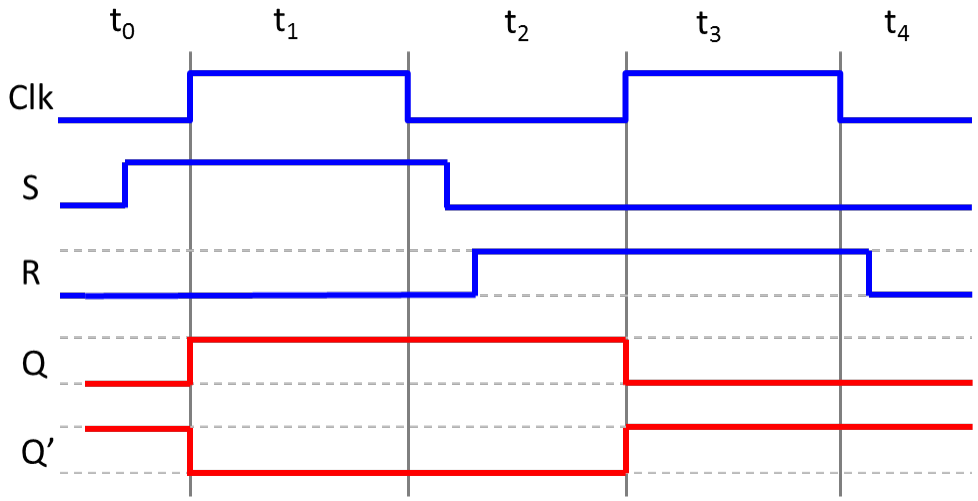
$$y_0 = (w_2' + w_1) w_0'$$

$$z = w_3 + w_2 + w_1 + w_0$$

P6. (10 points)

Complete the following timing diagram for a gated SR-latch. Assume there's no gate delay.

Solution:



P7. (20 points)

A full-adder (FA) has the following truth table:

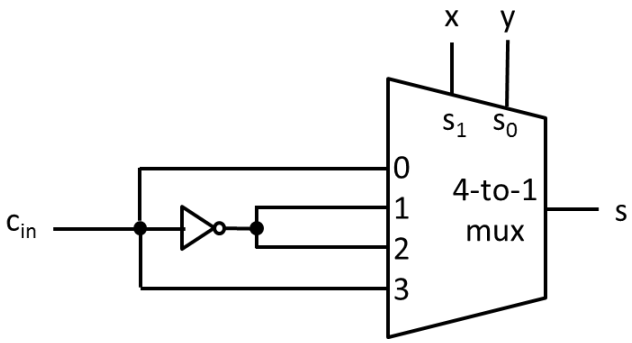
x	y	c_{in}	s	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

a) (10 points) Implement the circuit for output s by using one 4-to-1 multiplexer and a minimal number of gates.

b) (10 points) Implement the circuit for output c_{out} by using one 4-to-1 multiplexer. Please use x and y as control inputs s_1 and s_0 for the multiplexer.

Solution:

a)



b)