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Cpr E 281 LAB1
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 1 Answer Sheet

Name and Student ID: Hosam Abdeltawab, 838973172 **Lab Section:** K

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PRELAB:

Q1. Fill in the Truth Table below for an AND gate:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Q2. What does the .bdf file extension stand for?

Block design file

Q3. What is the name of the FPGA on the DE2-115 board?

- Cyclone IV EP4CE115F29C7 FPGA
- EPCS64 Serial configuration device.

TA Initials: MS

LAB:

2.0 Fill in the Truth Table for *lab1step1*:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Logic Expression: $f(A,B) = A \cdot B$

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sw[0] → AB28 = y
sw[1] → x
sw[2] → w

4.0 Fill in the Truth Table for *lab1step2*:

W	X	Y	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$\bar{w} x \bar{y}$

$w \bar{x} \bar{y}$

$w x y$

Logic Expression: $Z(w,x,y) = (\bar{w} x \bar{y}) + (w \bar{x} \bar{y}) + (w x y)$

TA Initials: MS

4.0 Fill in the Truth Table for *lab1step3*:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$\bar{A}\bar{B}C$

$\bar{A}BC$

$A\bar{B}C$

$AB\bar{C}$

Logic Expression: $F(A,B,C) = (\bar{A}\bar{B}C) + (\bar{A}BC) + (A\bar{B}C) + (AB\bar{C})$

TA Initials: MS