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Cpr E 281 LAB11
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 11 Answer Sheet

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PRELAB:

Complete the prelab and make sure you have your designs and circuit diagrams ready before the lab session. You may refer to your text book, Chapter 6.

Q1. Design a simple counting device (Section 2.0).

Number of States: 6
Number of State Variables: 3

State Table:

Present State	Next State		Output
	w=0	w=1	
A	A	B	0
B	B	C	1
C	C	D	2
D	D	E	3
E	E	F	4
F	F	A	5

State-Assigned Table:

Present State	Next State		Output
	w=0	w=1	
000	000	001	000
001	001	010	001
010	010	011	010
011	011	100	011
100	100	101	100
101	101	000	101

Canonical SOP Expressions for Next State Logic:

$*Y_2 = \bar{w}\, y_2\, \bar{y}_1\, \bar{y}_0 + \bar{w}\, y_2\, \bar{y}_1\, y_0 + w\, \bar{y}_2\, y_1\, y_0 + w\, y_2\, \bar{y}_1\, \bar{y}_0 + w\, y_2\, y_1\, y_0$? -2

Simplified Next State Logic Expressions:

$*Y_2 = \bar{w}\, y_2 + y_2\, \bar{y}_0 + w\, y_1\, y_0$ $*Y_0 = w \oplus y_0$

$*Y_1 = \bar{w}\, y_1 + y_1\, \bar{y}_0 + w\, \bar{y}_2\, \bar{y}_1\, y_0$

$*Y_1 = \bar{w}\, \bar{y}_2\, y_1\, \bar{y}_0 + \bar{w}\, \bar{y}_2\, y_1\, y_0 + \bar{w}\, \bar{y}_2\, \bar{y}_1\, y_0 + w\, \bar{y}_2\, y_1\, \bar{y}_0$

$*Y_0 = \bar{w}\, \bar{y}_2\, \bar{y}_1\, y_0 + \bar{w}\, \bar{y}_2\, y_1\, y_0 + w\, \bar{y}_2\, \bar{y}_1\, \bar{y}_0 + \bar{w}\, y_2\, \bar{y}_1\, y_0 + w\, \bar{y}_2\, y_1\, \bar{y}_0 + w\, y_2\, \bar{y}_1\, \bar{y}_0$

Circuit Diagram:

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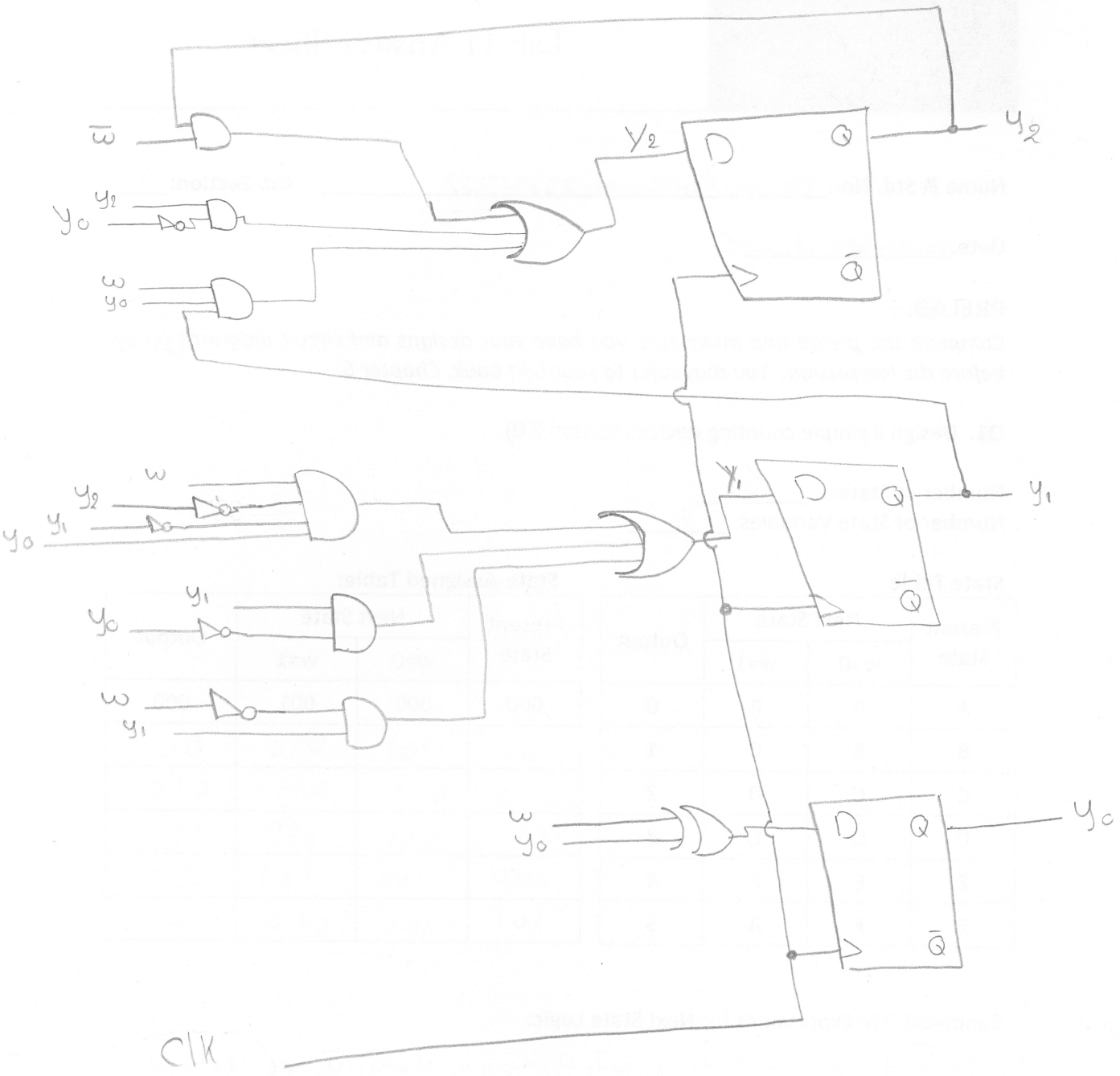
w
y_2
y_0
y_2
D
Q
$\bar{Q}$
Y_2
y_2
w
y_0
y_2
w
y_0
y_1
Y_1
D
Q
$\bar{Q}$
y_1
y_0
y_1
w
y_1
w
y_0
D
Q
$\bar{Q}$
Y_0
CLK

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Q2. Design a simple counter (Section 3.0).

Number of States: 4
Number of State Variables: 2

State Table:

Present State	Next State		Output
	w=0	w=1	
A	A	B	0
B	B	C	2
C	C	D	4
D	D	A	5

State-Assigned Table:

Present State	Next State		Output
	w=0	w=1	
00	00	01	000
01	01	10	010
10	10	11	100
11	11	00	101

Canonical SOP Expressions for Next State Logic:

$*Y_1 = \bar{w}\, y_1 \bar{y}_0 + \bar{w}\, y_1 y_0 + w \bar{y}_1 y_0 + w y_1 \bar{y}_0$

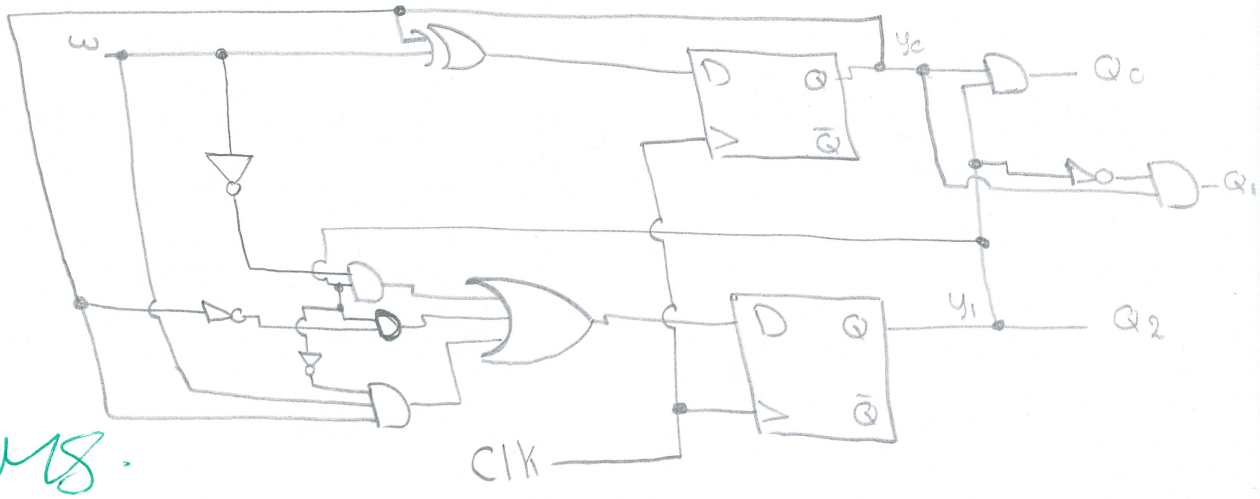
$*Y_0 = \bar{w}\, \bar{y}_1 y_0 + \bar{w}\, y_1 y_0 + w \bar{y}_1 \bar{y}_0 + w y_1 \bar{y}_0$

Simplified Logic Expressions:

$*Y_1 = \bar{w}\, y_1 + y_1 \bar{y}_0 + w \bar{y}_1 y_0$

$*Y_0 = \bar{w}\, y_0 + w \bar{y}_0 = w \oplus y_0$

Circuit Diagram:



LAB: M8

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2.0 A Simple Counting Device

How does the **clock_generator** module produce a signal with a period of about 2.68 seconds?

- A clock signal is produced by a clock generator. In this circuit, we are using a clock signal for syncronization which is activated by a rising edge. So, it manages to change every 2.68 seconds beause all the clock signals are transmitted on 1 wire.

the for Period = 1 / frequency

1,000,000 Hz = 1 MHz

Each TFF halves frequency/ doubles time

Hardware results demonstrate a functional design: M8

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3.0 A Simple Counter

Hardware results demonstrate a functional design: M8.