

1. Write a MIPS program fragment for the following high-level language statement:

$a = b + 100;$

Assume that  $a$  is in register  $\$t0$  and  $b$  is in register  $\$t1$ .

2. Write a MIPS program fragment for the following high-level language statement:

$g = h + A[14];$  // Assume  $A$  is an int array with each element taking 4 bytes

Assume that  $g$  is in register  $\$t0$ ,  $h$  is in register  $\$t1$ , and the base address of  $A$  is in register  $\$s1$ .

3. Write a MIPS program fragment for the following high-level language statement:

$A[275] = g + A[275];$  // Assume  $A$  is an int array with each element taking 4 bytes

Assume that  $g$  is in register  $\$t0$ , and the base address of  $A$  is in register  $\$s1$ .

4. Write a MIPS program fragment for the following high-level language statement:

$g = h + A[i];$  // Assume  $A$  is an int array with each element taking 4 bytes

Assume that  $g$  is in register  $\$t0$ ,  $h$  is in register  $\$t1$ , the base address of  $A$  is in register  $\$s1$ , and  $i$  is in register  $\$s2$ .

5. Write a MIPS program fragment for the following high-level language statement:

$x[10] = x[11] + c;$  // Assume  $x$  is an int array with each element taking 4 bytes

Assume that  $c$  is in register  $\$t0$ , and the base address of  $x$  is 4,000,000 in base 10. (Hint: You should use the Load Upper Immediate or *lui* instruction).

6.

(a) Write a MIPS program fragment for the following high-level language statement:

$B[350] = g + B[350];$  // Assume  $B$  is an int array with each element taking 4 bytes

Assume that  $g$  is in register  $\$s1$  and that the base address of the array  $B$  is in register  $\$s2$ .

Assume that registers  $\$s0$  through  $\$s7$  map to register numbers 16 through 23, and registers  $\$t0$  through  $\$t7$  map to register numbers 8 through 15. Use the instruction format information provided below to convert your instructions in Part (a) to machine language code. First express your machine language code using decimal numbers for the fields and then convert into Binary and eventually into hexadecimal representation for each instruction.

(b) Instructions for the program in Part (a) converted into Decimal

(c) Conversion of Part (b) into Binary

(d) Conversion of Part (c) into Hexadecimal

**Instruction Format of relevant MIPS instructions**

	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
<b>add</b> rd, rs, rt	0	rs	rt	rd	0	32

	6 bits	5 bits	5 bits	16 bits
<b>lw</b> rt, <i>d</i> (rs)	35	rs	rt	16-bit displacement <i>d</i>
<b>sw</b> rt, <i>d</i> (rs)	43	rs	rt	16-bit displacement <i>d</i>

1]  $a = b + 100;$  //  $a$  in  $\$t_0$ ,  $b$  in  $\$t_1$   
 addi  $\$t_0, \$t_1, 100$

2]  $g = h + A[14];$  //  $g$  in  $\$t_0$ ,  $h$  in  $\$t_1$ , &  $A$  is in  $\$S_1$   
 Lw  $\$t_2, 56(\$S_1)$   
 add  $\$t_0, \$t_1, \$t_2$

3]  $A[275] = g + A[275];$  //  $g$  in  $\$t_0$ ,  $A$  in  $\$S_1$

Lw  $\$t_1, 1100(\$S_1)$

Add  $\$t_0, \$t_0, \$t_1$

Sw  $\$t_0, 1100(\$S_1)$

4]  $g = h + A[i];$  //  $g$  in  $\$t_0$ ,  $h$  in  $\$t_1$ ,  $A$  in  $\$S_1$ , &  $i$  in  $\$S_2$

Add  $\$t_2, \$S_2, \$S_2$

Add  $\$t_2, \$t_2, \$t_2$

Add  $\$t_2, \$t_2, \$S_1$

Lw  $\$t_3, 0(\$t_2)$

Add  $\$t_0, \$t_1, \$t_3$

5]  $X[10] = X[11] + C;$  //  $C$  in  $\$t_0$ ,  $X$  base address is 4,000,000  
 $(4,000,000)_{10} = 0x003D0900$

Lwi  $\$t_1, 0x003D$

ORI  $\$t_1, \$t_1, 0x0900$

Lw  $\$t_2, 44(\$t_1)$

Add  $\$t_3, \$t_2, \$t_0$

Sw  $\$t_3, 40(\$t_1)$

6] (a)  $B[35c] = g + B[35c]; // g \text{ in } \$S_1, B \text{ in } \$S_2$

$Lw \$L_0, 1400 (\$S_2)$

Add  $\$L_1, \$S_1, \$L_0$

$Sw \$L_1, 1400 (\$S_2)$

$\$S_1 \rightarrow 17_{10}$

$\$S_2 \rightarrow 18_{10}$

$\$L_0 \rightarrow 8_{10}$

$\$L_1 \rightarrow 9_{10}$

~~(b)~~ (b)

$Lw \$L_0, 1400 (\$S_2)$	35	18	8	1400
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Add $\$L_1, \$S_1, \$L_0$	0	17	8	9	0	32
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$Sw \$L_1, 1400 (\$S_2)$	43	18	9	1400
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~~(c)~~ (c)

$Lw \$L_0, 1400 (\$S_2)$	100011	10010	01000	0000010101111000
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Add $\$L_1, \$S_1, \$L_0$	000000	10001	01000	01001	000000	100000
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$Sw \$L_1, 1400 (\$S_2)$	101011	10010	01001	000001010111000
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(d)

(3)

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