Cpr E 281 HW03 SOLUTIONS

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

NAND/NOR Gates and Synthesis
Assigned Date: Third Week
Due Date: Sep. 12, 2016

P1. (10 points) Prove that the following are true (using truth tables):

a) $A \oplus B = \overline{A} \oplus \overline{B}$

b) $\overline{A} \oplus B = A \oplus \overline{B}$

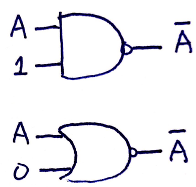
A	B	$\overline{A}$	$\overline{B}$	$A \oplus B$	$\overline{A} \oplus \overline{B}$	$\overline{A} \oplus B$	$A \oplus \overline{B}$
0	0	1	1	0	0	1	1
0	1	1	0	1	1	0	0
1	0	0	1	1	1	0	0
1	1	0	0	0	0	1	1

P2. (10 points) Show how to implement a NOT function by using:

a) a 2-input NAND gate only. (5 points)

b) a 2-input NOR gate only. (5 points)

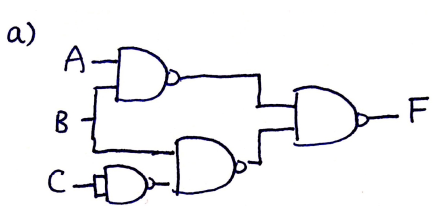
For part (a) and part (b), you should use **a different way from what has been shown in class** (connecting both terminals to the input signal). Note that you are allowed to connect constant voltages (i.e., logic values 0 or 1) to the gate inputs.

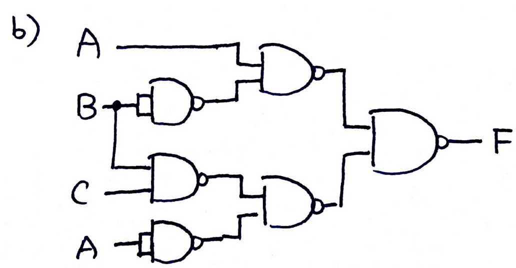


P3. (10 points) Implement the following functions using only NAND gates:

a) $F = AB + B\overline{C}$

b) $F = A\overline{B} + (\overline{B} + \overline{C})\overline{A}$

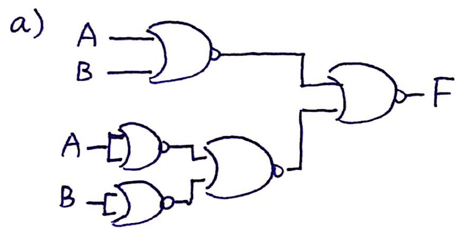


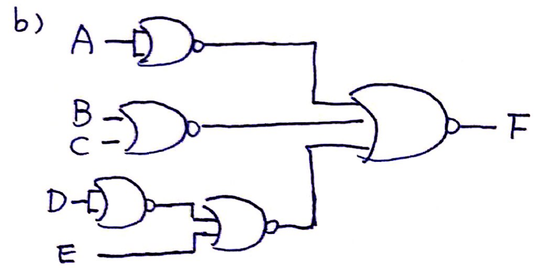


P4. (10 points) Implement the following functions using only NOR gates:

a) $F = (A+B)(\overline{A}+\overline{B})$

b) $F = A(B+C)(\overline{D}+E)$





P5. (20 points) A logic circuit has three inputs P, Q, R and one output S. The value of S is equal to 1 whenever $P = 0$ or whenever $Q = R = 1$.

a) Derive the truth table for this circuit. (5 points)

b) Use Boolean algebra to derive the simplified expression from the canonical SOP form. (5 points)

c) Draw the logic circuit for the simplified Boolean expression using only AND, OR, and NOT gates. (5 points)

d) Draw the logic circuit for the simplified Boolean expression using only NAND gates. (5 points)

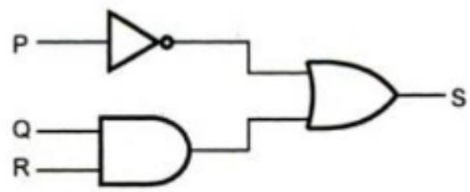
a)

P	Q	R	S
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

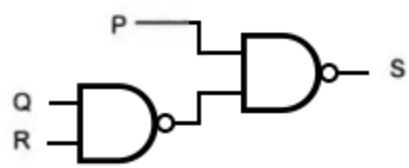
b)

$$\begin{aligned} S &= \overline{P}\,\overline{Q}\,\overline{R} + \overline{P}\,\overline{Q}R + \overline{P}Q\overline{R} + \overline{P}QR + PQR \\ &= \overline{P}\,\overline{Q}(\overline{R}+R) + \overline{P}Q(\overline{R}+R) + PQR \\ &= \overline{P}\,\overline{Q} + \overline{P}Q + PQR \\ &= \overline{P} + PQR \\ &= \overline{P} + QR \end{aligned}$$

c)



d)



P6. (20 points) Design a majority voting machine with three inputs *A*, *B*, *C* and one output *F*. $F = 1$ when at least two of the inputs are equal to 1 (e.g., $A = 1$, $B = 1$, $C = 0$), and $F = 0$ when the majority of the inputs are equal to 0 (e.g., $A = 0$, $B = 1$, $C = 0$).

a) Derive the truth table for the voting machine. (5 points)
b) Use Boolean algebra to derive the simplified expression from the canonical SOP form. (5 points)
c) Draw the logic circuit for the simplified Boolean expression using only AND, OR, and NOT gates. (5 points)
d) Draw the logic circuit for the simplified Boolean expression using only NAND gates. (5 points)

a)

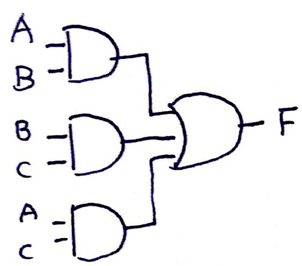
A	*B*	*C*	*F*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

b)

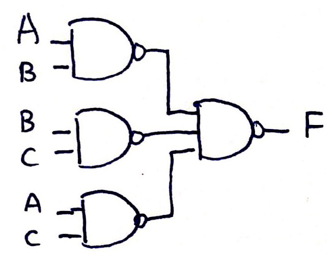
$$
\begin{aligned}
F &= \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC \\
&= \overline{A}BC + A\overline{B}C + AB \\
&= (\overline{A}BC + AB) + (A\overline{B}C + AB) \\
&= B(\overline{A}C + A) + A(\overline{B}C + B)
\end{aligned}
$$

$$= B(A+C) + A(B+C)$$
$$= AB + BC + AC$$

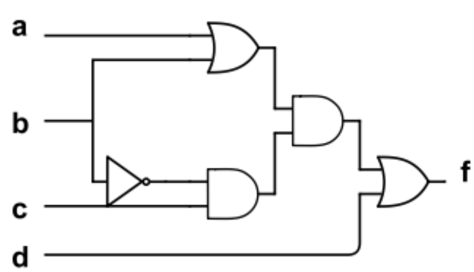
c)



d)



P7. (10 points) Write down the Verilog code for the following circuit by using gate-level primitives.




```
module P7 (a, b, c, d, f)

        input       a, b, c, d;
        output      f;
        wire        w1, w2, w3, w4;

        or (w1, a, b);
        not (w2, b);
        and (w3, w2, c);
        and (w4, w1, w3);
        or (f, w4, d);

endmodule
```

P8. (10 points) Write down the Verilog code for the circuit from P7, but this time use continuous assignments.

```
module P8 (a, b, c, d, f)

        input       a, b, c, d;
        output      f;

        assign f = ( (a|b) & (~b&c) ) | d;

endmodule
```