VLSI Circuit Design Lab
CSE-406

Experiment No : 01
Experiment Name : Design and simulation of CMOS NAND gate using DSCH2

Submitted by :
Name : Md. Habibur Rahman
Roll : 40

Name of Exp:

Design and simulation of CMOS NAND gate using DSCH2

Objective:

The main objective of this experiment is to get familiar with various features of the DSCH2 by designing and implementing CMOS and NAND gate using DSCH2 and to understand their working principle and behavior.

Introduction:

CMOS Stands for "Complementary Metal Oxide Semiconductor." It is a technology used to produce integrated circuits. CMOS circuits are found in several types of electronic components, including microprocessors, batteries, and digital camera image sensors

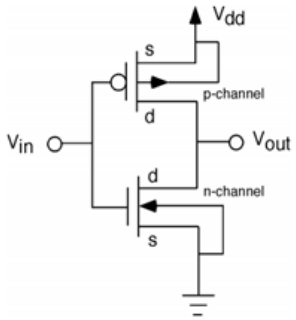


Fig7. Circuit diagram of CMOS Inverter

NAND gate:

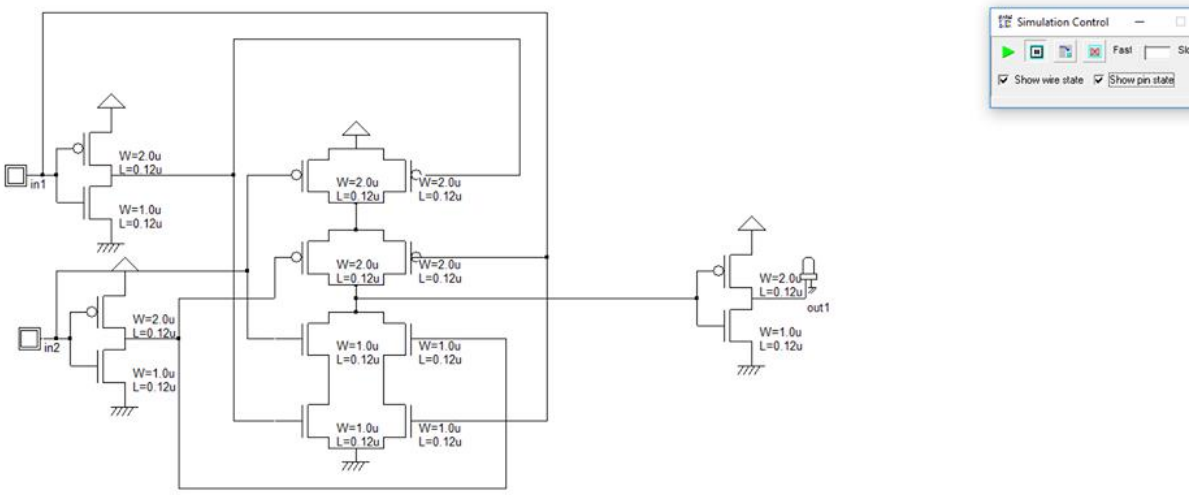
a NAND gate is a logic gate which produces an output which is false only if all its inputs are true; thus its output is complement to that of an AND gate. A LOW output results only if all the inputs to the gate are HIGH; if any input is LOW, a HIGH output results

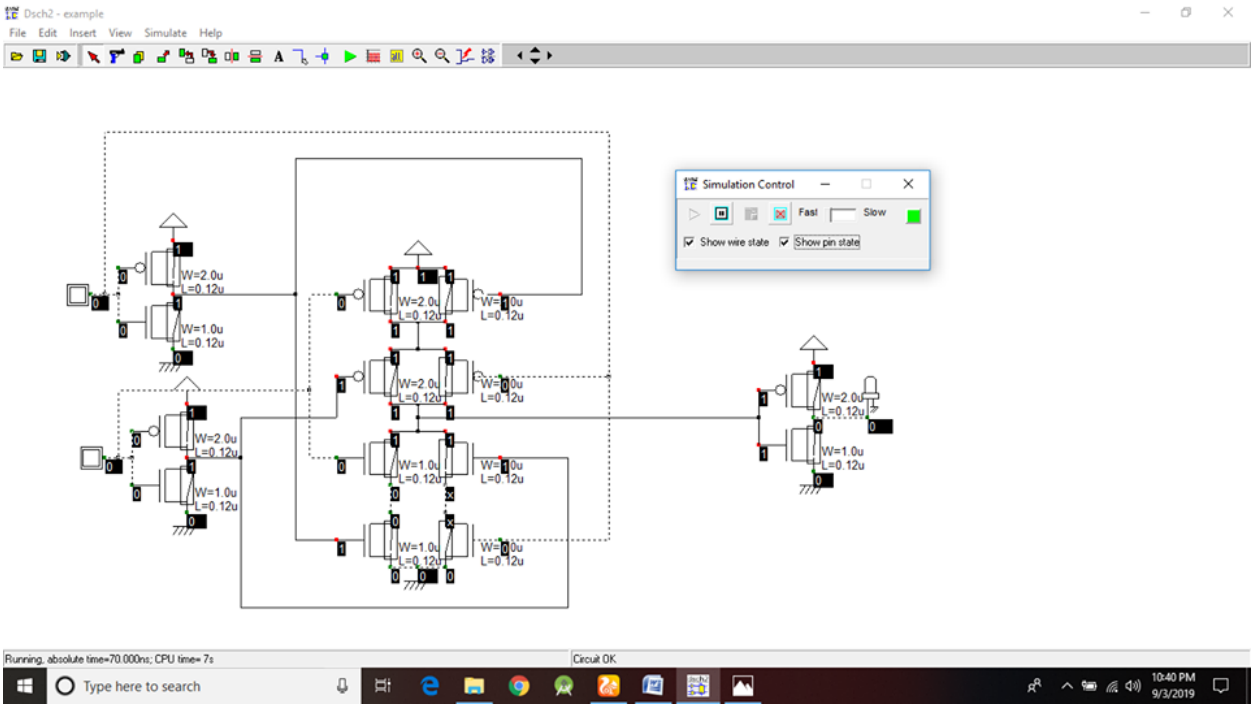
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

TruthTable:

A	B	A **XOR** B
0	0	0
0	1	1
1	0	1
1	1	0

Simulation:


Simulation Control
Fast
Show wire state
Show pin state
in1
in2
out1
W=2.0u
L=0.12u
W=1.0u
L=0.12u


Dsch2 - example
File Edit Insert View Simulate Help
Simulation Control
Fast
Slow
Show wire state
Show pin state
W=2.0u
L=0.12u
W=1.0u
L=0.12u
Running, absolute time=70.000ns; CPU time= 7s
Circuit OK
Type here to search
10:40 PM
9/3/2019

Conclusion:

As the software DSCH2 has no exe file,it got hanged now and then.It was needed to be restarted to perform the simulation now and then.The output of the truth table of A XOR B and the output of the resultant circuit after simulation matched exactly the same .So the experiment produced correct result.