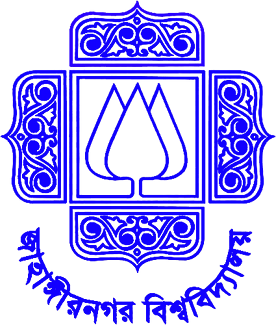
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**VLSI Circuit Design Lab**

**CSE-406**

**Experiment No :** 02

**Experiment Name :** Layout Design & Verification of CMOS NAND & NOR gate

**Submitted by :**

**Name :** Md.Habibur Rahman

**Roll :** 40

**Date of submission**: 17 september,2019

**Experiment name:**

Layout Design & Verification of CMOS NAND & NOR gate

**Objectives**:

The main purpose of this experiment is to impement the layout design of CMOS using NAND firstly and then with NOR gate to visualize the simulation and real structure of these gates.

**Introduction**:

A **NAND** gate (sometimes referred to by its extended name, Negated AND gate) is a digital logic gate with two or more inputs and one output with behavior that is the opposite of an AND gate. The output of a NAND gate is true when one or more, but not all, of its inputs are false. If all of a NAND gate's inputs are true, then the output of the NAND gate is false.

**Truth Table of NAND**

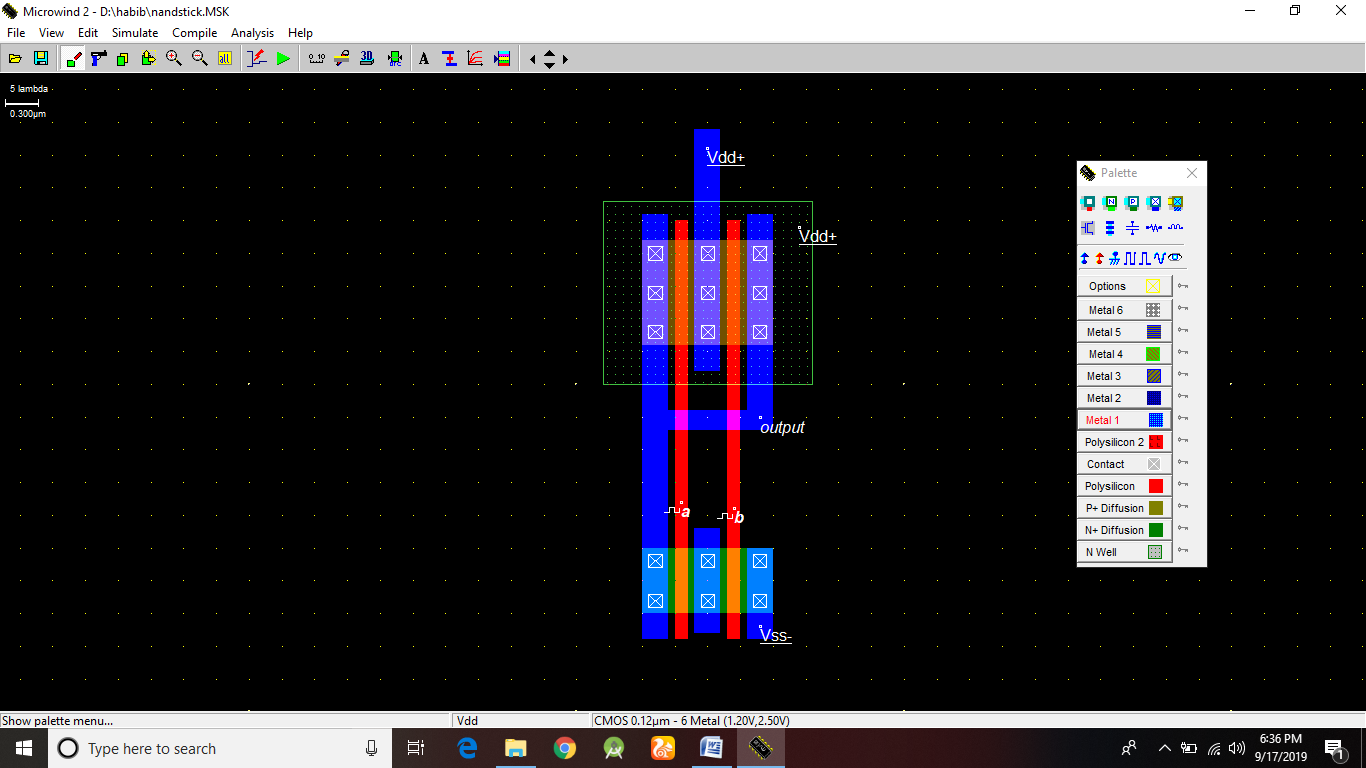
|  |  |  |
| --- | --- | --- |
| A | B |  |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

A **NOR** gate (sometimes referred to by its extended name, Negated OR gate) is a digital logic gate with two or more inputs and one output with behavior that is the opposite of an OR gate. The output of a NOR gate is true all of its inputs are false. If one or more of a NOR gate's inputs are true, then the output of the NOR gate is false.

**Truth Table of NOR**

|  |  |  |
| --- | --- | --- |
| A | B |  |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

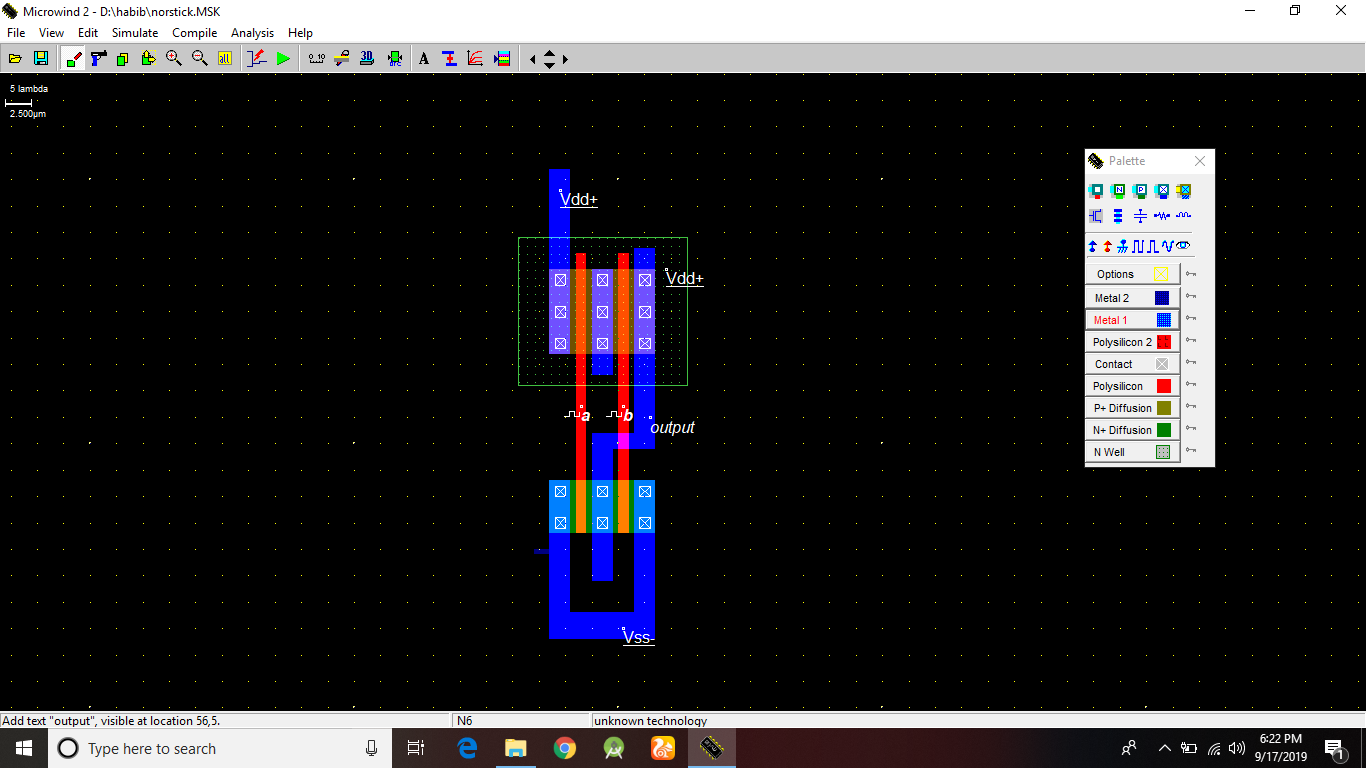
Layout design of NAND:



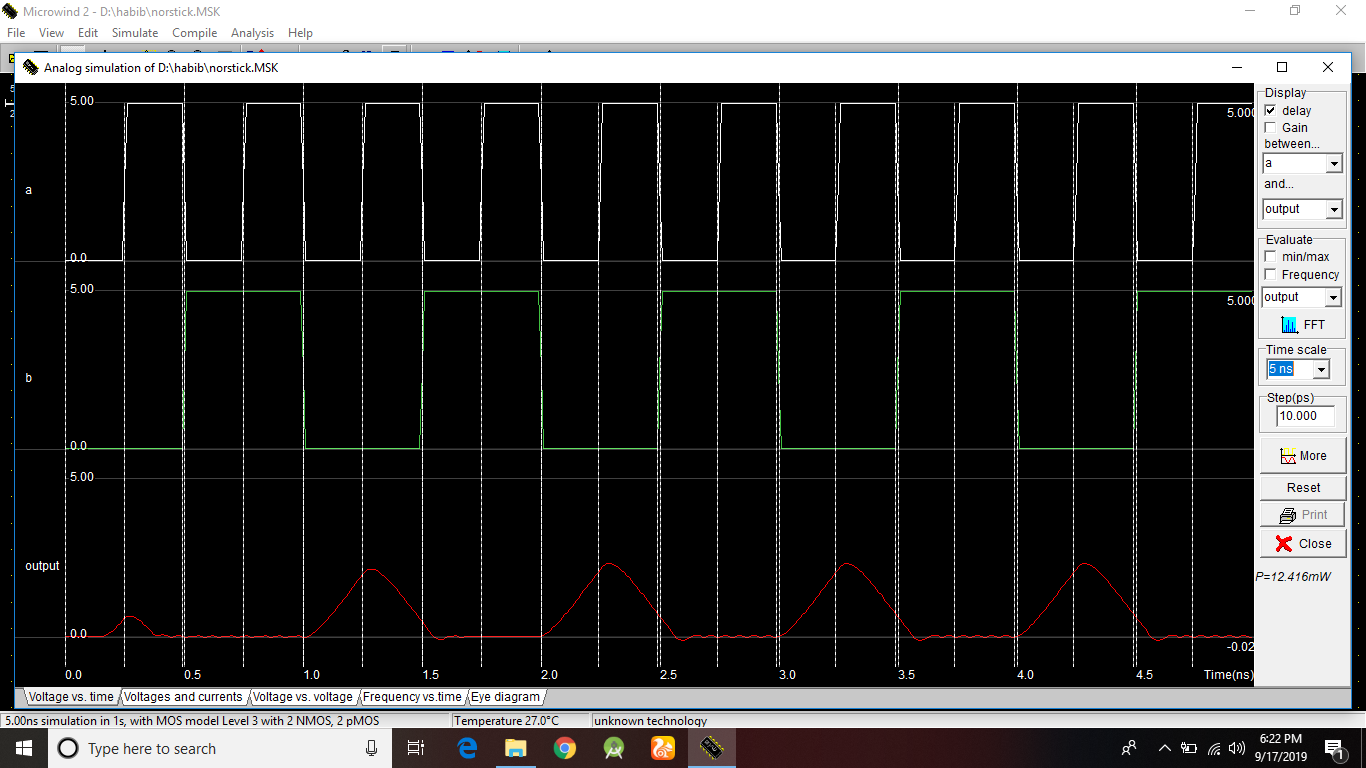
Result :



Layout Design of NOR:



Result:



Conclusion:

* Metal should be selected properly.
* VDD & VSS connections should be properly connected.