

**VLSI Circuit Design Lab**

**CSE-406**

**Experiment No :** 03

**Experiment Name :** Layout Design of the following logic function

**Submitted by :**

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**Roll :** 40

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**Name of the experiment:**

Layout Design of the following logic function

**Objective:**

The main purpose of this experiment is to impement the layout design of a function and then visualize the simulation and real structure of the function.

**Introduction**:

The **AND** gate is so named because, if 0 is called "false" and 1 is called "true," the gate acts in the same way as the logical "and" operator. The following illustration and table show the circuit symbol and logic combinations for an AND gate. (In the symbol, the input terminals are at left and the output terminal is at right.) The output is "true" when both inputs are "true." Otherwise, the output is "false." In other words, the output is 1 only when both inputs one AND two are 1.

The **OR** gate gets its name from the fact that it behaves after the fashion of the logical inclusive "or." The output is "true" if either or both of the inputs are "true." If both inputs are "false," then the output is "false." In other words, for the output to be 1, at least input one OR two must be 1.

**Truth Table**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D |  |  |  |  |
| 0 | 0 | 0 | 0 | 1 |  |  |  |
| 0 | 0 | 0 | 1 | 1 |  |  |  |
| 0 | 0 | 1 | 0 | 1 |  |  |  |
| 0 | 0 | 1 | 1 | 0 |  |  |  |
| 0 | 1 | 0 | 0 | 1 |  |  |  |
| 0 | 1 | 0 | 1 | 1 |  |  |  |
| 0 | 1 | 1 | 0 | 1 |  |  |  |
| 0 | 1 | 1 | 1 | 0 |  |  |  |
| 1 | 0 | 0 | 0 | 1 |  |  |  |
| 1 | 0 | 0 | 1 | 1 |  |  |  |
| 1 | 0 | 1 | 0 | 1 |  |  |  |
| 1 | 0 | 1 | 1 | 0 |  |  |  |
| 1 | 1 | 0 | 0 | 1 |  |  |  |
| 1 | 1 | 0 | 1 | 1 |  |  |  |
| 1 | 1 | 1 | 0 | 1 |  |  |  |
| 1 | 1 | 1 | 1 | 0 |  |  |  |
|  |  |  |  |  |  |  |  |

**Layout design:**

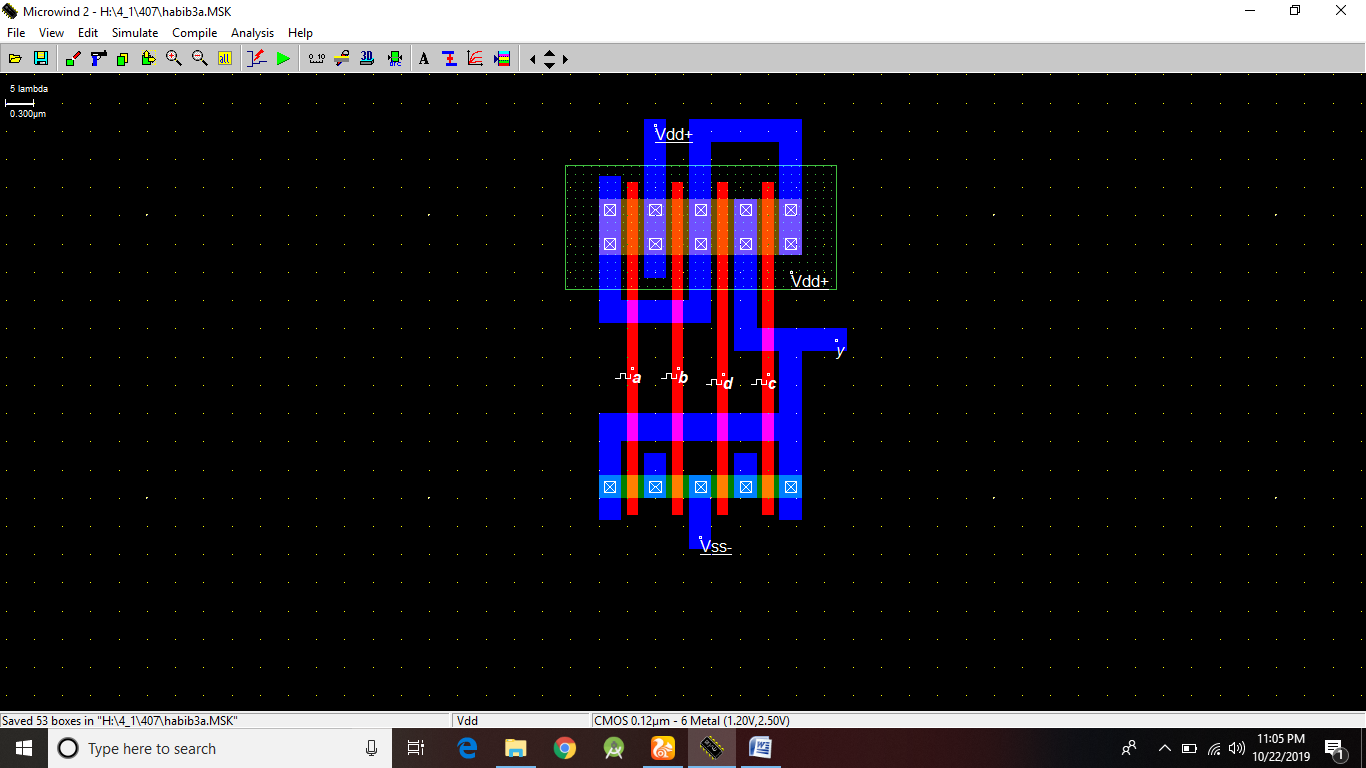


Fig : Layout design of

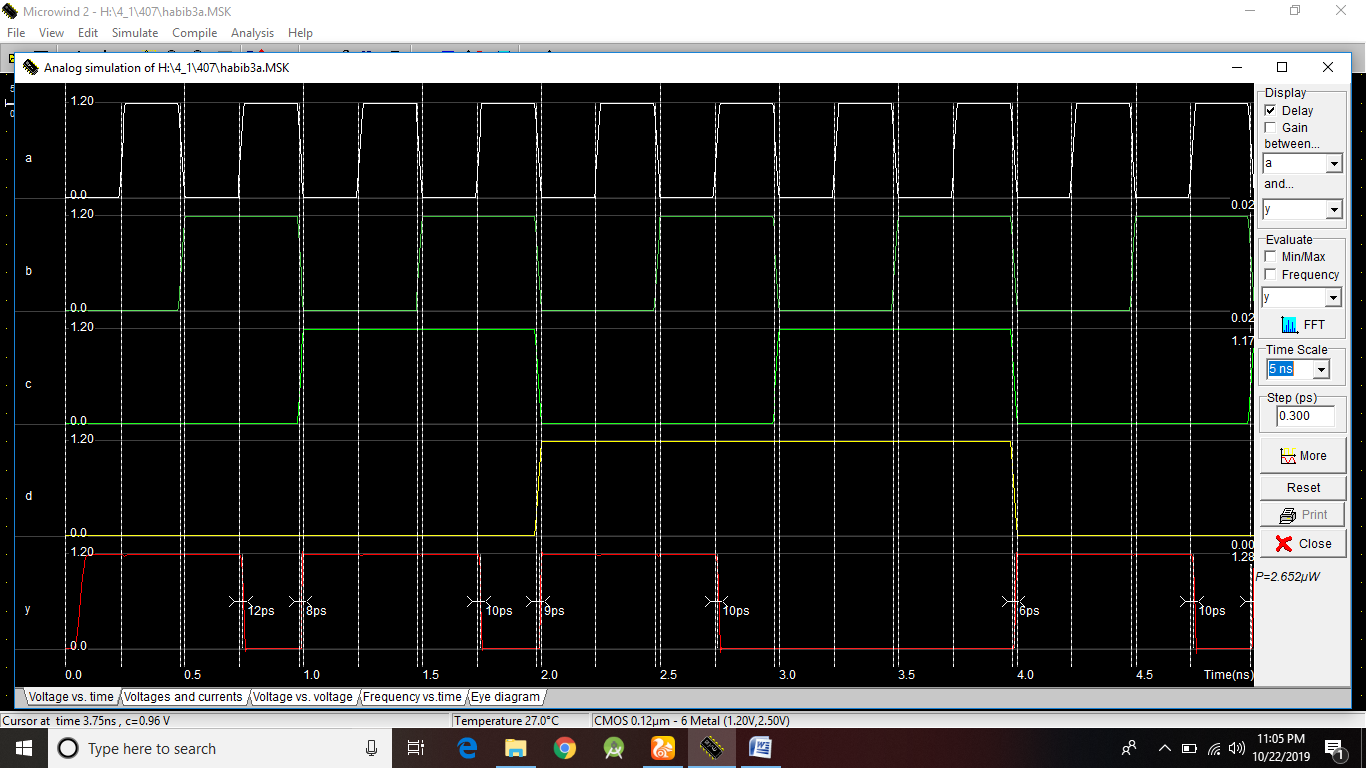


Fig :Timing Diagram

**Discussion**:

* During the implementation of layout it should be noted that the width and height are same in scale
* The connections have to be correct for the right output.