Faculty of Media Engineering and Technology
Dept. of Computer Science and Engineering
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CSEN/CSIS 402: Computer organization
Spring 2023

Project – milestone 1

Instructions

- The project should be implemented using LogiSim
- Every team should have one submission
- You are always welcome to discuss the project with the TAs during the available office hours.
- You must work with your team members only. Do not exchange information with other teams or individuals.
- Cheating and plagiarism will be strictly punished with a grade of 0 in the project.
- Please respect the submission deadline.

Submission guideline and deadlines

- The project should be submitted as a Zip file containing the Logisim files.
- The submission should sent via email to **cospring2024@gmail.com** by April 9, 2024.
- **Your file name should be your group number and the email subject should include it as well. Include your names and emails in the email body as well.**
- The evaluation will take place in the week from April 14-April 18. Slots will be available to you by then.

Description

In this milestone, you are required to implement a subset of the basic computer to do a simulation for a memory system and an arithmetic/logic unit and a group of registers. All components should be linked through a common bus that has 3 control select lines S2, S1 and S0.

- The memory (RAM) should have 128 addresses (words). Each word is 16-bits.
- Users should be able to read and write to the memory.
- The Address Register (AR) output should be linked to the address lines of the memory
- The memory's input and output lines are connected to the common bus.
- The available registers are:
  - DR
  - TR
  - AR
  - AC (Accumulator Register)
  - PC
  - IR

Each register has a load enable flag to control whether the data available from the bus, will update its content or not. **The registers don't have INC and CLR.**

ALU:
The functionalities and control numbers ($C_2C_1C_0$) of the arithmetic unit (ALU) which has 2 inputs A and B, coming from the DR and the AC:

- (001) Transfer input A. (coming from DR)
- (010) Increment A
- (011) Multiplying A*B
- (100) Subtracting the numbers A-B
- (101) Divide A/B
- (110) Add A+B
- (111) A XOR B

The selection of the bus should be done as follows:

S_2	S_1	S_0	Selection
0	0	0	Memory
0	0	1	AR
0	1	0	PC
0	1	1	AC
1	0	0	DR
1	0	1	TR
1	1	1	IR

Testing your circuit

Fill in the first 5 locations of the memory as follows:

Address	Value
0	22
1	5
2	0
3	1
4	0

And also fill in register [AR] initially with value 0

Part A) Generate the necessary RTLs (NOT instructions, just micro-operations) to achieve the following:

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M[2] = M[0] / M[1]
M[4] = M[2] – M[3]
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Example :

cycle X: DR←M[AR]
cycle X+1: AC←DR
and so on.

Part B) Construct the circuit and prepare the controls you need to do each clock cycle to achieve the equation in part A.

You need to show this cycle by cycle to the TAs during evaluation. It's a good idea to have a list of all your controls, and then cycle by cycle, you prepare them in a file or document.

The result should be = (22/5) - (1) = 4-1=3 and should be stored in M[4].

The TA will have the liberty to change the values of the RAM and simulate your controls again, and he/she should get the correct output accordingly.

Hint: you will not need to include any RTL dealing with PC and IR in this milestone, but you will use them in milestone 2.