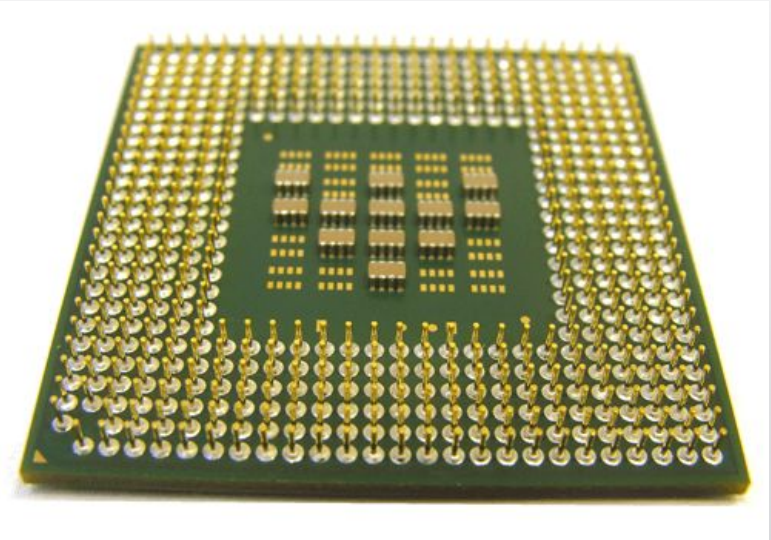
MICROPROCESOR AND INTERFACING

(PIN DIAGRAM)



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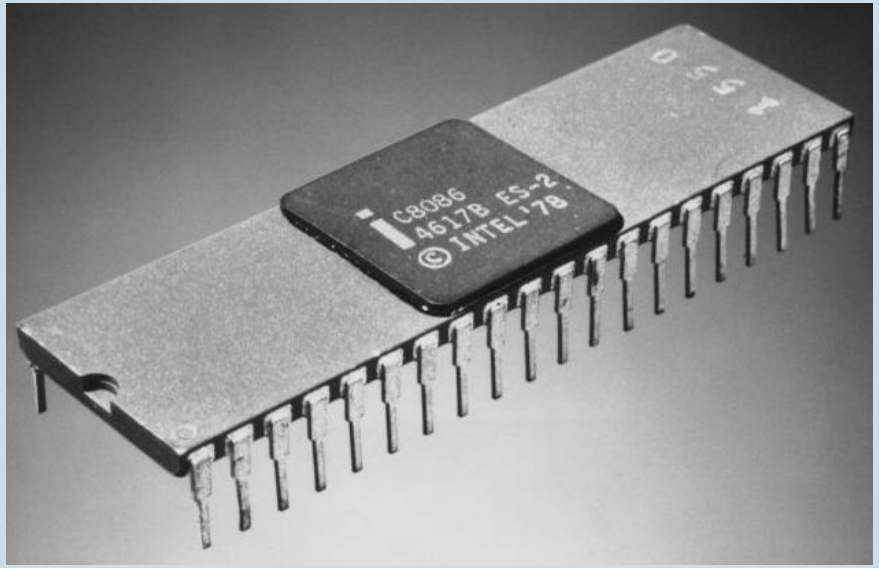
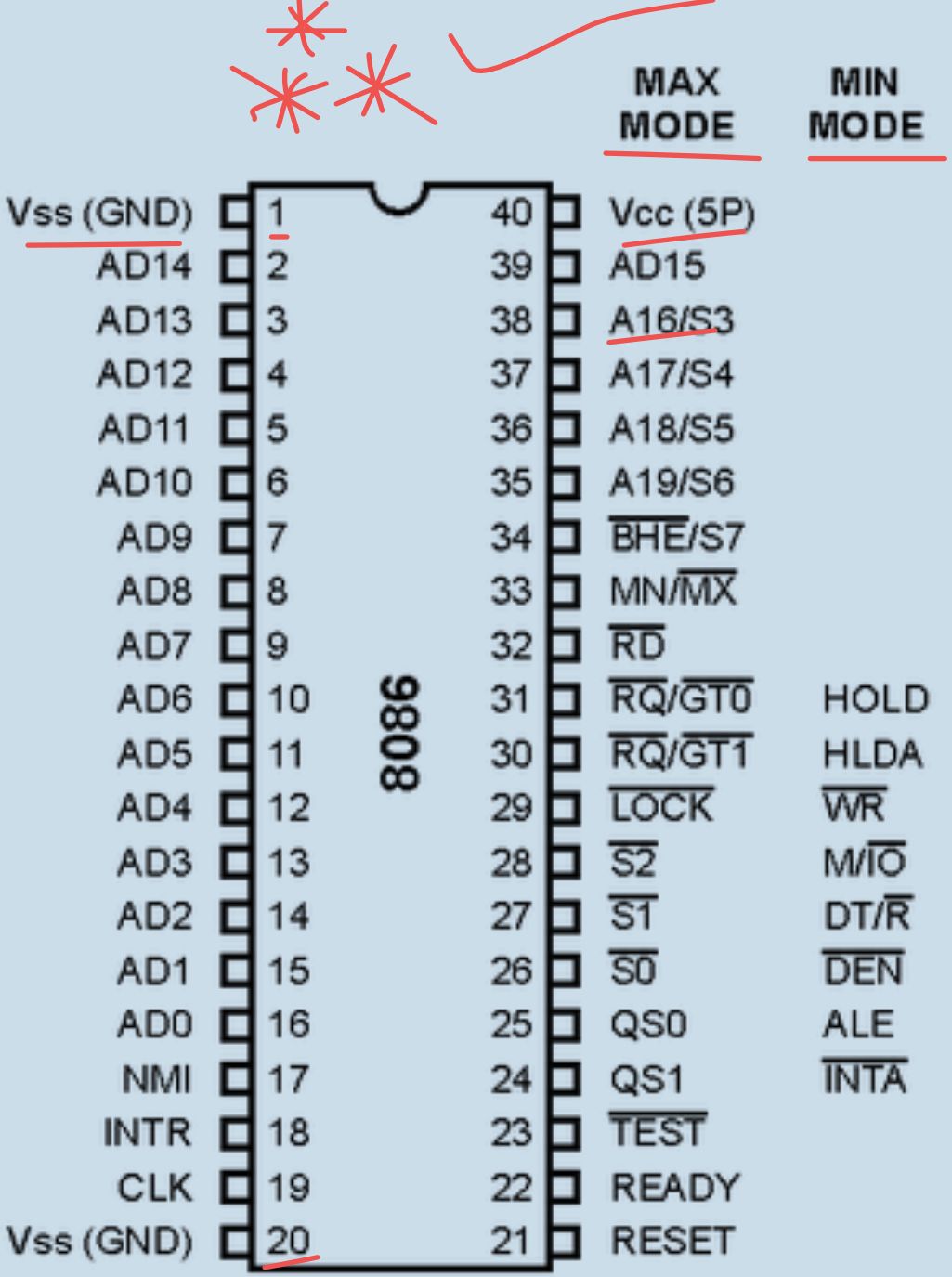
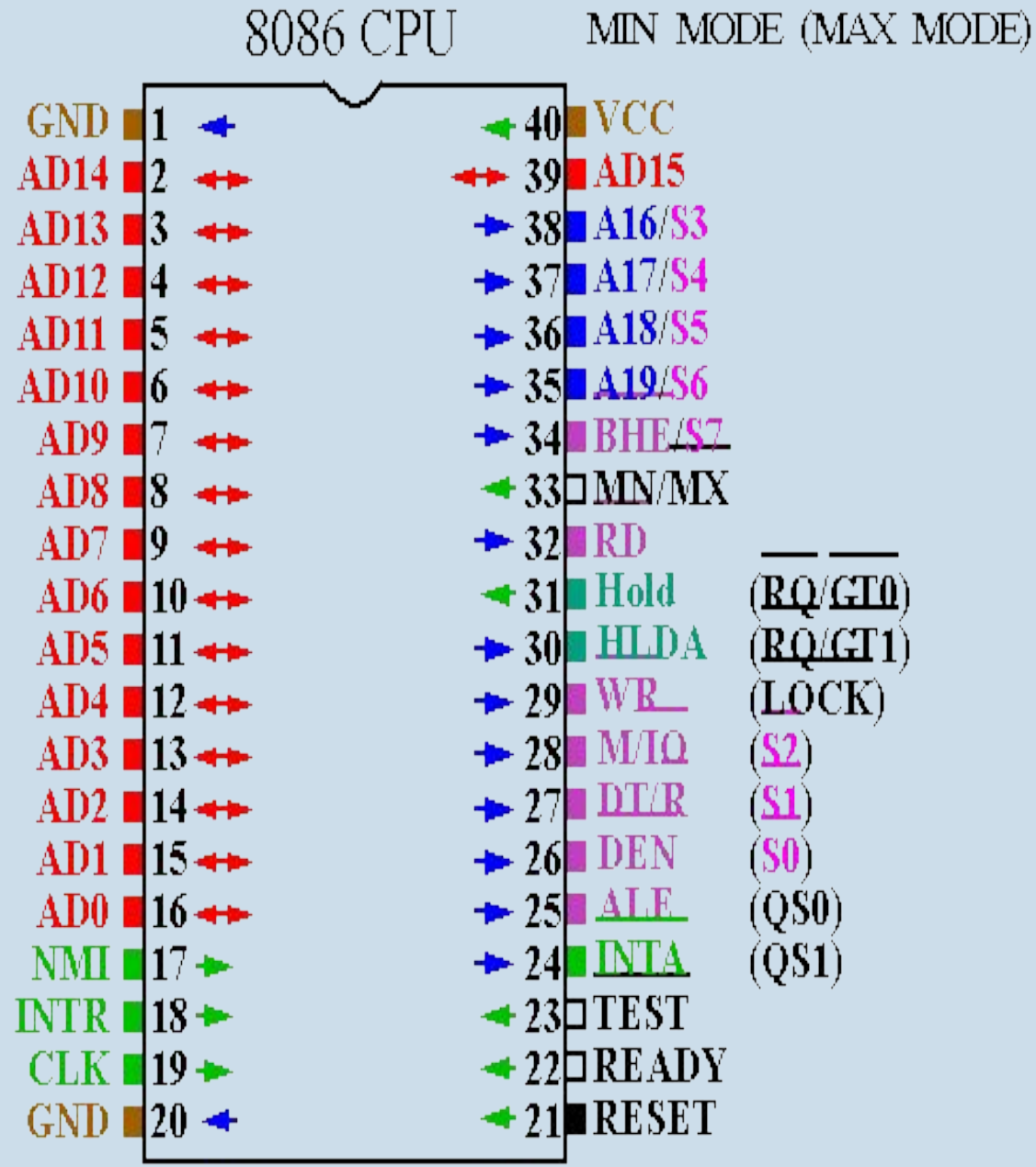
Introduction

- Pin diagram is shows all the signal pins used by the microprocessor and the sequence of the signals and their connections.
- 8086 microprocessor is a 40 pin Dual in package IC which operate on +5volt power supply.




MAX MODE
MIN MODE
8086
Vss (GND) 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
Vss (GND) 20
40 Vcc (5P)
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 RQ/GT0 HOLD
30 RQ/GT1 HLDA
29 LOCK WR
28 S2 M/IO
27 S1 DT/R
26 S0 DEN
25 QS0 ALE
24 QS1 INTA
23 TEST
22 READY
21 RESET


8086 CPU
MIN MODE (MAX MODE)
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 Hold (RQ/GT0)
30 HLDA (RQ/GT1)
29 WR (LOCK)
28 M/IO (S2)
27 DT/R (S1)
26 DEN (S0)
25 ALE (QS0)
24 INTA (QS1)
23 TEST
22 READY
21 RESET

Pin Description

- The 8086 operates in single processor or multiprocessor configuration to achieve high performance.
- It can be operated in two modes
  - Minimum Mode
  - Maximum Mode
- The pins serve a particular function in minimum mode (single processor mode) and other function in maximum mode configuration (multiprocessor mode).

Pin Description

- The 8086 signals can be categorized in three groups—
  - The first are the signal having common functions in minimum as well as maximum mode.
  - The second are the signals which have special functions for minimum mode
  - The third are the signals having special functions for maximum mode.

Power Supply, GND, CLK

- **Power supply and GND :**

  It uses 5V DC supply at Vcc pin 40, and uses ground at Vss pin 1 and 20 for its operation.

- **CLK- Clock Input :**

  The clock input provides the basic timing for processor operation and bus control activity. It synchronize internal operations in the processor. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz. Clock signal is provided through Pin19.

AD15-AD0

- **AD15-AD0 :**

These are the time multiplexed memory, I/O address and data lines. These are 16 address/data bus.

  - AD0-AD7 carries low order byte data and AD8-AD15 carries higher order byte data.
  - During the first clock cycle, it carries 16bit address and after that it carries 16bit data.
  - The address bus can be separated from these signals by using a latch.
  - Memory address or I/O port no : whenever ALE =1
  - Data : whenever ALE =0

A19/S6-A16/S3

- **A19/S6,A18/S5,A17/S4,A16/S3 :**

These are the time multiplexed address and status lines. These are the 4 address/status lines. During the first clock cycle, it carries 4bit address and later it carries status signals.

  - Memory address A19-A16, status bits S6-S3
  - S6: always remain logic 0
  - S5 : indicate condition of IF flag bits

A19/S6-A16/S3

- The S4 and S3 combinely indicate which segment register is presently being used for memory accesses as in below fig.

S4	S3	Function
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

$\overline{Rd}$ & READY

- **RD' – Read Signal(active low pin) :**

This signal on low indicates the peripheral that the processor is performing memory or I/O read operation and data are available on the data bus.

  - Data bus receive data from memory or I/O device ; RD'=0

- **READY :**

This is the acknowledgement from the slow I/O or memory device that they have completed the data transfer. The signal is active high.

  - Mp enter into wait state and remain idle : READY= 0
  - Mp does the normal operation : READY = 1

INTR

- **INTR-Interrupt Request :**

This is a triggered input. This signal is active high and internally synchronized. It is used to request a hardware interrupt.

If any interrupt request is pending, the processor enters the interrupt acknowledge cycle. This can be internally masked by resulting the interrupt enable flag.

- If INTR is held high when IF=1 : Mp enter interrupt acknowledge cycle (INTA' become active after current instruction has complete execution)

$\overline{\text{TEST}}$

- **$\overline{\text{TEST}}$' :**

This input is examined by a **WAIT** instruction. Commonly connected to the 8087 coprocessor.

- If the $\overline{\text{TEST}}$ pin goes low, execution will continue,
- else the processor remains in an idle state.

RESET & NMI

- **RESET**

It is available at pin 21 and is used to restart the execution. It causes the processor to immediately terminate its present activity. This signal is active high for the first 4 clock cycles to RESET the microprocessor and also clear the IF.

- **NMI :**

Non-maskable interrupt. Similar to INTR except that no check IF flag bit. If NMI is activated, it gives the services to the external devices.

MN/$\overline{MX}$, M/$\overline{IO}$

- **MN/MX' :**

Select either minimum or maximum mode. To select maximum mode processor should be connected directly to GND and to select minimum mode processor should be connected directly +5V

- **M/IO' :**

Select memory or I/O. Also indicates whether the address bus contains a memory address or I/O port address.

$\overline{\text{BHE}}$/S7

- **BHE'/S7 :**

The **bus high enable** is used to indicate the transfer of data over the higher order (D15-D8) data bus during read and write operation. It goes low for the data transfer over D15-D8 and is used to derive chip selects of odd address memory bank or peripherals.

BHE	A0	Indication
0	0	Whole Word
0	1	Upper byte to/from Odd Bank
1	0	Lower byte to/from even Bank
1	1	None

- **S7 :** always a logic 1

ALE, $\overline{\text{INTA}}$

- **ALE :**

It stands for address enable latch and is available at pin 25. This signal indicates the availability of a valid address on the address/data lines.

- **INTA' :**

It is an interrupt acknowledgement signal and is available at pin 24. When the microprocessor receives this signal, it acknowledges the interrupt.

$\overline{WR}$, HLDA, HOLD

- **WR' :**

It stands for write signal and is available at pin 29. It is used to write the data into the memory or the output device depending on the status of M/IO' signal.

- **HLDA :**

It stands for Hold Acknowledgement signal and is available at pin 30. This signal acknowledges the HOLD signal.

- **HOLD :**

This signal indicates to the processor that external devices are requesting to access the address/data buses. It is used to input request for DMA. It is available at pin 31.

DEN, DT/$\overline{R}$

- **DEN :**

  It stands for Data Enable and is available at pin 26. It enables external buffer.

- **DT/R' :**

  It stands for Data Transmit/Receive signal and is available at pin 27. It decides the direction of data flow through the microprocessor. When it is high, data is transmitted out and vice-versa.

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$

- **S0', S1', S2' :**

These are the status signals that provide the status of operation, which is used by the Bus Controller to generate memory & I/O control signals. Indicates the status of current bus cycle. These are available at pin 26, 27, and 28. Following is the table showing their status −

S2	S1	S0	Status
0	0	0	Interrupt Acknowledgement
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

LOCK, $\overline{RQ}/\overline{GT1}$, $\overline{RQ}/\overline{GT0}$

- **LOCK :**

When this signal is active, it indicates to the other processors not to ask the CPU to leave the system bus. It is activated using the LOCK prefix on any instruction and is available at pin 29.

- **RQ'/GT1' and RQ'/GT0' :**

Bi-directional, These are the Request/Grant signals used by the other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. RQ'/GT0' has a higher priority than RQ'/GT1'.

QS1, QS0

- **QS1 and QS0 :**

These are queue status signals and are available at pin 24 and 25. These signals provide the status of instruction queue. Their conditions are shown in the following table –

QS1	QS0	Status
0	0	No operation/Queue is idle
0	1	First byte of opcode from the queue
1	0	Queue is empty
1	1	Subsequent byte of opcode from the queue